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A VLSI ROBOTIC CONTROLLER

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Raj R. Kumar

August 1988

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DEDICATION

This thesis is dedicated to my parents, Prof. D .V. Ramachandra and R. Jayalakshmi, my late grandmother Smt. B. T. Tayarammal, whose love and support helped shape my career and life, and to my good friend, Robert Alexander, whose friendship, help, and encouragement strenghtened my motives and enabled me achieve my goal.

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ABSTRACT

The Dual Axis Manipulator Element (DAME) project is a research effort aimed at servoloop processing and signal conditioning in a robotic envoirnment. The objective is to build a complete DAME, including extensive software development, to control a pair of servomotors within the joint of a servo-manipulator. Its unique feature and the purpose of this research is the design and implementation of a 64-pin custom designed VLSI chip, the Dual Axis Robotic Controller (DARC). Two other chips, a 28-pin Pulse Width Modulator (PWM), and an alternative, a 40-pin Dual Pulse Width Modulator with Digital Interface (PWM2) are also designed with the use of the standard cell library. This thesis presents a conceptual description of the DAME project and emphasizes its importance as a fundamental building block of an advanced telerobotic system. Strategies adopted in the design, implemention, and testing of DARC are discussed in detail. A new, semi-automated approach, encountered in the design of PWM and PWM2 are discussed. A relative comparison between the standard cell design (PWM and PWM2) and the custom design (DARC) is highlighted.

DARC implements optical decoders, pulse-width modulators, and a coprocessor interface. Fabricated in the 3μ SCMOS technology it has the advantages of miniaturization of the servo electronics, very high reliability, and unparalleled precision. It replaces several bulky cables, over 130 SSI/MSI CMOS and TTL circuits, and has a bit resolution far greater than what is available with off-the-shelf components. Novel circuit techniques in implementing DARC increase operating speeds and reduce clock skews and inductive noise.

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CHAPTER 1

INTRODUCTION

1.1 Background Information

The Advanced Servomanipulator (ASM) system was designed in 1982 and is under development for operation in the Department of Energy (DOE) nuclear fuel cycle facilities [1]. The ASM accomplishes remote operation and maintenance utilizing a rugged and mechanical modular design. Now DOE is planning to operate and maintain nuclear fuel facilities using remote manipulators to control activities in a space that is restricted from having any human enter for thirty years. One means of achieving the required reliability is to place all the mechanical and electrical parts physically at the point where control is needed. Heretofore, the electronic control circuitry has been too large to be placed within the housing of a manipulator joint such that several bulky cables had to be routed through the arms and connected between the remote manipulator and the external master. Miniaturization of the electronics was needed to reduce the cable requirements to a minimum: one pair of wires for power and another for communication with the supervisory computer. Synthesis, analysis, and optimization of the original ASM, leading to a simplified and compact mechanical design, is the main purpose of the contract TeleRobotics International, Inc. has with DOE. A new concept for a two-degree-of-freedom telerobotic module which includes not only motors, sensors, and mechanical parts but local sensor interfacing, servo-loop processing, motor amplifiers, and intelligence are the requirements for the success of the project.

1.2 Scope of This Research

Teleoperation and robotics have been used extensively for decades but only recently have the two technologies merged to provide better solutions for today's ever expanding needs of remote manipulation. Telerobotics is currently being used in hazardous enviornments such as those encountered in chemical, nuclear, military, underwater, and space applications. State-of-the-art telerobotic systems are moving towards optimized modular designs. This modularity provides for highly maintainable, reliable, reconfigurable, hardenable, and cost effective systems. The development of a miniaturized control system architecture allows for a flexible and overall compact system. A complete dual axis manipulator element is developed and the successful implementation of this concept is the miniaturization of the servocontrol electronics which has been achieved with VLSI technology. The scope of this thesis is the design and implementation of three chips, DARC, PWM, and PWM2. The manipulation system with miniaturized controls will result in a commercial product available to address DOE's remote application needs. In addition, the technology and related products can be used in commercial applications, nuclear maintenance, space station construction, satellite servicing, and defense telerobotic implementations.

This thesis is designed to arouse and incite newcomers into the field of VLSI design. The custom and standard cell design methodologies described, allow a user to decide on a convenient approach for his/her design. As major pitfalls in any VLSI design frequently occur, this thesis recommends to designers that they primarily understand the concepts of VLSI design and learn how to efficiently communicate with the CAD/VLSI tools.

1.3 Synopsis

Chapter 2 in this thesis portrays an overview of the DAME concept. It describes how remote manipulation is intended to be carried out and sets the stage for the introduction of the DARC chip. Existing robotic systems are reviewed in this chapter. Chapter 3 gives a detailed description of how the custom chip, DARC, was designed, implemented, and tested laying stress on the various aspects of SCMOS VLSI design. Chapter 4 shows how part of DARC's circuitry was reimplemented with the standard cell library and details the design of PWM. This chapter explains a new approach encountered in the design and characterizes the new tools used in the design. Chapter 5 describes the implementation of PWM2, a Dual Pulse Width Modulator with Parallel I/O. Changes in the strategy, from that used for PWM, include improved CAD/VLSI tools, efficient area utilization, and faster operating speeds. The above chapters take into account the hardware considerations and software requirements used in the design. A comparision between the standard cell (PWM and PWM2) and custom design (DARC) is presented in Chapter 6. Finally, Chapter 7 presents the various results obtained from the three designs, and outlines the summary and conclusions drawn from this research.

CHAPTER 2

OVERVIEW OF THE DAME PROJECT

In this chapter a brief historical background of robots and robotics are presented. Existing robotic systems are considered with advances made in technology. A detailed overview of the entire DAME concept and it functionality in serving as a servoloop processing element are discussed. Finally specifiations for DARC are highlighted.

2.1 Historical Background

As early as in 1954, George C. Devol worked on his patent application for a programmable manipulator [2]. In 1956, along with Joseph Engelberger, he started Unimation, Inc. Their work to this day is highly acclaimed. It was during the second world war, though, that the following three new technologies helped robotics flourish.

1. Servo mechanism theory

2. Digital computation

3. Solid state electronics

The first industrial robots went to work in 1961 and between the years 1961-1975 Unimation, Inc.'s prospects and profits in the field seemed to be bleak indicating the "Clouded Crystal Ball Effect"[2]. Kawasaki Heavy Industries took license to all Unimation, Inc.'s technology in 1968. Two associations, Japan Industrial Robot Association (JIRA) in

1971, and the Robot Institute of America (RIA) in 1975 were formed. Research efforts by these associations saw a boom in the development of robots. Since then several companies around the world have ventured into the development of robots. In the United States of America, General Motors, Westinghouse, IBM, United Technologies, and several other companies are developing robots. GEC in England, Seimens in Germany, Renault in France, Fiat in Italy and also a legion of several smaller companies make their mark in specialized robots.

2.2 Existing Robotic Systems

Several robotic systems have been developed and are being extensively used in various fields of life. Robots play a major role in industrial automation. They assist in increasing productivity and quality, as well as in lessening work site hazards [3]. These "intelligent" machines [4] are capable of independently performing several factory tasks, and simplifying many repetitive operations, such as assembly, sorting, and inspection with reduced man-power. Basically, all robots are required to perform two major tasks:

1. Sensing: locate with accuracy the object it needs to work on.

2. Locomotion or Actuation: move towards the object and efficaciously perform its function such as coat the surface with the required amount of paint, execute the desired weld, or sort/assemble various products.

A high degree of precision is required for any operation and throughout the process a feedback loop enables the robot to check its performance against specified parameters. The boon of robots is expected to have a six-fold increase between the years 1983-1990 [5].

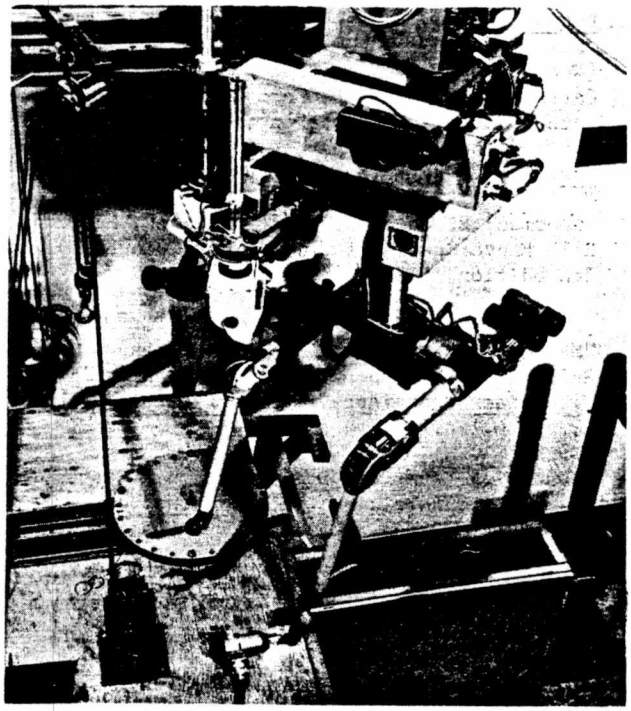


Figure 2.1: TOS arms at RSDF (Source: Killough *et. al* [1], page734)

Electronic servomanipulators are an outgrowth of the mechanical master/slave manipulators developed for handling radioactive materials. The earlier robots were designed entirely with analog closed feedback control systems. Analog control circuitry, however, limits reliability and performance. Due to drift characteristics of the potentiometers, capacitors, and resistors, frequent retuning is required [1]. In recent years, advances made in microcomputer and microprocessors have infused new life to the growth of digital control systems. With increased computer control and advances in sensory perception, tactile, and visual sensors, robots are "getting smarter" and their applications to new and more challenging tasks are increasing [6].

One commercially available analog servomanipulator is the TeleOperator Systems (TOS) model SM-299 designed in 1976 and shown in Figure 2.1. For two years the

SM-229's were on loan at Oak Ridge National Laboratory (ORNL) in their Remote Systems Development Facility (RSDF). The TOS SM-299 provides force feedback for all six degrees of freedom and the gripper. These manipulators use metal tape and pulley power transmission to provide very low friction. Both the master/slave arms are designed to be backdriveable, unlike typical robots.

ORNL then replaced the original analog system with the Model M-2 Servo manipulator shown in Figure 2.2. It significantly improved performance, maintainability, reliability, and force-reflection compared to the SM-299 system. It is also the first master/slave manipulator system controlled by an all-digital, distributed microprocessor based control system. Recent advances in servomanipulator development resulted in the Advanced Servomanipulator (ASM). The Advanced Servomanipulator represents significant advances in the state of the art, both in its mechanical and control aspects. Four Motorola 68000 microprocessors are used to control the joints rather than the 32 originally used in the M-2. Capable of assembling and disassembling nuclear power plant equipment, it is commended as the best available teleoperator to date [5]. The ASM, however, is yet to be commercialized as the cost to replicate it is estimated to be greater than $1,000,000.

2.3 Hardware Considerations

2.3.1 Overall Hardware Implementation

DAME is a primary module in the configuration of the control system architecture dipicted in Figure 2.3. The decentralized architecture employs a distributed microprocessor concept. Master/slave teleoperators are a class of teleoperators that have

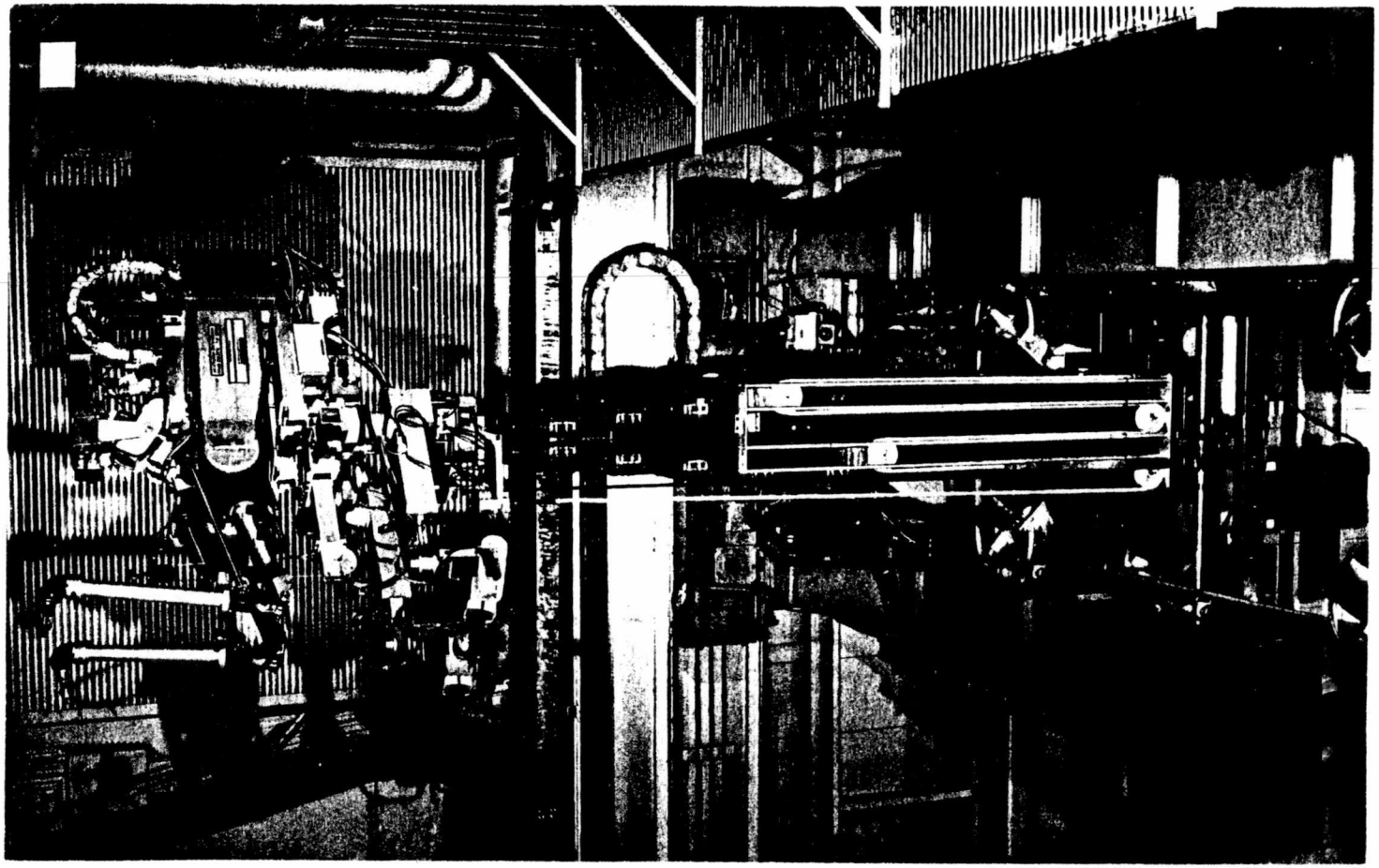


Figure 2.2:

The Model M-2 Servomanipulator at ORNL (Source: Handbook on Industrial Robotics [2], page 20)

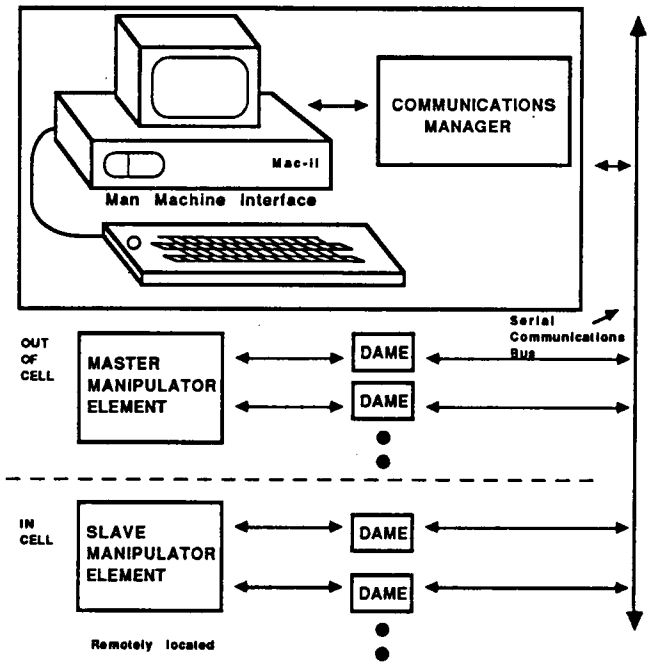


Figure 2.3: The Control System Architecture

geometrically isomorphic master and slave arms. The master is held and positioned by an operator and the slave duplicates the motion of the master automatically. The remotely located slave is capable of mimicking any of the control sequences performed by the master.

Several achievements resulted from using digital electronics to implement the control system:

1. Motion Scaling Features: For example, the slave could move 1 cm for every 2 cm of the master, increasing efficiency and permitting fine motion tasks.

2. Automated Control: Placing the slave unit at a work site and moving it under programmed control to a required position via simplified menu driven protocols.

3. User Friendly Architecture: Easily accessable systems that prevent operator fatigue.

4. Increased Precision and Reliability: Drifting analog devices are eliminated, and good resolution obtained.

5. Compact and Flexible Systems developed: Increased distance separation and greatly reduced conductor count between the master and slave.

The communication manager forms the communication link between the man-machine interface (MMI) computer and the master/slave arms. Serial data communication is achieved with a high speed serial port, which acts as the interface between the man-machine interface computer and the arms. Together, the human operator, the MMI computer, the communications manager, and the master arms comprise the out of cell equipment. This interface forms the main module in the program structure of the robotic control system and allows the operator to have authority over the functional response of the robots. It includes monitoring the robot, aiding it in doing what it is not capable of doing automatically, and taking over when automation fails or degrades. "Number crunching" techniques are employed to specify which activities have been completed or are changing status between the master and slave. Commands are executed from the control panel and the man-machine interface forms an integral part for debugging the system. The communication manager is configured with Intel's Advanced CHMOS Microcontroller architecture (80C197), a few memory elements (ROM's and RAM), and some additional logic.

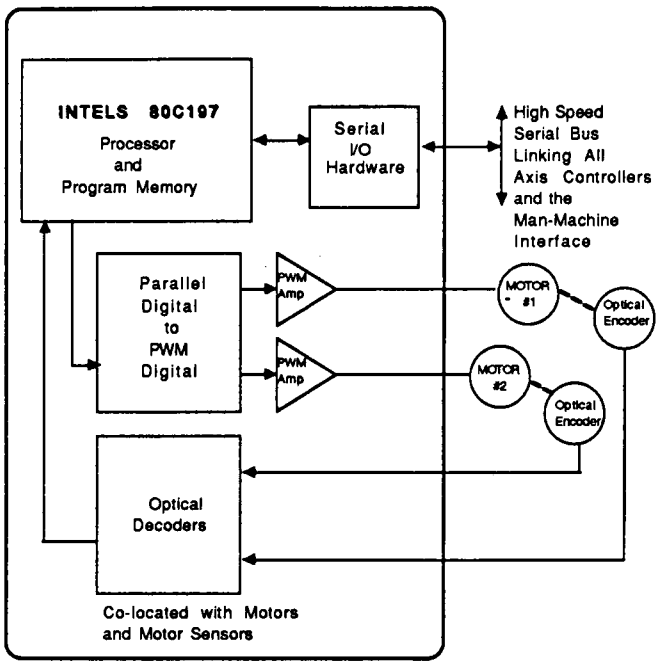


Figure 2.4: Conceptual Description of DAME

2.3.2 Conceptual Description of DAME

The Dual Axis Manipulator Element (DAME) is being developed in conjunction with the production of a complete, dual-arm, master/slave manipulator system. A third-generation robot is developed with eight degrees of freedom. Four DAME's are needed to implement each arm. A simplified version of the conceptual description of the DAME controller is depicted in Figure 2.4. It consists of a Microprocessor (Intel's 80C197), high speed I/O for communication, PWM waveform generators, optical decoders, PWM amplifiers, motors, and motor mounted quadrature phase optical encoders. Detailed descriptions of DAME and each of its functional modules are presented later in this chapter and in Chapter 3.

2.3.3 Hardware Description

The hardware configuration of the DAME μController, inclusive of control/interface lines and connections is illustrated in Figure 2.5. In addition to providing sensor interfacing, servoloop processing, and intelligence for a two-degree-of-freedom telerobotic module the basic requirement of the DAME μController is to control a pair of servo motors. Intel's 80C197 was selected as the main processor because of its off-the-shelf availability, immense adaptability, high speed capability, and moderately new technology.

A 16K×8 PROM (U10) containing the Serial Port Startup Loader Program activates the interface bus architecture. Address decoding logic selects either of the 32K×8 RAMS (U8,U9), the PROM (U10), or DARC (U2). U8 and U9 are the main memory elements. Together with two address latches (U3,U4), and additional logic (U5,U6,U7), the overall architecture can be described. At this point the main processor is described and a detailed hardware description of DARC is postponed until Chapter 3.

The Address Latch Enable or Address Valid output (ALE/$\overline{\text{ADV}}$) facilitates demultiplexed addresses from the address/databus [7,8]. The Read ($\overline{\text{RD}}$) is a read signal output to the external memory. The Write ($\overline{\text{WR}}$) and the Write Low ($\overline{\text{WRL}}$) signals enble the Write operation to external memory. $\overline{\text{WR}}$ will go low for external write, while $\overline{\text{WRL}}$ will go low for external writes were an even byte is being written. The Write High output, ($\overline{\text{WRH}}$), will go low if the bus cycle is writing to an odd memory location. The $\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles. Individual timing diagrams for the Write Strobe Mode [Figure 2.6] and the Address Valid With Write Strobe Mode [Figure 2.7] are shown.

The BUSWIDTH pin is an input for the buswidth selection. If the BUSWIDTH a 1,

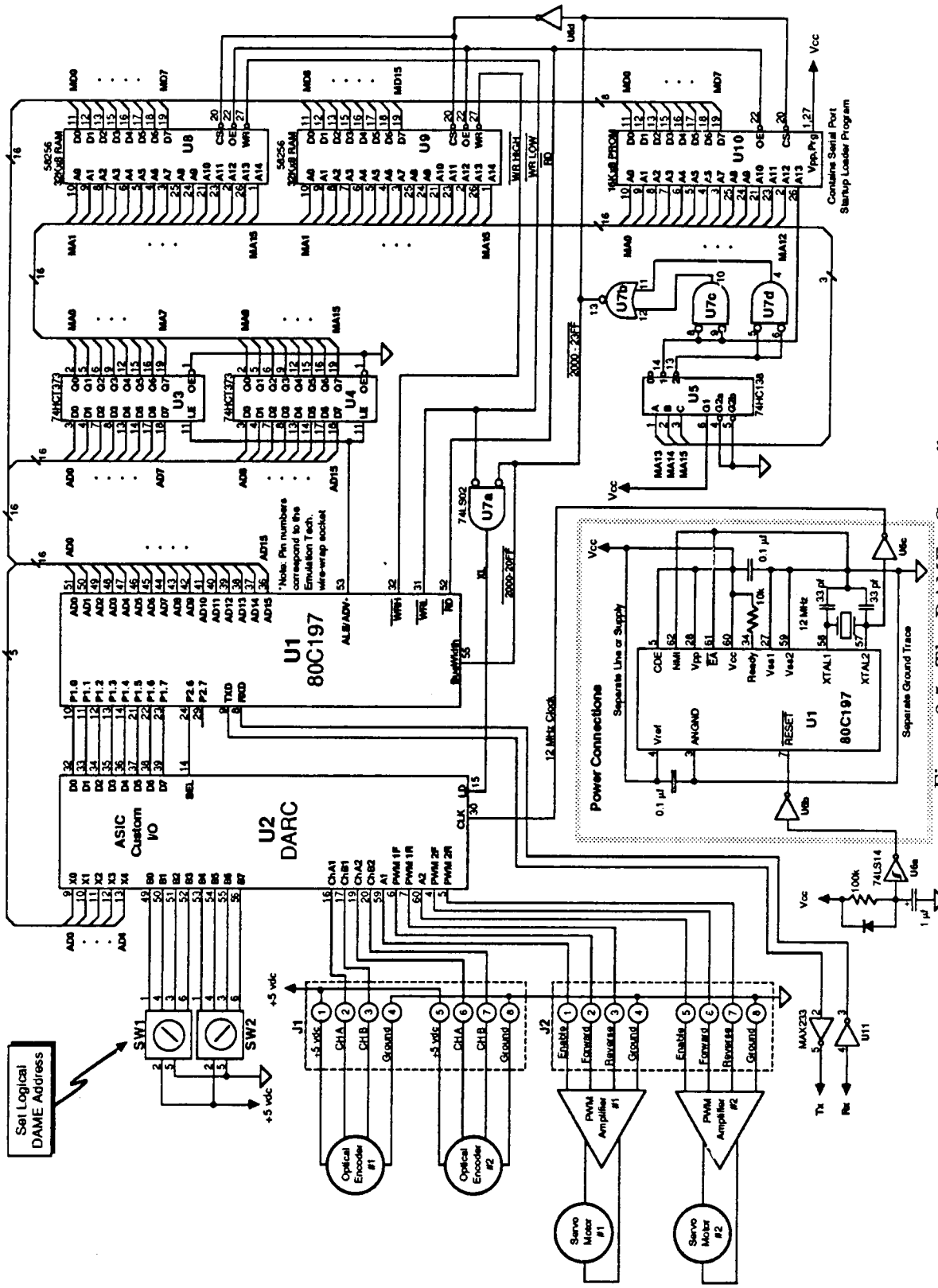


Figure 2.5: The DAME μController

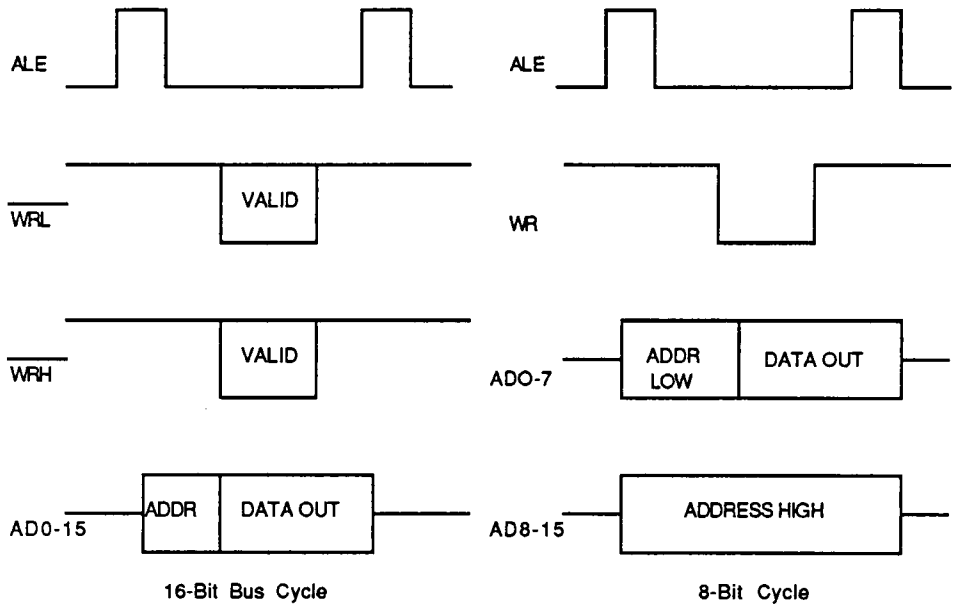


Figure 2.6: Write Strobe Mode Timing (After Intel [7], page 7)

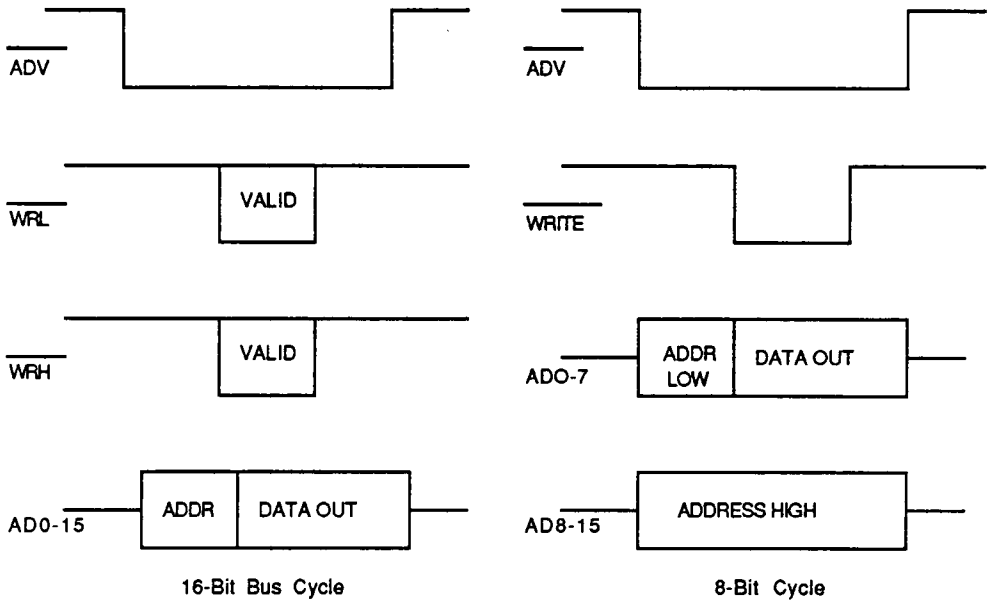


Figure 2.7: Address Valid with Write Strobe Mode (After Intel [7], page 8)

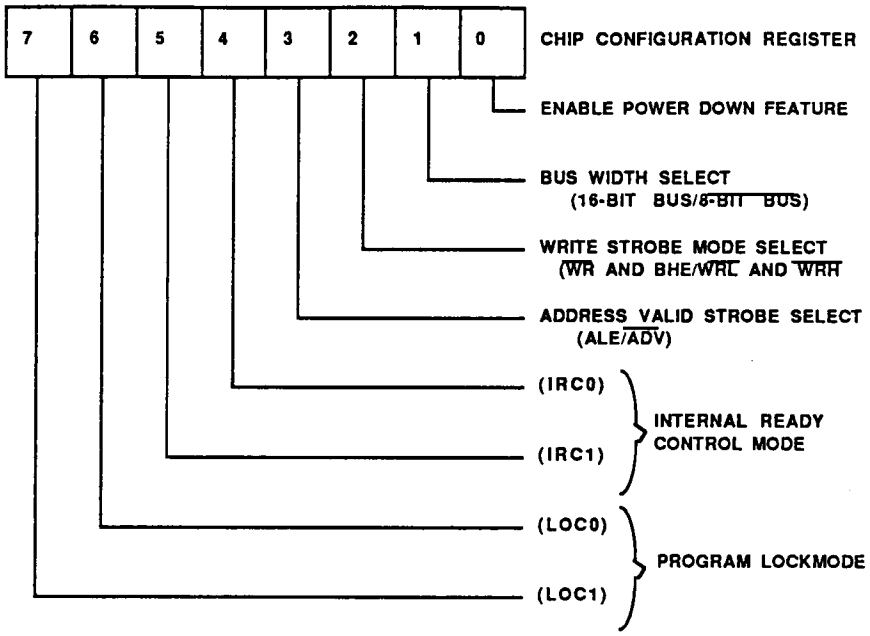


Figure 2.8: Format for Chip Configuration (After Intel [7], page 7)

a 16-bit bus cycle occurs and if it is a 0 an 8-bit cycle occurs. All the above options are governed by the Chip Configuration Register (CCR) and the format for the register is illustrated in Figure 2.8. The IRC0 and IRC1 bits control the internal wait states, and set a READY pin limit. A zero on LOC0 enables read protection and a zero on LOC1 enables write protection. The Non-Maskable Interupt (NMI) is the highest priority interupt. A high on this pin vectors indirectly through location 203EH. The External Access ($\overline{EA}$) is an input for memory select. $\overline{EA}$ equal to a high causes memory access to on chip PROM/EPROM. This pin is tied low when it is not used. A low on the $\overline{RESET}$ pin for 4 state times resets the chip. Additional pins used on the main processor are 16 address pins (AD0-AD16), and interface pins to DARC (P1.0-P1.7, and P2.6).

Of the four available modes of operation for the Serial Ports, Mode 0 (Synchronous

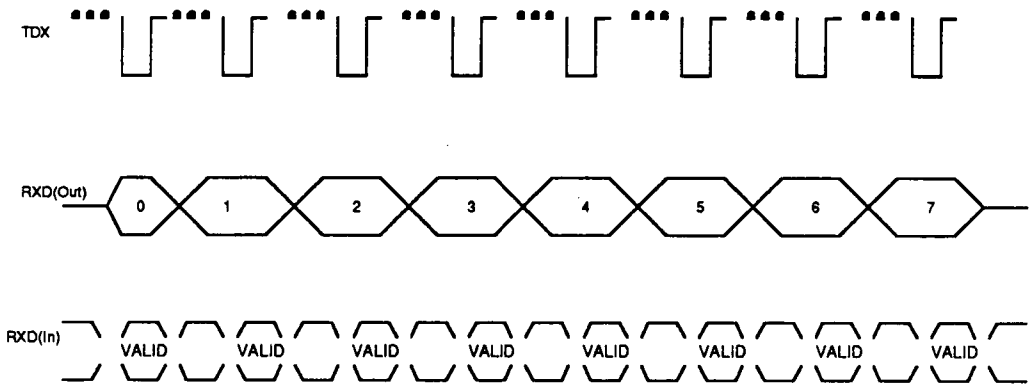


Figure 2.9: Serial Port 0 Timing (After Intel [7], page 26)

Mode) is chosen for operation. This mode uses the RXD pin to input or output 8-bits at a time. TXD is used to output the clock signal. The low time of the clock is always two states, except in the fastest mode. In the fastest mode the low and high times of the clock are each one state time. Figure 2.9 shows the relative timing of the serial port operating in Mode 0.

2.4 Software Considerations

2.4.1 Communication Protocol

As with any computer-based application, much of the creativity and effort of DAME, was in its software development. The main criteria of rapid prototyping and integration were kept in mind during development. A number of interface requirements, such as

communication, providing for clocking, system addressing, data input/output, synchronizing logic, and signal availability, were prime factors in writing the software. The clock for the custom designed (DARC) chip is derived from the external clock used by the main processor (80C197).

When access to the system bus by the main processor (U1) [Figure 2.5, page 13] is required DARC uses a synchronous request/acknowledge transaction protocol to issue the request to U1. U1 then translates this simple protocol into the correct sequence of signals to gain control of the bus or request service form DARC. U1 automatically latches the system address and data bus when required. The entire operation can be reversed as quasi-bidirectional pins are used on both DARC and U1. Both memory and I/O addressing are provided. The width of the data transfer is fixed at 8-bit's.

2.4.2 Software Architecture

All the DAME software is written in FORTH. A large effort, by TeleRobotics International, Inc., was put into making the software modular. The result was modular software tasks, with more reliable and understandable code. FORTH is used since it has several advantages as listed below:

1. It is the fastest high-level language available. It is only about 2-3 times slower than any equivalent machine language program.

2. Easy access to many input/output devices on the bus is provided for, since low-level bit addressing commands are part of the language.

3. It enables trial-and-error experimentation, and memory addressing commands are part of the language.

2.5 Specifications for DARC

2.5.1 Design Constraints

In developing a third-generation robot system several constraints occur in the design. Of primary importance are:

1. Size: Bulky cables and large components should be avoided.

2. Reliability: Efficient and long lasting systems must be developed.

3. Precision: Accurate estimation of the position variable is required.

4. Communcation Protocols: User friendly, understandable protocol definitions must be specified.

In implementing VLSI ASIC's the following *abstract* [9] constraints occur:

1. Conceptuality: Easily understandable and recognizable definitions.

2. Universitality: Useable for a wide range of applications.

3. Robustness: The system must be long term protected from intermediate potential problems.

4. Standardization: Must meet specific standards if required.

5. Systematics: The naming, availability, and placement of cells within a frame must be systematic and uniform.

2.5.2 Techniques Adapted

Specific design goals to miniaturize existing printed circuit boards and efficiently reduce chip count, led to the introduction of the DARC chip. The miniaturization of the entire DAME layout leads to implementation on a circular PCB (Printed Circuit Board) of 4-inch diameter, and its symmetrical embedding into the robots arm. Figure 2.10, and Figure 2.11 are an overview of DAME controller as it would appear internally within the housing of the manipulator joint, depending on the package used for the DARC chip. A key to the successful implementation of this concept, miniaturization of the servocontrol electronics, is achieved with VLSI technology.

The reliability of the system was enhanced by using digital control electronics instead of the traditional analog techinques. Precision was improved by developing pulse-width modulated waveform generators with a 11-bit precision and optical decoders with a 16-bit precision. Extensive software development yielded simplified and user friendly protocol definitions.

DARC was designed with easily understandable methodology (Conceptual). The basic functional blocks of DARC can be used in several other applications such as nuclear maintainance, space station construction, satellite servicing, defense telerobotic implementation, high technology manufacturing, and commercial applications (Universal). A long life (Robust) chip was developed which was interfaceable with several moderately new existing processors such as A8097BH, 80C186KA, and 80C197 (Standardized). All pin specifications are easy to understand from discussions in Chapter 3, and a symmetric layout, with well partioned and systematically placed functional modules was achieved (Systematic).

Since *physical* constraints [10] were also encountered in the design, DARC was im-

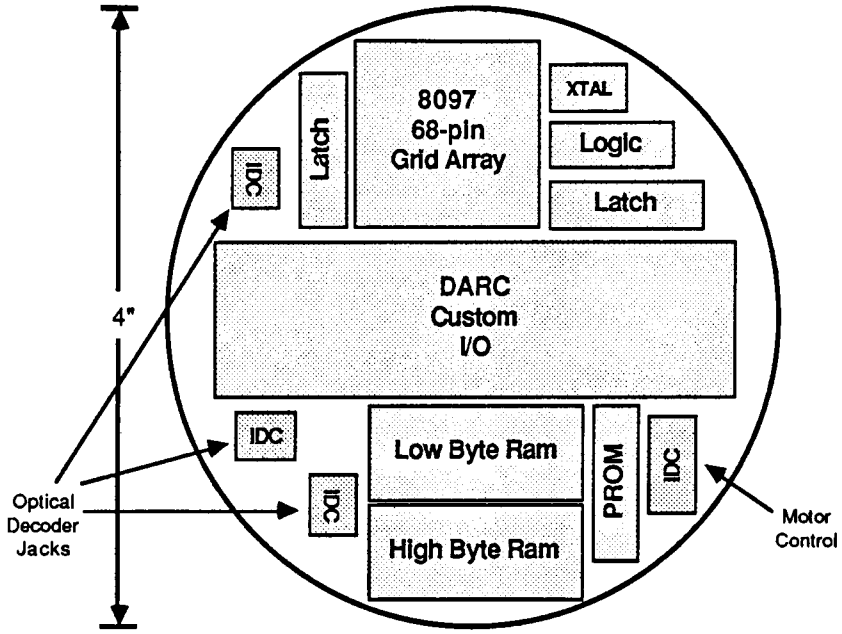


Figure 2.10: Layout of DAME using DIPS

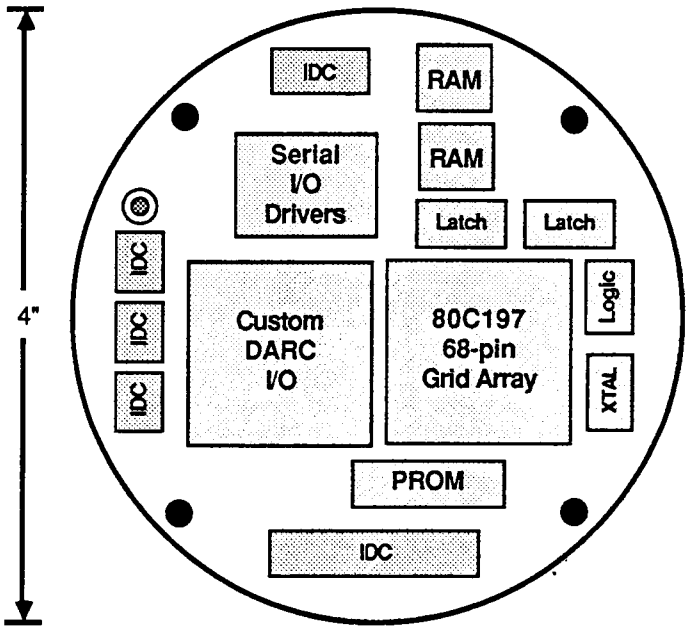


Figure 2.11: Surface Mount Layout of DAME

plemented to overcome these constraints. These can be classified as constraints on geometry, electrical specification, and assembly. DARC was designed with a simple and consistent layout, and therefore avoided geometric constraints. Exortic circuitry was not used, and the electrical characteristics were conservative. In this manner, it overcame the constraints on electrical specification. Pin packaging was initially done in a 64-pin DIP, though at later stages in the design of DAME, a PLCC (Plastic Leaded Chip Carrier) is intended to be used. Constraints on packaging and assembly were therfore eliminated. Hence an overall design frame, capable of withstanding the *abstract*, as well as the *physical* constraints was implemented.

CHAPTER 3

THE DESIGN AND IMPLEMENTATION OF DARC

3.1 Choice of Technology

The 1980's are known as the decade of VLSI. With transistor counts approaching a million, power dissipation has become a fundamental issue. Current packaging technology limits power dissipation to a few watts per chip to avoid high temperature induced reliability problems [11,12]. Sophisticated packages are being developed, but at great expense [13,14]. CMOS, with its low-power characteristics, may be the only VLSI technology that can live up to thermal packaging limitations and overcome this major limitation of power dissipation. Conventional air cooling and packaging techniques are still used for chips operated at room temperature, though new methods are constantly researched with increasing chip complexity. Implementing digital and analog systems in CMOS have several advantages [3,15,16,17]:

- Superior operating speeds: the same CMOS chips that can be debugged at room temperature can be operated at high speeds at low temperature (liquid nitrogen = 77K).

- Longer life cycle: CMOS is amenable to scaling with advances in technology as no ratio rules are enforced.

- Supply voltages are variable over a wide range (3-15V): as a result easily compatable with DTL/TTL circuits.

- Good noise immunity.
- High fan-out capability.
- Effective implementation of both analog and digital circuitry.
- Capability to handle more applications that require low-power consumption such as portable PC's and field instruments.
- The closest technology to Gallium Arsenide which will be even faster when it achieves reasonable yields in the next five years.
- Facilitates a regular layout style.

3.2 Design Methodology

The design starts as a top level designers 'mental' model [16], represented in the form of a schematic diagram of interconnected subsystems. The system-level specifications are then converted into functional building blocks defined by logic equations, state diagrams, and piecewise verbal specification of input/output behavior. The functional modules are then transformed into logic diagrams, and then together with sequencing and timing information into gate and switch-level structures for the target technology. A combination of a bottom-up and top-down approach is used [Figure 3.1]. 'Leaf cells' capable of performing the most primitive functions are designed with an insight towards using them in an array so as to maximize area utilization, regularity of interconnection, and keeping an overall global strategy for the simplicity of clocking, control, and power intact. The total system is subsequently implemented as an interconnection of subsys-

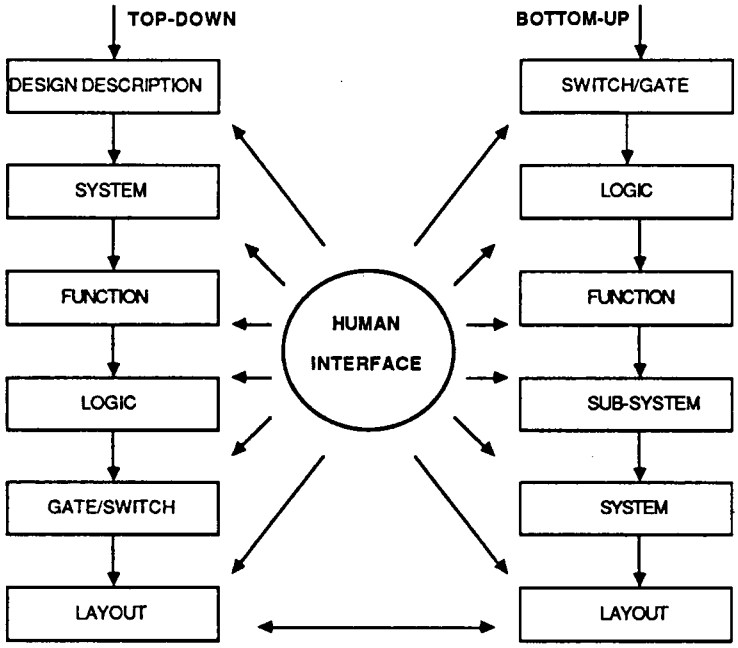


Figure 3.1: Multilevel Design Strategy

tems with a capability to communicate with the external world via the pads. At all stages of the design, verification tools such as dynamic simulator programs (*esim* and *spice*) and design rule checks are enforced to ultimately achieve a regular and symmetric layout. At each level, constraints similar to syntax and semantic rules of a program compilation process are observed such as design rules. Methodically, a multi level design process is encountered and systematically enforced.

3.3 Hardware Considerations

3.3.1 Functional Specification

DARC is designed to provide optical decoding, pulse width modulation, and an interface methodology for the DAME project [18]. The optical decoders and the pulse width modulators are designed to work at 3 MHz and 10 MHz respectively. Replicated layouts of the optical decoders and pulse width modulators allow for controlling two degrees of freedom of the manipulator with a single chip. An additional pulse width modulator was introduced to provide an analog output if and when required. Internally located 'Device-Select logic' enables the various specified functions to interact and interface with the DAME microprocessor. The digital I/O ports are designed to read/write digital data. All the above mentioned subsystems fit into a 64-pin DIP package. DARC is laid out in a die with external dimensions of 4600×6800 micron^2 (3066×4533 λ^2). Once the pads that communicate with the external world were introduced, the internal available silicon was reduced to 3680×2220 λ^2.

3.3.2 Functional Description

DARC is an interface chip, which when combined with a microprocessor is capable of maneuvering the manipulator by controlling the actuators. Its implementation enables it to perfectly fit into a predefined socket prespecified on the DAME PCB that is symmetrically embedded inside the robots arm. It is decomposed into four major building blocks.

- Optical Decoders

- Pulse Width Modulated Waveform Generators
- Device Select Logic
- Digital Input/Output

Each of these building blocks are considered independently in the following subsections. All pin references made in this section are identical to those shown obtained after the fabrication [Table 3.2, page 46].

Optical Decoders

FUNCTION: Accept quadrature phase input signals from the optical encoders and produce motor shaft position data with a 16-bit precision.

The encoders, which are internally housed within the robots arm, employ optical techniques to convert rotatory motion into electrical waveforms that are easily transformed into uniform and precisely spaced digital pulses. They are high speed, low noise, low friction, and high accuracy digitizers that can encode the shaft position as well as provide direction sensing. The optical decoders are designed to read these encoded signals and decode them into binary format, hence obtaining the angular position of the shaft. Two identical decoders are provided to read shaft positions for two-degrees-of-freedom.

Figure 3.2 shows a single optical decoder as it was implemented. Both decoders are implemented with digital filters on their input. These filters remove unwanted high frequency components of the input signal. Noise and line frequency are also attenuated by filtering. Since high-speed processing is required, this pre-filtering phase is essential. ChA1 and ChB1 form the inputs to the first decoder, and ChA2 and ChB2 form the

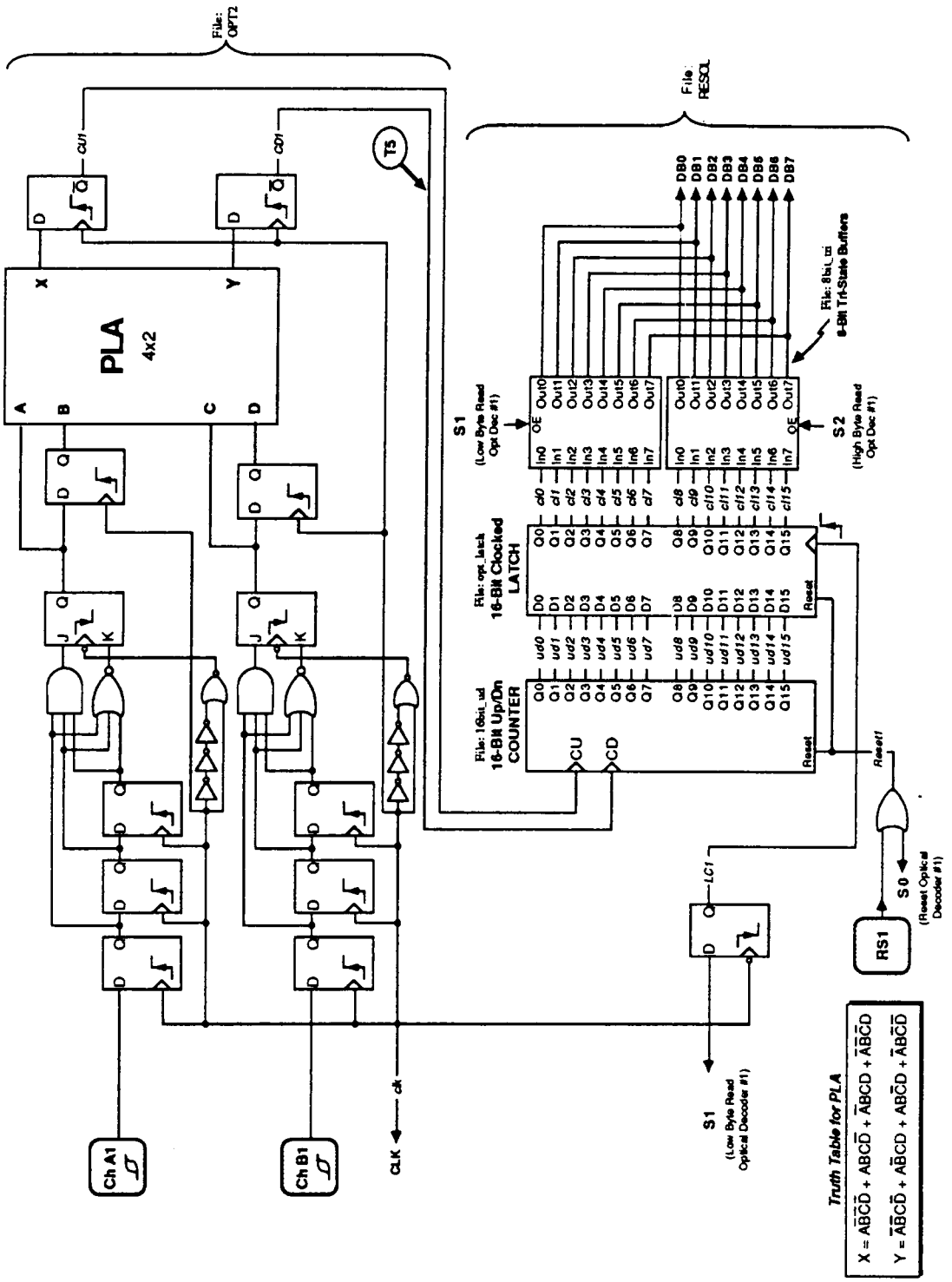
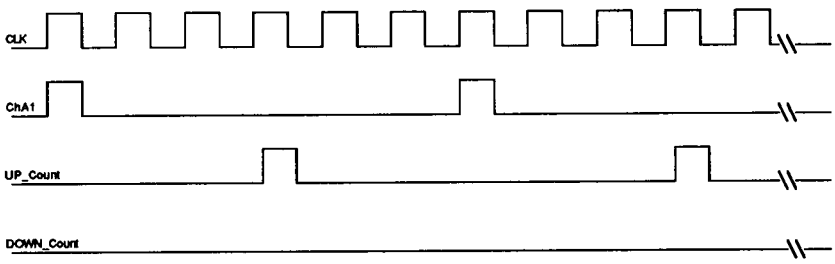
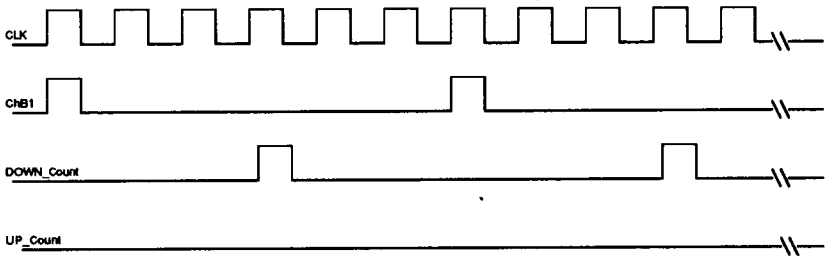


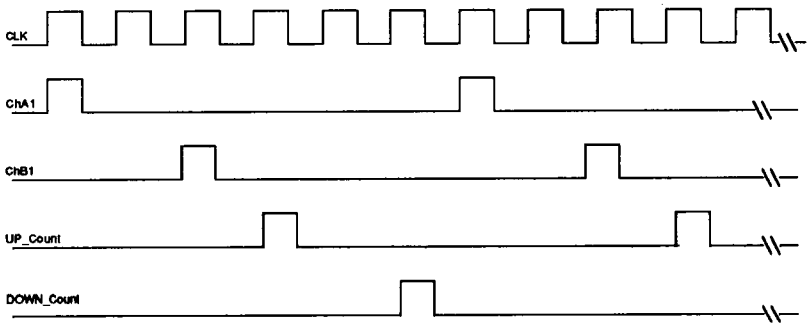
Figure 3.2: The Optical Decoder



a) The Up Count Generated by the digital filters



b) The Down Count Generated by the digital filters



c) A Combination of an Up/Down Count Generated by the digital filters

Figure 3.3: Digital Filters Timing Diagram

inputs to the second optical decoder. The external hardware resets are RS1 and RS2. Internal software resettability is also provided. Since only an 8-bit data bus is provided internally in the circuit, the high byte and low byte are independently read by software. Figure 3.3 illustrates the timing diagrams for the digital filters. The two quadrature phase inputs are viewed on ChA1 and ChB1 respectively. The three-bit shift register, additional delay elements and the PLA-based state decoder convert these signals into pulses that are recorded in the 16-bit up/down counter. The counter reading is gated on the bus, as required, to indicate the position of the shaft. Software routines input the data and derive accurate shaft position and velocity.

Pulse Width Modulated Waveform Generators

FUNCTION: Accepts 11-bit signed integer motor-drive command and outputs a 20 KHhz variable duty-cycle waveform to directly drive an all digital PWM motor amplifier.

In order to drive two motors only two pulse width modulated waveform generators were required. The availability of additional internal silicon, and future requirements for an approximated analog output (*eg.* precision variable frequency generator) led to the introduction of a third pulse width modulator. The functional block diagram of the pulse-width modulators is shown in Figure 3.4. A unique feature of the pulse width modulator is that it is capable of driving the motors in either the clockwize or counter clockwise directions.

The inputs to the pulse-width modulators come from the 8-bit data bus (D0-D7) [Figure 2.5, page 13]. These inputs are interfaced with the main processor. The pre-settable counters get their preset values from the latches and divide the pulse width

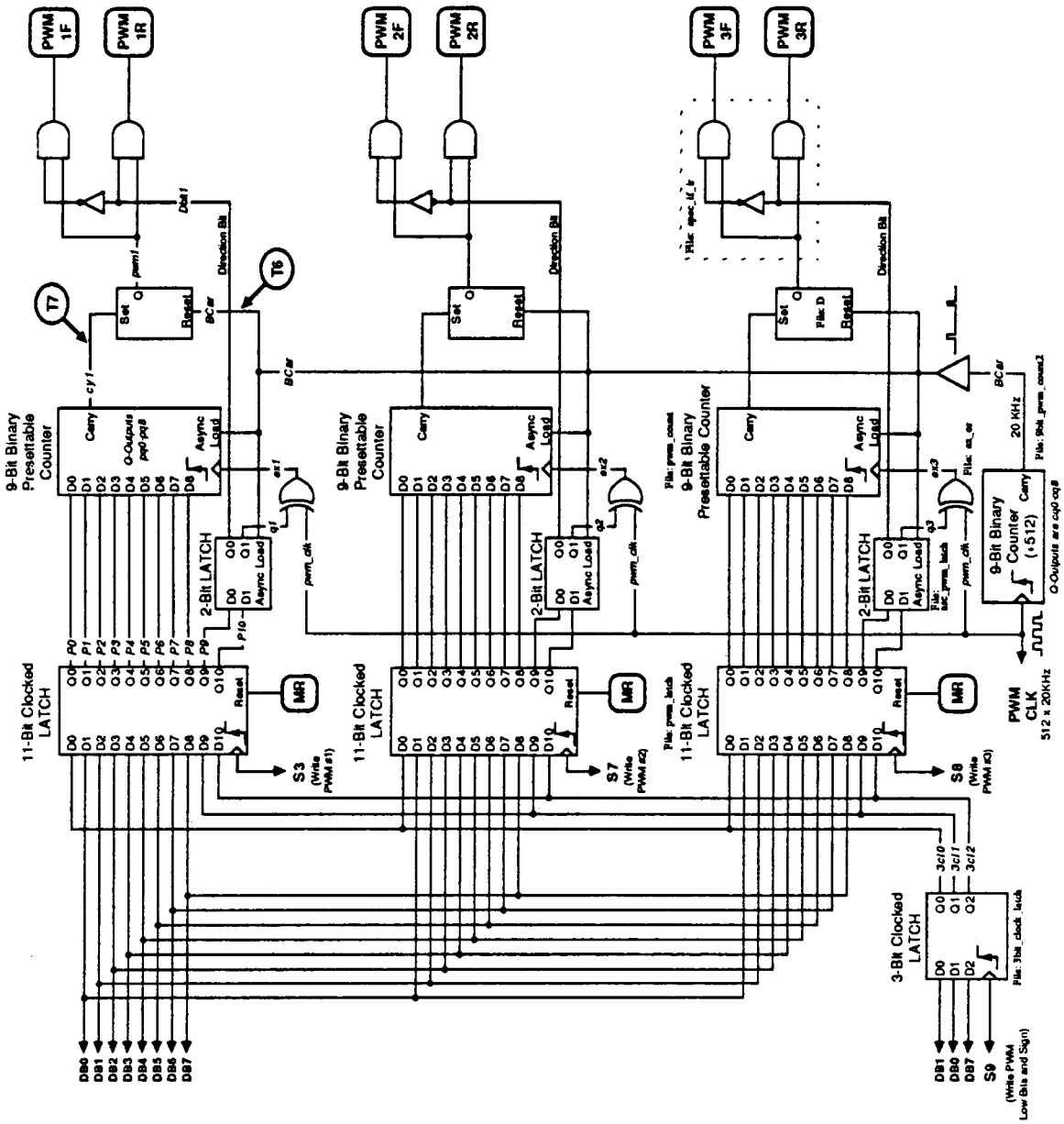


Figure 3.4: Pulse Width Modulators

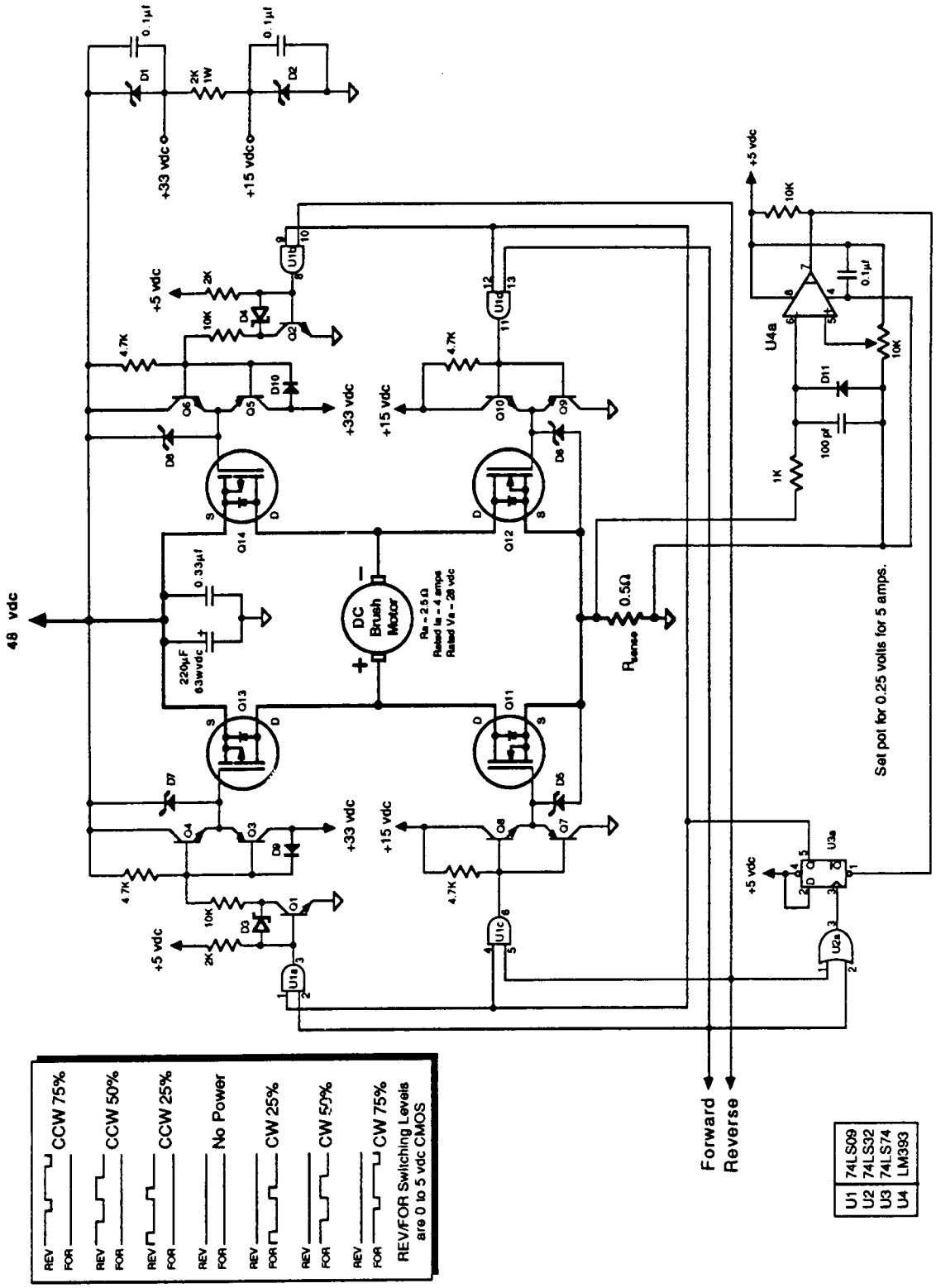


Figure 3.5: Servo Amplifier

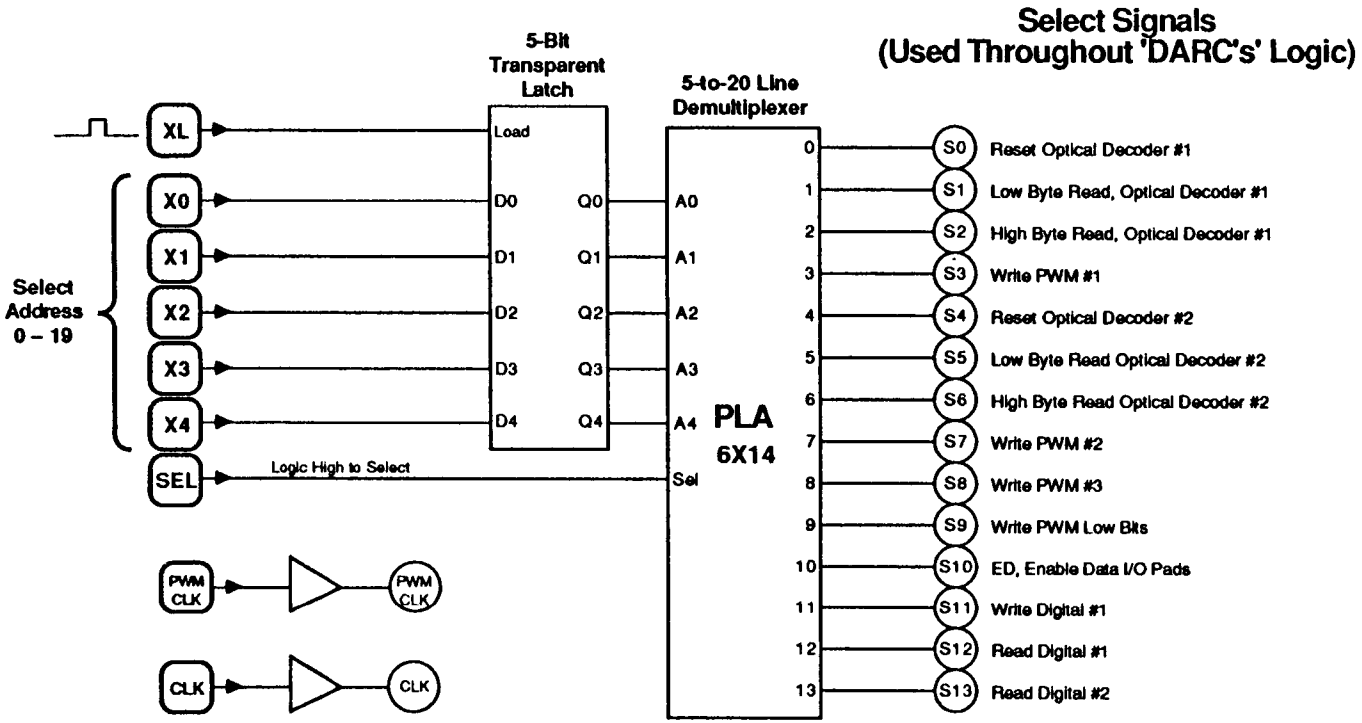
modulators basic frequency to provide a variable duty cycle, 0% to 100% (20 KHz). The outputs of the three pulse width modulator's are PWM1F, PWM1R, PWM2F, PWM2R, PWM3F, and PWM3R respectively. An externally provided master reset (MR) resets all the internal modulators. The entire control sequence consists of presetting the counters based on the required duty cycle and running the PWM_CLK at 10 MHz. The 9-bit presettable counter then generates a 20 KHz output waveform that simultaneously enables the direction bit output of the two bit transparent latch, and resets the output latch, and the presettable counter. Simple additional logic is used to provide the required pulses in either the forward or reverse directions. When the counter is in any of its other states, other than the overflow, the presettable counter can generate a carry which causes the forward direction pulse, provided the direction bit is high. Similar reasoning explains the reverse direction pulse. These pulses form the input to the Servo-Amplifier. The Servo-Amplifier with associated timing diagrams, indicating forward and reverse drive for various duty cycles, is illustrated in Figure 3.5.

Device Select Logic

FUNCTION: Provide control signals to DARC's internal circuitry.

The circuit diagram for this building block is shown in Figure 3.6. A five bit transparent latch and a 5×13 demultiplexer, implemented as a PLA performs the role of device selection. Select signals which are used throughout DARC's configuration originate here, at the heart of the chip.

The inputs are labelled X0-X4, LD, and SEL. The active high state of the SEL line which interfaces with 80C197 enables this functional block to carry out any of its output functions such as reset the optical decoders, enable the I/O pads, write the



PLA Truth Table

A4	A3	A2	A1	A0	Sel	Output = 1
0	0	0	0	0	1	S0
0	0	0	0	1	1	S1 & S10
0	0	0	1	0	1	S2 & S10
0	0	0	1	1	1	S3
0	0	1	0	0	1	S4
0	0	1	0	1	1	S5 & S10
0	0	1	1	0	1	S6 & S10
0	0	1	1	1	1	S7
0	1	0	0	0	1	S8
0	1	0	0	1	1	S9
0	1	0	1	0	1	S10
0	1	0	1	1	1	S11
0	1	1	0	0	1	S12 & S10
0	1	1	0	1	1	S13 & S10
1	X	X	X	X	X	None
X	X	X	X	X	0	None

Figure 3.6: Device Select Logic

PWM low bits, or even read or write digital signals on the bi-directional bus. The LD line is activated by the CS output of the EPROM, as shown in Figure 2.5, page 13. The truth table for the designed PLA is shown alongside the block diagram with its various functional aspects. System software is written to appropriately comply with required gate and interface delays.

Digital Input/Output

FUNCTION: Provide two 8-bit digital input ports and one 8-bit digital output port.

Implemented over the bi-directional data path the digital I/O embodies two sets of 8-bit synchronously clocked digital inputs, and an 8-bit synchronously clocked digital output latch. These ports serve as a major link in the interface with the rest of the circuitry of DAME [Figure 2.5, page 13]. The input ports are labelled A0-A7, and B0-B7. The output port is labelled C0-C7. The B-port of DARC is used to set the logical DAME address via the switches SW1 and SW2. A couple of the A-port outputs are utilized to enable the Servo Amplifiers. These ports are illustrated in Figure 3.7.

3.4 Layout and Floorplan

The heirarchial building of DARC starts at the lowest level of cell design. In order to implement all the functional modules several basic cells were generated as shown in Table 3.1. Initial chip floor plans were sketched, but were repeatedly modified to ultimately achieve the floor plan shown in Figure 3.8. A major setback to the design was the floor plan, as it could not be conceived at the initial stages of the design. The basic reasons were that the top-down design process was not carried out methodically,

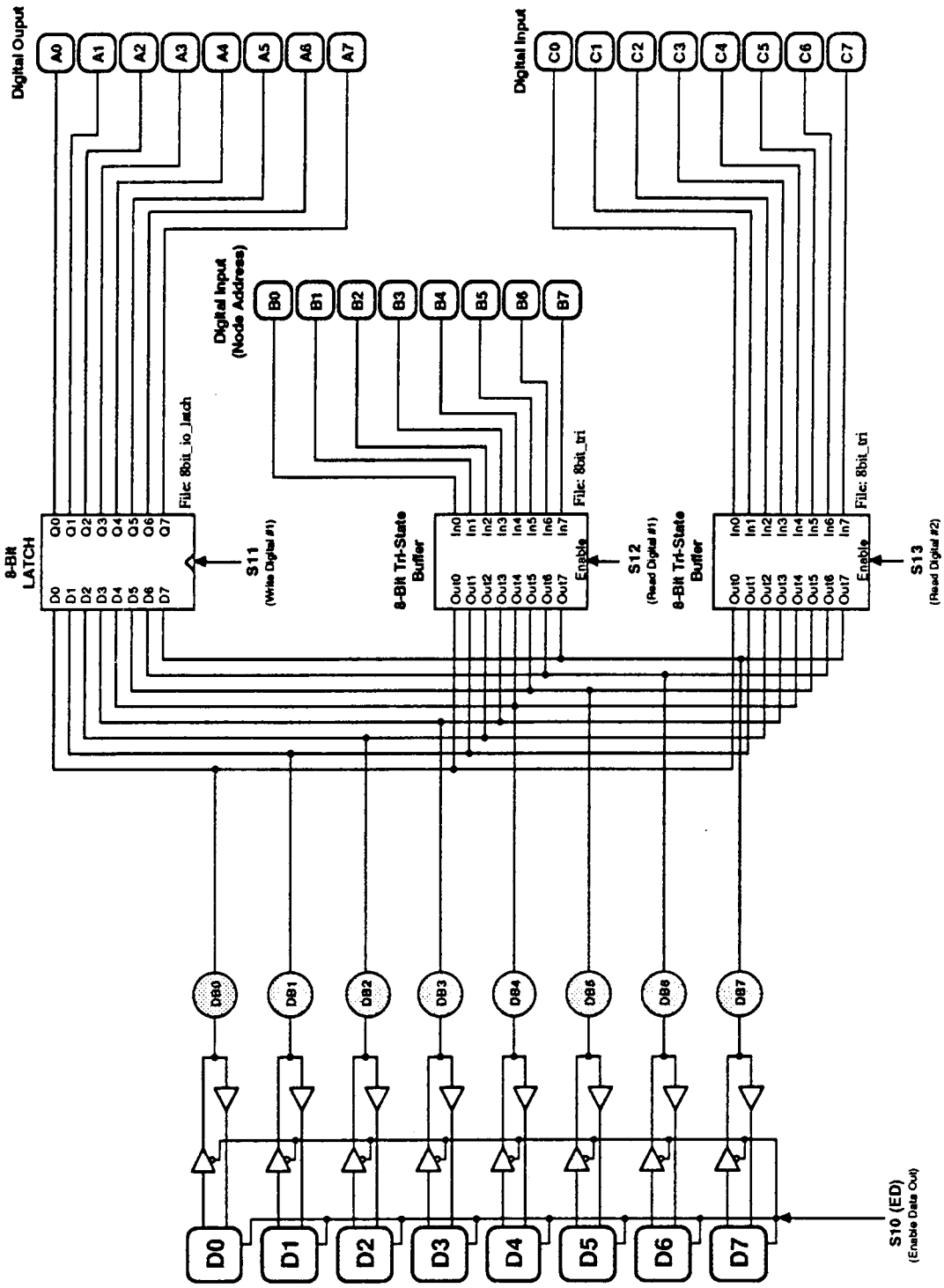


Figure 3.7: Digital Input/Output

DUAL AXIS ROBOTIC CONTROLLER

HEIRARCHIAL LIST OF ELEMENTS DESIGNED AND SUBMITTED TO MOSIS

DARK -DAME3

1

FRAME 64

PADS - frame64

68p46x68
PadGND
PadVdd
Padin
PadinR
Padout
corner
cornerBL
cornerBR
cornerTR

2

BUFFERS

TG_Buf
mis
I_in_buf
I_out_buf
clk_buf
pwm_clk_buf
in_buf
inv_sup_buf
ex_sup
sup_buf
spec_sup_buf
r_out_buf

3

DEV_SEL_LOGIC

decfin
trans_pla
1bit_asc_latch
2bit_asc_latch
new2

4

PWM

asc_pwm_latch
asc_1bit_latch
asc_2bit_latch
pwm_count2
1bit_pwm_count
pwm12
short
9bit_pwm_count
1bit_up_count
count12
count21
ex_or
latch2_pwm
pwm_latch
1bit_pwm_latch
3bit_clock_latch
1bit_clock_latch2
D
spec_if_ir
asc_pwm_latch

5

DIGITAL I/O

1bit_tri
8bit_tri
1bit_io_latch
8bit_io_latch

6

OPTICAL DECODER

a) **OPT2**

D1
K1
Oopt
Fun

b) **RESOL**

16bit_ud
car_lah
stage1_ud
opt_latch
latch1
stage2_ud
1bit_ud
2bit_ud
3bit_ud
4bit_ud
pullup
pulldown
or
1bit_tri
opt_tri
D_neg

7) **MISC**

inv
nor

Table 3.1: Individual Elements Designed for DARC

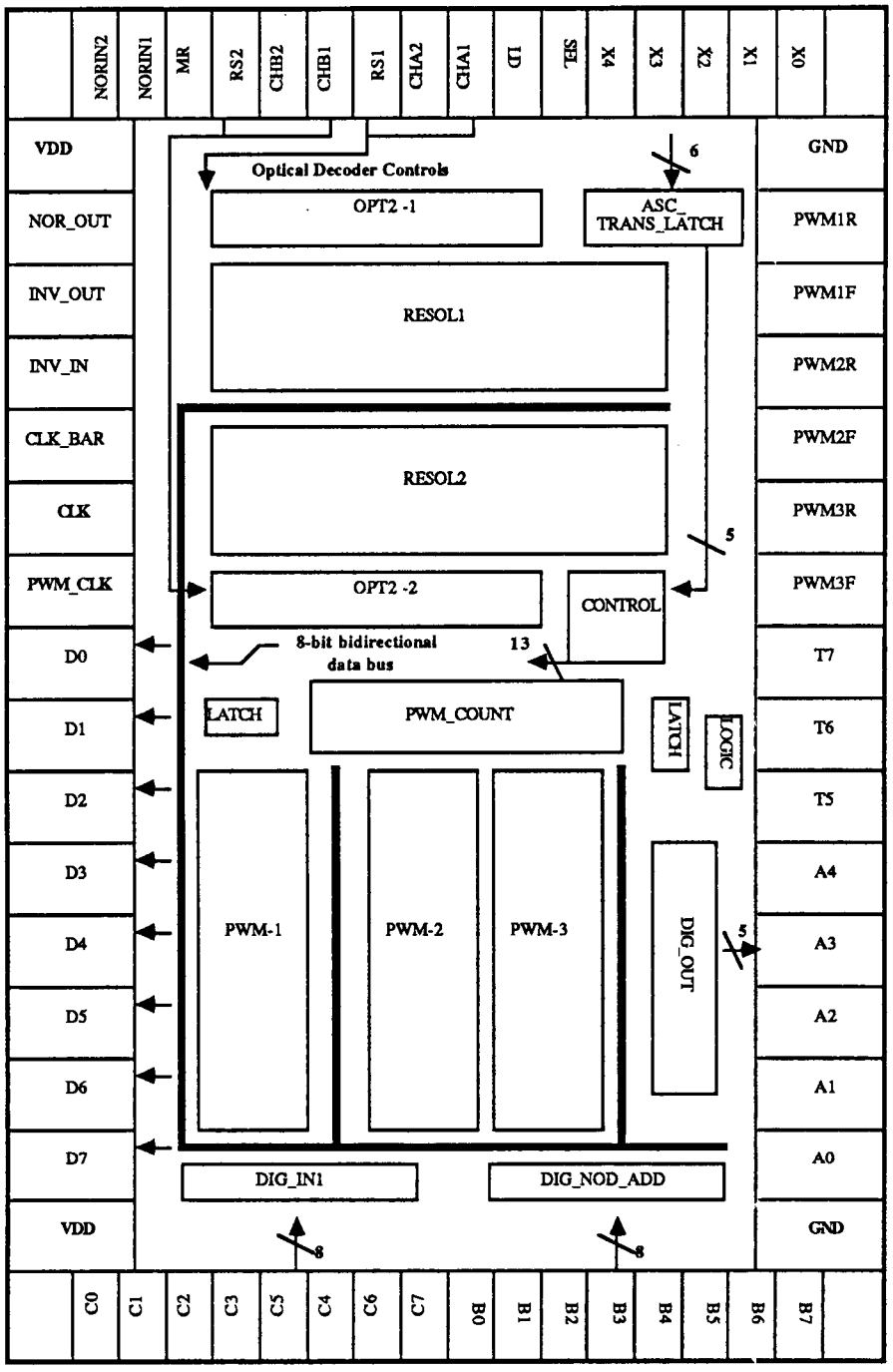


Figure 3.8: Functional Floor Plan for DARC

and several intermittent changes in the overall DAME layout repetitively occured. Some modules, such as a Frame_Timer, were designed, but due to insufficient silicon area where not eventually implemented on the chip.

In this section we discuss the details of the major cells that were implemented in the DARC chip. All these major cells were composed of basic cells that are mentioned briefly within the discussion. All references made within the brackets refer to the basic cells shown in Table 3.1, page 36.

OPT2:

OPT2 is a fundamental building block of DARC. It consists of 8 dynamic D flip-flops (D1), 2 J.K. flip-flops (K1), a state decoding PLA (Oopt) and some additional logic gates and delay introducers (Fun). OPT2 is a digital filter that reduces the noise margin and is designed to function with a synchronous clock.

RESOL:

RESOL is a combination of a 16-bit up/down counter (16_bit_ud), a 16-bit synchronous latch (optlatch), a couple of 8-bit tri-state devices (opt_tri), and a negative edge triggered D flip-flop (D_neg) with counter reset capability. This subsystem resolves the filtered outputs of OPT2's signals to a 16-bit data output. Together OPT2 and RESOL perform the optical decoding function.

PWM:

PWM is the pulse width modulated waveform generating circuitry. It is a union of a 9-bit presettable counter (pwm_count_2), a 11-bit synchronous latch (pwm_latch), a 2-bit

asynchronous latch (asc_pwm_latch) and additional logic (ex_or and inv). Additional logic (spec_if_ir) introduced at the output was used to switch the outputs either in the clockwise or counterclockwise direction. The outputs eventually drove the motors to provide the required duty cycle.

ASC_TRANS_LATCH:

The five-bit asynchronous transparent latch (trans_latch) is required in order to interface to the 80C197. The latch's output forms an input to the control PLA.

CONT_PLA:

Generated with *espresso* and *mpla*, this kernel resets, clocks, and enables all the logic internally in the chip. Input vectors to the PLA enable testing of some of the essential building blocks within DARC.

DIG_INP, DIG_OUT, and DIG_NOD_ADD:

These components form the interface process devices between DARC and 80C197. The basic cells used are 8bit_tri (8×1bit_tri) and 8bit_out_latch (8×1bit_out_latch).

PADS AND SUPERBUFFERS:

In all DARC utilizes 64 pads. Of these 8 are quasi-bidirectional with superbuffers, that yield large driving capabilities in both directions. Of the remaining pads, 4 are utilized for power (2 Vdd, and 2 GND), 35 as input pads and 21 as output pads. Input pads are evenly distributed amongst the Optical Decoders (6), Digital inputs (16), Clocks (2), and Control (7). Additional spare pads were made use of by implementing SS1 CMOS

functions of the Nor operation and providing accessability to test vectors for onboard testing.

POWER:

The strategy adopted was 'interdigitation' where the Vdd and GND layout of DARC are an interleaved structure of two planar trees , woven together so that their branches near the "leaves" meet the active devices. DARC was designed to operate with a 5V power supply. Internally the main bus is a maximum of 50 λ wide though in some locations a minimum of 8 λ was used. All current limits are below the metal migration limit for the 3μ SCMOS technology and are determined by the maximum dc current required [19,20,16,15]. Figure 3.9 shows the power and ground layouts for DARC.

3.5 Simulation, Testing, and CAD tools

The imitative process of simulation, on the designed models, was efficiently carried out, and the interaction of various parameters on designed functional modules were studied [21]. Switch-level, event-driven, timing and worst-case propagation delay simulators such as Esim, Spice, Relax, Cosmos, and Crystal were used to provide modelling accuracy at various levels of abstraction. Available resources were utilized and information feedback aided in detecting glitches and potential bottlenecks. The approach of levelizing circuitry and simulating with multiple passes through database was enforced. Common regions of ambiguity, catastrophic in nature, were discovered and rectified. A great deal of time was spent in testing the low-level and composite modules of DARC. Some of the results obtained along with their respective input files are given in Appendix

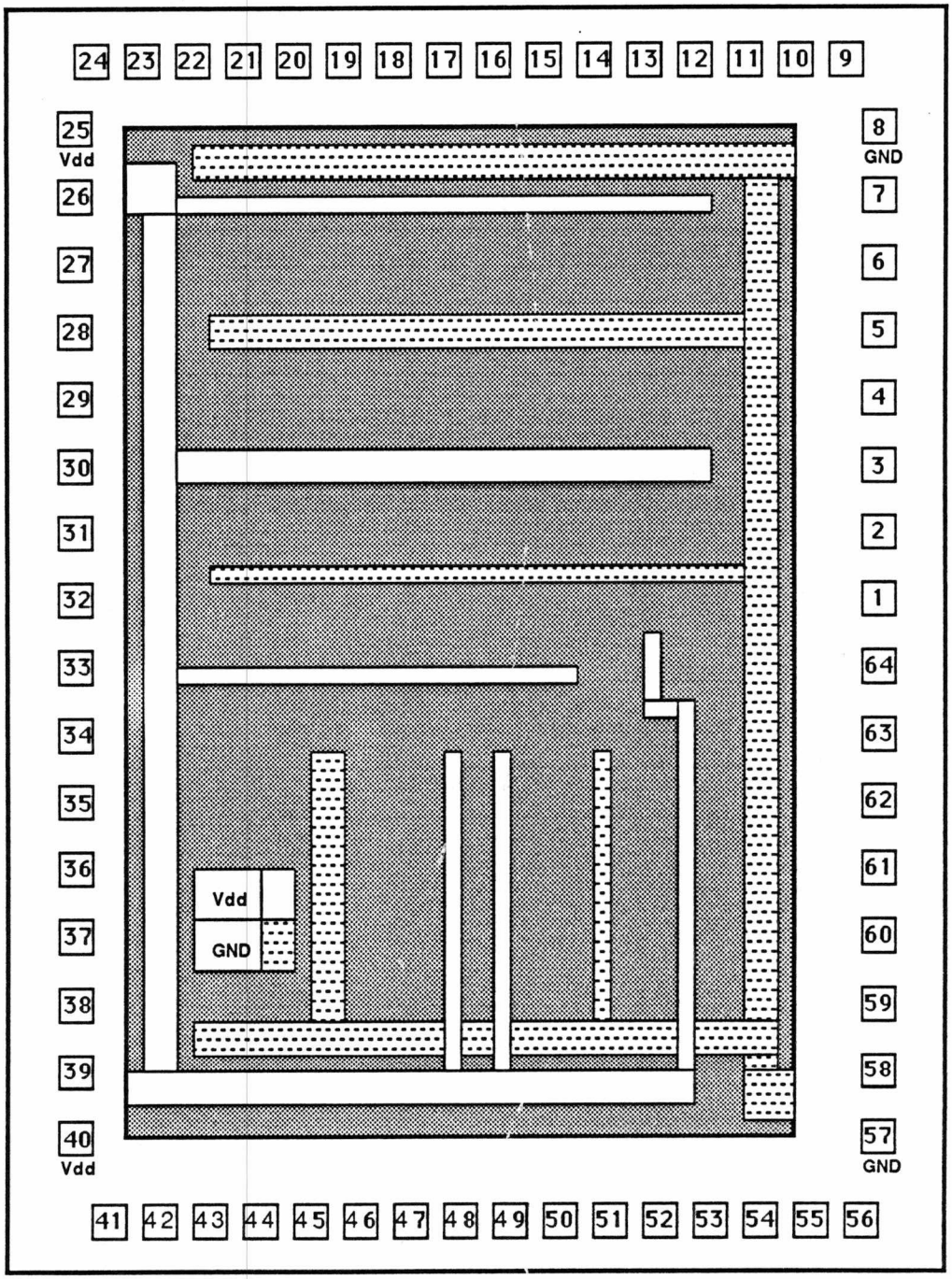


Figure 3.9: Floor Plan: Power and Ground

A and Appendix B.

In VLSI circuits, with the ever increasing chip complexity and transistor counts, "Testing a designed circuit is not as efficacious as designing a testable circuit". In the internal configuration of DARC, various access points were introduced to enhance the controllability and observability of the system. Heuristics determined the location of these points. Skillful partitioning and implementation of most subsystems over a bi-directional data bus contributed to simplify onboard testing. The digital filters were contrived so as to cultivate, a simple method of testing, an integrated version of Signature Analysis and the traditional Scan Path technique. Though a 100% fault coverage was not obtained during the testing procedure, DARC was designed with easy access to onboard fault detection and location. Three additional test pads and the 8 bi-directional pads were used for this tremendous onboard test capability.

Prototype hardware for testing DARC was ready before it returned from MOSIS (MOS Implementation Service). A sample software routine for the testing procedure is shown in Appendix C. This is a FORTH routine that tests all the individual modules within the chip. DARC was extensively debugged at TeleRobotics International, Inc. and the results obtained are summarized in Chapter 7.

Several CAD (Computer Aided Design) tools were utilized in implementing DARC. The flowchart that is given in Figure 3.10 portrays the custom design CAD tools and software facilities provided at the University of Tennessee, Knoxville.

When the original design of DARC commenced in July, 1987, the plan was to use *Vem* (View Editor Monolith) to create the entire design. *Vem* is an interactive graphics shell/editor for I/C designs represented in the OCT CAD/VLSI data representation system [22]. *Vem* provides standard editing capabilities, for both physical and symbolic

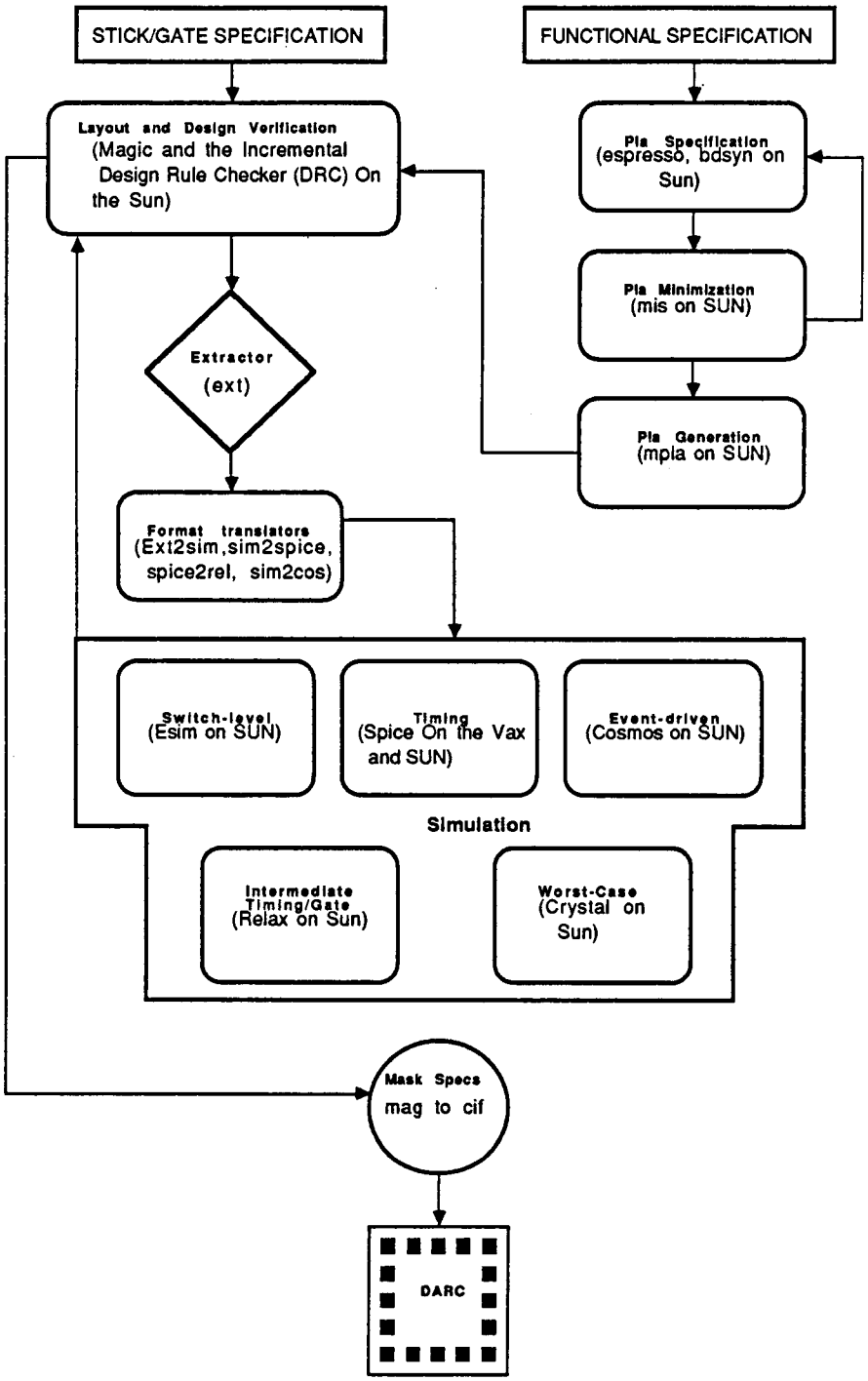


Figure 3.10: Design Flow of DARC : Custom Design Cad Tools

views. It is a multi-window **X** application designed to run on bitmapped based graphic workstations. *Oct* uses a scaled lambda grid *i.e.,* 20 *oct* units is equal to 1 λ. Though routing and layout seemed fairly simple with *Oct*, several bugs in its 1.0 version restricted its use. An immediate switch to Berkeley's *magic* and its associated tools was made.

Basic 'leaf cells' were designed using the layout/editing tool *magic*, which was provided with an on-line design rule checker - *drc*. The created cells were extracted with *magic's* hierarcial extracter. The extracted files contained envoirnmental information (scaling, timestamps etc.), information about the geometry of the cells, and connection between mask geometries and subcell names. Translating routines (*ext2sim*,*sim2spice*) were then used to convert the extracted files into formats that the simulators could understand. Simulation of the various cells and modules was performed with the event-driven/switch-level simulator, *esim*, and the timing simulator *spice*. Whenever errors were detected, the geometric layout editor *magic* was reinvoked, and the 'leaf cells' redesigned. The simulators provided accurate information about some of the design errors that had been committed, though not all. The PLA's on the other hand were specified by a two level description of Boolean switching functions (input format for *espresso*), or a pascal-like routine (input for *bdsyn*). The automatic PLA generator *mpla* was then used to achieve a SCMOS layout of the required combinational logic.

3.6 Resulting Design

Table 3.2, gives the pin descriptions for all the pins, as used for DARC. The final result of the entire effort was a 64-pad die with external dimensions of 3066×4533 λ^2

(4600×6800 micron^2) and internal available silicon area of 2220×3680 λ^2. A photomicrograph of the final DARC *cif* plot, that was mailed to MOSIS is shown in Figure 3.11. The chip was fabricated on a 3μ SCMOS p-well run, through MOSIS, by HP (Hewlett Packard, Inc), and returned to the University of Tennessee, Knoxville in January 1988. It was intensively tested at TeleRobotics International, Inc. and the results are summarized in Chapter 7.

Table 3.2: Pin Description of DARC

PIN #	NAME	TYPE	FUNCTION
1	OPEN	Substrate	Connected to n-type substrate
2	PWM_1F	Output	Forward drive output for 1st PWM
3	PWM_1R	Output	Reverse drive output for 1st PWM
4	PWM_2F	Output	Forward drive output for 2nd PWM
5	PWM_2R	Output	Reverse drive output for 2nd PWM
6	PWM_3F	Output	Forward drive output for 3rd PWM
7	PWM_3R	Output	Reverse drive output for 3rd PWM
8	GND	Power	Ground Pin No. 1 for the chip
9-13	X0-X4	Inputs	Externally interfaced to control DARC
14	SEL	Input	Selects individual internal functions
15	LD	Input	Loads externally interfaced connands
16	ChA1	Input	Quadrature Phase inputA to Opt. Dec. #1
17	ChB1	Input	Quadrature Phase inputB to Opt. Dec. #1
18	RS1	Input	External Reset to first Optical Decoder
19	ChA2	Input	Quadrature Phase inputA to Opt. Dec. #2
20	ChB2	Input	Quadrature Phase inputB to Opt. Dec. #2
21	RS2	Input	External Reset to second Optical Decoder
22	MR	Input	Common Master Reset to all three Pulse Width Modulators
23	NOR1	Input	Input 1 to nor-gate
24	NOR2	Input	Input 2 to nor-gate
25	VDD	Power	Power Pin No.1 to DARC
26	NOR_OUT	Output	Output of the nor-gate
27	INV_IN	Input	Test input to an inverter
27	INV_OUT	Output	Test output from the inverter
28	SPARE	-	Unused Pin
29	CLK_OUT	Output	Output of internal CLK (test pin)
30	CLK	Input	Main clock for optical decoders
31	PWM_CLK	Input	Main clock for all three pulse width modulators
32-39	D0-D7	QDB	Quasi-bidirectional port capable of reading and writing data from external circuitry with an internal strobe
40	VDD	Power	Power Pin No.2 to DARC
41-48	C PORT	Inputs	Miscellaneous input port
49-56	B PORT	Inputs	Input Nodal address port
57	GND	Power	Ground Pin No. 2 for the chip
58-61	A PORT	Outputs	Interfaceable Output bus
62-64	TEST	Outputs	Output pins that test internally mal-functioning regions in DARC

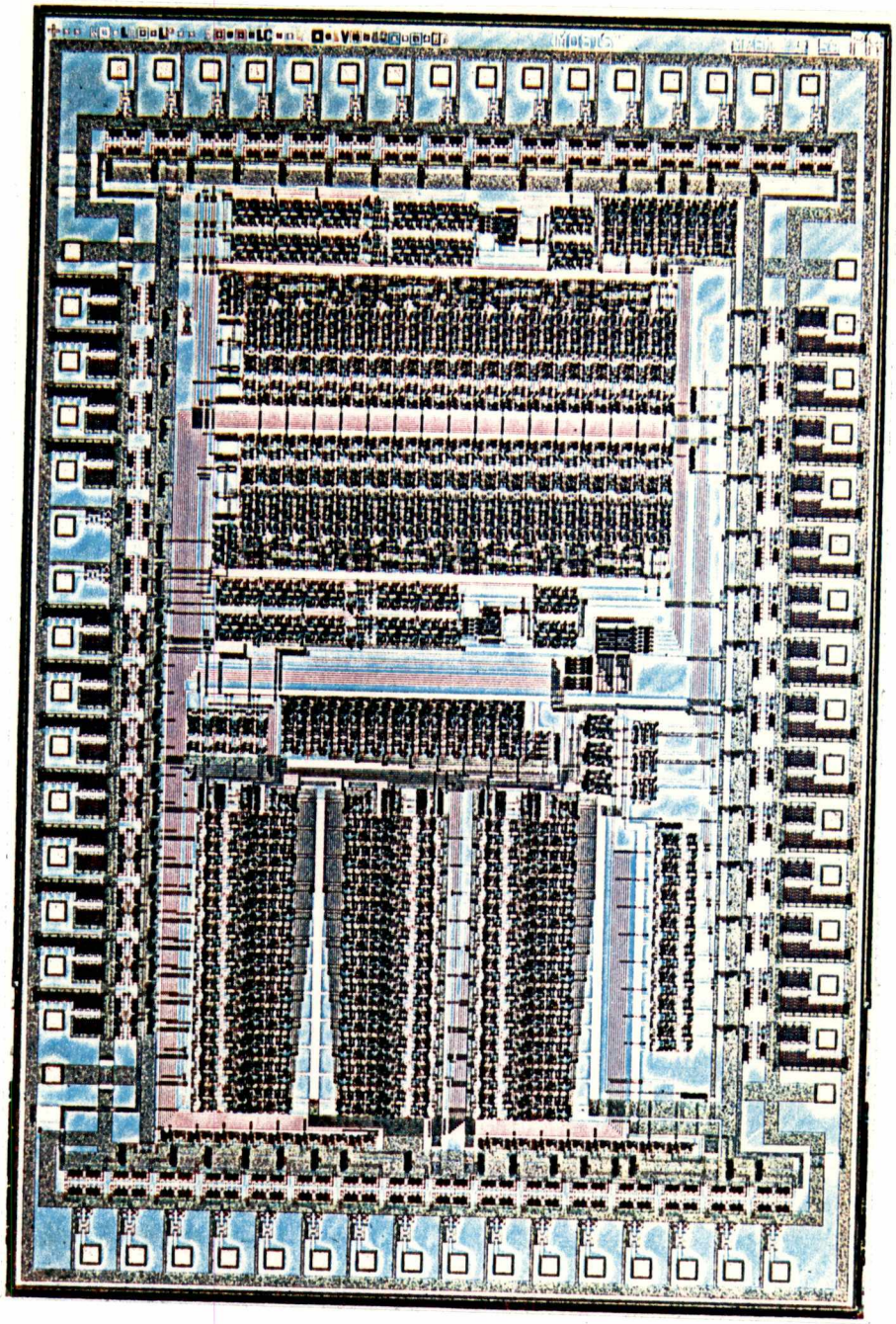


Figure 3.11: A Photomicrograph of DARC

CHAPTER 4

THE DESIGN AND IMPLEMENTATION OF PWM

PWM was realized with an entirely new concept, that of designing ASIC's with pre-defined cells from a standard cell library. These cells were originally designed at Missisippi State University (MSU), and are available to VLSI designers all over the United States. The cells are capable of performing all basic operations that may be required of available hardware. Standard cells in SCMOS have a fixed height (112 lambda) and variable widths (8 to 130 lambda), and are designed to have maximum possible efficiencies within their restricted areas. An automated approach was encounted in the design, with access to several of Berkeley's new software packages.

A couple of major changes that occured in the DAME layout necessitated the design of a new pulse-width modulated waveform generator. The original circuitry of the Servo Amplifier [Figure 3.5, page 31] was too large to be housed within the robots arm. A new PWM amplifier became available, and it only required an additional 4-inch PCB to be mounted within the manipulator joint. This new amplifier, the AMC-250D, required driving capability only in one direction to produce the required motor rotation. Hence PWM was designed in a short span of time to meet project deadlines.

Table 4.1: Standard Cells Used in the Design of PWM

ITEM NUMBER	CELL NUMBER	FUNCTION/ DESCRIPTION
1	1120	2-Input Nor
2	1140	4-Input Nor
3	1220	2-Input Nand
4	1230	3-Input Nand
5	1240	4-Input Nand
6	1410	Nand Latch
7	1520	4x-Inverting Buffer
8	1530	Clocked Latch W/Reset
9	1560	Delay cell
10	1660	2-Input Nand/And
11	1830	D Flip-Flop w/Q and Qbar
12	2310	2-Input Ex-OR

4.1 Hardware Considerations

4.1.1 Functional Specification

PWM is designed to provide pulse width modulation for the DAME project. It outputs signals that are amplified by the AMC-250D, which in turn drive the motors. The new amplifier, the AMC-250D, takes a 50% duty cycle for zero drive. When the duty cycle is less or greater than 50%, negative and positive dirves are achieved respectively. Though the interface is different, it is still bidirectional. PWM is designed to work at 12 MHz and a variable duty cycle of approximately 24 KHz. In all, PWM utilizes 28 pins. Of these 15 are input pads, 11 are output pads, and two pads are used for power and ground. Internally, superbuffers are used to provide large drive capabilities where required. The standard cells used in the design are shown in Table 4.1. Specification for each of cells are provided along with the basic cells [23].

4.1.2 Functional Description

FUNCTION: Accept 10-bit signed integer motor-drive command and produce a 15 KHz variable duty-cycle waveform to directly drive the AMC-250D

In terms of major building blocks, PWM is almost similar to the PWM's designed for DARC. Figure 4.1 shows the schematic of PWM. It basically is comprised of two 10-bit holding latches, a 9-bit presettable counter, and miscellaneous logic. The tenth bit flips the input clock to achieve a 10-bit resolution of the duty cycle. The input to the PWM is over the 8-bit data bus (D0-D7). The inputs are interfaced with the main processor. The required output of PWM is PWM_OUT. The presettable counters get their preset values from the two sets of synchronous latches, and divide the pulse width modulators basic frequency to provide a variable duty cycle of 0% to 100%. The control sequence consists of presetting the counters based on the required duty cycle, from external pre-programmed PROM, and running the main CLK of PWM at 12 MHz. The presettable counter overflow then generates a 15KHz output waveform that drives the off chip amplifiers. Several test points were internally located within PWM (*eg.* L0, L1), in order to efficiently debug the chip when it returned from fabrication. Additional miscellaneous outputs (Q0-Q3, and Q8) from the counter could also be used for various applications.

4.2 Layout and Floorplan

The primary layout of PWM was done with the *OrCad* package on an IBM-PC, at TeleRobotics International, Inc. Basic standard cells required from the MSU SCMOS library were picked up with the help of menu driven commands. These cells were

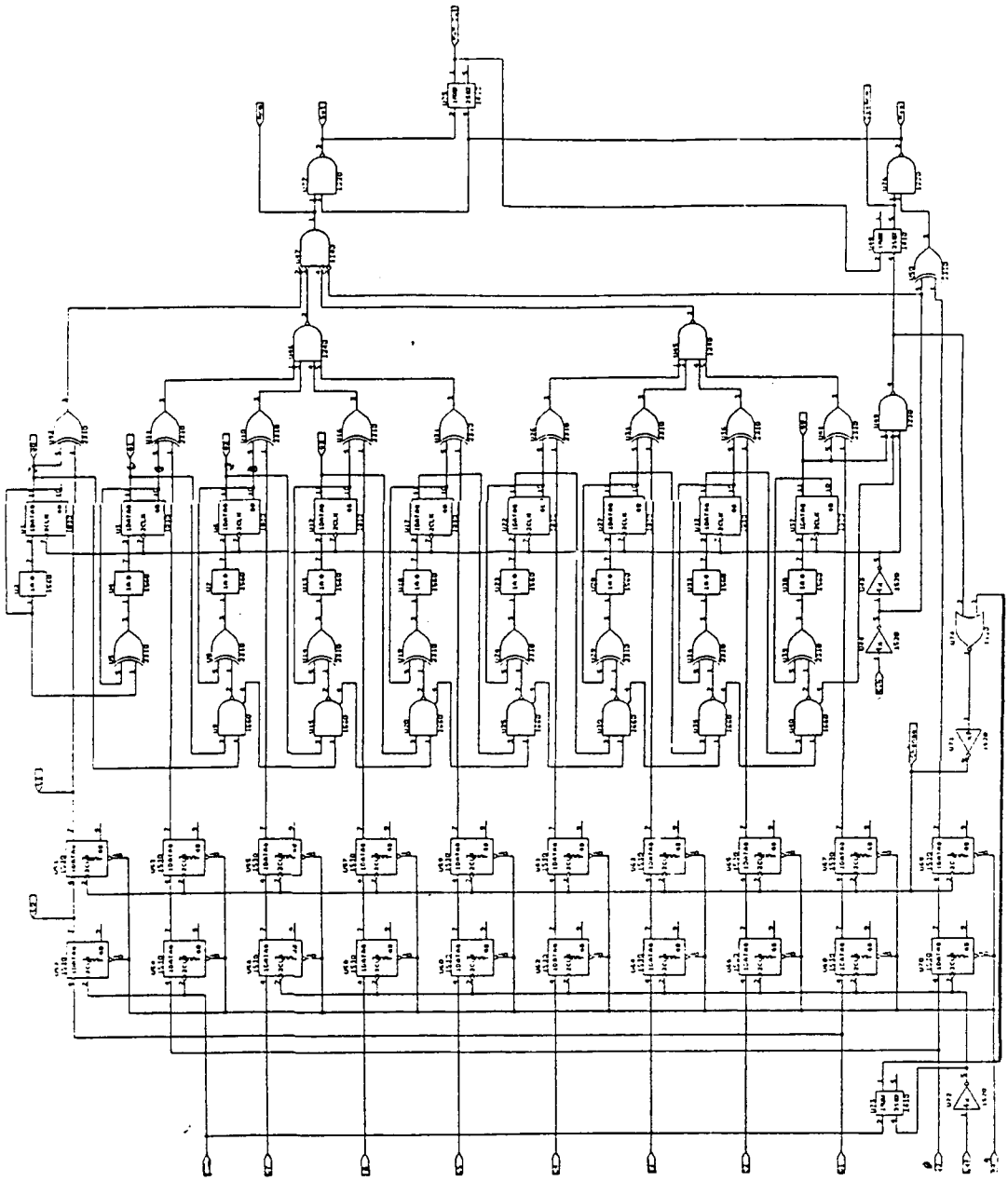


Figure 4.1: Schematic Capture Layout of PWM

then placed on the monitor and routed together as required with the help of a 3-button mouse. Schematic capture of the entire design [Figure 4.1] was accomplished and a valid electronic design file (*pwm.edf*) was generated. This file specified the interconnections between the 'leaf cells' and provided a valid net-list of the various elements in the design. The file was then transferred to the Sun workstation at the University.

On the Sun workstation the entirely automated standard cell placement and routing packages, *TimberwolfSC* and *YACR* (Yet Another Channel Router) were invoked to provide an optimal layout based on the simulated annealing technique [24,25]. After performing an initial random placement, *TimberwolfSC* and *YACR* converged to provide a cell placement specification, with externally appearing node labels, ready to be routed to the pad frame. These packages are described more precisely in the CAD tool description in this chapter. Figure 4.2 depicts the final layout of PWM as it appeared after the automated placement and routing was accomplished. *Wolfe* placed the original schematic [Figure 4.1] in 7 rows with the standard cells abutting each other to utilize silicon area efficiently.

4.3 Simulation, Testing, and CAD tools

An entirely new concept was used in the testing procedure. The only form of simulation that was done, was with the *Douglas CAD* simulator on a Mac-II. Absolutely no simulation was done on the Sun workstation before the *cif* was mailed to MOSIS. Proficiency with the use of the cad tools, and success encountered in the original DARC project simplified the layout process. Care was taken to meet all required design rule specifications, and accurate routing to the 28-pin tiny chip stuffed pad frame was estab-

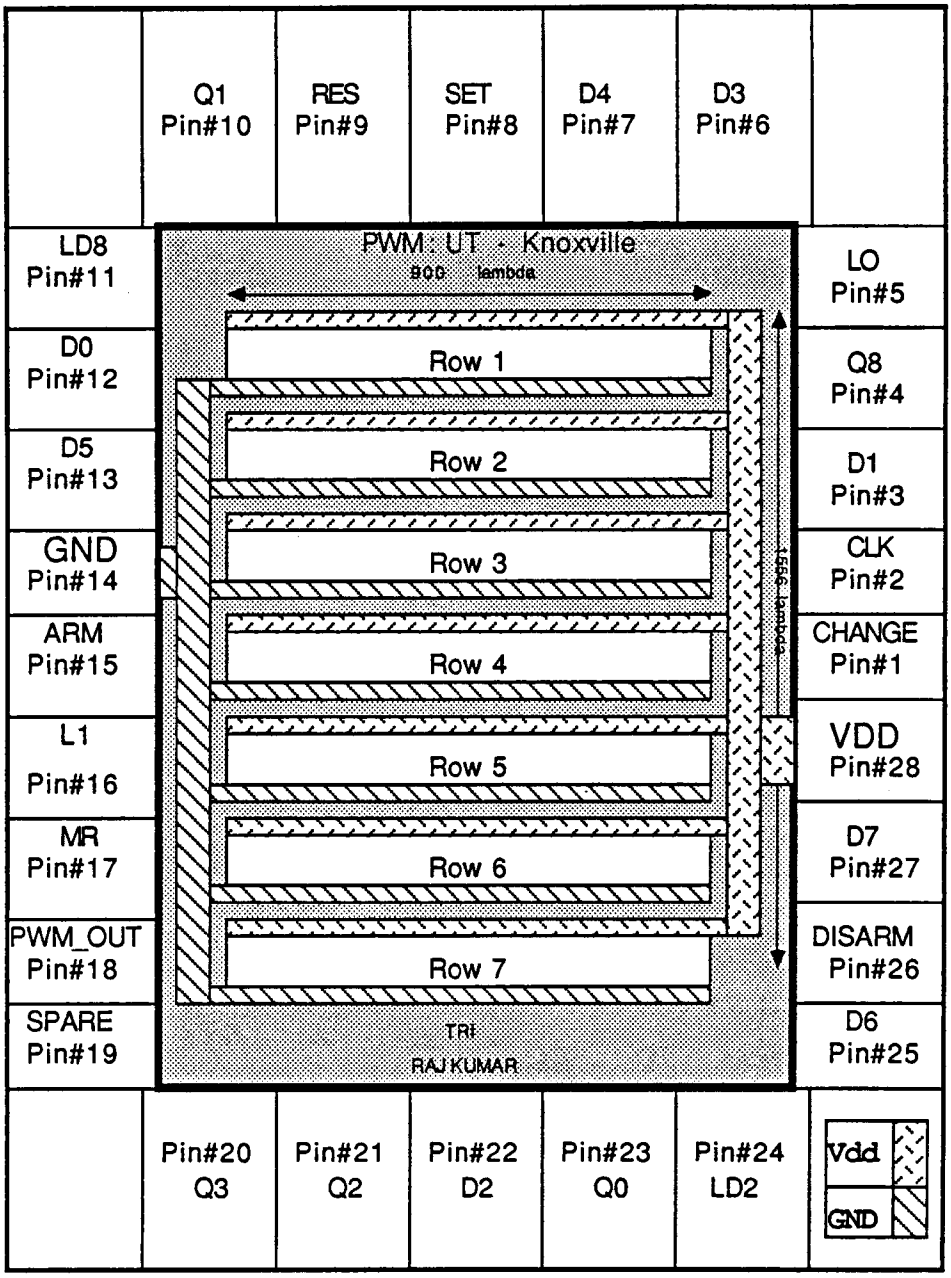


Figure 4.2: Layout and Floorplan of PWM

lished. The lack of time, in order to meet the fabrication deadlines, prevented us from simulating the design on the Sun Workstation.

In the internal configuration of PWM several access points were introduced to enhance observeability and controllability of the functional attributes of the chip. As was done in the case of DARC, prototype hardware was ready for testing the chip before it returned from MOSIS. Test routines were once again writtten in FORTH. The results obtained are summarized in Chapter 7.

The flowchart for the design proceedure followed in implementing PWM is shown in Figure 4.3. Though no PLA's were intoduced within PWM, the flowchart indicates the facilitites available for future designers at the University of Tennessee, Knoxville.

OrCad is used for schematic capture of the functional design. *OrCad* has an associated high-level simulator with it, that enables the designer to specify various test vectors and check his design at the highest level of heirarchy. Once satisfactory results are obtained a valid electronic design file *edf* is generated. This file specifies the interconnections between the 'leaf cells', and a net-list of the various elements in the design. A format translator, *ed2bd*, converts this file, to create the required and necessary view of the file. *TimberWolf*, and *YACR* are then invoked to provide optimal layouts. *Wolfe* is a standard cell placement and global routing package. The input to *Wolfe* is a standard net-list, and based on the phenomenon of 'probabilistic hill climbing' [24,25,22] minimization of the number of wiring tracks required to route the chip is enforced. Software defined adjustments include cell orientation, neighboring cell interchanges, and row shifting. *YACR*, a two-layer symbolic router then takes over and completes the final routing. If PLA's are required, a similar strategy, as that encountered with the custom designed chips, is enforced. *Espresso* and *bdsyn* are normally

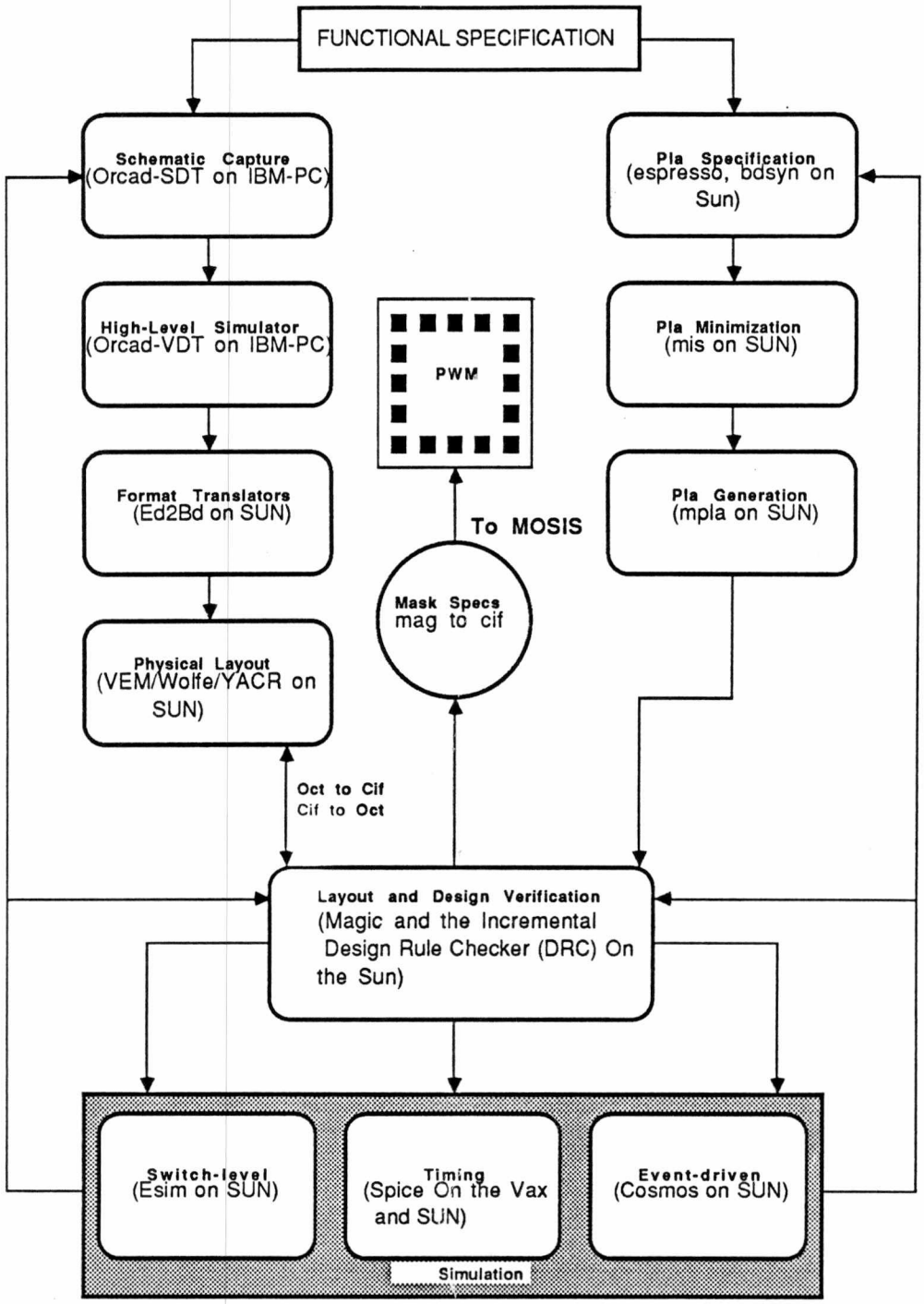


Figure 4.3: PWM Design Flow

used to generate Boolean-equation minimization, and *mpla* to produce the SCMOS layout for the combinational logic. Again format converting routines, *ext2sim*, *sim2spice*, *etc.* convert the files to be understood by the various simulators, *esim*, *cosmos*, *spice*, *relax*, *etc.* Multiple iterations, are carried out to interact with the various problems encountered during debugging with the simulators. A major disadvantage, is of course, wasted use of *cpu* time.

4.4 Resulting Design

The final pin configuration as it appears on the 28 pin-DIP is shown in Table 4.2. The result of the effort was a 28-pad die with external area dimensions of 1533×2266 λ^2 (2300×3400 micron^2) in the 3μ p-well SCMOS technology. The final layout of the *mag* view of PWM is shown in Figure 4.4. The internal available silicon area on the standard tiny chip frame was 1137×1870 λ^2, whereas the actual optimized PWM layout from *TimberWolf* was 900×1556 λ^2. The chip was packaged in a 28-pin DIP by MOSIS, and fabricated by HP (Hewlett Packard). PWM returned to the University of Tennessee, Knoxville in April, 1988 and was tested at TeleRobotics International, Inc. The results of this venture are also summarized in Chapter 7.

Table 4.2: Pin Description of PWM

PIN #	NAME	TYPE	FUNCTION
1	CHANGE	Output	Clock for the second set of latches
2	CLK	Input	Main clock for PWM
3	D1	Input	Data bit-1 input to the holding latch
4	Q8	Output	Counter's most significant bit output
5	LO	Output	Externally indicates lowest bit data
6	D3	Input	Input data bit-3 to holding latch
7	D4	Input	Input data bit-4 to holding latch
8	SET	Output	Overflow output of presettable counter
9	RES	Output	Resets external circuitry when required
10	Q1	Output	Least significant bit of the counter
11	LD8	Input	Loads the (8-bit) required data on counter
12	D0	Input	Input data bit-0 to holding latch
13	D5	Input	Input data bit-5 to holding latch
14	GND	Power	Ground pin for PWM
15	ARM	Output	Enables required data out
16	L1	Output	The test point output from the latches
17	MR	Input	Master reset, resets the counter to 0
18	PWM_OUT	Output	PWM drive the motors
19	SPARE	Unused	This pin is currently unused
20	Q3	Output	Third bit output of the counter
21	Q8	Output	Fourth bit output of the counter
22	D2	Input	Input data bit-2 to holding latch
23	Q8	Output	Counter's least significant bit output
24	LD2	Input	Loads 1'st two bits of data on counter
25	D6	Input	Input data bit-6 to the holding latch
26	DISARM	Output	Disables access to the pwm_output
25	D7	Input	Input data bit-7 to the holding latch
28	VDD	Power	The Power connection for PWM

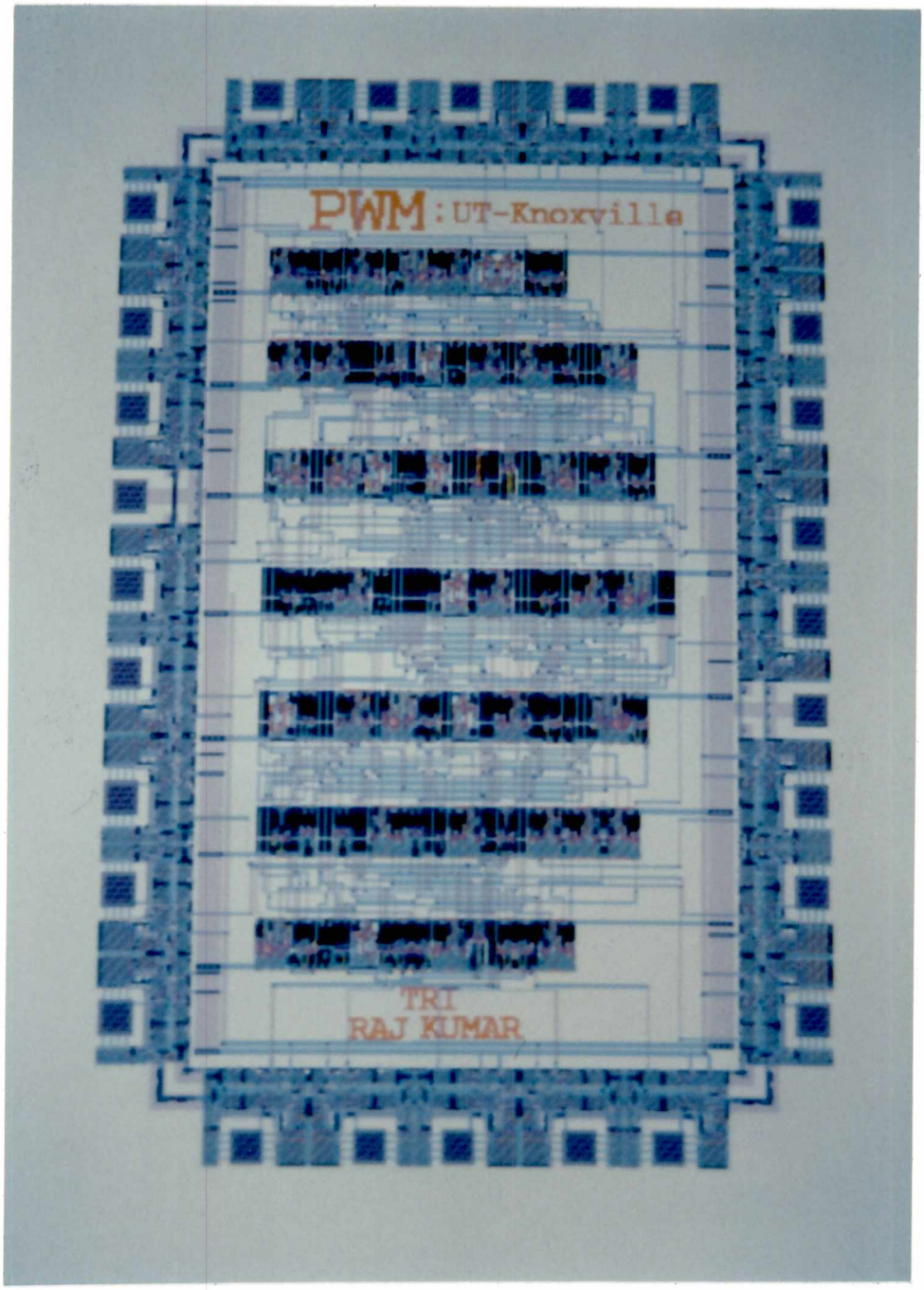


Figure 4.4: Photograph of the *Mag* layout of PWM

CHAPTER 5

THE DESIGN AND IMPLEMENTATION OF PWM2

Dual Pulse Width Modulator generators and digital I/O (PWM2) were realized with a concept similar to that used in designing PWM. This ASIC was also designed with pre-defined cells from a standard cell library (MSU library). An automated approach was encounted in the design, with access to several of Berkeley's new software packages. Improvements in the VLSI/CAD tools consisted of a faster and improved version of *Timberwolfe* and *YACR*, and a change in technology from the 3μ SCMOS to a 2μ SCMOS run. The requirement to place more standard cells in a single package, in order to perform dual pulse width modulation and digital interfacing, led to 2μ run, in a 40-pin package.

5.1 Hardware Considerations

5.1.1 Functional Specification

PWM2 is designed to provide dual pulse width modulation, and parallel I/O interface circuitry for the DAME project. The amplifiers used are the AMC-250D, which are similar to those explained in Chapter 4. PWM2 is designed to work at above 24 MHz and provide a variable duty cycle of approximately 48 KHz. In all, PWM2 utilizes 40 pins. Of these 21 are input pads, 7 are output pads, 8 are quasi-bidirectional, and six pads are used for power and ground. Internally, superbuffers are used to provide large

Table 5.1: Standard Cells Used in the Design of PWM2

ITEM NUMBER	CELL NUMBER	FUNCTION/ DESCRIPTION
1	1120	2-Input Nor
2	1140	4-Input Nor
3	1220	2-Input Nand
4	1230	3-Input Nand
5	1240	4-Input Nand
6	1350	Data Select
7	1410	Nand Latch
8	1520	4x-Inverting Buffer
9	1530	Clocked Latch W/Reset
10	1560	Delay cell
11	1660	2-Input Nand/And
12	1830	D Flip-Flop w/Q and Qbar
13	2310	2-Input Ex-OR

drive capabilities where required. The standard cells used in the design are shown in Table 5.1. Specification for each of cells are provided along with the basic cells [23].

5.1.2 Functional Description

FUNCTION: Provide Dual Pulse Width Modulation and Parallel I/O:
Accept 10-bit signed integer motor-drive command and produce a
40 KHz variable duty-cycle waveform to directly drive the AMC-250D,
and provide parallel interface ports for communication

In terms of its functionality, a single Pulse Width Modulator in PWM2 is exactly similar to PWM. The schematic for the PWM was shown earlier in Figure 4.1, page 51. PWM2's functionality is enhanced in that it is capable of Dual pulse width modulation and parallel interfacing. It basically is comprised of two identical PWM's. The working of an individual PWM is described in Chapter 4. The input to the PWM2 is over

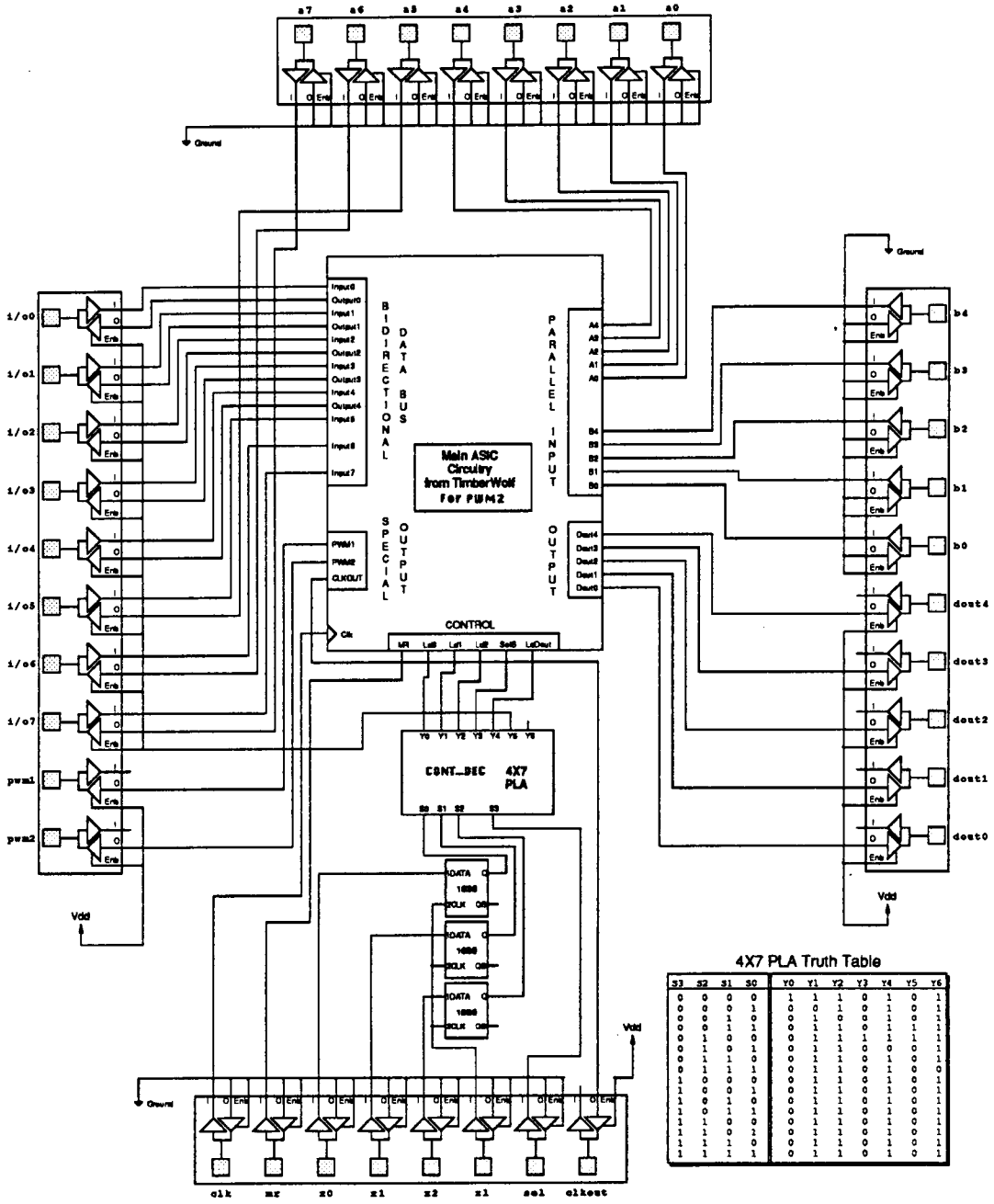
the 8-bit data bus (D0-D7). The inputs are interfaced with the main processor. The required output of PWM2 are the *pwm1* and *pwm2*.

The schematic of PWM2 is a twin replication of the schematic shown in Figure 4.1, page 51. The only additional circuitry introduced was additional latches and data selectors for the Parallel I/O. These data selectors enable data into the chip providing for efficient communication.

5.2 Layout and Floorplan

The primary layout of PWM2 was done with the *OrCad* package on the an IBM-PC, at TeleRobotics International, Inc. Similar techniques to that used in designing PWM, were employed in routing together the standard cells. Schematic capture of the entire design was accomplished and a valid electronic design file (*pwm2.edf*) was generated. This file, that specified the interconnections between the 'leaf cells', was transferred to the Sun workstation at the University of Tennessee. The expected, functional layout and routing to the pad frame are shown in Figure 5.1. This functional layout also shows the truth table of the PLA (Cont_Dec) that was implemented within PWM2.

On the Sun workstation an improved version of the automated standard cell placement and routing packages, *TimberwolfSC* and *YACR* were invoked to provide an optimal layout. After performing an initial random placement, *TimberwolfSC* and *YACR* converged to provide a cell placement specification, with externally appearing node labels, ready to be routed to the pad frame. An additional PLA, generated by *espresso* and *mpla*, and three latches, were added to the final layout achieved by *wolfe*. Figure 5.2 depicts the final layout of PWM2 as it appeared after the automated placement



4X7 PLA Truth Table

S3	S2	S1	S0	Y0	Y1	Y2	Y3	Y4	Y5	Y6
0	0	0	0	1	1	1	0	1	0	1
0	0	0	1	0	0	1	0	1	0	1
0	0	1	0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0	1	1	1
0	1	0	0	0	1	1	1	1	1	1
0	1	0	1	0	1	1	0	1	0	1
0	1	1	0	0	1	1	0	1	0	1
0	1	1	1	0	1	1	0	1	0	0
1	0	0	0	0	1	1	0	1	0	1
1	0	0	1	0	1	1	0	1	0	1
1	0	1	0	0	1	1	0	1	0	1
1	0	1	1	0	1	1	0	1	0	1
1	1	0	0	0	1	1	0	1	0	1
1	1	0	1	0	1	1	0	1	0	1
1	1	1	0	0	1	1	0	1	0	1
1	1	1	1	0	1	1	0	1	0	1

Figure 5.1: Functional Layout and Floorplan of PWM2

and routing was accomplished, the additional circuitry introduced, and final routing accomplished. *Wolfe* was forced to place the original schematic in 8 rows, and room was made for the additional PLA and the required latches.

5.3 Simulation, Testing, and CAD tools

Though a major part of the similation was done with the *Douglas CAD* simulator on a Mac-II, after the final routing to the pads was completed some simulation of the functionality of PWM2 was done with *esim* before the *cif* was mailed to MOSIS. Proficiency with the use of the CAD tools, and success encountered in the original PWM project simplified the layout process. Care was taken to meet all required design rule specifications, and accurate routing to the 40-pin tiny chip stuffed pad frame was established.

In the internal configuration of PWM2 a few access points were introduced to enhance observeability and controllability of the functional attributes of the chip. PWM2 was mailed to MOSIS on July 14th, 1988 and is expected to return to the University of Tennessee around about August 14th, 1988.

The strategy adopted in the use of CAD tools is the same as that depicted in the flowchart shown for the implementation of PWM2 [Figure 4.3, page 55]. A single PLA was intoduced within PWM2 and was generated with *espresso* and *mpla*.

5.4 Resulting Design

The final pin configuration as it appears on the 40-pin package is shown in Table 5.2. In order to maintain consistency and uniformity in notation, in order to develop a

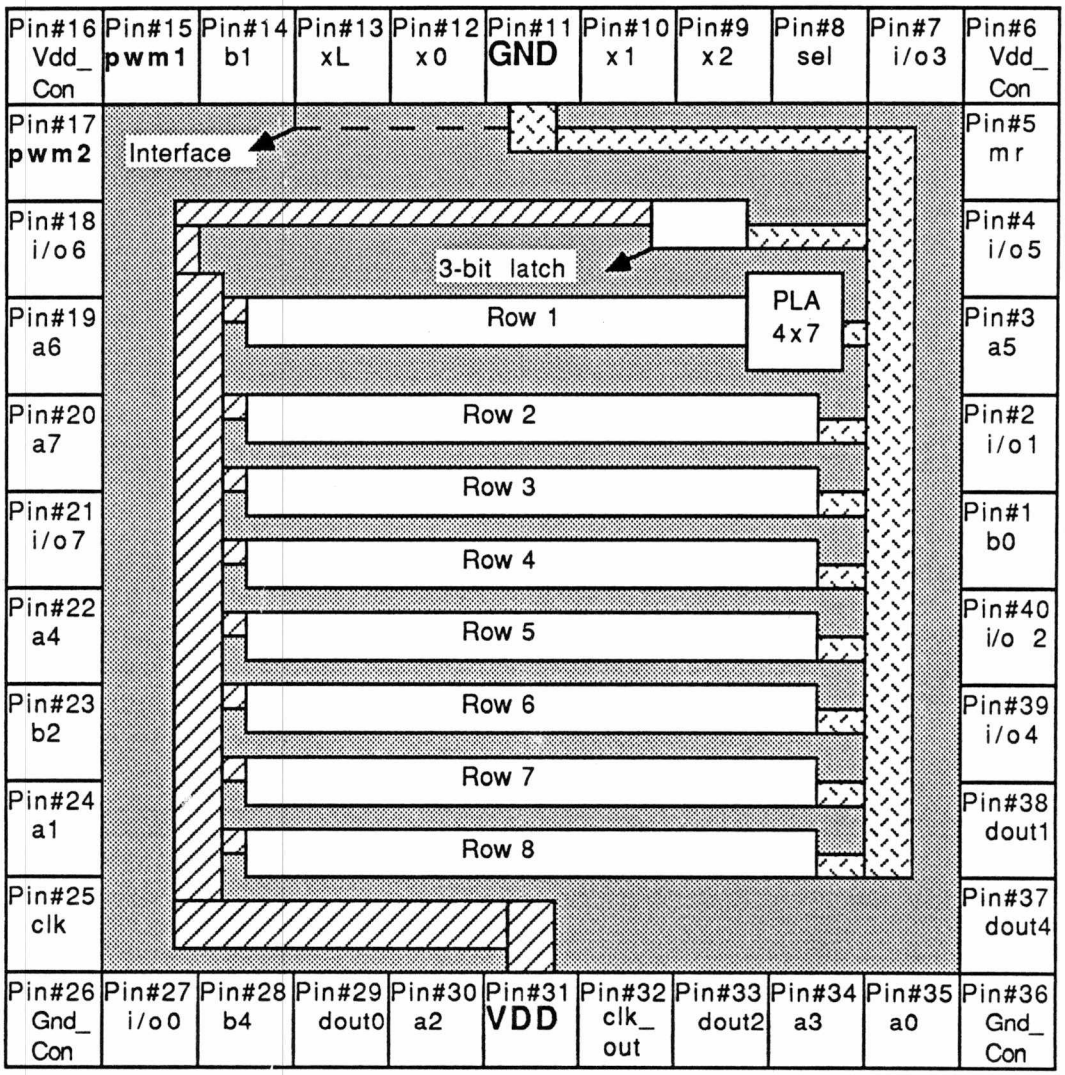


Figure 5.2: Physical Layout and Floorplan of PWM2

standardized chip, lower-case alphabets are used throughout the description of PWM2. The result of the effort was a 40-pad die with external area dimensions of 2222×2252 λ^2 (2220×2250 micron^2) in the 2μ SCMOS technology. The final layout of the *mag* view of PWM2 is shown in Figure 5.3. The internal available silicon area on the standard tiny chip frame was 1793×1823 λ^2, whereas the actual optimized PWM2 layout from *TimberWolf* was 1039×1893 λ^2. The chip is currently being packaged in a 40-pin package by MOSIS, and fabricated by VTI (VLSI Technology, Inc). At this stage PWM2 has not yet returned to the University of Tennessee and its arrival is anicipated with great enthusiasm, being the first chip to be developed at UTK in the 2μ SCMOS, n-well process.

Table 5.2: Pin Description of PWM2

PIN #	NAME	TYPE	FUNCTION
1	b0	Input	LSB of parallel input portB
2	i/o1	QBD	Quazi Bi-directional pin #1
3	a5	Input	Parallel input portA pin#5
4	i/o5	QBD	Quazi Bi-directional pin #5
5	mr	Input	External 'master reset' for both PWM's
6	Vdd	Power	Power pin#1 for PWM2
7	i/o3	QBD	Quazi Bi-directional pin #3
8	sel	Input	Control the PLA (Cont_Dec) Operation
9	x2	Input	Latched Input Data pin#2
10	x1	Input	Latched Input Data pin#1
11	x2	Input	Latched Input Data Pin#0
12	xL	Input	Interfaced enable for 3-bit latch
13	b2	Input	Second bit of parallel input portB
14	b1	Input	First bit of parallel input port
15	pwm1	Output	Pulse Width Modulated drive #1
16	Vdd	Power	Power pin for PWM2
17	pwm2	Output	Pulse Width Modulated drive #2
18	i/o6	Input	Sixth bit of parallel input port
19	a6	Input	Parallel input portA pin#6
20	a7	Input	Parallel input portA pin#7
21	i/o7	QBD	Quazi Bi-directional pin #7
22	a4	Input	Parallel input portA pin#4
23	b2	Input	Second bit of parallel input portB
24	a1	Input	Parallel input portA pin#1
27	i/o0	QBD	Quazi Bi-directional pin #0
25	clk	Input	Basic Clock input for both PWM's
27	i/o0	QBD	Quazi Bi-directional pin #0
28	b4	Input	Forth bit of parallel input portB
29	dout0	Output	Output port data-bit 0
30	a2	Input	Parallel input portA pin#2
31	Vdd	Power	Power pin for PWM2
32	clk_out	Output	Second bit Output of the counter
33	dout2	Output	Output port data-bit 2
34	a3	Input	Parallel input portA pin#3
35	a0	Input	Parallel input portA pin#0
36	Gnd	Power	Gnd Pin for PWM2
37	dout4	Output	Output port data-bit 4
38	dout1	Output	Output port data-bit 1
39	i/o4	QBD	Quazi Bi-directional pin #4
40	i/o2	QBD	Quazi Bi-directional pin #2

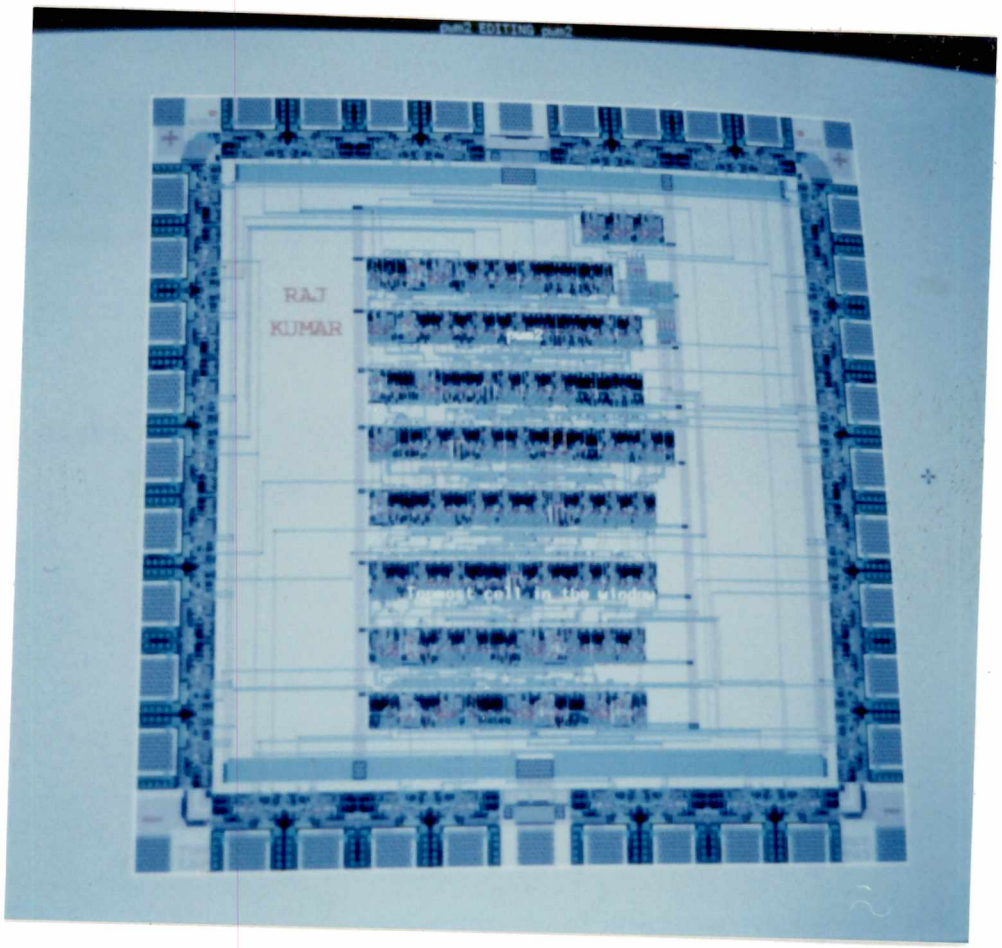


Figure 5.3: Photograph of the *Mag* layout of PWM2

CHAPTER 6

CUSTOM DESIGN VERSUS STANDARD CELL DESIGN

6.1 Decision Making Criteria

This chapter presents a comparison between the three designs that were explained in the earlier chapters. DARC was implemented as a custom ASIC, PWM, and PWM2 as standard cell ASIC's. The criteria for selecting either custom or standard cell designs to implement ASIC's are listed below:

- Transistor count required
- Total time to implement design
- Total time from concept to market
- Availablity of computing equipment
- Total cost including design, prototyping and production
- Number of units required for production
- Service record of vendor

The basic principle is that cost savings increases as the level of integration and the number of units required increases. DARC, PWM, and PWM2 were implemented based on the above requirements. A comparison of the two styles of VLSI design follows.

6.2 A Relative Comparison

6.2.1 Silicon Utilization

DARC, PWM, and PWM2 were designed to functionally perform pulse-width modulation. Figures 4.2 (page 53), 4.4 (page 58), and Figures 5.2 (page 64), 5.3 (page 67 show the final placement of all elements used in the standard cell design of PWM and PWM2 respectively. Figures 3.8 (page 37) and 3.11 (page 47), on the other hand show the layouts for the custom designed DARC. DARC has three pulse-width modulated waveform generators defined within its silicon area. Though these pulse-width modulators are more complex when compared to PWM, the area utilized in putting together the required circuitry is far less on the custom chip. DARC used only $400\times1100\ \lambda^2$ for a single pulse width waveform generator, compared to PWM's using $900\times1500\ \lambda^2$. As can be seen from the layouts, custom design is capable of achieving a more symmetric layout, reduced routing, compact placement, and hence more efficient use of silicon area. On the other hand, standard cell designed ASIC's, designed with automated tools lose silicon area in the channel spacing provided for routing between the rows of the layout or macro block. The automated tools also have the disadvantage of introducing 'feed cells' within the rows. PWM when run through *Wolfe* and *YACR* introduced 54 feed cells between the simple design structure causing a total loss of silicon of $48384\lambda^2$, where each individual feed cell was $8\times112\ \lambda$. The improved version of *Wolfe*, however did not introduce any 'feed cells' within the layout of PWM2. Silicon area was lost only due to channel routing, and the pre-defined standard cell sizing.

6.2.2 Design Time

Four man-months were spent on designing and implementing DARC, as compared to four man-weeks spent in implementing PWM and PWM2, individually. In designing DARC, a major amount of time, was spent in layout and floor plan considerations. Most of the CAD tools were also fairly new at the University of Tennessee, and quite some time was spent understanding their use. Since the procedure adopted was custom design, more complex circuitry and self-designed cells evolved. The external pad frame for DARC was created at the University of Tennessee, since no stuffed frame was readily available as in the case of PWM. Independent cells had to be simulated several times, in order to ensure their working in real time. Bugs had to be detected not only in the design, but also in the software used. PWM on the other hand, was almost completely automated. Standard cells and automated placement and routing tools, such as, *Wolfe* and *YACR* were used. For PWM, no simulation was done on the Sun and as a result, the design was developed much faster. In the case of PWM2, the overall routing, the PLA, the interface, and the power rails were briefly tested with *esim* before the chip was mailed to MOSIS.

6.2.3 Turnaround Time

DARC was mailed to MOSIS for fabrication on September 30th, 1987, whereas PWM was sent on February 25th, 1988. Both DARC and PWM took about 10-12 weeks, from the time they were sent to MOSIS, to be fabriacted by the vendor, packaged by MOSIS, and returned to the University of Tennessee. Both DARC and PWM were fabricated by Hewlett Packard (HP). Currently both the standard cell designs and custom designs have regular monthly runs. PWM2 was submitted to MOSIS for fabrication on July

14th, 1988. It is expected back in about a month, around August 14th, 1988.

6.2.4 Computer Time

In designing DARC, a great deal of *cpu* time (600 hrs) was used to re-extract and simulate functional modules. PWM on the other hand was only routed out to the pads after final placement and loose routing. Though some *cpu* time was used, in exploiting the benefits of *Wolfe* and *YACR*, it was comparatively negligible to that used for DARC.

6.2.5 Production cost

This includes design and fabrication costs. The design cost is accounted for in the installation of software and hardware used by CAD designers, and computer time spent on implementing the design. Fabrication costs are compared here. DARC was fabricated on a commercial run through MOSIS, at a cost of $2800. PWM, on the other hand, cost a meagre $400. Twelve packaged chips were returned by MOSIS for the custom design (DARC) and four for the standard cell design (PWM). A dozen unpackaged dies also came with both chips. This roughly puts the cost for the fabrication at $84 per custom chip, and $25 per standard cell chip. PWM2 is expected to cost $600 for four packaged chips and a dozen dies, which averages the cost for a 2μ 40-pin tiny chip run to be estimated at $37.50 per chip.

6.2.6 Layout Definitions

Designing circuits as custom modules allows for a more regular and symmetric layout. As can seen from Figure 3.8 (page 37) and Figure 4.2 (page 53), the pad definitions for DARC are more orgainized and systematic. PWM and PWM2, though, have their pins

defined in a hap-hazard fashion. The automated tools caused this problem. To ease the strain on the designer's routing abilities, and save time in order to meet the fabrication deadlines, the shortest and simplest 'manhattan paths' where used to route to the pad frame.

6.2.7 Computing Equipment

To date, the University of Tennessee, Knoxville's CAD/VLSI equipment and software are unparalleled. Throughout the implementation of DARC, PWM, and PWM2, new equipment and software was purchased and installed, to meet the designers requirements. Though there does not seem to be an end for the development of new and advanced CAD/VLSI software tools, the University's quest to bring to its designers the latest resources available will never fade away. Currently available tools have been discussed in greater detail in Chapter 3 and Chapter 4.

CHAPTER 7

RESULTS, SUMMARY, AND CONCLUSIONS

7.1 Results Obtained

Both DARC and PWM were functional on first silicon. PWM was fully functional, and DARC was approximately 60% functional. PWM2's results, are at this stage patiently, but confidently awaited. PWM, though expected to work at 10 MHz, accurately worked at 18 MHz capable of producing a 36 KHz variable duty cycle. The chip was used to drive the amplifiers which in turn drove the motors, as the software routines commanded. Most of the 'leaf cells' designed for DARC were functional. The design frame, the quasi bi-directional bus, and all the specified SSI functions were functional. The control circuitry, the I/O ports, internal latches, tristate devices, miscellaneous logic, the CLK, and all super-buffers, performed excellently. One basic problem was in our definition of pin 1 as a test pin, instead of as a substrate connection. We determined that the digital filter's were not working as their test-out points showed no valid changes of input data. The delay elements introduced at a very late stage in the design were probably one of the main causes for the filters malfunction. Another cause could most likely be the improper estimation of the power and ground rails for the digital filters. One of the counter's 'leaf cell's' in the PWM generators also failed to operate.

7.2 Problems Encountered During the Design and Testing

Several reasons contributed to the delay in the design and implementation of DARC and PWM. Of these, the major setbacks, are discussed below.

Late Changes in the Design:

Though an adequate amount of functional modelling was done, repetitive changes in the design caused major negative effects. Frequent changes in the layouts were made and very often we found ourselves trying to make room for a new element within the final layout.

Inadaquate Floor Plan and Layout Definitions:

No floorplan was laid out in the initial stages of the design, as a predefined pad frame was not available at that time. The sizes of the various 'leaf cells' was unknown at the initial stages. It was only later on in the design that we found ourselves scrounging for space. As a result, several pre-designed, tested blocks were not implemented. A bottom-up design venture was attempted, which created serious problems in the latter stages. The intent to integrate more functional modules within DARC caused repeated changes in the intended floor plan.

Inadaquate Timing Verification:

In a mad rush to meet MOSIS's deadlines and fabricate DARC most of the Spice testing was omitted. Insufficient simulation of the 'leaf cells' caused problems when the chip was simulated at the top level, and an iterative process in detecting early errors was a major setback.

CAD Tool Deficiencies:

The general saying is – "If you need a CAD tool, stop and get it!" Several bugs were detected in the existing CAD tools, but time restrictions prevented us from correcting these tool deficiencies. The simulators incompetence to handle large circuits, understand basic cells such as the EX_OR, not verify electrical protection requirements, and to not estimate well resistances were major drawbacks. *Magic* ran out of virtual memory several times. Format translators, such as *sim2spice*, did not recognize resistive values.

Global Understanding Limitations:

VLSI is considered 'too thin-tall for one man to know it all'[20]. There were not enough people with a global understanding of the chip (DARC) and its layout definitions. Though TeleRobotics International, Inc. assisted a great deal in the simulation procedure, most of the implementation, layout, and communication with the several new cad tools was done by the designer.

Unfamiliarity with Custom design and VLSI/CAD tools:

This is another basic setback in the design. Lack of sufficient documentation, communicating with the available software, and understanding several concepts of custom design restricted the design during the initial stages.

Insufficient On Chip Testing:

As the hardest part in any design, the fault location coverage internally within the chip, was not accurately specified. Heuristics determined faults encountered by functional building blocks. It was rather difficult to pin-point which node was stuck at a partic-

ular value. ATPG (Automatic Test Pattern Generators) were unavailable during the implementation of DARC.

7.3 Summary and Conclusions

An overview of the DAME project, with requirements for miniaturized control circuitry and digital computation, has been presented. The development of this miniaturized control system architecture allowed for a flexible and overall compact system. A key to the successful implementation of the concept of miniaturization of the servo electronics was achieved with VLSI technology. The basic concept behind DAME, its hardware and software considerations, and the constraints on the design that led to the introduction of DARC, PWM, and PWM2 are specified.

DARC, a 64-pin DIP, was designed and implemented in the 3μ SCMOS technology. It replaced several bulky cables, over 130 SSI/MSI CMOS and TTL circuits, and had a bit resolution that was far greater than what is available with off-the-shelf components. Functionally, it performs optical decoding, pulse-width modulation, and I/O interfacing with the main processor. The design methodology and various aspects in custom VLSI design have been presented. The different CAD/VLSI tools used in the design were discussed.

PWM, a 28-pin DIP, was implemented using an entirely new strategy. Automated CAD/VLSI tools and pre-defined standard cells that efficiently reduced design time were used. PWM is a pulse-width modulated waveform generator with a 10-bit resolution.

PWM2, a 40-pin 2μ tiny chip, was implemented using improved and more efficient CAD/VLSI tools. Dual pulse width modulation and parallel I/O were the specified

functions of PWM2. The 2μ SCMOS run is anticipated to produce faster operating speeds. It has proved the level of integration and the tranistor count approximately doubled with the switch from the 3μ technology.

A comparison between the custom design circuit (DARC) and the standard cell design (PWM and PWM2) was detailed. The comparison was based on silicon utilization, design time, turnaround time, computer time, production cost, layout definitions, and computing equipment.

Several problems were encountered during the design process. It is important that every new designer understands these stumbling blocks and pitfalls in VLSI design. As a stepping stone to both custom and standard cell design, this thesis would probably be a good backbone to fresh designers. The author suggests that future designers read this thesis, and anticipate the likely setbacks in design, before commencing their respective projects.

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BIBLIOGRAPHY

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APPENDICES

APPENDIX A

Switch-Level/Event-Driven Simulation

Of primary and utmost importance in VLSI design is the phenomenon of testing. It is next to impossible to test a large circuit for a 100% fault coverage or with all possible vectors. Exhaustive testing, could probably take years, and computer-time bills could mount up 'stack high'. It is important for the designer to understand, that in order to achieve good results , he has to be capable of efficiently communicating with the available software. He should be well conversant with the various packages available, and understand the functionality of his basic design thouroughly. The desire to learn, the designers sharpness to pick-up errors, and the ability to communicate with the software, will allow for functional chips.

In these sections we outline, how DARC and PWM2 were tested with the available Switch-level/event-driven simulator, *esim*. Since DARC was a complex chip with 64 global signals to account for, *esim*, was very often confused and not understandable. But, as a fundamental advantage, it picked up some major errors in design and routing. It is an excellent simulator for higher levels of heirarchy and for global input definitions, since it is comparatively much faster than Spice and Relax. The amount of *cpu* used by esim is also relatively lower when compared to the other simulators. *Esim*, as any other simulator, has its own flaws. It is incapable of understanding the ex_or gates, sense amplifiers, and quite often has problems with transmission gates.

In the design of DARC, *esim* was the most convienent and user friendly simulator

available. Initially, the 'leaf cells' designed were simulated with multiple passes through the data base, and minor errors detected and instantaneously rectified. Almost all possible states of the basic cells designed were efficiently simulated with *esim*. At higher levels, functional modules such as a 16-bit counter, a 9-bit presettable counter, 8-bit tristate latches, *etc* were simulated to check their functionality. The next stage was the simulation of the sub-systems, 'pwm', 'resol', 'opt', *etc*. Finally, a global simulation on the entire chip DARC was encountered, and it was here that several basic problems began to occur. We managed to overcome these problems, and simulate the entire chip at the highest level of hierarchy.

A few examples of the control and result files generated with *esim* are shown below. The first set of files are the input and output files used in the simulation of a latch. The simulation indicates the D, clock, and reset input, along with the Q and Qbar outputs.

```
I
I
w CLK D Q Qbar CLEAR
V CLK    0000001000100010001000100010001000100010000000
V D      0000011100000100000001100000001000000000000
V CLEAR 01111111011111111111111111111111111111111111
G

30 transistors, 20 nodes (0 pulled up)
initialization took 27 steps
initialization took 0 steps
>0000001000100010001000100010001000100010000000:CLK
>0000011100000100000001100000001000000000000:D
```

```
>000000110000001111000011110000000000000000:Q
>111111001111111000111100001111111111111111:Qbar
>011111110111111111111111111111111111111111:CLEAR
30 transistors, 20 nodes (0 pulled up)
```

As a second example is shown the input and output files of the pwm counter. Though several lengthy files were generated to test the counter, the file shown below indicates only a small portion of one of the files used. Nine counter outputs (Q0-Q8) are indicated along with the clock and carry output of the counter.

```
I
I
w Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 carry clk
V load 0000000000000000000000000000000000000000000000000000000000000000
V clk  0101010101010101010101010101010101010101010101010101010101010101
G
V load 0000000000000000000000000000000000000000000000000000000000000000
V clk  0101010101010101010101010101010101010101010101010101010101010101
G
V load 0000000000000000000000000000000000000000000000000000000000000000
V clk  0101010101010101010101010101010101010101010101010101010101010101
G
V load 0000000000000000000000000000000000000000000000000000000000000000
V clk  0101010101010101010101010101010101010101010101010101010101010101
G


506 transistors, 268 nodes (0 pulled up)
```

```
initialization took 473 steps

initialization took 0 steps

>00000000000000000000000000000000000000000000000000000000:Q8

>00000000000000000000000000000000000000000000000000000000:Q7

>00000000000000000001111111111111111111111111111111111111:Q6

>11111111111111111100000000000000000000000000000000000000:Q5

>11111111111111111100000000000000000000000000000000111111:Q4

>00011111111111111100000000000000011111111111111111000000:Q3

>01100000000111111110000000011111111000000001111111000000:Q2

>01100001111000011110000111100001111000011110000111100011:Q1

>01100110011001100110011001100110011001100110011001100110:Q0

>00000000000000000000000000000000000000000000000000000000:carry

>01010101010101010101010101010101010101010101010101010101:clk

>00000000000000000000000000000000000000000000000000000000:Q8

>00000000000000000000000000000000000000000000000000000000:Q7

>11111111111111111111111111111111111111111111111111111111:Q6

>00000000000000000000000001111111111111111111111111111111:Q5

>11111111111111111111111110000000000000000000000000000000:Q4

>00000000001111111111111110000000000000001111111111111111:Q3

>00011111111000000001111111100000000111111110000000111111:Q2

>11100001111000011110000111100001111000011110000111100011:Q1

>01100110011001100110011001100110011001100110011001100110:Q0

>00000000000000000000000000000000000000000000000000000000:carry

>01010101010101010101010101010101010101010101010101010101:clk

>00000000000000000000000000000000000000000000000000000000:Q8

>00000000000000000000000000000001111111111111111111111111:Q7
```

```
>111111111111111111111111111111111100000000000000000000000:Q6
>111111111111111111111111111111111100000000000000000000000:Q5
>000111111111111111111111111111111100000000000000000000000:Q4
>111000000000000000011111111111111100000000000000000111111:Q3
>111000000001111111100000000111111110000000011111111000000:Q2
>111000011110000111100001111000011110000111100001111000011:Q1
>011001100110011001100110011001100110011001100110011001100:Q0
>000000000000000000000000000000000000000000000000000000000:carry
>010101010101010101010101010101010101010101010101010101010:clk
>000000000000000000000000000000000000000000000000000000000:Q8
>111111111111111111111111111111111111111111111111111111111:Q7
>000000000000000000000000000000000000000000000000000000000:Q6
>000000000000000000000000000000000000000000000011111111111111:Q5
>000000000001111111111111111111111111111111100000000000000:Q4
>111111111100000000000000001111111111111111100000000000000:Q3
>000111111110000000011111111000000001111111100000000111111:Q2
>111000011110000111100001111000011110000111100001111000011:Q1
>011001100110011001100110011001100110011001100110011001100:Q0
>000000000000000000000000000000000000000000000000000000000:carry
>010101010101010101010101010101010101010101010101010101010:clk
506 transistors, 268 nodes (0 pulled up)
```

APPENDIX B

Low-Level Timing Simulation

Several software packages for timing simulation are currently available at the University of Tennessee, Knoxville. These include *Spice*, *Relax*, and *Crystal*. During the design of DARC, some low-level timing simulation, with *spice* was done. Some of the 'leaf cells', were simulated for a transient respone. The major disadvantage in using *spice* is the *cpu* time. The basic 'leaf cells', in themselves take several minutes to run through a single iteration. On larger functional modules, *spice* takes almost forever to run. *Relax* is a simulator that is much faster than *spice*, and can be considered an intermediate simulator between event-driven and timing simulators. *Crystal* is a 'worst-case propogation delay' simulator.

The following example shows the simulation results obtained from a 'spice deck' of one of the 'leaf cells' used in the design of DARC. This cell is a negative-edge-triggered D_flip_flop. Plot 2.1 shows the the transient analysis response with the specified parameters, shown in the 'spice deck' created for D1. Node #22 is the Q output of the flip_flop, node #9 is the clock input, and node #6 is the D input. The cell has super-buffers at its input to provide larger current drive capabilities.

```
*******28-AUG-87 *******  SPICE 2G.5 (10AUG81)  *******01:04:10*****

*** SPICE DECK created from D1.sim, tech=scmos

****      INPUT LISTING                    TEMPERATURE =   27.000 DEG C

******************************************************************************


M1 1 6 5 4 CMOSP L=3.0U W=42.0U
M2 7 5 1 4 CMOSP L=3.0U W=82.5U
M3 1 9 8 4 CMOSP L=3.0U W=42.0U
M4 10 8 1 4 CMOSP L=3.0U W=82.5U
M5 11 7 1 4 CMOSP L=3.0U W=4.5U
M6 12 7 1 4 CMOSP L=3.0U W=4.5U
M7 14 13 1 4 CMOSP L=3.0U W=4.5U
M8 1 15 12 4 CMOSP L=3.0U W=4.5U
M9 12 16 1 4 CMOSP L=3.0U W=4.5U
M10 0 7 11 17 CMOSN L=3.0U W=4.5U
M11 18 15 1 4 CMOSP L=3.0U W=4.5U
M12 1 12 14 4 CMOSP L=3.0U W=4.5U
M13 14 1 1 4 CMOSP L=3.0U W=4.5U
M14 19 7 0 17 CMOSN L=3.0U W=4.5U
M15 20 15 19 17 CMOSN L=3.0U W=4.5U
M16 12 16 20 17 CMOSN L=3.0U W=4.5U
M17 15 10 0 17 CMOSN L=3.0U W=4.5U
M18 0 6 5 17 CMOSN L=3.0U W=27.0U
M19 7 5 0 17 CMOSN L=3.0U W=43.5U
M20 0 9 8 17 CMOSN L=3.0U W=27.0U
M21 10 8 0 17 CMOSN L=3.0U W=43.5U
M22 1 18 21 4 CMOSP L=3.0U W=4.5U
M23 21 14 1 4 CMOSP L=3.0U W=4.5U
M24 1 21 22 4 CMOSP L=3.0U W=4.5U
M25 22 16 1 4 CMOSP L=3.0U W=4.5U
M26 23 13 0 17 CMOSN L=3.0U W=4.5U
M27 24 12 23 17 CMOSN L=3.0U W=4.5U
M28 14 1 24 17 CMOSN L=3.0U W=4.5U
M29 0 15 18 17 CMOSN L=3.0U W=6.0U
M30 26 15 25 17 CMOSN L=3.0U W=4.5U
M31 27 11 26 17 CMOSN L=3.0U W=4.5U
M32 0 22 27 17 CMOSN L=3.0U W=4.5U
M33 28 25 13 17 CMOSN L=3.0U W=4.5U
M34 29 14 28 17 CMOSN L=3.0U W=4.5U
M35 0 1 29 17 CMOSN L=3.0U W=4.5U
M36 30 18 0 17 CMOSN L=3.0U W=4.5U
M37 21 14 30 17 CMOSN L=3.0U W=4.5U
M38 31 21 0 17 CMOSN L=3.0U W=4.5U
M39 22 16 31 17 CMOSN L=3.0U W=4.5U
M40 1 15 25 4 CMOSP L=3.0U W=4.5U
M41 25 11 1 4 CMOSP L=3.0U W=4.5U
M42 1 10 15 4 CMOSP L=3.0U W=4.5U
M43 33 18 32 17 CMOSN L=3.0U W=4.5U
M44 0 13 33 17 CMOSN L=3.0U W=4.5U
M45 1 25 13 4 CMOSP L=3.0U W=4.5U
M46 13 14 1 4 CMOSP L=3.0U W=4.5U
M47 1 22 25 4 CMOSP L=3.0U W=4.5U
M48 34 22 16 17 CMOSN L=3.0U W=4.5U
M49 0 32 34 17 CMOSN L=3.0U W=4.5U
M50 1 18 32 4 CMOSP L=3.0U W=4.5U
M51 32 13 1 4 CMOSP L=3.0U W=4.5U
M52 1 22 16 4 CMOSP L=3.0U W=4.5U
M53 16 32 1 4 CMOSP L=3.0U W=4.5U

M54 1 1 13 4 CMOSP L=3.0U W=4.5U
C55 25 0 111.0F
C56 22 0 111.0F
C57 14 0 131.0F
C58 13 0 131.0F
C59 16 0 111.0F
C60 15 0 102.0F
C61 12 0 111.0F
C62 10 0 406.0F
C63 7 0 417.0F
C64 8 0 229.0F
C65 5 0 229.0F
C66 1 0 1244.0F
* The following parameters are user specified for a transient
* analysis run with spice.
VDD 1 0 DC 5.0
VSUBN 17 0 DC 0
VSUBP 4 0 DC 5.0
VIN1 6 0 PULSE(0 5 0.0ns 3.0NS 3.0NS 10.0NS 30.0NS)
.TRAN  0.2NS 20NS
VIN2 9 0 PULSE(0 5 0.0NS 3.0NS 3.0NS 10.0NS 350.0NS)
*.PLOT TRAN V(22) V(6) V(9)
.MODEL CMOSN NMOS(LEVEL=3 LD=0.6825U
+ TOX=454.0E-10 NSUB=1.44995E+16 VTO=0.803734 KP=3.87E-05
+ GAMMA=0.9193 PHI=0.60 UO=508.827 DELTA=2.93638 VMAX=66268.4 XJ=0.40U
+ NFS=3.82944E12 NSS=1.0E12
+ CGSO=5.19091E-10 CGDO=5.19091E-10
+ CJ=0.0003825 MJ=0.464 CJSW=0.0005839 MJSW=0.3118
+ PB=0.75)
.MODEL CMOSP PMOS(LEVEL=3 LD=0.7415U
+ TOX=454.00E-10 NSUB=2.57089E+15 VTO=-0.947595 KP=1.3992E-05
+ GAMMA=0.3871 PHI=0.60 UO=183.967 DELTA=0.0126418 VMAX=33779.2 XJ=0.40U
+ NFS=1.0E+12 NSS=1.0E12
+ CGSO=5.63965E-10 CGDO=5.63965E-10
+ CJ=0.0001408 MJ=0.4225 CJSW=0.0004904 MJSW=0.2505
+ PB=0.7)
.PLOT TRANS V(22) V(9) V(6)
.END
```

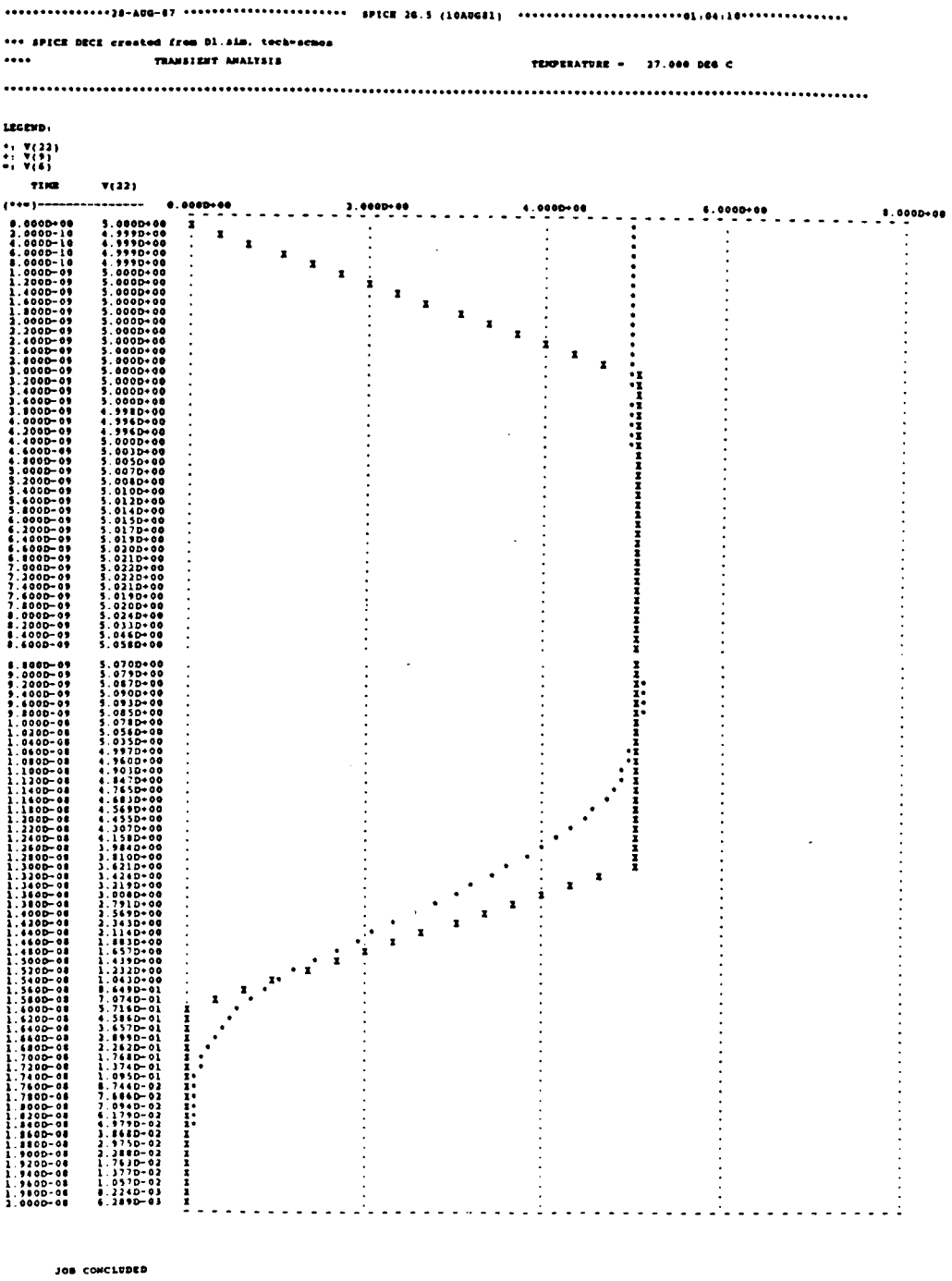


Figure 2.1: Transient analysis waveform generated for the D-flip-flop

APPENDIX C

FORTH Routine Used to Test DARC

The folowing file was used to test DARC when it returned after fabrication from MOSIS. The software was written to test each of the functional blocks individually. The entire prototype hardware enviornment consisted of a Mac-II, the 80C197 μprocessor and DARC. The results were observed on the Mac-II monitor and a CRO (Cathode Ray Oscilloscope).

```
Forth Definitions
Hex

2000 constant ASIC
0F constant P1
10 constant P2

Decimal

: BINARY   2 BASE ! ;

: GOTO  ( R C - )
        128 + emit   208 + emit ;

: CLS   255 emit  0 0 GOTO ;
```

```
: clrP2Bit   not  P2 c@  and  P2 c! ;
: setP2Bit        P2 c@  or   P2 c! ;


Decimal

0000 constant RESET.OPT1
0001 constant OPT1.LOW.BYTE
0002 constant OPT1.HIGH.BYTE
0003 constant PWM1
0004 constant RESET.OPT2
0005 constant OPT2.LOW.BYTE
0006 constant OPT2.HIGH.BYTE
0007 constant PWM2
0008 constant PWM3
0009 constant PWM.LOW/SIGN.BITS
0010 constant ENAB.DATA
0011 constant DIG1.OUT
0012 constant DIG1.INP
0013 constant DIG2.INP


: >DATA  ( Byte - )  ( Write a byte to ASIC data port)
        P1 C!  ;
```

```
: DATA>  ( - Byte )  ( Read a byte from ASIC data port)
        P1 C@  ;

: SEL          ( - )    ( Select the ASIC)
        64 SetP2Bit  ;

: DESEL  ( - )    ( Deselect the ASIC)
        64 ClrP2Bit  ;

: >ADR  ( Adr - )  ( Address the ASIC at Adr and select it)
        DESEL  ASIC C!  SEL  ;

: Strobe  ( - )  ( Deselect then select the ASIC (Strobe slect line)
        64 ClrP2Bit  64 SetP2Bit  ;

: WRITE   ( Byte Adr - )  ( Write the byte to the ASIC at ASIC Adr)
        DESEL    ASIC C!    >DATA    SEL   DESEL  ;

: READ  ( Adr - Byte )   ( Read a byte from ASIC at ASIC Adr)
        255 >DATA    >ADR  DATA>  ;

: OPT1>  ( - n )   ( Read optical Decoder #1)
        OPT1.LOW.BYTE  READ  drop   DATA>
 OPT1.HIGH.BYTE READ  256 *  +  ;

: OPT2>  ( - n )   ( Read optical Decoder #1)
```

```
        OPT2.LOW.BYTE  READ  drop   DATA>
 OPT2.HIGH.BYTE READ  256 *  +  ;

: DIG1>  ( - Byte )   ( Read byte from digital input port #1)
        DIG1.INP READ  ;

: DIG2>  ( - Byte )   ( Read byte from digital input port #2)
        DIG2.INP READ  ;

: >DIG1  ( Byte - )   ( Write a byte to digital output port #1)
        DIG1.OUT WRITE  ;

: >PWM1  ( n - )   ( Write 11-bit signed number to PWM #1  ( -1024 to +1023 )
        dup  abs  3 and  over  0 <   if  128 or  then
 PWM.LOW/SIGN.BITS WRITE
        abs  4 /  PWM1 WRITE  ;

: >PWM2  ( n - )   ( Write 11-bit signed number to PWM #1  ( -1024 to +1023 )
        dup  abs  3 and  over  0 <   if  128 or  then
 PWM.LOW/SIGN.BITS WRITE
        abs  4 /  PWM2 WRITE  ;

: >PWM3  ( n - )   ( Write 11-bit signed number to PWM #1  ( -1024 to +1023 )
        dup  abs  3 and  over  0 <   if  128 or  then
 PWM.LOW/SIGN.BITS WRITE
        abs  4 /  PWM3 WRITE  ;
```

```
: HELP   cr cr cr          ( Display list of test words)
         cr ."  T1 - Digital Input Test"
         cr ."  T2 - Digital Output Test"
         cr ."  T3 - Display Optical Decoder #1"
         cr ."  T4 - Display Optical Decoder #2"
         cr ."  T5 - Display Both Optical Decoders"
         cr ."  T6 - Ramp PWM #1"
         cr ."  T7 - Ramp PWM #2"
         cr ."  T8 - Ramp PWM #3"
         cr ."  T9 - Ramp all three PWMs"
         cr ." T10 - Do it all!"  cr ;

: Exit.test  ( - )    decimal cr cr 7 EMIT  ;

: NL     BASE @  DECIMAL 4 0 GOTO   BASE !  8000 0 DO I I + DROP LOOP ;

: T1     CLS ." Display Digital input ports #1 and #2:" cr cr
            ." Digital1 Digital2" cr  binary
         begin
           NL   DIG1>  8 .r  DIG2>  9 .r
           ?KEY
         until  Exit.test ;

: T2     CLS ." Binary increment to digital output port #1 ..." cr cr
```

```
        0
        begin
          1+  dup  >DIG1
          ?KEY
        until  drop Exit.test  ;

: T3    CLS ."  Optical Decoder #1 Test:" cr cr  decimal
        begin
          NL  OPT1>  6 .r
          ?KEY
        until  Exit.test  ;

: T4    CLS ."  Optical Decoder #2 Test:" cr cr  decimal
        begin
          NL  OPT2>  6 .r
          ?KEY
        until  Exit.test  ;

: T5    CLS ."  Optical Decoder #1 and #2 Test:" cr cr  decimal
        ."   Opt1   Opt2"  cr
        begin
          NL  5 spaces OPT1>     binary u.  decimal  OPT2>
  binary  u.
          decimal ?KEY
        until  Exit.test  ;
```

```
: T6     CLS ." Ramping PWM #1 ..."  cr cr   0
         begin
           1+  dup  >PWM1
           ?KEY
         until  drop Exit.test  ;

: T7     CLS ." Ramping PWM #2 ..."  cr cr   0
         begin
           1+  dup  >PWM2
           ?KEY
         until  drop Exit.test  ;

: T8     CLS ." Ramping PWM #3 ..."  cr cr   0
         begin
           1+  dup  >PWM3
           ?KEY
         until  drop Exit.test  ;

: T9     CLS ." Ramping all three PWMs ..."  cr cr   0
         begin
           1+  dup  >DIG1   dup  >PWM1  dup  65535 xor  >PWM2
           dup 1024 +  >PWM3
           ?KEY
         until  drop Exit.test  ;

: T10    CLS ." Do it all"  cr cr  0
```

```
." Digital1 Digital2   Opt1   Opt2"
begin
   NL
   binary   DIG1>  8 .r    DIG2>  9 .r
   decimal  OPT1>  7 .r    OPT2>  7 .r
   1+  dup  >PWM1  dup  65535 xor  >PWM2
   dup 1024 +  >PWM3    dup  >DIG1
   ?KEY
until  drop Exit.test  ;
```

VITA

Raj R. Kumar was born in Bangalore, India on 3rd December, 1959. He attended Clarence High School in Bangalore, India and graduated with honours in 1975. After successfully completing a two year Pre-University Course at the St. Josephs College of Arts and Science, Bangalore he joined the University Vishweshvaraya College of Engineering, Bangalore. During the last couple of years of his Engineering curriculum he served as a part time employee, with Cauvery Cables and Conductors, Bangalore. His work was appreciated, and soon he rose to the position of Production Supervisor. He continued to serve with Cauvery Cables and Conductors, and assisted them in establishing a sister concern, Ribbon Cables, Inc. At school, he came out with flying colors and was graduated with a Bachelor of Science Degree in Electrical Engineering in April 1985, specializing in the field of Electronics.

As an engineer, he served with Electronic Devices, Inc., Bangalore, for over a year. He was admitted to the University of Tennessee, Knoxville, in the Winter of 1987. At UTK he concentrated his research to microelectronics, a field that had long fascinated him. As a newcomer to the field, his hard work and sincere effort paid off, and the results he obtained were astounding, and highly acclaimed.