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Towards a Universal Multi-Standard RF Receiver

A Thesis

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Master of Science

Degree

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Yongping Han

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Abstract

Future wireless communication market calls for the need of an extreme compact wireless device that can easily access to all the available services at any time and at any location with minimum power consumption and cost. The key is to find a multi-standard wireless receiver that can cover all the service specifications while keeping redundant components to minimum. Reconfigurable concept is right fit the need. In this thesis, a fully integrated universal multi-standard receiver using low-cost CMOS technology has been proposed based on the survey for different wireless receiver specifications and optimum architectures. Tunable receiver building blocks such as filters, LNAs, Mixers, VCOs, gain blocks are the main factor to approach this novel receiver. In order to realize frequency agility, low cost as well as low power consumption, a good switch is a must. In this thesis, MEMS switches are preferred rather than active switches or active tuning elements based on their performance comparisons. In the feasibility study, as an example, first, a reconfigurable LNA and a reconfigurable oscillator using hard wires as switches have been developed, and then a LNA and an oscillator have been designed using a MEMS switch. The effect of hard-wire connection and MEMS to the circuits has been evaluated. No performance degradation has been found when using hard-wire connections, while some has been observed when using MEMS. However, MEMS could be integrated with other circuits on the same die if it could be built on low resistive silicon substrate without performance degradation.

Tables of Contents

1 Introduction ……..……1

1.1 What to reconfigure……..……2

1.2 Examples of reconfigurable structures……..……2

1.3 Our work……..……4

2 Survey of Various Wireless Services and Standards…….5

2.1 Introduction……..…5

2.1.1 Main blocks of RF receivers.....5

2.1.2 Various RF front end options……....6

2.1.3 Reconfigurable RF front ends as a valid option……8

2.2 Specifications and architectures of various services……...…8

2.2.1 GSM…….……10

2.2.2 DECT……14

2.2.3 UMTS……..……..…18

2.2.4 WLAN……..……21

2.2.5 Bluetooth……..……26

2.3 Universal reconfigurable receiver architecture……...……28

2.4 Conclusions…….……32

3 Tuning Blocks…….……..33

4 Development of a Reconfigurable Low Noise Amplifier…….…….40

4.1 LNA design concept……41

4.2 LNA design equations……42

4.3 Principle for single-stub matching……..……42

4.4 Implementation……45

4.4.1 Single-service design……46

4.4.1.1 LNA at 1.9GHz….....47

4.4.1.2 LNA at 2.4GHz…….50

4.4.1.3 LNA at 5.2GHz……54

4.4.2 Multi-service design……58

4.4.3 LNA design using MEMS…….……65

4.5 Conclusions……69

5 Development of a Reconfigurable Oscillator …….……..72

5.1 Oscillator design concept……72

5.1.1 Principle for basic oscillator design…….....74

5.1.2 Principle for reconfiguability……...……76

5.2 Strategy for reconfigurable oscillator design……..……77

5.3 Implementation……..……78

5.3.1 Single-service design……79

5.3.1.1 Oscillator operating at 850MHz……80

5.3.1.2 Oscillator operating at 1.85GHz……84

5.3.1.3 Oscillator operating at 2.35GHz……88

5.3.2 Multi-service design……88

5.3.3 Oscillator design using MEMS……96

5.4 Conclusions……99

6 Conclusions and Future Work……..……100

References……103

Vita……..……105

List of Tables

Table2.1: Frequency plan for WCDMA, EDGE, GPRS and GSM ……..…….7

Table 2.2: Comparison of multi-band, parallel-path and reconfigurable receivers in tuning, design, performance and area ……9

Table 2.3: GSM frequency plan ……..……..…10

Table 2.4: GSM signal characteristics……..…10

Table 2.5: E-GSM receiver specifications ……...11

Table 2.6: E-GSM blocking requirements …….....12

Table 2.7: E-GSM intermodulation requirements …….....12

Table 2.8: E-GSM receiver front-end specifications ……...14

Table 2.9: DECT frequency plan and signal characteristics ……....16

Table 2.10: DECT receiver specifications …….....16

Table 2.11: DECT blocking requirements …….....16

Table 2.12: DECT receiver front-end specifications …….....18

Table 2.13: UMTS receiver specifications…….....19

Table 2.14: UMTS blocking requirements…….....19

Table 2.15: UMTS receiver front-end specifications …….……..21

Table 2.16: WLAN receiver specifications …….……23

Table 2.17: Comparison of zero-IF and low-IF architectures for WLAN 802.11a, b and g……....25

Table 2.18: WLAN receiver frond-end requirements ……..…25

Table 2.19: Bluetooth signal characteristics ……27

Table 2.20: Bluetooth receiver specifications……..……..27

Table 2.21: Multi-standard receiver front-end requirements…….…..……..31

Table 3.1: Tuning range of active resistor, MOS capacitor and active inductor vs. applied voltage ……...…...38

Table 3.2: Performance comparison of active switches to RF MEMS switch……..38

Table 3.3: Performance comparison of RF MEMS to active tuning components…….....39

Table 4.1: Gain and noise figure requirements for UMTS and WLAN ….……..40

Table 4.2: Simulated and measured performance summary for single-service and multi-service LNA designs ……..65

Table 5.1: Required oscillator frequency for individual service…….……..73

Table 5.2: Phase noise specification for different services ……..73

Table 5.3: Comparison of the simulated and measured output power for single-service and multi-service designs ……...…….95

Table 5.4: Comparison of the output power of the 1st and 2nd harmonic components for an oscillator operating at 1.85GHz with and without MEMS…….....99

List of Figures

Figure 2.1: CMOS low-IF receiver architecture for E-GSM ……..…….….14

Figure 2.2: CMOS zero-IF receiver architecture for DECT ……..…..……..18

Figure 2.3: CMOS zero-IF receiver architecture for UMTS…….…….…….…...21

Figure 2.4: WLAN frequency plan ……..…….23

Figure 2.5: CMOS zero-IF receiver architecture for WLAN …….…….…….25

Figure 2.6: CMOS low-IF receiver architecture for Bluetooth ……...….27

Figure 2.7: Multi-standard receiver architectures (a) Parallel RF (b) Multi-band (c) Reconfigurable or switchable…….…….…..29

Figure 2.8: Proposed universal multi-standard receiver architecture……31

Figure 3.1: Multi-mode LNA…….…..….34

Figure 3.2: Mixer with tunable IIP2…….....….34

Figure 3.3: VCO using tunable active inductor…..…….…….35

Figure 3.4: Simulated tuning range of active resistor……..…....36

Figure 3.5: Simulated parasitic capacitance associated with the active resistor ……..…36

Figure 3.6: Simulated tuning range of varactor ……...……37

Figure 3.7: Simulated tuning range of active inductor…….…...….38

Figure 4.1: Reconfigurable LNA concept diagram with three various matching stubs ……..…….41

Figure 4.2: Single-stub matching network…….……..43

Figure 4.3: (a) Single-stub matching using ADS Smith Chart (b) Single stub generated by ADS Smith Chart ……44

Figure 4.4: Schematic diagram of single-service LNA at 1.9GHz……..48

Figure 4.5: PCB of single-service LNA at 1.9GHz……48

Figure 4.6: Simulated gain, noise figure and return loss of single-service LNA at 1.9GHz……..49

Figure 4.7: Measured and simulated gains of single-service LNA at 1.9GHz……50

Figure 4.8: Measured and simulated return losses of single-service LNA at 1.9GHz.....51

Figure 4.9: Schematic diagram of single-service LNA at 2.4GHz……...51

Figure 4.10: PCB of single-service LNA at 2.4GHz……...52

Figure 4.11: Simulated gain, noise figure and return loss of single-service LNA at 2.4GHz……..53

Figure 4.12: Measured and simulated gains of single-service LNA at 2.4GHz……...53

Figure 4.13: Measured and simulated return losses of single-service LNA at 2.4GHz……...54

Figure 4.14: Schematic diagram of single-service LNA at 5.2GHz……55

Figure 4.15: PCB of single-service LNA at 5.2GHz……...55

Figure 4.16: Simulated gain, noise figure and return loss of single-service LNA at 5.2 GHz……56

Figure 4.17: Measured and simulated gains of single-service LNA at 5.2GHz……...57

Figure 4.18: Measured and simulated return losses of single-band LNA at 5.2GHz…….....57

Figure 4.19: PCB of LNA at 5.2 GHz……..…….…….58

Figure 4.20: Measured and simulated gains and noise figures of LNA at 5.2GHz….....59

Figure 4.21: Layout of multi-service LNA designed at 1.9GHz, 2.4GHz and 5.2GHz with switches (In this stage switches are replaced by hard wires.) ….……60

Figure 4.22: PCB of multi-service design configured at 2.4GHz ……...….61

Figure 4.23: Measured and simulated gains of multi-service LNA configured at 1.9GHz …….....62

Figure 4.24: Measured and simulated return losses of multi-service LNA configured at 1.9GHz ……..……62

Figure 4.25: Measured and simulated gains of multi-service LNA configured at 2.4GHz……..….63

Figure 4.26: Measured and simulated return losses of multi-service LNA configured at 2.4GHz ……..……..…….…63

Figure 4.27: Measured and simulated gains of multi-service LNA configured at 5.2GHz……..…..…..….64

Figure 4.28: Measured and simulated return losses of multi-service LNA configured at 5.2GHz ……...…..……...….64

Figure 4.29: (a) Equivalent circuit when MEMS is on (b) Equivalent circuit when MEMS is off ……..……66

Figure 4.30: Schematic diagram of LNA at 5.2GHz using MEMS switch…….…67

Figure 4.31: Simulated gain, noise figure and return loss of LNA at 5.2GHz with MEMS switch on …….68

Figure 4.32: PCB of LNA at 5.2GHz using MEMS……...……..……68

Figure 4.33: Measured and simulated gains for LNA at 5.2GHz using MEMS……...70

Figure 4.34: Measured and simulated return losses for LNA at 5.2GHz using MEMS……...70

Figure 5.1: Common block diagram of an oscillator feeding a mixer……..…73

Figure 5.2: Two-port transistor oscillator circuit …….……75

Figure 5.3: A proposed reconfigurable oscillator operating at different frequencies……77

Figure 5.4: Schematic diagram of single-service oscillator at 850MHz …….…..……81

Figure 5.5: PCB of single-service oscillator at 850MHz…….….82

Figure 5.6: Simulated output power of single-service oscillator at 850MHz……...82

Figure 5.7: Simulated phase noise of single-service oscillator at 850MHz……..…....83

Figure 5.8: Measured output power of single-service oscillator at 850MHz……..…..83

Figure 5.9: Measured phase noise of single-service oscillator at 850MHz…….…..…84

Figure 5.10: Schematic diagram of single-service oscillator at 1.85GHz……....85

Figure 5.11: PCB of single-service oscillator at 1.85GHz……...….85

Figure 5.12: Simulated output power of single-service oscillator at 1.85GHz……..…...86

Figure 5.13: Simulated phase noise of single-service oscillator at 1.85GHz…….…..….87

Figure 5.14: Measured output power of single-service oscillator at 1.85GHz…….....87

Figure 5.15: Schematic diagram of single-service oscillator at 2.35GHz…….…....89

Figure 5.16: PCB of single-service oscillator at 2.35GHz……..…..89

Figure 5.17: Simulated output power of single-service oscillator at 2.35GHz…….…90

Figure 5.18: Simulated phase noise of single-service oscillator at 2.35GHz……..…..90

Figure 5.19: Measured output power of single-service oscillator at 2.35GHz…….…....91

Figure 5.20: PCB of multi-service oscillator configured at 850MHz…….…..92

Figure 5.21: PCB of multi-service oscillator configured at 1.85GHz…….….92

Figure 5.22: PCB of multi-service oscillator configured at 2.35GHz…….....93

Figure 5.23: Measured output power of multi-service oscillator at 850MHz ……..…93

Figure 5.24: Measured output power of multi-service oscillator at 1.85GHz ……..…94

Figure 5.25: Measured output power of multi-service oscillator at 2.35GHz……..…....94

Figure 5.26: Schematic diagram of oscillator at 1.85GHz using MEMS……...….……..97

Figure 5.27: Simulated output power of oscillator at 1.85GHz using MEMS…...….…..98

Figure 5.28: Simulated phase noise of oscillator at 1.85GHz using MEMS….....98

List of Abbreviations

2G – second Generation wireless technology

3G – third Generation wireless technology

3GPP – 3rd. Generation Partnership Project

DCS – Digital Cellular Communication System

DECT – Digital Enhanced Cordless Telephone

E-GSM – Enhanced Global System for Mobile communications

EDGE- Enhanced Data GSM Environment

GPRS – General Packet Radio Service

GPS – Global Positioning System

GSM – Global System for Mobile Communications

PCS – Personal Communication Services

UMTS – Universal Mobile Telecommunication System

WCDMA – Wideband Code Division Multiple Access

WLAN – Wireless Local Area Network

1
Introduction

In anticipation of a near-future realization of integrated computing and communication functional silicon chips, researchers should start today addressing potential interfacing problems. This includes multi-standards, multi-bands, and multi-functions as it is sought by various wireless service providers. In particular, there is a need for adaptable, reconfigurable integrated radio frequency (RF) front-ends in a very compact size rather than utilizing many antenna platforms and many receivers with redundant components.

Currently both wireless devices and computers are operating at higher and higher microwave frequencies, and it is believed that silicon-based technologies with integrated computing and communication functions will open the doors for further expansion plans into other areas, thereby delivering new capabilities for customers' benefits.

The trend to develop compact multifunctional integrated systems or subsystems is aimed at developing universal wireless receivers. It requires using one receiver set that supports many standards (GSM, GPRS, EDGE, DECT and UMTS/3GSM) for cell-phones, and many other services like Bluetooth, WiMax, WLAN, Zigbee, GPS and more to come. Researchers are diligently inventing various ways to develop such universal multi-standard receivers to cover all these highly challenging and technically demanding services using reconfigurable structures and circuits, which ultimately will be on silicon chips and would cover both computational and wireless applications.

1.1 What to reconfigure

Reconfigurable RF front ends and their associated antennas have been seriously considered to develop such products rather than use multi-band or even wide-band antennas. Reconfigurability is really driven by market needs for low-cost, compact, and light wireless receivers, where these reconfigurable structures are designed to provide multi-service flexibility. Receivers are configured to optimally offer one service or more at a time, which might require more than one antenna. However, use of dedicated antennas and RF front ends for each service is costly. If many redundant components are used, then they can be easily eliminated when systems are reconfigurable. Use of many antennas would also lead to performance degradation due to the unwanted proximity coupling, besides occupying a large real estate. Similarly, use of wide-band receivers would require the use of filters with stringent requirements, or the use of many redundant receivers.

1.2 Examples of reconfigurable structures

There is no need to have one receiver addressing every service or standard. Many blocks and components can be combined and reconfigured to provide the same function of whichever individual receiver is used. For example, one oscillator could be dynamically reconfigured for various standards and services [2], gain blocks and low noise amplifiers (LNAs) could also be dynamically adjusted to address various demanding requirements or specifications for gain, S/N, IIP3 and dynamic range [3].

Reconfigurability, in general, is achieved by using MEMs, PIN diodes, or other active devices compatible with CMOS technology. MEMS technology is maturing very fast, and is becoming a viable means requiring the least dc power consumption. PIN diode technology is a completely established alternative technology but requires relatively high dc power consumption to sustain long battery life time which is a prime concern for wireless receivers. Meanwhile, CMOS transistors are currently used for switching applications in many receivers, although they are dc power hungry and ultimately need to be replaced by MEMS switches.

Active resistors, inductors, and varactors are also basic tools for reconfigurability [2]. Their values can be controlled by using either current or voltage applied. Adjusting their values can be utilized to accommodate various operating conditions for the various services and standards. Issues related to reconfiguration tools are discussed in detail in this thesis.

Another area suitable for reconfigurability is antennas. They are bulky and relatively large, especially at the lower wireless frequencies such as 800-900 MHz. Besides, the use of many antennas to address the different standards/services contradicts miniaturization efforts. The proximity of many antennas would lead to performance degradation due to their strong coupling. When antennas are reconfigured to best suit one or more service at a time, their form, shape, and function can be dynamically configured according to the specific overall system requirements. Efforts to develop reconfigurable antennas are not part of this thesis, but a good reference of current efforts.

1.3 Our work

This thesis includes six chapters. Chapter 1 briefly introduces the driving force for this research topic. Chapter 2 reviews the receiver specifications and architectures for different services including GSM, DECT, UMTS, WLAN and Bluetooth. Based on the detailed analysis and discussion for each service, a universal multi-standard multi-functional reconfigurable RF receiver architecture is addressed at the end of this Chapter.

Chapter 3 introduces some examples of reconfigurable RF building blocks such as LNAs, mixers and VCOs, which are the key components to realize a reconfigurable receiver. The tuning performance of active resistor, varactor and active inductor is described. The performance comparison of MEMS to active switches is also addressed.

Chapter 4 presents design, fabrication and test of a reconfigurable LNA. First, the design software and design steps are introduced. Next, the single-service design for UMTS and WLAN covering 3 frequency bands is detailed. Then, the multi-service design is addressed using hard wires rather than using switches. Finally, a MEMS switch is employed into the design and its effect on the performance is discussed.

Chapter 5 demonstrates the development of a reconfigurable oscillator. It covers the design software, design steps, single-service design as well as multi-service design. The design using a MEMS switch is simulated and discussed.

Chapter 6 summarizes the achievements of this work and some recommendations for the future work.

2

Survey of Various Wireless Services and Standards

2.1 Introduction

In the following sections, various wireless standards will be investigated with the emphasis on the receiver specifications and optimal architectures based on CMOS technology as well as the associated design challenges. It covers global system for mobile communications (GSM), digitally enhanced cordless telephone system (DECT), universal mobile telecommunication system (UMTS) for cellular telephony, IEEE802.11a/b/g, HiperLNA2 for wireless local area network (WLAN) access, and Bluetooth for short range communications. Then, a reconfigurable multi-standard terminal will be presented, and its front-end specification will be summarized.

The goal here is to survey the main design parameters of the various services, identify commonalities and differences, and pick up the most probable reconfigurable blocks.

2.1.1 Main blocks of RF receivers

The basic idea in building these RF front-end circuits is to maximize the digital domain circuits, and to minimize the circuits in the analog domain, where ADCs are utilized directly after the mixers in the receiver side. Meanwhile, the VCOs are phase

lock loop (PLL) driven. This circuit structure can easily render reconfigurable circuits as will be outlined in the subsequent sections.

RF front ends can be classified into two different categories: a direct conversion (zero IF) or low IF architectures. Direct conversion receivers can be used for various services such as WLAN, WCDMA, EDGE, GPRS, and GSM. Meanwhile, from the bandwidth point of view, WLAN and WCDMA require wide band operation, while EDGE, GPRS, and GSM require relatively narrow band receivers. Table 2.1 lists the frequency plan for WCDMA, EDGE, GPRS and GSM.

Low IF receivers offer various advantages such as no DC offset, high integration, few components, and low power consumption. However, they are only suitable for relatively narrow band receivers. Meanwhile, direct conversion receivers (zero IF) are preferred for multi-services and multi-standards as they can be used for all frequency bands. But, they suffer from DC offset, noise, and linearity.

2.1.2 Various RF front end options

In building a RF front end, one could pick one of the various options that include using an off-chip SAW filter and an off-chip GaAs LNA, or an off-chip SAW filter and a silicon chip. The off-chip GaAs LNA is preferred for its low DC power consumption. It would consume 2-4mA, as compared to 7-10mA for silicon chips.

Table 2.1: Frequency plan for WCDMA, EDGE, GPRS and GSM

Parameter	WCDMA	EDGE	GPRS	GSM
Required bandwidth per channel	1.25/5/10/20 MHz	200KHz	200 KHz	200KHz
	Band 1: IMT			GSM850
Uplink(MHz)	1920-1980			824-849
Downlink(MHz)	2110-2170			869-894
	Band2:PCS			GSM900
Uplink(MHz)	1850-1910			880-915
Downlink(MHz)	1930-1990			925-960
	BAND3: DCS			
Uplink(MHz)	1710-1785			
Downlink(MHz)	1805-1880			
	BAND4: FDD			
Uplink(MHz)	1710-1770			
Downlink(MHz)	2110-2170			
	BAND5: LB			
Uplink(MHz)	824-849			
Downlink(MHz)	869-894			
	BAND6:			
Uplink(MHz)	830-840			
Downlink(MHz)	875-885			

2.1.3 Reconfigurable RF front ends as a valid option

Future wireless receivers may contain several radios for different applications. GPS, WLAN, and Bluetooth could have separate receivers, meanwhile other services such as GSM, DCS, PCS, WCDMA, IS-95, and CDMA2000 may be integrated in the same die. Having many concurrent systems on the same die is not optimal as these various systems can interfere with each other and would have very different specifications. Thus, it is preferred to have only one system operating at a time by utilizing reconfiguration. Compared to the parallel and multi-band receiver architectures, the reconfigurable receiver has the following advantages:

1) Each signal path can be separately configured.
2) The number of interfering signals can be reduced.
3) Relatively smaller areas can be achieved, if parallel structures are avoided.
4) No off-chip components would be required.

But, their design becomes challenging because of the required programmable filters.

Table 2.2 presents a comparison among these three different receiver architectures: the multi-band, the parallel-path, and the reconfigurable receivers in terms of tuning requirements, design complexity, performance tradeoffs and area required.

2.2 Specifications and architectures of various services

In the following section the basic requirements of the various RF blocks for different services including GSM, DECT, UMTS, Bluetooth and WLAN will be detailed.

Table 2.2: Comparison of multi-band, parallel-path and reconfigurable receivers in tuning, design, performance and area

	Multi-band	Parallel-Path	Reconfigurable
Tuning	Does not require tuning for multi-band operation	Each can be optimized separately	Programming is difficult in order to comply with all various modes specifications
Design Complexity	Difficult design to meet all different specifications of all various modes	Straight forward design as each design is completely independent	Difficult design, would require many added elements and switching mechanisms
Performance degradation	Performance should not traded to wider bandwidth operation	No performance degradation as no additional elements are needed	This is the challenging task due to the presence of many parasitic
Area	Small	Large	Compromised / smaller

2.2.1 GSM

GSM is one of the second-generation (2G) mobile phone system originally developed by Europe. Today, the GSM standard has three sub-systems. Two of them, enhanced global system for mobile communications (E-GSM) and the digital cellular communication system (DCS1800), are used in Europe, while the third one, personal communication services (PCS1900), has been utilized in U.S.A.

Table 2.3 summarizes the frequency plan of GSM system. The most important characteristics of the GSM signal are listed in Table 2.4 [1].

According to the standards, the most stringent receiver specifications are set for E-GSM. Therefore, the following efforts will be focused on E-GSM.

Table 2.3: GSM frequency plan

	E-GSM	DCS1800	PCS1900
Uplink (MHz)	880 - 915	1710 - 1785	1850 - 1910
Downlink (MHz)	925 - 960	1805 - 1880	1930 – 1990

Table 2.4: GSM signal characteristics

Parameters	E-GSM, DCS1800, PCS1900
Modulation	Gaussian-MSK
Channel Bandwidth	200 kHz
Bit Rate	270kb/s
Spectral Efficiency	1.3b/s/Hz

GSM receiver requirements

Table 2.5 shows the receiver specifications for E-GSM [1] [5]. From the E-GSM standard, the antenna-referred noise floor is -111 dBm, which is calculated from the sensitivity level of -102 dBm and the maximum carrier-to-noise ratio of 9 dB set by the standard.

The phase noise PN requirement can be derived from the following equation based on the E-GSM blocking requirements set by the standard shown in Table 2.6 [5].

$$PN = \text{desired signal power} - \text{blocker power} - 10 * \log(\text{noise bandwidth}) - 12\ \text{dB} \quad (2.1)$$

For E-GSM, the worst-case phase noise is -141dBc/Hz set by the 3MHz blocker.

The third-order input intercept point IIP3 of -18dBm can be obtained by the intermodulation test specified by the standard. Table 2.7 shows the intermodulation requirements for E-GSM [5]. Since the interferer's power is set to be -49dBm and the

Table 2.5: E-GSM receiver specifications

Parameters	E-GSM Requirements
Sensitivity @ BER = 10^{-3} (dBm)	-102
Input noise (dBm)	-120.8
Input SNR (dB)	18.8
Required C/N (dB)	9
Required noise figure (dB)	9.8
Noise floor (antenna-referred) (dBm)	-111
Phase noise @ 3 MHz offset (dBc/Hz)	-141
IIP3 (dBm)	-18
IIP2 (dBm)	> + 49

Table 2.6: E-GSM blocking requirements

In-band offset (MHz)	Blocker power (dBm)
0.6 to 1.4	-43
1.6 to 2.8	-33
> 3	-23

Table 2.7: E-GSM intermodulation requirements

	E-GSM
Desired GMSK signal level	-99dBm
Continuous wave interferer	-49dBm @ 800 kHz offset
GMSK modulated interferer	-49dBm @ 1600 kHz offset

antenna-referred noise floor is at -111dBm, the IM3 component should be

$$\text{IM3} = \text{interferer power} - \text{noise floor} \qquad (2.2)$$

$$= (-49\ \text{dBm}) - (-111\ \text{dBm}) = 62\ \text{dBc}$$

Therefore, the input referred IIP3 can be calculated by the following equation

$$\text{IIP3} = \text{interferer power} + \frac{IM_3}{2}\ \text{dBc} \qquad (2.3)$$

$$= (-49\ \text{dBm}) + (\frac{62}{2})\ \text{dBc} = -18\ \text{dBm}$$

The requirement for second-order intercept-point IIP2 is very stringent here to be minimum of +49dBm, which comes from an AM suppression test specified by the standard. This means for an LNA with a gain of 18 dB, at least 70 dBm of IIP2 is required for a mixer, which is very challenging for zero-IF or low-IF receiver.

Proposed GSM receiver architecture

Through years of development in device technology, higher level of circuit integration has become feasible for lower cost and lower power consumption application. Recently, there are some commercial multi-band (E-GSM, DCS1800, PCS1900) products using CMOS zero-IF and low-IF architectures [1] that demonstrated considerably lower power consumption as well as lower cost. Compared to the low-IF architecture, the zero-IF implementation requires larger area and higher-resolution ADC to meet the stringent IIP2 requirement [1]. Therefore, the low-IF architecture is the best candidate for a CMOS fully integration purpose. Fig. 2.1 shows the CMOS low-IF receiver architecture for E-GSM. In this architecture, the IF frequency is set to be 100 kHz, therefore the image signal lies at the edge of the adjacent channel band. In order to keep the BER performance, a 32 dB image rejection is required [1].

Table 2.8 lists RF front-end specifications including LNA and active mixer for E-GSM [1]. From this table, the most critical block is the mixer for which very stringent noise and linearity performances are required. In the base band, two variable gain blocks with a fourth-order Butterworth filter in between together with a 9-bit ADC are needed. A high pass filter may be required in front of the first variable gain block to remove the dc offset due to local oscillator (LO) self-mixing and mixer mismatches. The image suppression is performed in the digital domain. The tuning range of the voltage-controlled oscillator (VCO) should be at least 60 MHz.

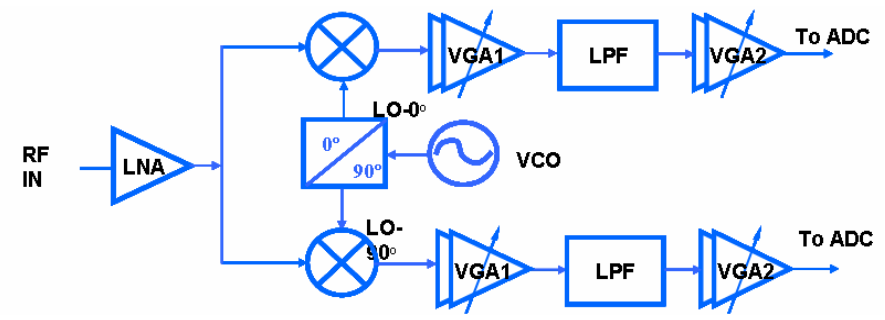


Figure 2.1: CMOS low-IF receiver architecture for E-GSM

Table 2.8: E-GSM receiver front-end specifications

	Gain	Noise	IIP3	IIP2
LNA	23 dB	3dB	-5 dBm	---
Mixer	12 dB	9 nV/$\sqrt{Hz}$	+7 dBm**	+ 75 dBm**

** 50Ω- referred

GSM design challenges

For this CMOS low-IF receiver architecture, the most challenges are listed as follows: first, 1/f noise is a major concern due to narrow 200 kHz channel bandwidth. Second, a very high linearity requirement is set for the down-converter. Last, dc offset cancellation is very critical due to the significant desired signal energy at very low frequencies.

2.2.2 DECT

Digital Enhanced Cordless Telecommunications (DECT) is an ETSI standard for digital portable phones. It is a cellular system like GSM. The main difference between

DECT and GSM is the cell radius. DECT cells have a radius range from 15 to 100 meters, while GSM cells are 2 to 10 km.

DECT receiver requirements

Table 2.9 lists the DECT frequency plan and signal characteristics [5]. The receiver specifications are presented in Table 2.10 [5].

The antenna-referred noise floor of -94 dBm can be obtained from the sensitivity level and the required C/N.

Phase noise requirement can be given by the blocking requirements set by the standard listed in Table 2.11[5]. Compared to GSM, DECT has more relaxed blocking requirements. According to the standards, a single Gaussian minimum-shift keying (GMSK) modulated blocker is applied to the input of the receiver together with the desired signal. Different from the GSM block requirements, DECT requires an -83 dBm co-channel blocker which shared the same band as the desired signal. Based on the equation (2.1), the phase noise requirement at 2.2 MHz offset $PN_{2.2MHz}$ is

$$PN_{2.2MHz} = -80 - (-58) - 10 * \log(1.728*10^{6}) - 12 \quad (2.4)$$

$$= -96 \text{ dBc/ Hz}$$

which is pretty relaxed compared to that of GSM.

Same as GSM, the DECT standard also sets intermodulation test with a designed signal of -80 dBm and two adjacent channel signals of -46 dBm. Using equations (2.2) and (2.3), the IM3 and IIP3 for DECT should be

Table 2.9: DECT frequency plan and signal characteristics

Parameters	DECT
Frequency band (MHz)	1880 – 1897
Modulation	Gaussian-MSK
Channel bandwidth (MHz)	1.728

Table 2.10: DECT receiver specifications

Parameters	DECT Requirements
Sensitivity @ BER = 10^{-3} (dBm)	-83
Input noise (dBm)	-112.3
Input SNR (dB)	29.3
Required C/N (dB)	10.3
Required noise figure (dB)	19
Noise floor (antenna-referred) (dBm)	-94
Phase noise @ 2.2 MHz offset (dBc/Hz)	-96
IIP3 (dBm)	-22

Table 2.11: DECT blocking requirements

In-band offset (MHz)	Blocker power (dBm)
0 to 2.2	-58
2.2 to 3.9	-39
3.9 to 5.6	-33
5.6 to 9	-33

$$IM3_{DECT} = -46\ dBm - (-94\ dBm) = 48\ dBc \quad (2.5)$$

$$IIP3_{DECT} = -46\ dBm - (48/2)\ dBc = -22\ dBm \quad (2.6)$$

Since DECT standard sets relative relaxed requirements compared to those of GSM both for noise figure and linearity, it is not hard to meet the specifications based on either zero-IF or low-IF receiver.

Proposed DECT receiver architecture

For a fully integrated DECT receiver architecture, both zero-IF and low-IF can be chosen. Compared to the zero-IF structure, the low-IF would suffer from a higher image rejection and ADC dynamic-range requirements [1]. Meanwhile, due to a relatively wide-band desired signal, 1/f noise is not critical any more for the zero-IF approach. Therefore the zero-IF is the better choice.

Fig. 2.2 shows the CMOS zero-IF receiver architecture for DECT, and the DECT front-end specifications are listed in Table2.12 [5]. In the front end, a total gain of 20 dB from LNA and mixer is adequate due to the quite relaxed noise requirement. But the linearity requirement for LNA is higher compared to GSM.

In the base band, two VGAs with a fourth-Butterworth filter in between together with an 11-bit ADC right after the second VGA is adequate. For VCO, the minimum tuning range of 60 MHz is required.

For the CMOS DECT zero-IF architecture, the receiver requirements can easily be met although the linearity requirement for LNA is slightly high.

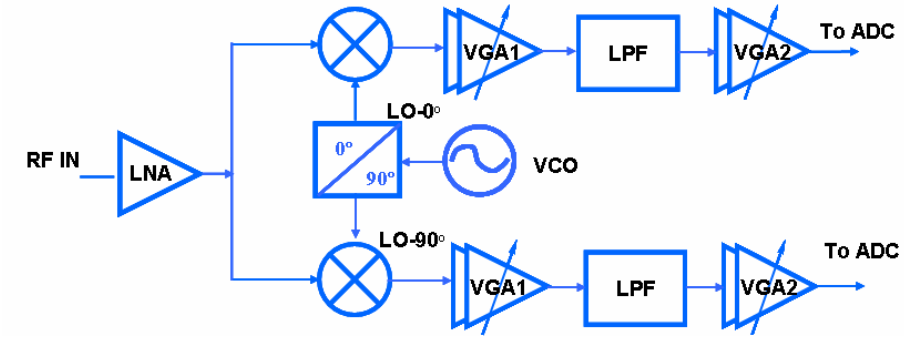


Figure 2.2: CMOS zero-IF receiver architecture for DECT

Table 2.12: DECT front-end specifications

	Gain	Noise	IIP3
LNA	12 dB	5dB	-10dBm
Mixer	8 dB	8 dB	+8dBm**

** 50Ω- referred

2.2.3 UMTS

Universal Mobile Telecommunications System (UMTS) is one of the third-generation (3G) mobile phone technologies. It uses W-CDMA as the underlying standard, is standardized by the 3GPP, and represents the European answer to the ITU IMT-2000 requirements for 3G Cellular radio systems.

UMTS receiver specification

The UMTS receiver requirements are listed in Table 2.13 [1], [5]. From this table, a -99 dBm antenna-referred noise floor is required to keep BER to be less than 10^{-3} [1]. Requirements for phase noise and IIP2 can be obtained from the sensitivity test based on the blocking requirements shown in Table 2.14 [5].

Table 2.13: UMTS receiver specifications

Parameters	UMTS (FDD) Requirements
Frequency band (MHz)	2110 – 2170
Channel spacing (MHz)	5
Sensitivity @ BER = 10^{-3} (dBm)	-107 (12.2 kHz) or -117 (3.84MHz)
Input noise (dBm)	-107
Input SNR (dB)	16.2
Required C/N (dB)	7.2
Required noise figure (dB)	9
Noise floor (antenna-referred) (dBm)	-99
Phase Noise @ 10MHz offset (dBc/Hz)	-129
IIP3 in-band (dBm)	-17
IIP2 (dBm)	+ 46

Table 2.14: UMTS blocking requirements

In-band offset (MHz)	Blocker power (dBm)
10 to 15	-56
> 15	-44

Using the equation (2.1), phase noise of -129dBc/Hz can be calculated at 10 MHz offset.

For the antenna-referred in-band IIP3, it can be given by the in-band intermodulation test set by the standard. In this test, two -46dBm interferers – a simple sinusoid wave and a WCDMA-modulated signal are placed at 10MHz and 20 MHz away from the desired signal. From the specification table, a high linearity is required for the UMTS receiver.

Proposed UMTS receiver architecture

Regarding a UMTS integrated receiver architecture, either zero-IF or low-IF is a good candidate. Here the zero-IF approach is preferred based on the same reason mentioned in DECT section. Moreover, the I/Q accuracy is easy to meet due to the low SNR requirement. Therefore, the zero-IF is the better solution.

Fig. 2.3 shows the CMOS zero-IF receiver architecture for UMTS, and the UMTS front-end specifications are listed in Table 2.15 [1]. In the front end, a gain of approximate 33 dB from the LNA and mixer is high enough to neglect the noise effect from the subsequent blocks. Even though the IIP2 requirement for the mixer is very stringent here, it can be met by calibration in CMOS technology.

The base-band of UMTS is similar to that of DECT, just a 6-bit ADC is adequate here. The tuning range of VCO is still at least 60MHz, like the GSM low-IF architecture.

For the CMOS UMTS zero-IF architecture, the most challenging requirement is set for linearity, but can be met by careful design. IIP2 and IIP3 requirements can be

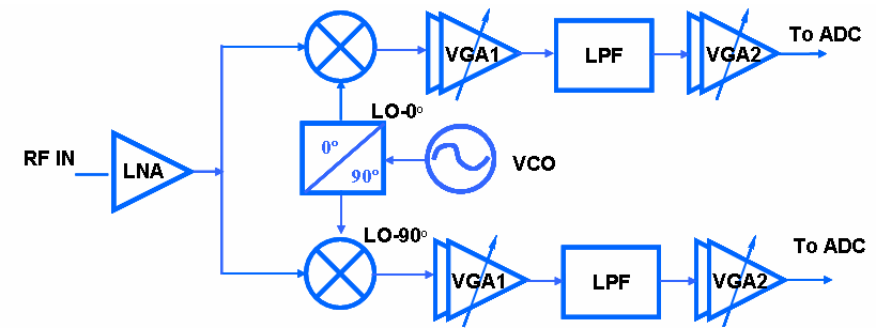


Figure 2.3: CMOS zero-IF receiver architecture for UMTS

Table 2.15: UMTS receiver front-end specifications

	Gain	Noise	IIP3	IIP2
LNA	18 dB	3dB	0 dBm	---
Mixer	15 dB	4.5 nV/$\sqrt{Hz}$	12 dBm**	+ 60 dBm**

** 50Ω- referred

satisfied by the proper choice of the duplexer and the class of the transmitter. 1/ f noise and the dc offset are minor concern due to the wide signal bandwidth. The dc offset can be removed by adding a high pass filter with a pole at several kilohertz.

2.2.4 WLAN

A wireless LAN is a wireless local area network which can provide high-speed internet access worldwide in work environment, at home, and in "hot-spot" at airports, hotels, and other public places. The original IEEE 802.11 standard provides maximum data rate of 2 Mb/s with frequency-hopping spread spectrum (FHSS) or direct-sequence spread spectrum (DSSS) in 2.4 GHz license-free ISM band. Due to the need of more speed, a, b, and g amendments to the original standard have been made by the committee.

IEEE 802.11a was standardized up to 54 Mb/s in 5-GHz band, while IEEE 802.11b was defined up to 11 Mb/s in 2.4-GHz band based on the original IEEE802.11 standard. Finally, IEEE802.11g has been drafted to support data rate up to 54 Mb/s in 2.4-GHz band, which is backward compatible with 802.11b.

WLAN receiver specification

Fig. 2.4 illustrates the frequency plan for WLAN and Table 2.16 [1] shows the receiver requirements for WLAN. For the standard IEEE802.11 b, it has 4 modes with data rates of 1, 2, 5.5 and 11 Mb/s respectively. According to the standard, the most challenging mode is set at the data rate of 11 Mb/s. The required C/N of 14.8 dB can be calculated based on the sensitivity level, channel bandwidth and 11.5 dB SNR. In this standard, the linearity requirement is expressed by the 1-dB compression point.

For the high gain mode, 1 dB compression point of -26 dBm can be obtained based on the test with a -30 dBm simple sinusoid wave interferer placed at 30 MHz away from the -70 dBm desired signal when taking 4 dBm safety margin into account. The phase noise requirements can also be given from this test. The 1 dB compression point for low gain mode can be calculated from the maximum allowed input power set by the standard and 4 dBm safety margin.

For the standard IEEE802.11a, the most stringent requirements are set for the mode of 54 Mb/s. The required C/N is 7.5 dB, which can be derived from the sensitivity level, channel bandwidth and 29 dB SNR. For the requirements of linearity and phase noise, they both can be given from the similar test as for 802.11b. Same as

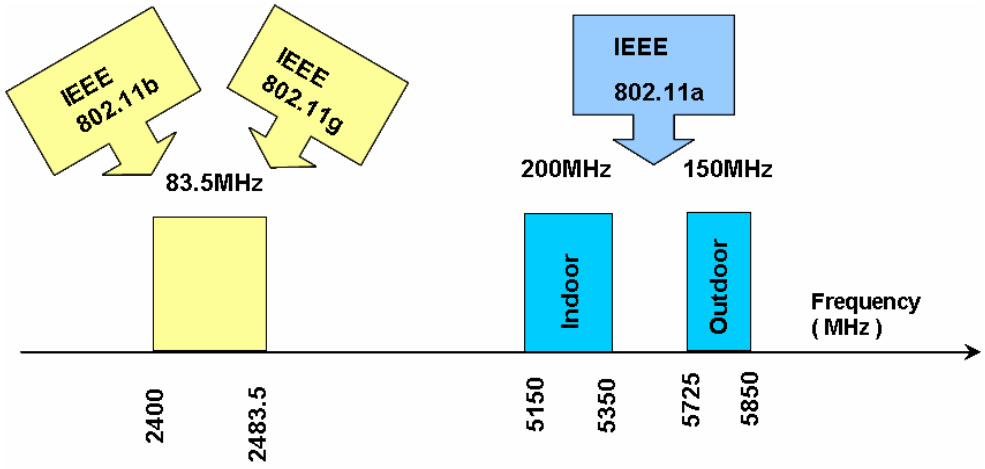


Figure 2.4: WLAN frequency plan

Table 2.16: WLAN receiver specifications

	802.11 b	802.11 a	802.11 g
Channel spacing (MHz)	14	16.6	16.6
Sensitivity @ BER = 10^{-3} (dBm)	-76	-65	-65
Maximum allowed input power (dBm)	-4 (2Mb/s)	-30 (54 Mb/s)	-20 (54 Mb/s)
Required C/N (dB)	14.8	7.5	7.5
1dB compression point (high gain) (dBm)	-26	-26	-26
1dB compression point (low gain) (dBm)	0	-20	-10
Phase noise @ 1 MHz offset (dBc/Hz)	-101	-102	-102

the case in 802.11b, the low gain 1 dB compression point can be given by the maximum allowed input power level plus 10 dB safety margin.

Regarding the standard IEEE802.11g, since it is backward compatible with IEEE 802.11b and allows the data rate as high as IEEE802.11a, its receiver covers the most stringent requirements set both by 802.11b and 802.11a with the exception of 1 dB compression point for the low gain mode due to the maximum allowed received signal of -20 dBm set by the standard.

Proposed WLAN receiver architecture

For a fully integrated solution, zero-IF and low-IF CMOS architectures are both the primary candidates. Table 2.17 [1] compares the challenges for both zero-IF and low-IF architectures.

From Table 2.17, the CMOS zero-IF architecture is a more attractive approach to the fully integrated solution. Fig. 2.5 illustrates the receiver architecture for WLAN. The important specifications are listed in Table 2.18[1].

In the RF front end, noise figure of LNA should be less than 3 dB. A total gain of 30 dB is enough to limit noise effects from the base band. The IIP2 requirement for the mixer is set to be +60dBm. In the base band, a seventh-order filter, two VGAs with a fourth-order Butterworth filter in between, and a 10-bit ADC are required [1].

Table 2.17: Comparison of zero-IF and low-IF architectures for WLAN 802.11a, b and g

	Zero-IF	Low-IF
802.11b	1/f noise and DC offset are minor concern due to the large signal bandwidth.	Extremely high image rejection is needed.
802.11a	1) 1/ f noise is not critical due to the large signal bandwidth. 2) DC offset can be cancelled using a high pass filter. 3) A quadrature accuracy of 38 dB is required to avoid signal corruption.	High power consumption due to a higher maximum signal centered around 10 MHz.
802.11g	1/f noise, DC offset and quadrature accuracy are minor concern due to the half of the operation frequency regarding to 802.11a.	----

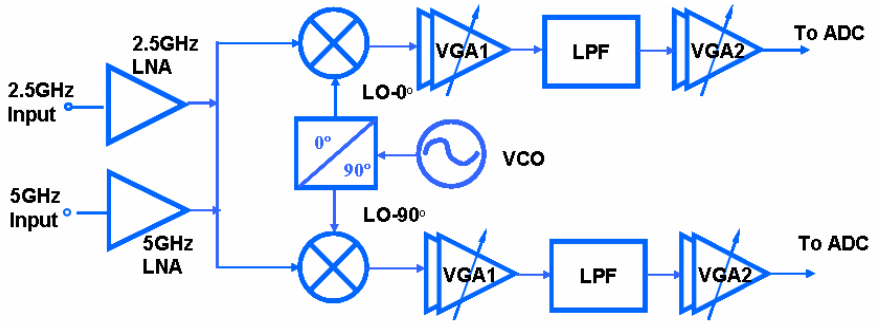


Figure 2.5: CMOS zero-IF receiver architecture for WLAN

Table 2.18: WLAN receiver front-end requirements

	Gain	Noise	IIP3	IIP2
LNA	18 dB	3dB	-15 dBm	---
Mixer	12 dB	4 nV/$\sqrt{Hz}$	-5 dBm**	+ 60 dBm**

** 50Ω- referred

2.2.5 Bluetooth

Bluetooth is an industrial specification for wireless personal area networks (WPAN). It provides a way to connect and exchange information between devices like personal digital assistants (PDAs), mobile phones, laptops, PCs, printers and digital cameras via a secure, low-cost, globally available short range radio frequency. The communication range of Bluetooth is 10 meters (32 feet).

Bluetooth receiver specification

Tables 2.19 and 2.20 summarize the main characteristics of the Bluetooth signal and the main receiver specifications for Bluetooth [1].

From Table 2.20, the Bluetooth standard sets relatively relaxed requirements compared to that of the cellular standards previously discussed. The tuning range of VCO is set to be at least 80 MHz.

Bluetooth receiver architecture

For a fully integrated receiver, the low-IF architecture overwhelms the zero-IF based on the following two reasons: first, higher image rejection is required for the zero-IF architecture. Second, 1/f noise is a major problem for the zero-IF approach because most of the signal energy is within 200 kHz. Fig. 2.6 demonstrates the CMOS low-IF receiver architecture for Bluetooth with an IF at 2MHz.

In the RF front-end side, for LNA, the noise figure can be as high as 5 dB due to the relaxed noise requirement, gain is still 18 dB, and IIP3 is as low as -5 dBm. In the

Table 2.19: Bluetooth signal characteristics

	Bluetooth
Access scheme	FHSS
Channel bandwidth	1 MHz
Modulation	BFSK
Date rate	1 Mb/s

Table 2.20: Bluetooth receiver specifications

Parameters	Bluetooth
Frequency band (MHz)	2400 - 2483
Channel Bandwidth (MHz)	1
Sensitivity @ BER = 10^{-3} (dBm)	-70
Required C/N (dB)	23
Phase Noise @ 1MHz offset (dBc/Hz)	-109
IIP3 (dBm)	-15

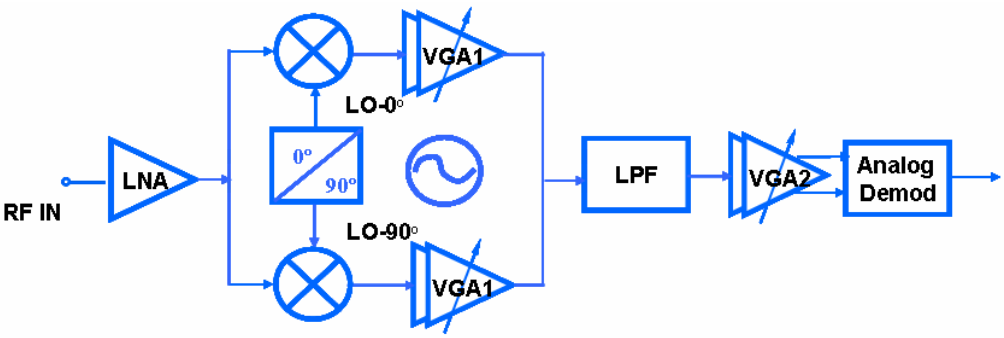


Figure 2.6: CMOS low-IF receiver architecture for Bluetooth

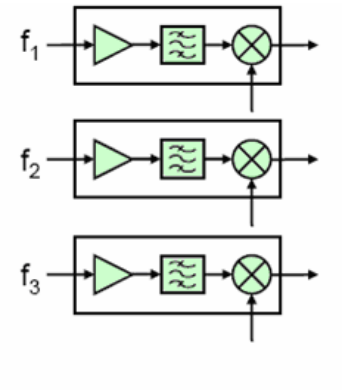
base band, a fourth-order complex active filter is required for the image suppression purpose. An ADC is replaced by an analogy demodulator to reduce the power consumption [1].

2.3 Universal reconfigurable receiver architecture

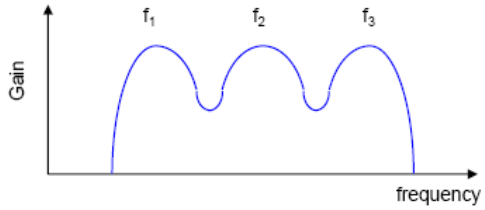
Through decades of continuous efforts on improving the quality and expanding the functionality of wireless communication services, many standards have been brought to the market. Since these standards were originally developed on different continents such as Europe, USA and Japan, they are not compatible with each other. This leads to the disadvantages of high cost and communication inconvenience. Therefore the emergence of a universal multi-standard terminal which can support different standards in different networks at the same time is inevitable.

There are three ways towards multi-standard terminal illustrated in Figs. 2.7 (a) to (c) [7]. Their pros and cons have already been addressed in Table 2.2.

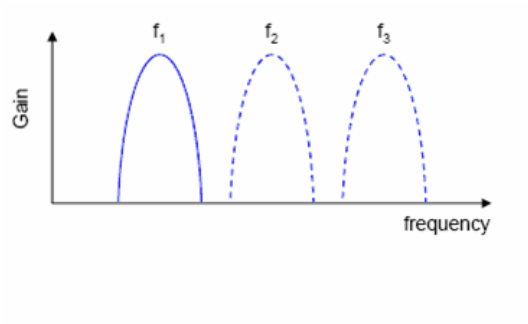
Here the pure parallel RF architecture is excluded due to its extremely large area requirement. Considering the real case that there is no need to access the different cellular standards at the same time, the concurrent operation provided by the multi-band architecture is not necessary. Also keeping other services active requires more power. Meanwhile, the reconfigurable architecture can provide convenient frequency switching, very small area, low cost and low power consumption without sacrificing the performance of the services. Therefore, for a fully integrated universal multi-standard RF



(a)



(b)



(c)

Figure 2.7: Multi-standard receiver architectures: (a) Parallel RF (b) Multi-Band (c) Reconfigurable or switchable

receiver, the reconfigurable architecture is preferred for the services only used one at a time and a separate parallel receiver path is suggested for services used concurrently.

Fig. 2.8 illustrates the proposed universal multi-standard terminal. Based on the previous analysis of different wireless standards, since Bluetooth is needed concurrently with other services, and also because of the unique analog demodulator for Bluetooth, it occupies a separate RF receiver chain. For all other services such as GSM, DECT, UMTS and WLAN, since the low-IF architecture is best choice for the GSM, while the zero-IF is the most proper solution for DECT, UMTS and WLAN, they can be combined into one RF receiver chain considering the fact that these two architectures are the same if the image suppression is performed in the digital domain for the low-IF.

Finally, the universal multi-standard receiver front-end requirements are summarized in Table 2.21 [1] [5].

From Table 2.21, for a fully integrated multi-standard receiver path, we need a reconfigurable LNA and a reconfigurable mixer. Since both of them should cover most stringent requirements set by these four standards, the gain of LNA should be able to tune to cover the range from 12 dB to 23 dB while keeping the noise figure as low as 3dB when taking the balun loss into account. The IIP3 requirement of LNA is set to 0dBm, which comes from DECT. For the reconfigurable mixer, the gain should be able to tune from 8 dB to 15 dB, while its noise figure can be switched from 4nV/$\sqrt{Hz}$ for WLAN to 9nV/$\sqrt{Hz}$ for all other three services. The IIP3 requirement for the mixer is set to be +12dBm, which is from UMTS, while the IIP2 requirement is set by the GSM mixer.

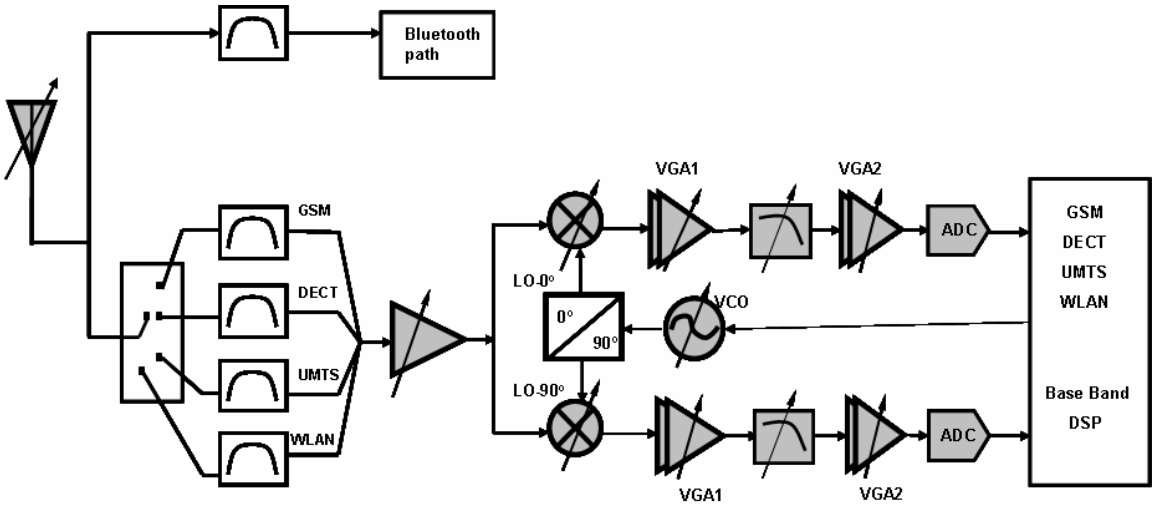


Figure 2.8: Proposed universal multi-standard receiver architecture

Table 2.21: Multi-standard receiver front-end requirements

	Max. Gain (dB)	Noise	1 dB C. P. (dBm)	IIP3 (dBm)	IIP2 (dBm)
LNA GSM	23	3 dB	-15	-5	--
LNA DECT	12	5 dB	-10	0	--
LNA UMTS	18	3 dB	-15	-5	--
LNA WLAN	18	3 dB	-25	-15	--
Reconfigurable LNA	**12 - 23**	**3 dB**	**-10**	**0**	**--**
Mixer GSM	12	$9\text{nV}/\sqrt{Hz}$	- 3	+ 7	+75
Mixer DECT	8	8 dB	- 2	+ 8	--
Mixer UMTS	15	$4.5\text{nV}/\sqrt{Hz}$	+ 2	+12	+60
Mixer WLAN	12	$4\text{ nV}/\sqrt{Hz}$	-15	-5	+60
Reconfigurable Mixer	**8 – 15**	**9 nV/$\sqrt{Hz}$ *** **4 nV/$\sqrt{Hz}$ ****	**+ 2**	**+ 12**	**+75**

2.4 Conclusions

Based on the previous survey, it is important to recognize that RF front end blocks can be reconfigured. Different services can share common blocks such as the LNA, oscillator and mixer in the receiver side. For the feasibility study here, only the development of reconfigurable LNAs and oscillators will be discussed as a proof of the concept of reconfiguration. This study could be easily extended to include mixers and power amplifiers using very similar reconfigurability concepts and tools.

3
Tuning Blocks

In chapter 2, the different service specifications and requirements at the receiver side and a proposed universal terminal have been overviewed. For a fully integrated universal receiver solution, the goal is generally maximizing hardware share to reduce the area, cost and power consumption without significant system performance degradation. In order to realize this goal, the tunable RF building blocks such as filters, LNAs, mixers, VCOs and gain blocks are a must. In fact, the performance of a universal terminal is largely relied on the performance of the tunable blocks. By employing the switches in the RF blocks, the receiver can easily switch from one service to another.

In the following part, some examples presented in some recent publications[2],[3] will be reviewed to show reconfigurablility of RF building blocks such as tunable LNAs, mixers and VCOs. Fig. 3.1 shows a multi-mode LNA which can serve at GSM900, DCS1800, PCS1900 and WCDMA [3]. The unique feature of this LNA is that it is capable of switching between different modes by tuning the biasing current of the device and choosing the proper load using multitude of switches. Six different gains can be achieved for this LNA and still utilize the same chip of a single-mode LNA.

Fig. 3.2 represents the mixer with tunable IIP2 [3]. For different wireless services, distinct IIP2 requirements for down-converter are specified. These specifications have already been summarized in chapter 2. In this circuit, the IIP2 requirements can be enhanced up to +42 dBm for GSM, DCS and PCS and +47 dBm

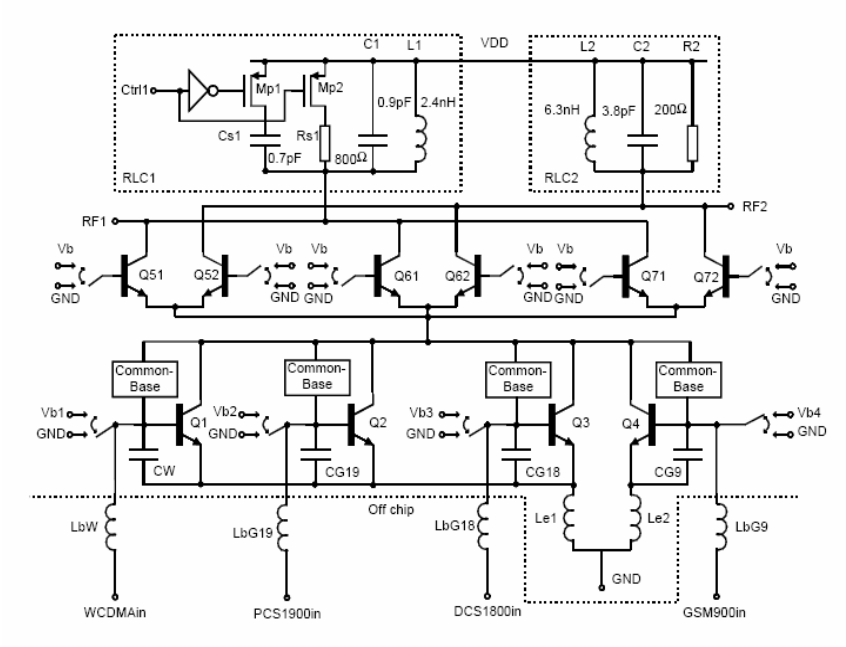


Figure 3.1: Multi-mode LNA [3]

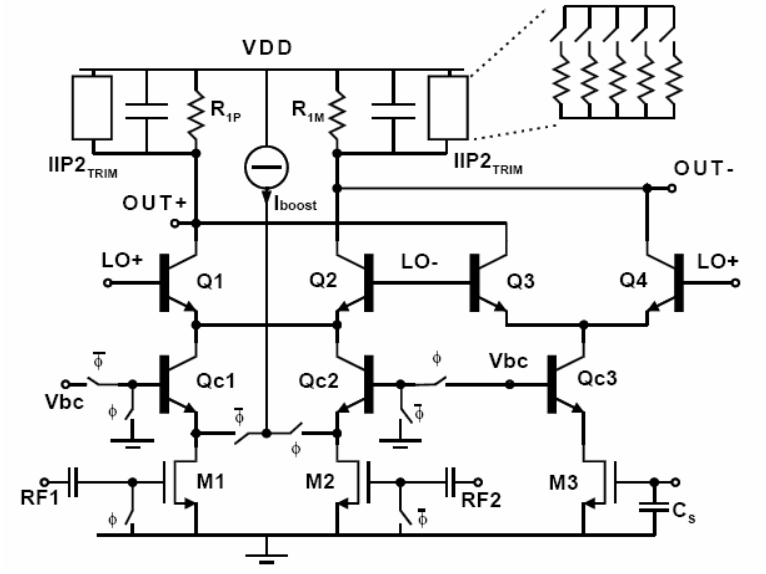


Figure 3.2 : Mixer with tunable IIP2 [3]

for WCDMA by switching the binary-weighted resistors shown on the upper right corner of the circuit. Even though the circuit cannot reach IIP2 as high as +60 dBm for UMTS (WCDMA) and +75 dBm for GSM [1], it does provide a good approach towards a reconfigurable mixer for a universal terminal.

Fig. 3.3 illustrates the use of a tunable CMOS active inductor to build a VCO [2]. By tuning the active inductor from 0.1 to 15 nH, the VCO can cover a frequency range from 500 MHz to 2 GHz. The advantage of this circuit is the continuous tuning range, but it cannot cover the services located at higher frequencies such as WLAN.

There are some tuning elements which can be realized using CMOS technology, such as active tunable resistor, MOS capacitor and active tunable inductor [2]. Fig. 3.4 shows the simulated tuning range for the active resistor. The resistor value is reverse proportional to the tuning voltage, while the parallel parasitic capacitance associated with the active resistor is proportional to the tuning voltage shown in Fig. 3.5, which means

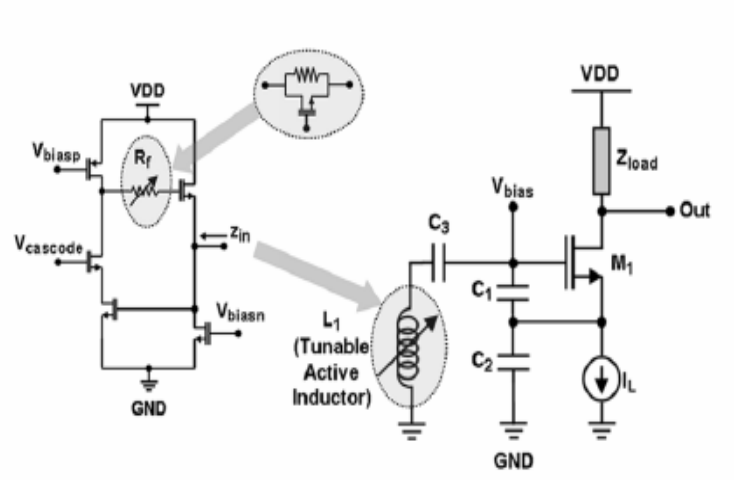


Figure 3.3: VCO using tunable active inductor [2]

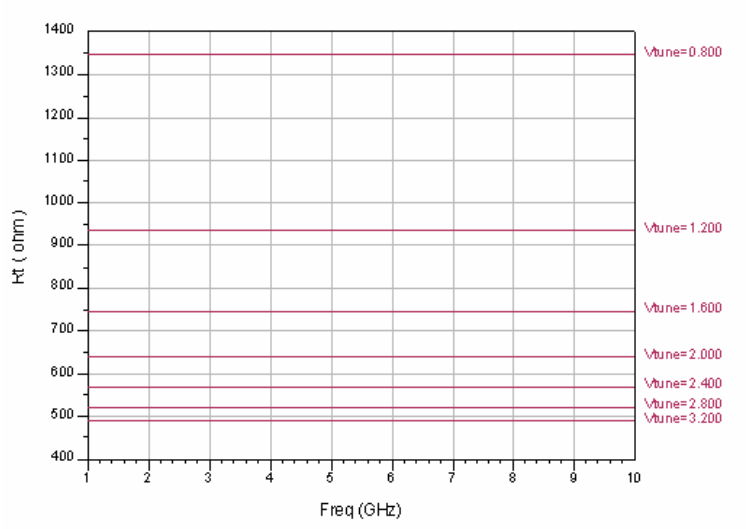


Figure 3.4: Simulated tuning range of active resistor

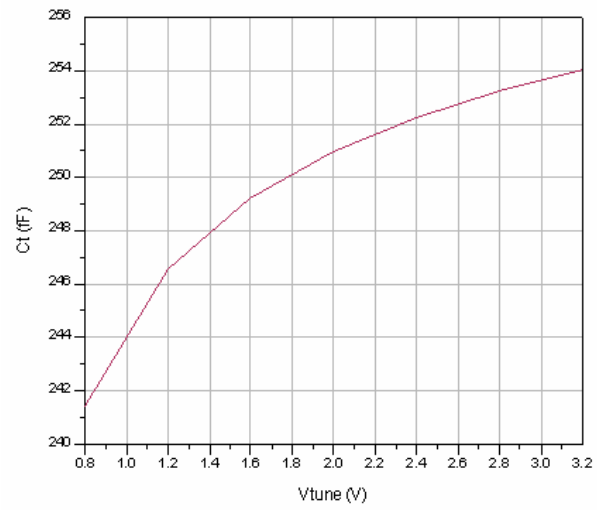


Figure 3.5: Simulated parasitic capacitance associated with the active resistor

the active resistor can work at higher frequency. Fig. 3.6 shows the simulated tuning range for a tunable MOS capacitor. The tuning diagram for an active inductor [2] is presented in Fig. 3.7. Table 3.1 lists the tuning range vs. applied voltage for active resistor, MOS capacitor and active inductor.

In the design of tunable building blocks, the switch plays a very important role. In order to meet the stringent requirements for low power consumption in the future wireless communication, a high performance switch is needed. Nowadays designers have options, as there are different kinds of switches on the market such as GaAs switches,

PIN diodes and MEMS. MEMS offers the lowest DC power dissipation. Table 3.2 shows a performance comparison of active switches to RF MEMS, and Table 3.3 lists the performance comparison of RF MEMS to active tunable components such active resistor, active inductor and varactor.

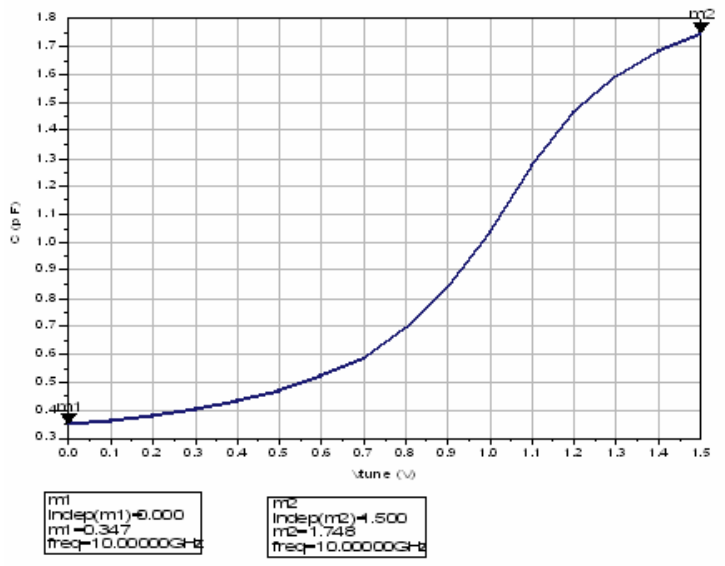


Figure 3.6: Simulated tuning range of varactor

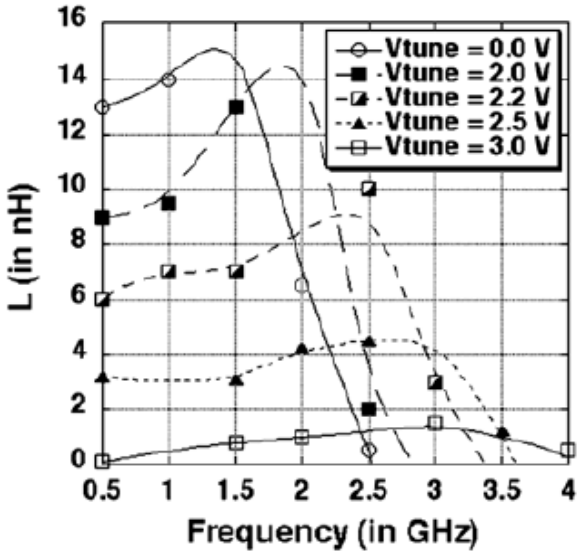


Figure 3.7: Tuning range of active inductor

Table 3.1: Tuning range of active resistor, MOS capacitor and active inductor vs. applied voltage

	Active Resistor (ohm)	MOS Capacitor (pF)	Active Inductor (nH)
Tuning range	490 to 1350	0.35 to 1.75	0.1 to 15
Vtune (V)	0.8 to 3.2 V	0 to 1.5V	0 to 3 V

Table 3.2: Performance comparison of active switches to RF MEMS switch

Performance	Active Switches (GaAs switch , PIN diode)	RF MEMS Switch
Insertion loss [Teravicta MEMS switch]	0.6 dB – 1.5 dB depending on frequency and power	0.15 dB – 0.3 dB over 2GHz to 6 GHz
Linearity [4]	Low	High (IP3 > +66dBm)
Current consumption [4]	Yes	No
Size [4]	compact	compact

Table 3.3: Performance comparison of RF MEMS to active tuning components

Type	RF MEMs	Active Resistor	Active Inductor	Varactors
DC Power Consumption	Few nW	Hundreds of mW	Hundreds of mW	Reactive only
Speed	< 5 μs	>100 ns	>100ns	Few ns
MMIC Integration	Difficult to integrate with Silicon	Easy	Easy	Easy
Packaging	Need hermetic sealing	No special requirements	No special requirements	No special requirements
Area	Smaller	Small	Large	Small

From Tables 3.2 and 3.3, it can be seen that RF MEMS can provide much better performance in terms of insertion loss, linearity and power consumption. Low insertion loss and zero current consumption mean that the battery life time can be extended much longer when using RF MEMS instead of using active switches or active tuning elements for wireless portable devices.

Currently, a packaged RF MEMS switch is utilized for building reconfigurable circuits. But eventually RF MEMS will be built on low resistive CMOS silicon substrate. This means that they can be integrated with all other RF front-end circuits. Therefore, RF MEMS is the first choice to be used in tunable RF blocks in a fully integrated universal multi-standard terminal. In Chapters 4 and 5, MEMS switches will be used in the reconfigurable LNA and oscillator designs, and their effects on the performance of LNA and oscillator circuits will be addressed.

4

Development of a Reconfigurable Low Noise Amplifier

In pursuing a universal design of a wireless receiver, the various requirements and specifications of a low noise amplifier for the different services have been investigated. In this study, the design is concentrated on UMTS at 1.9 GHz, and WLAN at 2.4 GHz and 5.2GHz. The low noise amplifier stage is the first stage after the reconfigurable or the multi-band antennas cascaded by bank of filters. Table 4.1 shows a comparison between UMTS and WLAN, where the gain and noise figure requirements are clearly specified.

In the feasibility study, it has started by designing various stages that conform with each service. This step was followed by developing a multi-service design that would require using one service at a time. When using a specific service, other services need to be switched off. In this step, hard-wired connections have been utilized rather than using switchable elements. As the last step in the design, RF MEMS switches have

Table 4.1: Gain and noise figure requirements for UMTS and WLAN

Wireless Services	Frequency	Gain	Noise Figure
UMTS [2]	1.92 – 2.17 GHz	18 dB	3 dB
WLAN [2]	2.4 – 2.484 GHz	18 dB	3 dB
	5.15 -5.35 GHz	18 dB	3 dB

been used for switching services on and off. Details of the design, fabrication, and measurements will be given in the following section.

4.1 LNA design concept

In the preliminary design of individual LNA stages, it was clear that the narrow band design is sufficient to cover the various required service bandwidths. This conclusion was very essential to define a strategy for building simple single and reconfigurable LNA structures. As a narrow band design, it only needs a single stub matching at the input and output ports. Therefore, the standard methods have been used for designing LNAs, where the input match is compromised for low noise figure, while the output match is optimized for maximum gain.

Meanwhile, for implementing these designs, a 50-Ohm line at both the input and the output ports was used, while the required match was obtained by specifying the location and the length for a single shunt stub at both the input and output sides. Based on this simple design method, the circuit is able to accommodate the inclusion of three various stubs to cover three frequency bands. The concept diagram is shown in Fig. 4.1.

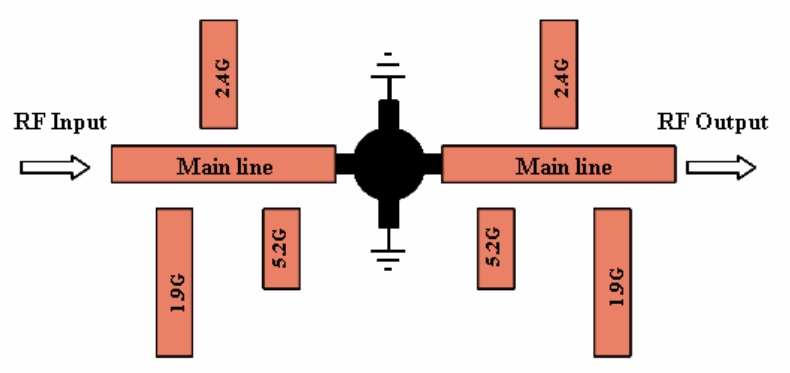


Figure 4.1: Reconfigurable LNA concept diagram with three various matching stubs

4.2 LNA design equations

Here a GaAs MESFET NE3210S01 transistor has been used to design the reconfigurable LNA circuit. The manufacture generally supplies the common noise parameter data in addition to the S-parameters. These noise parameters mainly the minimum noise figure F_{min}, the noise resistance R_n, and the optimum noise admittance $Y_{on} = G_{on} + jB_{on}$, where the noise figure F of the two port network is given by the source admittance presented to the input terminal and calculated based on the following expression:

$$F = F_{\min} + \frac{R_n}{G_G}|Y_G - Y_{on}|^2 \qquad (4.1)$$

Meanwhile, the output is tuned for the maximum available gain, where the device is loaded with the optimum noise admittance at the input Y_{on}. Then the new output impedance is recalculated after matching the input to this previously known optimum noise load. Finally, for maximum available gain, the output matched network is the conjugate of the above calculated output impedance.

4.3 Principle for single-stub matching

The simple single-shunt-stub matching network is shown in Fig. 4.2. First, change all the impedances and admittances to their normalized values. Second, transfer the normalized load admittance to Y_{in1} through a transmission line l_1 so that Y_{in1} is located on the unit conductance circle on the Smith Chart shown in Fig. 4.3 (a), which means Y_{in1} should be equal to $1 \pm j\,B_{in1}$ when looking into the port ①. Third, use a stub l_2 (open or

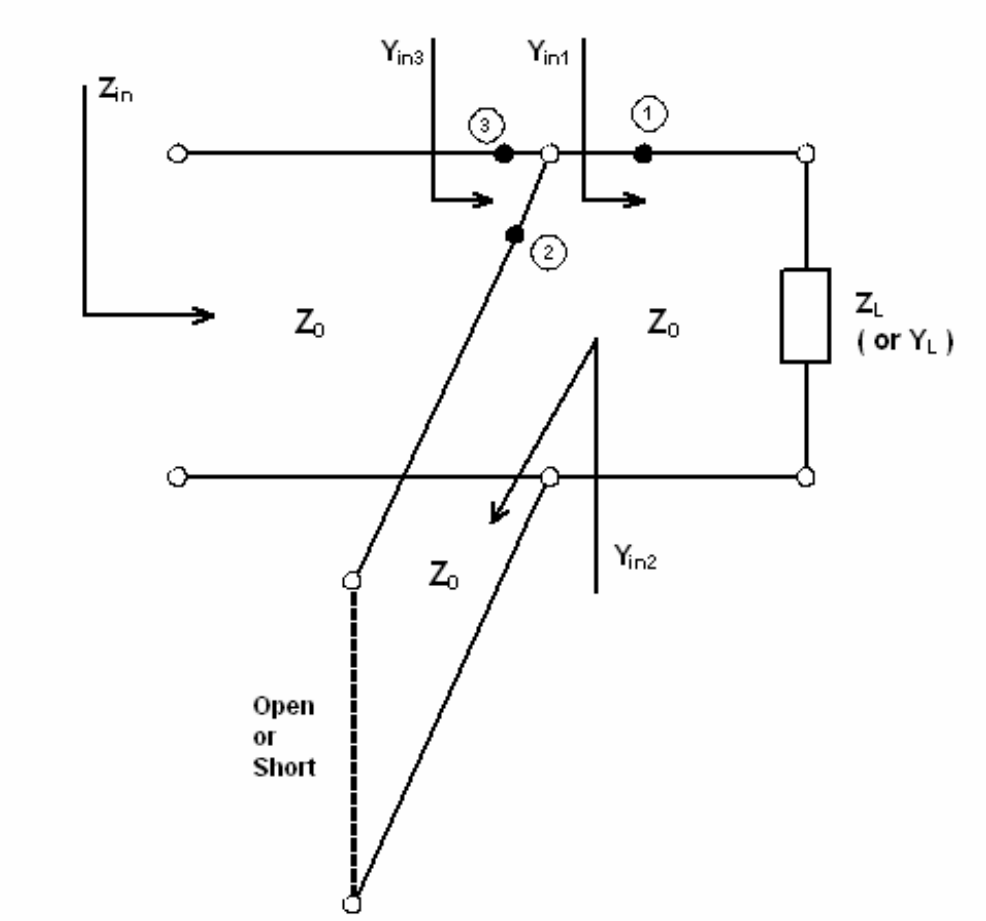
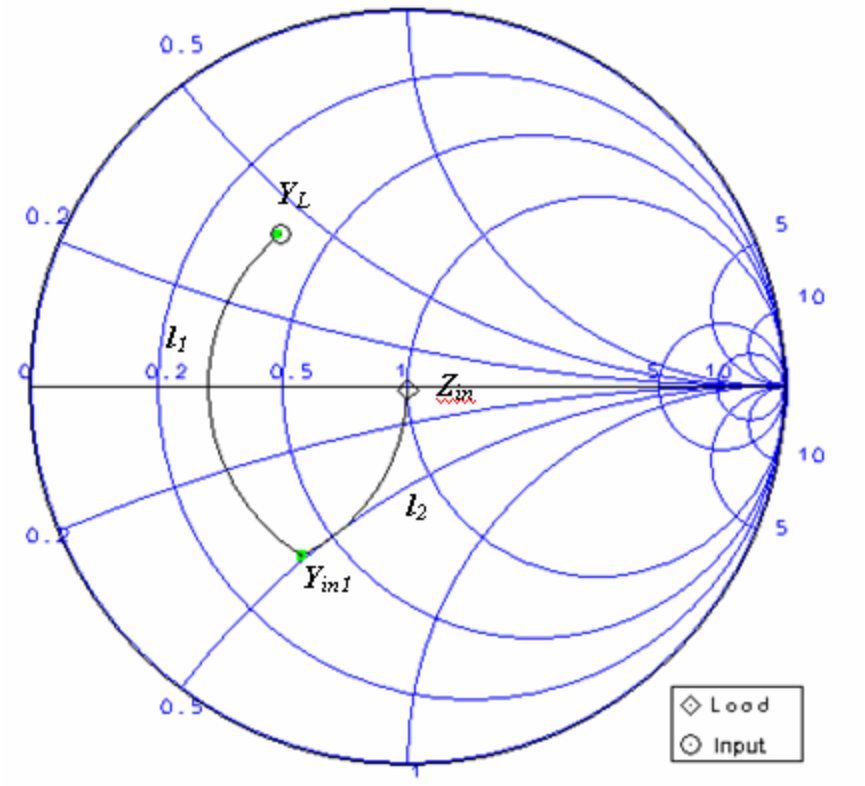
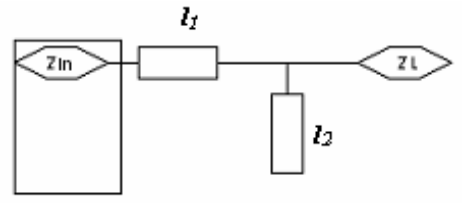


Figure 4.2: Single-stub matching network



(a)



(b)

Figure 4.3: (a) Single stub matching using ADS Smith Chart

(b) Single stub generated by ADS Smith Chart

short) and tune the length of the stub to cancel the imaginary part of Y_{in1}, which means the admittance looking into port ② Y_{in2} should be ∓ j B_{in1}. Finally, the admittance looking into port ③ Y_{in3} should be unity indicating that matching is accomplished. The exact length of transmission line l_1 and the stub l_2 can be obtained from the Smith Chart. Actually, ADS Smith Chart provides a very convenient way to create a matching network. It can generate a matching network and automatically calculate the length when the matching is performing. Fig. 4.3 (b) shows the matching network with the calculated lengths using Advanced Design Suite (ADS) Smith Chart.

4.4 Implementation

Here the Agilent ADS software package has been used to finalize the design of the reconfigurable LNA. In the following sections, various designs will be discussed and the final circuit layouts will be demonstrated. As previously mentioned, the design is started by a single-service design, followed by a hard-wired reconfigurable multi-service design. The last step is the design of the reconfigurable structure which is implemented by using MEMS switches and their biasing networks. All the designs in this section are realized on the same FR4 substrate with a permittivity of 4.4 and a thickness of 62 mil. The S-parameter measurement is done using HP8510C vector network analyzer, and noise figure is measured using HP8970A noise figure meter.

4.4.1 Single-service design

The motivation of designing single services is to find the common parts of individual services which can be shared by the multi-service design. The shared parts should include the transistor, input and output matching networks as well as the biasing networks. Therefore, the amplifiers should be stable at all designed frequencies. Unfortunately, the stability factor K of the device datasheet shows that the transistor is unstable at all these frequencies (i.e. $K<1$), especially at 1.9 GHz. In order to improve the K factor, a small microstrip line was used to emulate an inductor and placed between the source and ground. Its size has been tuned so that the transistor is almost stable at all the designed frequencies, however, such a step is not generally recommended as it might produce severe oscillation at other frequencies. After the transistor stability has been established in our case, the small signal parameters such as gain, minimum noise figure and return loss have been recalculated using the newer S-parameter set. All the following single service designs are based on the re-simulated small signal parameters. In order to ease the following multi-service design, the length of $\lambda/4$ dc feed for both 1.9 GHz and 2.4 GHz has been adjusted to be the same. Such adjustment has little effect on the LNA performances.

ADS is a very powerful tool for microwave circuit design. The Smith Chart tool, for example, in ADS provides a convenient way for matching using passive components such as inductors and capacitors or using distributed microstrip lines. For all the single-service designs including LNA at 1.9GHz, 2.4GHz and 5.2GHz, ADS Smith Chart was used as a tool to design these matching networks. A summary of the design procedures

that was adapted for all services is given here:

1. Select the transistor and the biasing condition which can provide a low noise figure and high gain at the same time.
2. Check the stability factor of the transistor. If the transistor is unstable, stabilize the transistor first without significant noise figure degradation.
3. Obtain optimum source impedance Z_{opt} of the transistor and use the Smith Chart tool to design the input matching network. The input-matching network should be conjugately matched to Z_{opt} to achieve good noise figure.
4. Obtain the output impedance Z_{out} of the transistor after step 3, and use the Smith Chart tool to design the output matching network. The output matching network should be conjugately matched to Z_{out} to get a good output return loss and high gain.
5. Optimize the input and output matching circuits to obtain the best performance in terms of noise figure, gain and return loss.
6. Add the biasing network into the circuit and re-optimize the circuit.

4.4.1.1 LNA at 1.9 GHz

Following the design steps mentioned above, the LNA operating at 1.9GHz has been built. Fig. 4.4 illustrates the ADS schematic diagram including the biasing circuitry. The real circuit board is presented in Fig. 4.5. Simulation results including gain, noise figure and return loss are shown in Fig. 4.6.

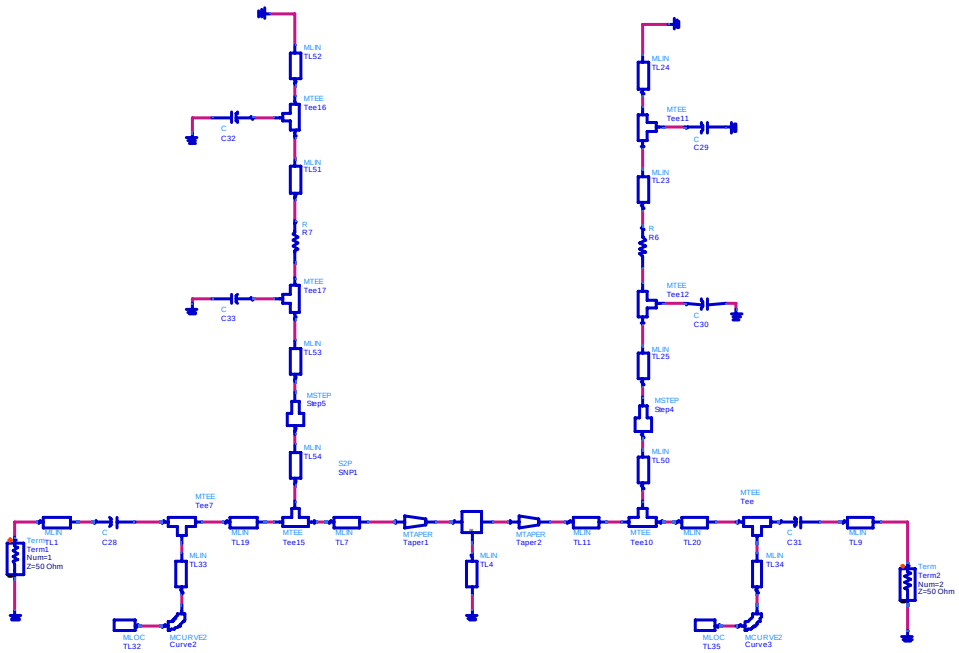


Figure 4.4: Schematic diagram of a single-service LNA at 1.9GHz

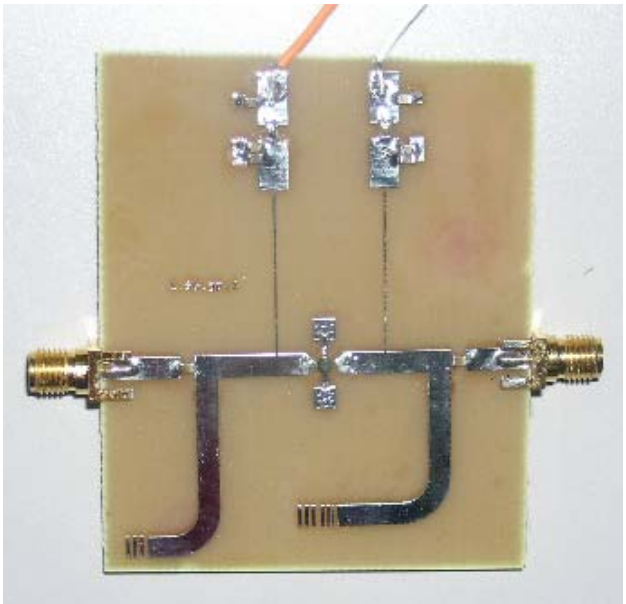


Figure 4.5: PCB of single-service LNA at 1.9GHz

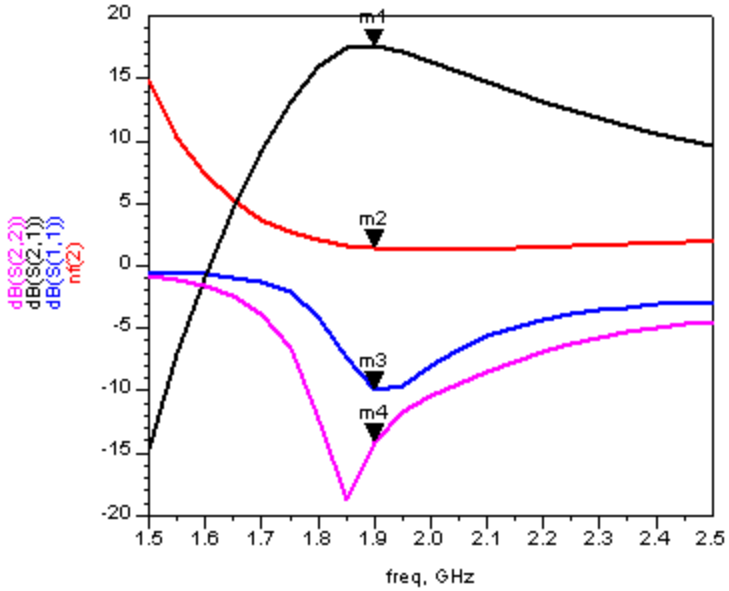


Figure 4.6: Simulated gain, noise figure and return loss of single-service LNA at 1.9GHz

From Fig. 4.6, a simulated gain of 17.5 dB was predicted. Noise figure at 1.9GHz is 1.4 dB, which is slightly higher than 1dB, where the relatively high noise figure is related to the utilized FR4 substrate. Compared to the gain and noise figure requirements of UMTS listed in Table 4.1, 18 dB gain can be achieved by using a two-stage amplifier with the first stage designed for low noise figure purpose and the second stage designed to achieve maximum gain. Since the noise from the second stage has little effect on the noise performance of the whole amplifier, the noise figure should not be degraded and should still be around 1.4 dB, which can meet the noise specification requirement of less than 3 dB. From the simulation results, good return loss is expected at both the input and output stages.

Figs. 4.7 and 4.8 show the measured gain and return loss of the single-service designed at 1.9GHz as compared to the simulated results.

A measured gain of 14.8 dB can be obtained from one stage, which is slightly lower than predicted results. The drop in gain is related to the use of the relatively lossy FR4 substrate. Meanwhile, measured and predicted input and output return loss results are very similar.

4.4.1.2 LNA at 2.4 GHz

Repeating the previous design procedures, an LNA operating at the frequency of 2.4 GHz has been designed, fabricated, and tested. Figs. 4.9 and 4.10 show the schematic diagram, the board realization, and the simulation results.

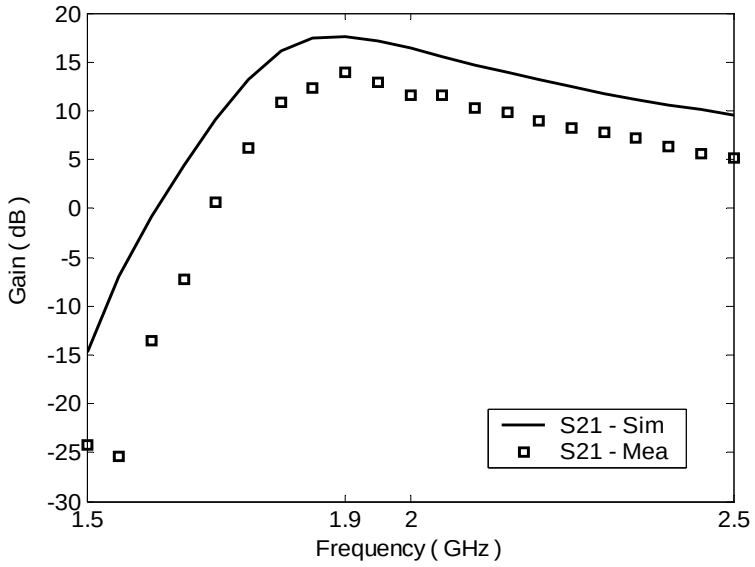


Figure 4.7: Measured and simulated gains of single-service LNA at 1.9GHz

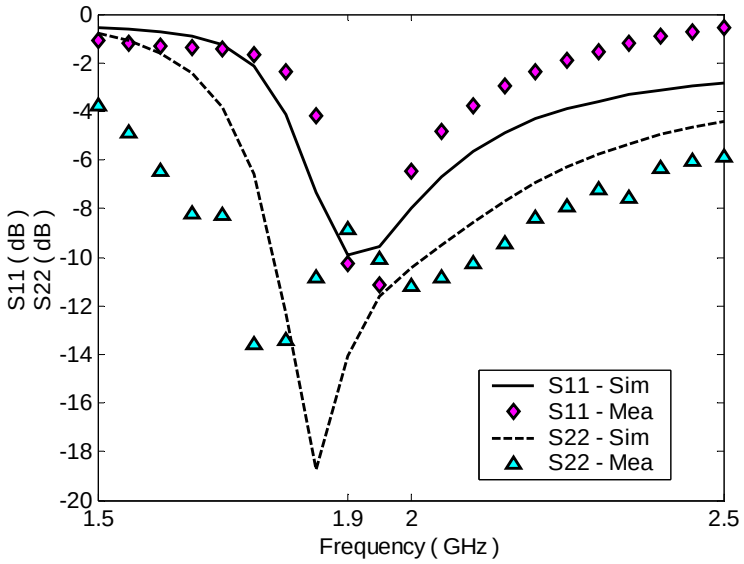


Figure4.8: Measured and simulated return losses of a single-service LNA at 1.9GHz

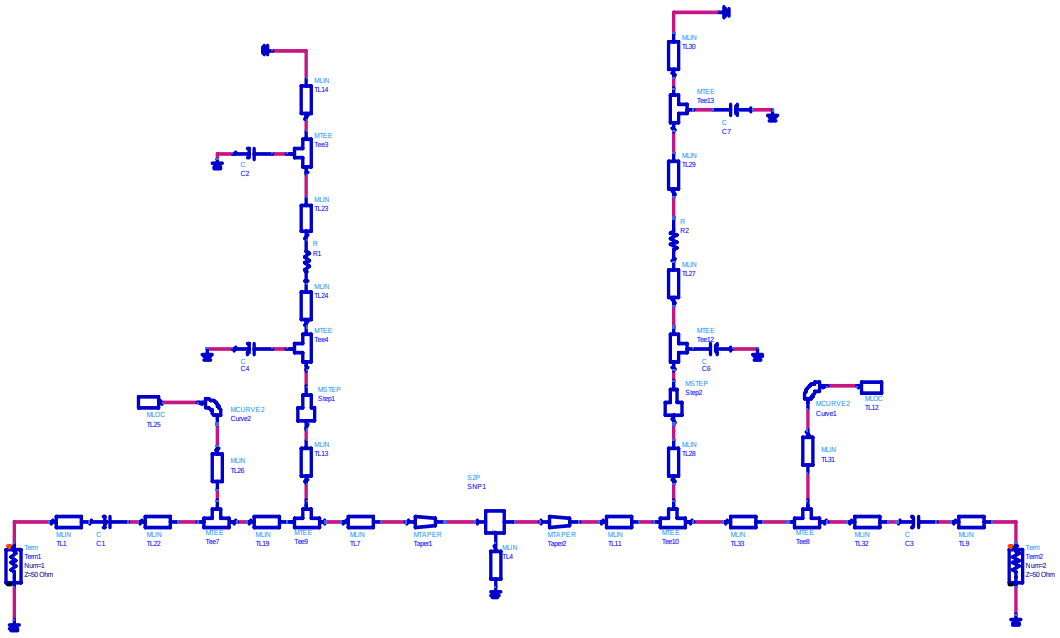


Figure 4.9: Schematic diagram of single-service LNA at 2.4 GHz

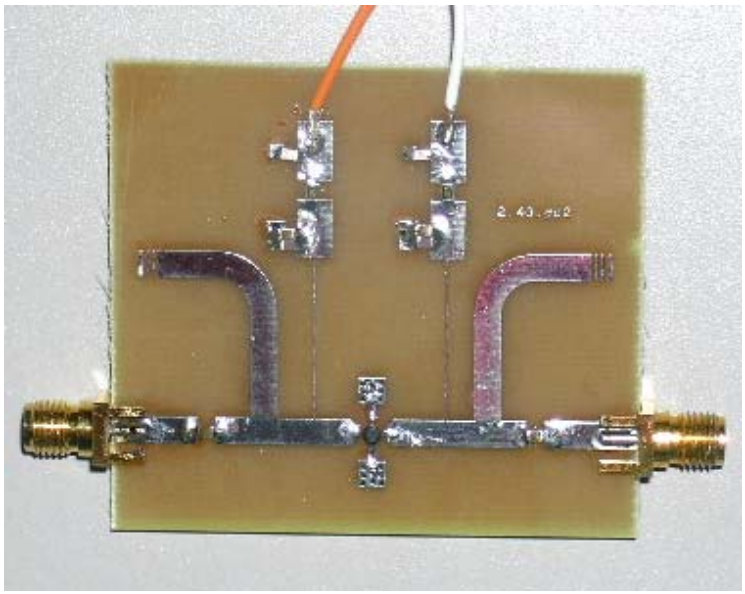


Figure 4.10: PCB of a single-service LNA at 2.4 GHz

From Fig. 4.11, a gain of 16.4 dB can be obtained at 2.4GHz. In order to meet the gain requirement of 18 dB, a two-stage design with a low noise stage followed by a maximum gain stage is needed. The noise figure is 1.5 dB due to the same reason of the FR4 substrate, but still less than 3 dB. The input and output matching are quite good with S_{11} of 12.8 dB and S_{22} of -18.2 dB.

For this design, measured results compared to the simulated results are presented in Figs. 4.12 and 4.13. Fig. 4.12 shows the measured and simulated gains. Fig. 4.13 illustrates the measured and simulated return losses.

More than 14 dB gain has been demonstrated. Due to the relatively high loss tangent of the FR4 substrate of the real circuit board, the measured gain is around 2 dB less than the simulated one. Measured results, however, are very similar to the simulated ones.

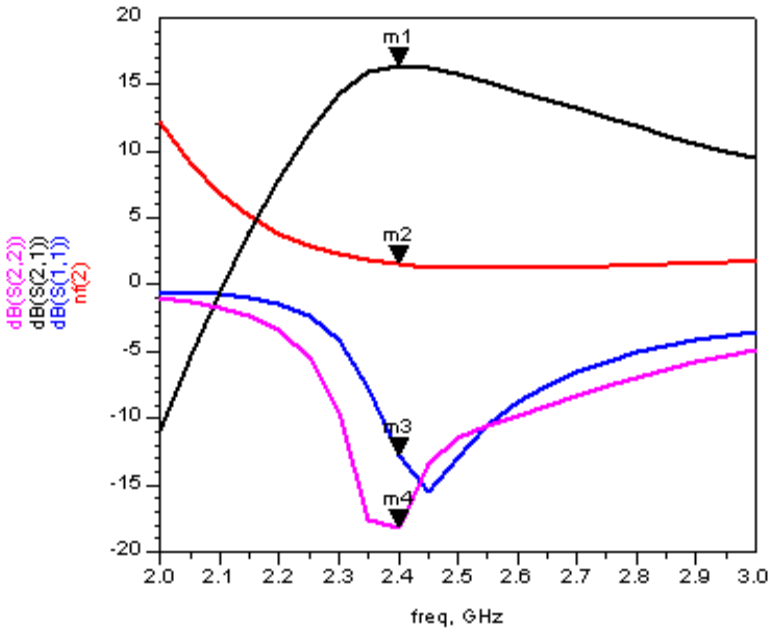


Figure 4.11: Simulated gain, noise figure and return loss of single-service LNA at 2.4 GHz

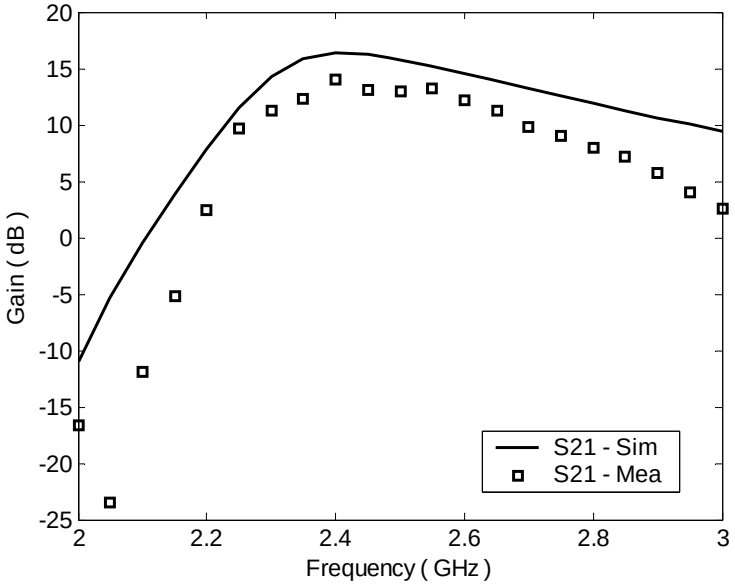


Figure 4.12: Measured and simulated gains of a single-service LNA at 2.4 GHz

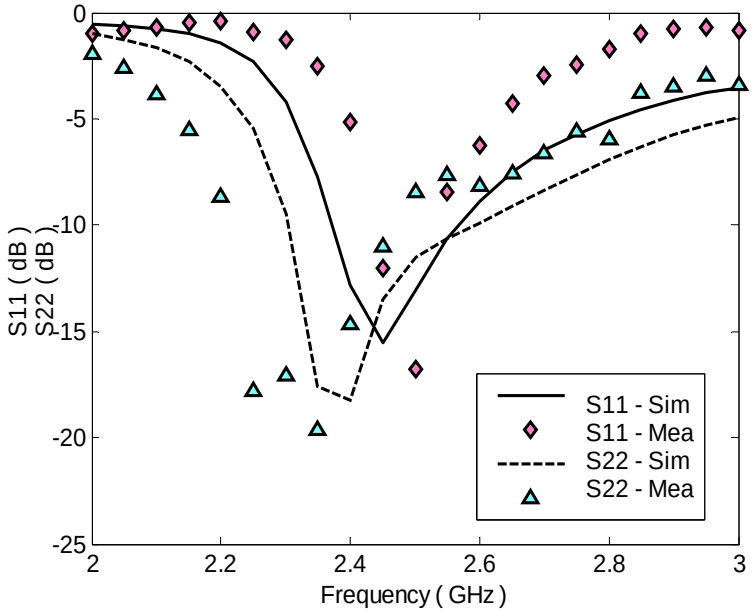


Figure 4.13: Measured and simulated return losses of single-service LNA at 2.4GHz

From the return loss diagram, at least 12 dB output return loss can be achieved. However, input matching, though poor, is still acceptable with S_{11} of -5.9 dB.

4.4.1.3 LNA at 5.2 GHz

Again, following the design steps mentioned above, an LNA operating at 5.2 GHz has been designed. Figs. 4.14 and 4.15 show the schematic diagram and the board realization of the design. Simulation results including gain, noise figure and return loss have been demonstrated in Fig. 4.16.

From the simulated result diagram shown in Fig. 4.16, the measured gain is 10.5 dB, which is far less than the requirement of 18 dB. Therefore, a gain stage must be used

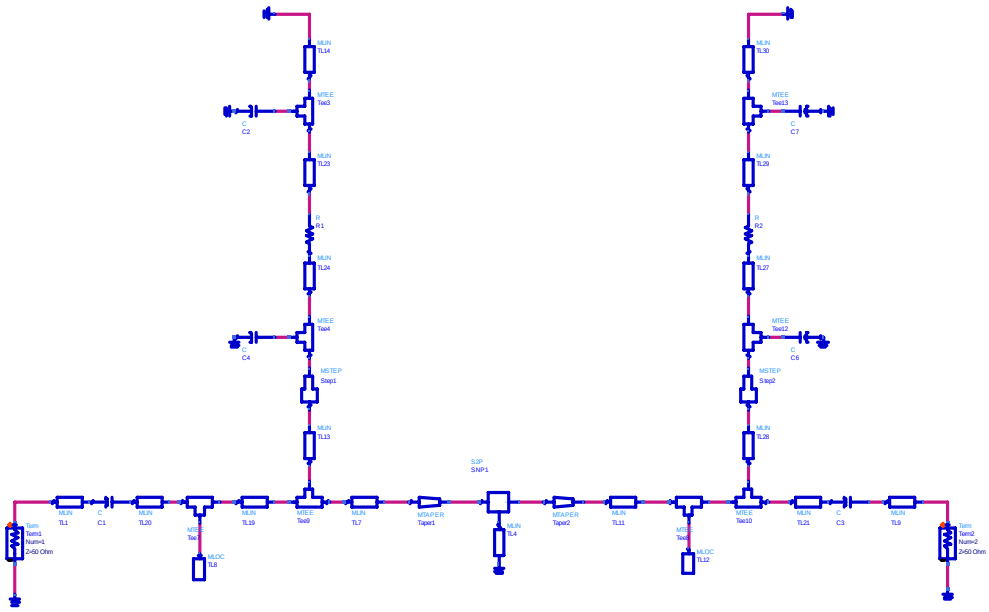


Figure 4.14: Schematic diagram of single-service LNA at 5.2 GHz

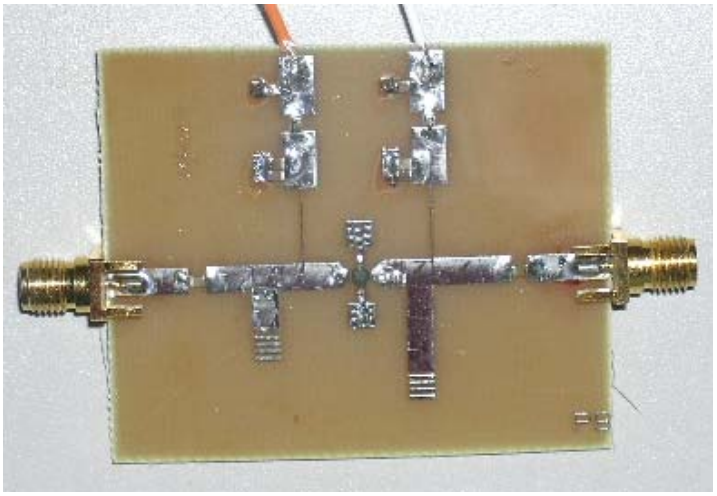


Figure 4.15: PCB of single-service LNA at 5.2 GHz

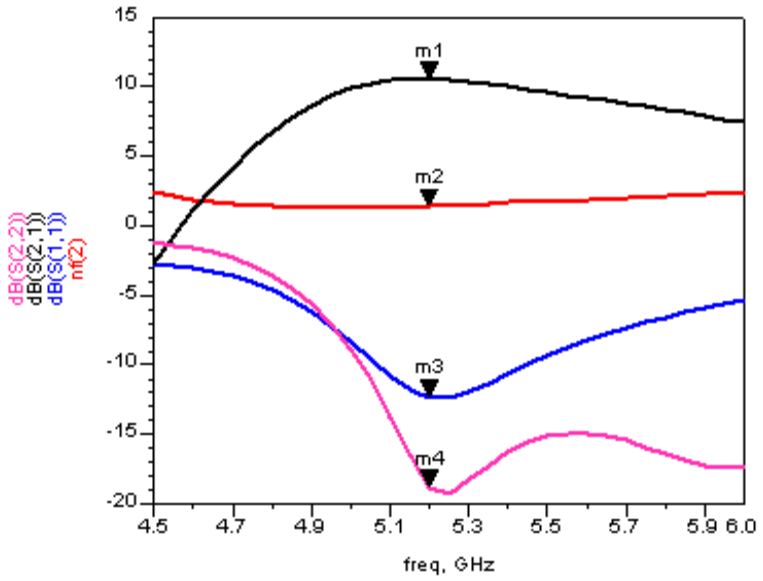


Figure 4.16: Simulated gain, noise figure and return loss of single-service LNA at 5.2 GHz

right after the low noise stage to meet this requirement. The simulated noise figure is 1.4 dB, which is acceptable. S_{11} is -12.3 dB and S_{22} is -18.8 dB, which means good matching at both the input and output stages.

Figs. 4.17 and 4.18 illustrate the measured results compared to simulated results with regard to gain and return loss. A measured gain of 9.3 dB can be achieved. Compared to the simulated result, it is 1.2 dB lower. Again, the measured gain is very similar to the simulated one.

Regarding the return loss diagram, at least 10 dB can be measured both at the input and output stages, which means good matching.

In order to verify the real noise performance of the LNA when using the design steps addressed in this chapter, the noise performance of an LNA operating at 5.2 GHz

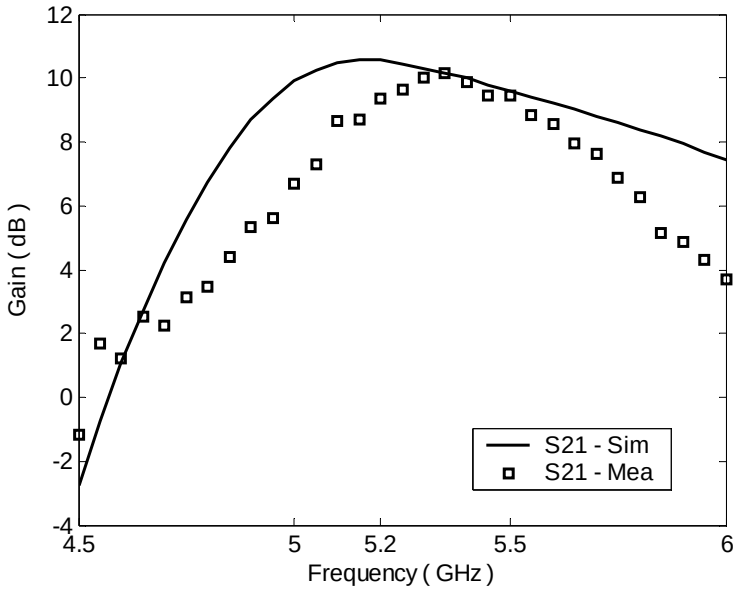


Figure 4.17: Measured and simulated gains of single-service LNA at 5.2 GHz

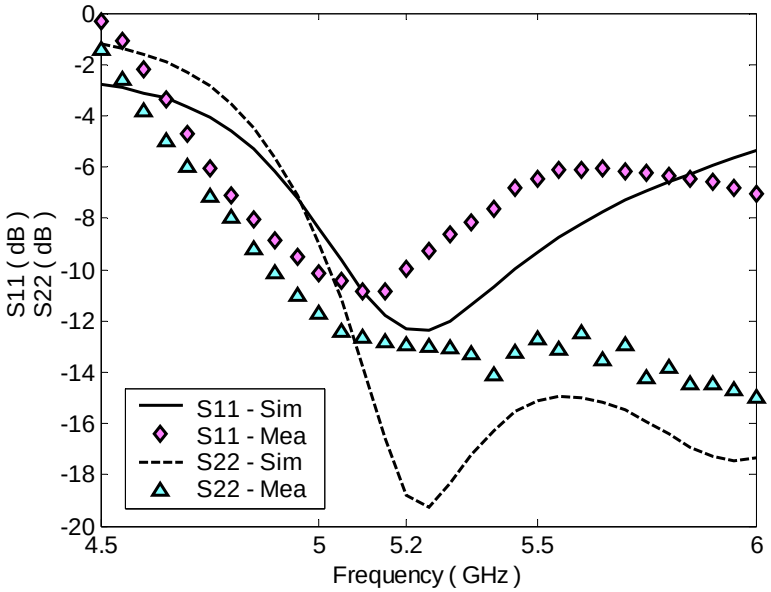


Figure 4.18: Measured and simulated return losses of single-service LNA at 5.2GHz

will be checked here. The board realization is shown in Fig. 4.19, and the simulated and measured gains and noise figures are compared in Fig. 20.

The measured noise figure is quite good, which is 1.8 dB at 5.2GHz, only 0.4 dB higher than the simulated one. This means that following the LNA design steps presented in this chapter, a good noise performance can be achieved.

4.4.2 Multi-service Design

As mentioned in section 4.4.1, the multi-service design is based on sharing common parts of the individual services and minimizing the components and size of the board. By observing layouts of single-service circuits illustrated in Figs. 4.5, 4.10 and 4.15, RF main lines shown in Fig. 4.1, transistor, and part of $\lambda/4$ dc feed can be shared. For dc feed at 5.2GHz, since $3\lambda/4$ has the same effect as $\lambda/4$, $3\lambda/4$ dc feed has been employed in the reconfigurable structure to simplify the layout. For dc feeds at 1.9 GHz and 2.4 GHz, the same length has been used as previously mentioned.

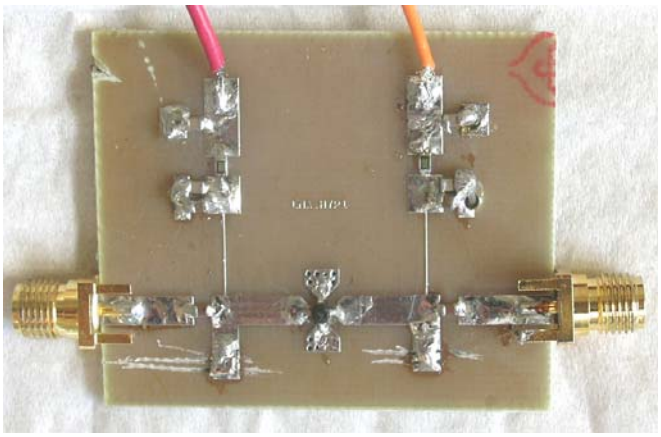


Figure 4.19: PCB of LNA at 5.2 GHz

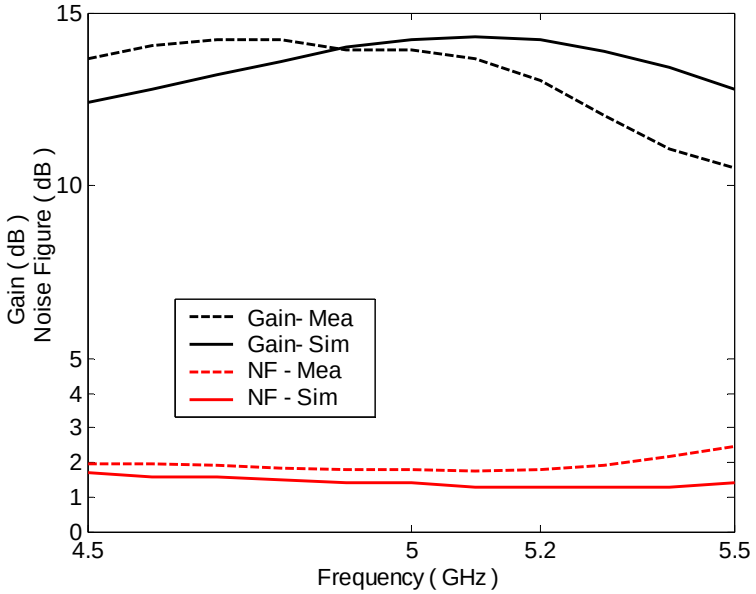


Figure 4.20: Measured and simulated gains and noise figures of LNA at 5.2GHz

Fig. 4.21 shows the layout of the multi-service design with switches which are replaced by hard wires at this stage. In the multi-service LNA, 20 switches are needed. When switches S1_1, S1_2, S2_3, S2_4, S2_5, S2_6, S1_7 and S1_8 are closed while others are off, the LNA is configured to serve at 1.9 GHz. When switches S2_1 to S2_8 are on, while others are off, the LNA is operating at 2.4 GHz. When switches S3_1 to S3_8 are closed with other switches disconnected, the LNA is switched to 5.2 GHz. By using switches, the multi-service circuit consumes the same board area as the single-service LNA at 1.9 GHz, which means large real-estate savings. Simulation results for the multi-service design are the same as the single-service ones because only adjustment of $\lambda/4$ dc feed to be $3\lambda/4$ dc feed for LNA at 5.2 GHz has no effect on the amplifier performances. Board realization is presented in Fig. 4.22.

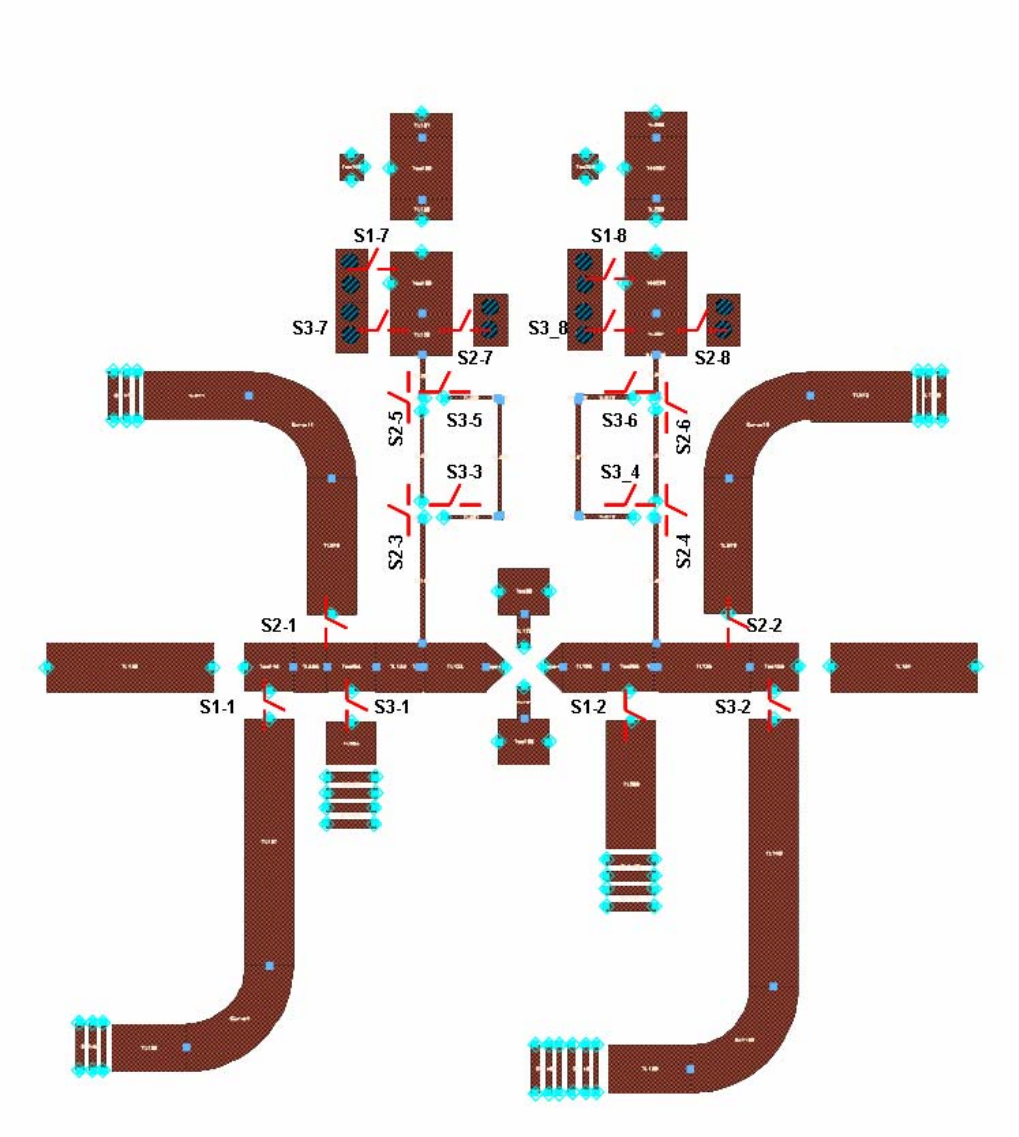


Figure 4.21: Layout of multi-service LNA designed at 1.9GHz, 2.4GHz and 5.2 GHz with switches (In this stage switches are replaced by hard wires)

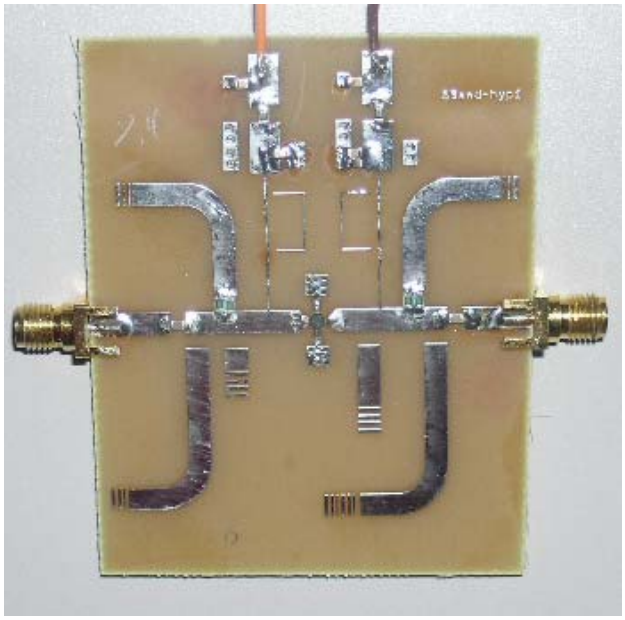


Figure 4.22: PCB of multi-service design configured at 2.4 GHz

Figs. 4.23 to 4.28 illustrate the measurement results compared to the simulated results in terms of gain and return loss for the multi-service design.

The performance of simulated and measured single-service designs and measured multi-service design is compared and summarized in Table 4.2. From the data in this table, the measured gains for the multi-service design are very close to the single-service associated values. Regarding the measured output return losses for the multi-service, at least 12 dB was observed for the multi-service design, which shows a good output match. As anticipated, the input return loss is slightly degraded as it is compromised for the noise figure performance. Upon the previous comparison, it is clear that hard-wired connection used in the multi-service design has only a little effect on the LNA performance.

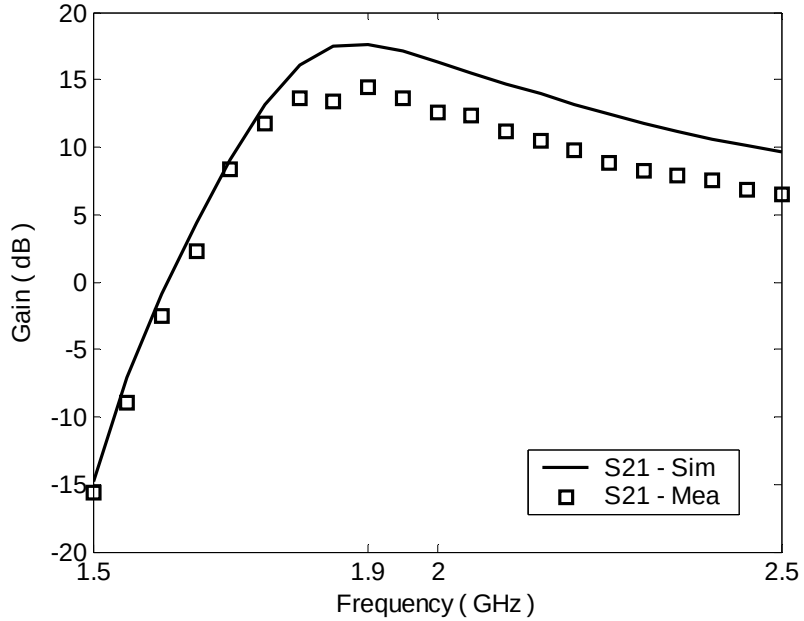


Figure 4.23: Measured and simulated gains of multi-service LNA configured at 1.9GHz

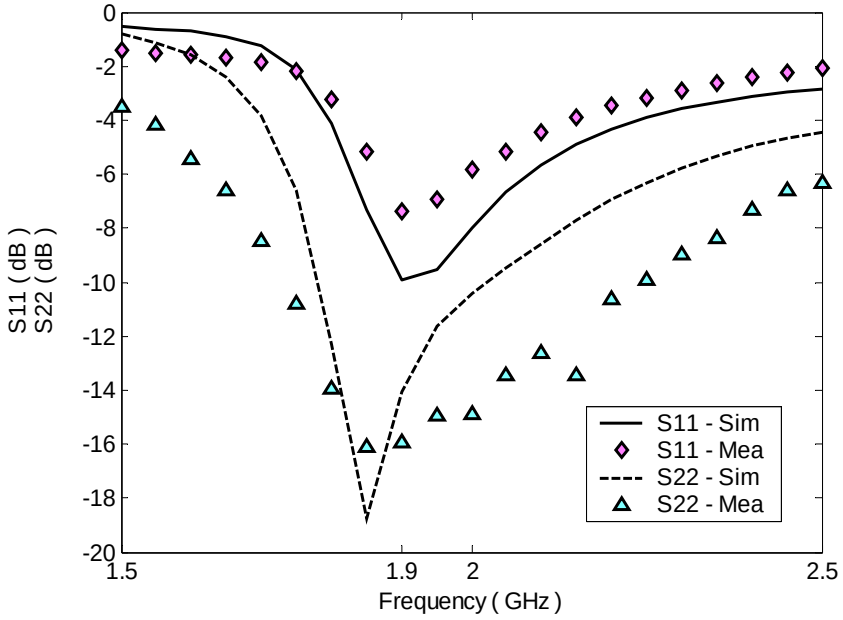


Figure 4.24: Measured and simulated return losses of multi-service LNA configured at 1.9GHz

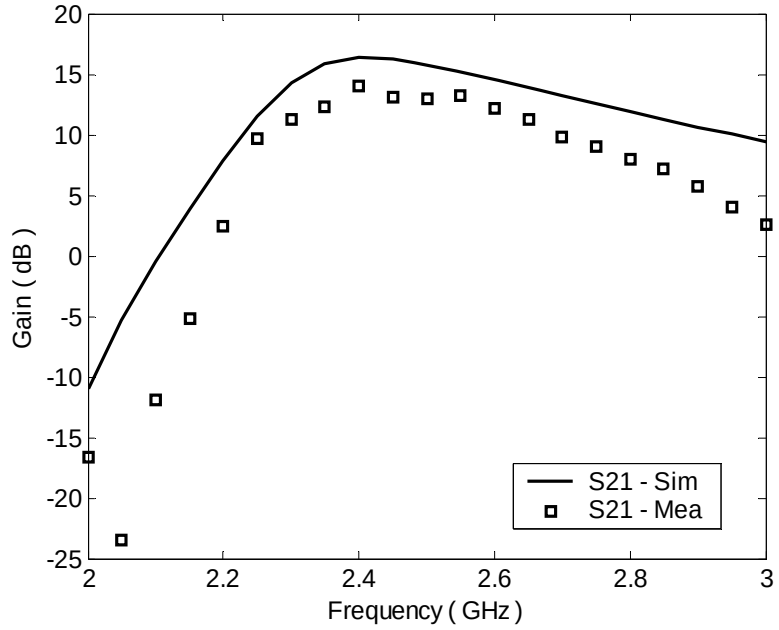


Figure 4.25: Measured and simulated gains of multi-service LNA configured at 2.4 GHz

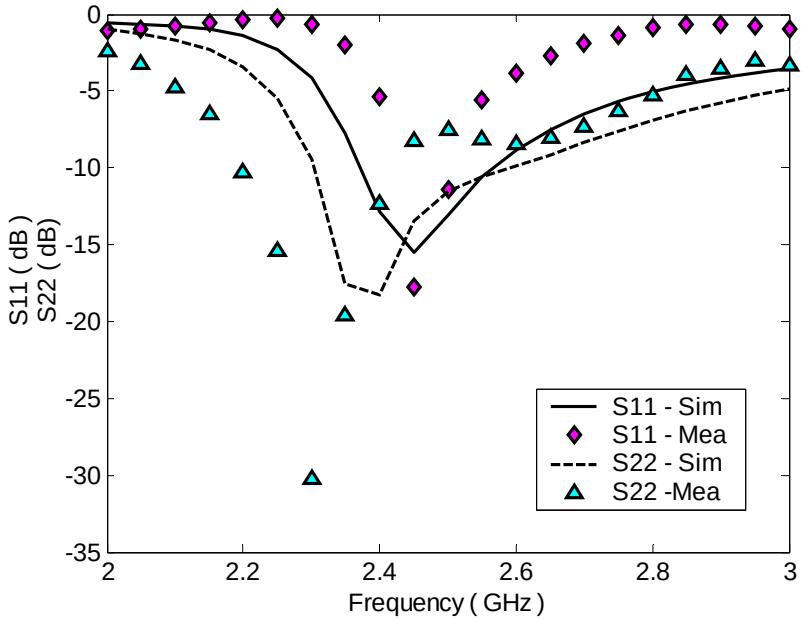


Figure 4.26: Measured and simulated return losses of multi-service LNA configured at 2.4 GHz

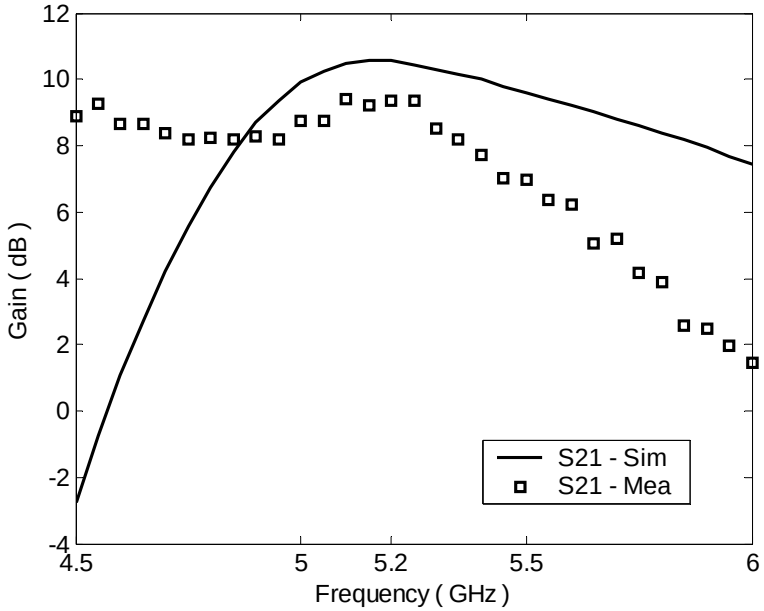


Figure 4.27: Measured and simulated gains of multi-service LNA configured at 5.2 GHz

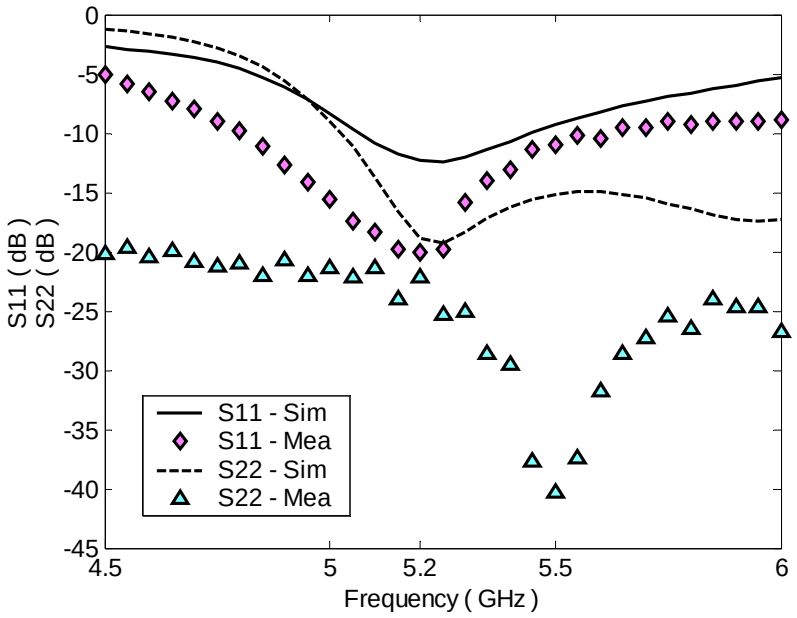


Figure 4.28: Measured and simulated return losses of multi-service LNA configured at 5.2 GHz

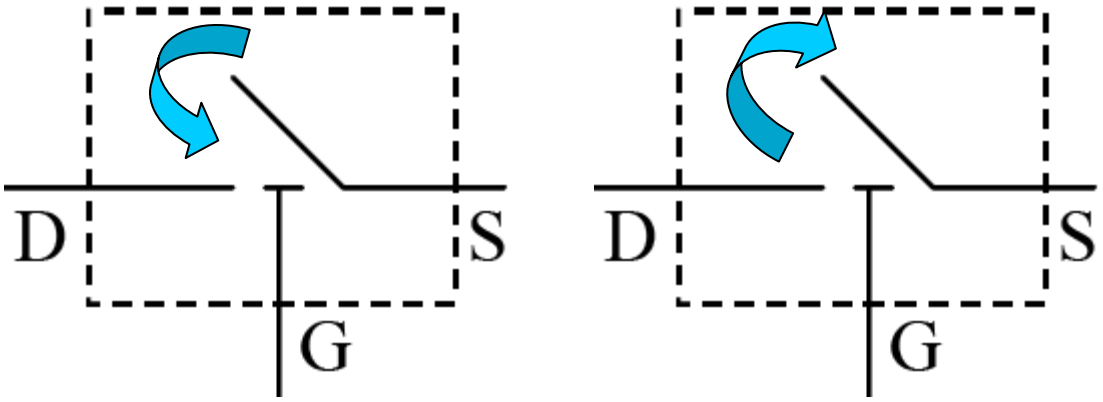
Table 4.2 : Simulated and measured performance summary for single-service and multi-service LNA designs

1.9G	Sim	Mea Single Band	Mea Multi-Band	2.4G	Sim	Mea Single Band	Mea Multi-Band	5.2G	Sim	Mea Single Band	Mea Multi-Band
S21 (dB)	17.6	14.8	14.5		16.4	14.1	14.4		10.5	9.4	9.3
S11 (dB)	-9.9	-11.5	-7.4		-12.8	-5.9	-6.6		-12	-10	-20
S22 (dB)	-14	-14	-15.9		-18.2	-13.8	-12.3		-18	-13	-22
NF (dB)	1.4	--	--		1.5	--	--		1.4	--	--

4.4.3 LNA design using MEMS

For mobile wireless services such as cell phones, low power consumption is a must. Less power usage means longer battery standby time and more talking minutes after one charge. As mentioned in Chapter 3, MEMS switches have the unique advantage of almost zero power consumption over active devices such as PIN diodes and GaAs switches. Besides MEMS switches can be made smaller than active switches to save more die area. Therefore, for future wireless services, MEMS can help mobile wireless devices to meet even stringent power and size requirements. Applying enough dc supply voltage (positive or negative) between G and S as shown in Fig. 4.29, MEMS is turned on as shown in Fig. 4.29 (a). By removing the dc power supply from G and S, MEMS switch is turned off as shown in Fig. 4.29 (b).

In the following design, a MEMS switch is employed to replace a hard-wire connection in the previous LNA design at 5.2 GHz. Since a MEMS switch needs a dc



(a) (b)

Figure 4.29: (a) Equivalent circuit when MEMS is on

(b) Equivalent circuit when MEMS is off

voltage between gate and source to turn it on, an individual dc biasing network is required. Fig. 4.30 illustrates the schematic diagram of LNA served at 5.2 GHz using one MEMS switch at the input stage. Simulation results regarding gain, noise figure and return loss when MEMS is on are demonstrated in Figs. 4.31. The PCB of the design is shown in Fig. 4.32.

Based on the simulated results shown in Fig. 4.31, a simulated gain of 13.9 dB can be expected. Compared to the simulated gain of the previous LNA designed at 5.2 GHz (only 10.5 dB), higher gain at this design is due to the perfect grounding of the source of the transistor. The simulated noise figure here is 1.1 dB. The output return loss is very good at -19.9 dB, while the input return loss is only -6.2 dB as it is compromised to achieve a good noise figure.

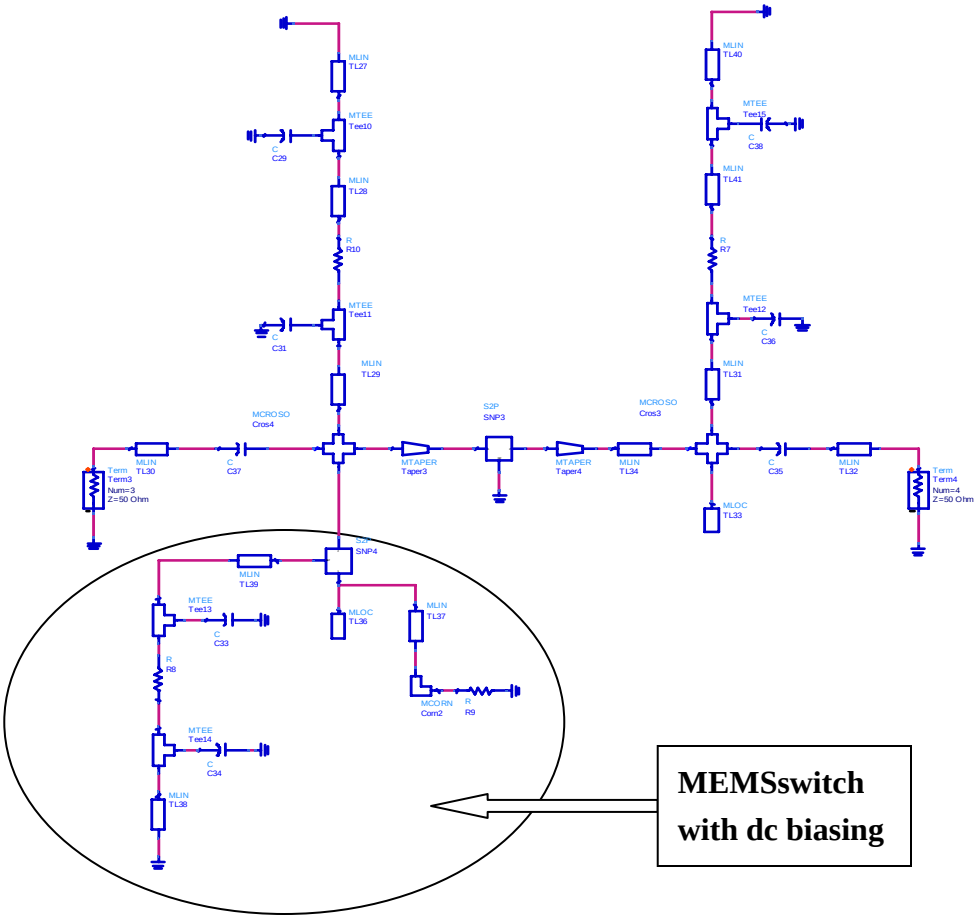


Figure 4.30: Schematic diagram of LNA at 5.2GHz using MEMS switch

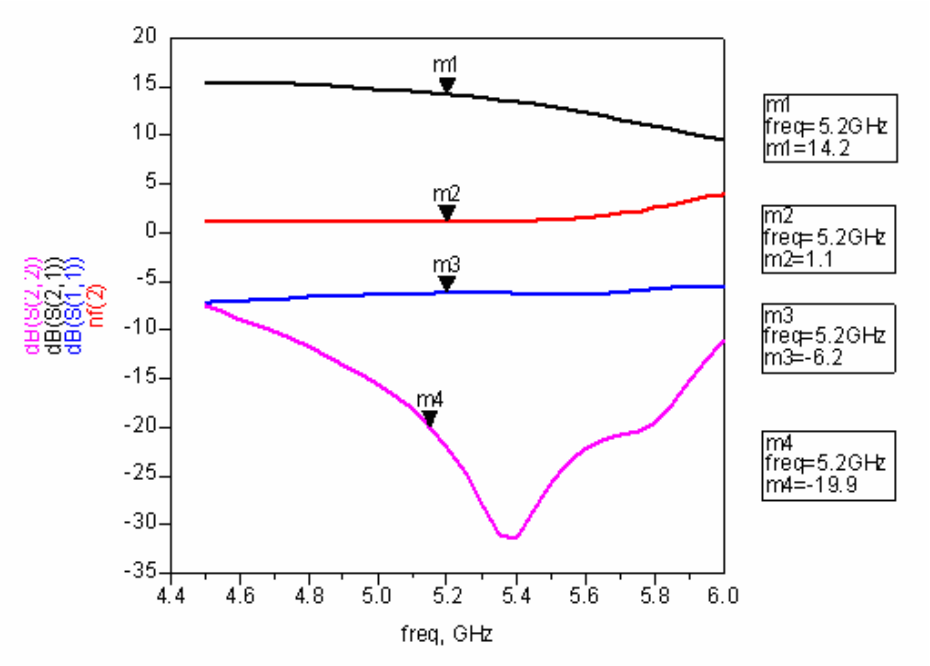


Figure 4.31: Simulated gain, noise figure and return loss of LNA at 5.2 GHz with MEMS switch on

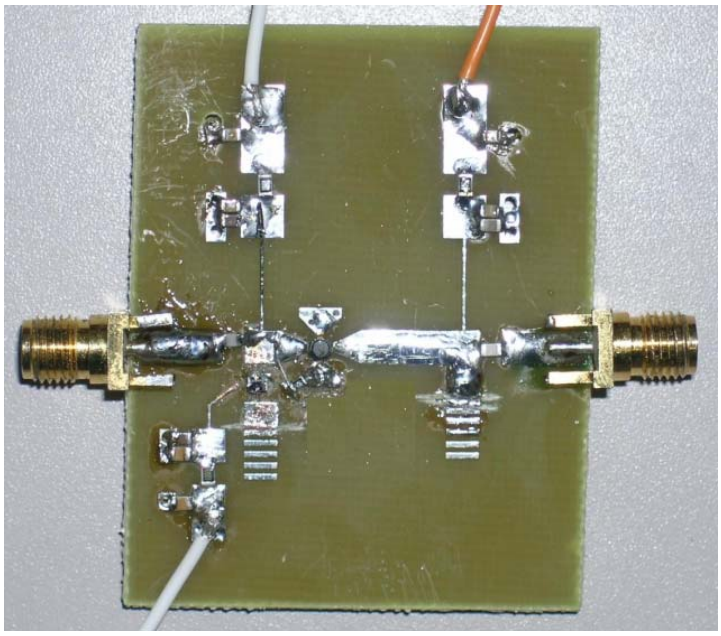


Figure 4.32: PCB of LNA at 5.2GHz using MEMS

According to the datasheet of the MEMS switch used this time, the gate, drain and source pads and ground are not solderable, therefore special procedures should be followed in mounting the MEMS switch to the board. First, attach the bottom of the MEMS to the ground pads of the board via electrically conductive epoxy glue. Then, use a bonding machine to bond the gate and the source pads of the MEMS to the gate and source dc biasing lines (fine line). Finally, bond the drain and source pads of the MEMS to the fat RF microstrip lines. Since the bonding wires have some inductance, their effects should be counted in the design.

Fig. 4.33 shows the measured and simulated gains for LNA at 5.2GHz with MEMS. The measured gain is 10.3 dB, around 4 dB lower than the simulated gain. Lower gain in reality could result from the effects of the bonding wires, the MEMS switch and the accuracy of the small-signal model of MEMS provided by the manufacturer. From the return loss diagram shown in Fig. 4.34, the measured S_{22} at 5.2 GHz is, though not as good as the simulated one, still very good at -20.8 dB, while the measured S_{11} is around -5.4 dB, close to the simulated result.

4.5 Conclusions

According to the various designs in this chapter from single- to multi-service and to the service using a MEMS switch, it is concluded that the multi-service design using hard wires at this stage as switches can provide good performance with little performance degradation. Meanwhile, it consumes the same board area as the single-service designed at the lowest frequency. MEMS as a switch replacing the hard-wire connection for

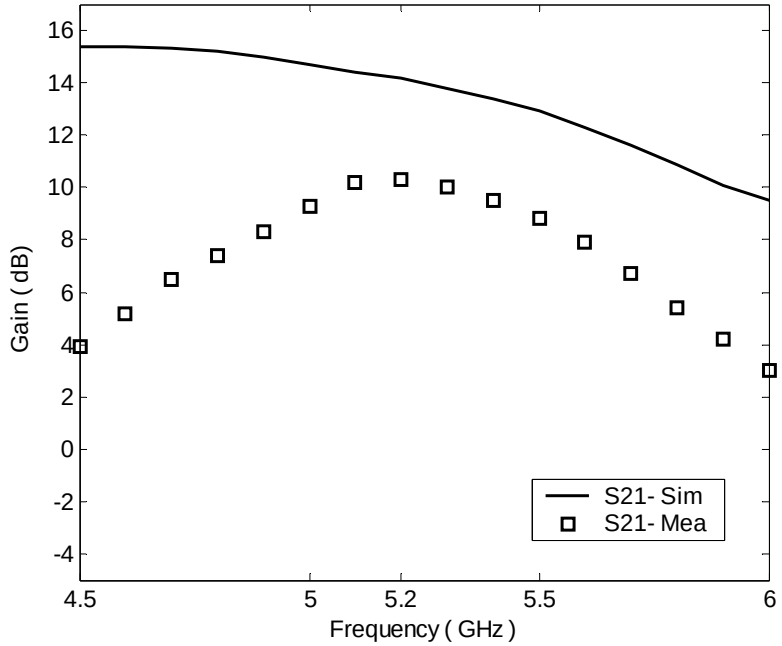


Figure 4.33: Measured and simulated gains for LNA at 5.2GHz using MEMS

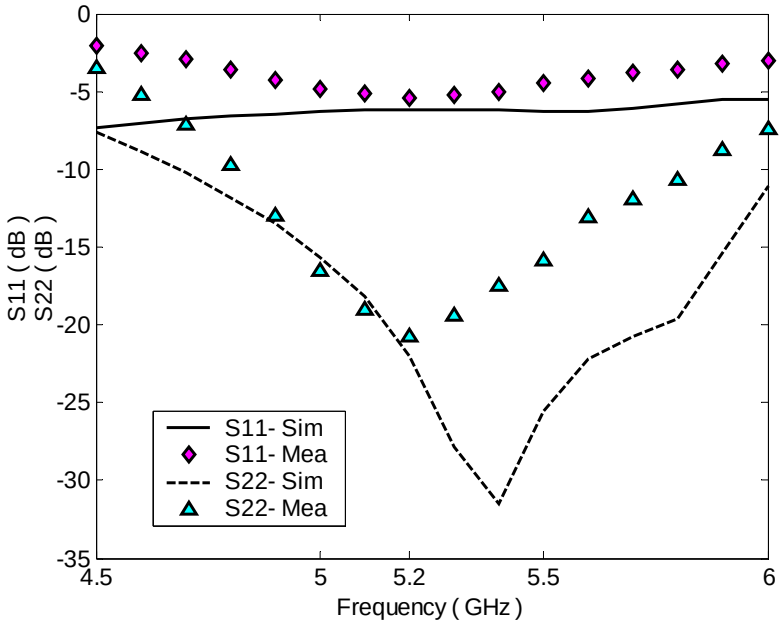


Figure 4.34: Measured and simulated return losses for LNA at 5.2GHz using MEMS

multi-service design could result in a little degradation in gain, but can be optimized. Compared to the power hungry active switches, MEMS switches are the best choice to be integrated together with other RF circuits using CMOS technology to provide low-cost switchable circuits with lower power consumption, if MEMS can be made on low resistive silicon substrate.

5

Development of a Reconfigurable Oscillator

A basic building block in the front-end chain is the oscillator. In order to develop a universal RF terminal to receive multi-services, the oscillator needs to be reconfigurable. It would include GSM900, DCS1800, PCS1900, DECT, UMTS, GPS, WLAN and Zigbee, where both oscillator frequencies and power levels should be tuned to provide variable IF signals whose frequencies are very close to their base band signals or zero IF signals which frequencies are located at their base bands. It is common in most of these wireless receivers to have the IF close to or at base band frequencies, where many commercial low-IF and zero-IF IC products utilize reconfigurable base band detectors/receivers.

Table 5.1 summarizes the required oscillator frequency range for each service that is needed to feed the mixer to provide variable IF signals. Such function is demonstrated in the common block diagram shown in Fig. 5.1.

Table 5.2 summarizes the phase noise specification for different services. From this table, the most stringent phase noise requirement is set to the GSM including GSM900, DCS1800 and PCS1900, which is -141 dBc/ Hz at 3MHz offset.

5.1 Oscillator design concept

After studying the various requirements for different services, it is concluded that the required oscillator design is straightforward. The phase noise requirements do not

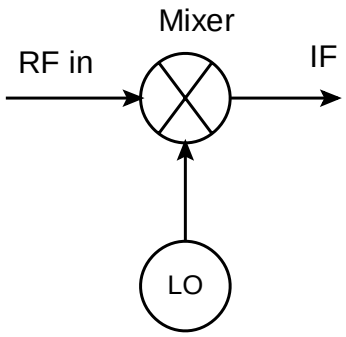


Figure 5.1: Common block diagram of an oscillator feeding a mixer

Table 5.1: Required oscillator frequency for individual service

Service	Oscillator Frequency (MHz)	IF
GSM 900 [1]	915 - 950	100 kHz
DCS 1800 [1]	1795 - 1870	100 kHz
PCS1900 [1]	1920 - 1980	100 kHz
DECT [5]	1880 - 1897	0
UMTS [1]	2100 - 2170	0
WLAN [1]	2400 – 2483.5 (802.11b,g) 5150 – 5350 (802.11a indoor)	0

Table 5.2: Phase noise specification for different services

Service	Phase Noise
GSM900, DCS1800, PCS 1900 [1]	-141 dBc@ 3MHz offset
DECT	-96 dBc@ 2.2 MHz offset
UMTS (WCDMA) [1]	-132 dBc @ 10 MHz offset
WLAN [1]	-103 dBc @ 1MHz offset
Zigbee [6]	-103 dBc @ 4 MHz offset

necessitate the use of dielectric resonators. Using these dielectric resonators though would render higher performance, but would be expensive and difficult to reconfigure. As a matter of fact, most of these requirements are very relaxed and the use of printed circuit resonators would suffice. These open printed circuit resonators would include either an open or short-circuited transmission line termination. However, phased locked loop (PLL) could be utilized to improve the phase noise performance of these free running oscillators.

5.1.1 Principle for basic oscillator design

For any transistor, its two-port S-parameters are given by

$$[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{5.1}$$

and the stability factor K is defined by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|}{2|S_{12}S_{21}|} \tag{5.2}$$

The oscillation conditions for a two-port transistor shown in Fig. 5.2 are provided by

$$K < 1 \tag{5.3}$$

$$\Gamma_{in}\Gamma_T = 1 \tag{5.4}$$

$$\Gamma_{out}\Gamma_L = 1 \tag{5.5}$$

where K is the stability factor, Γ_{in} and Γ_T are the reflection coefficient looking into the transistor input and the termination network respectively, while Γ_{out} and Γ_L are the

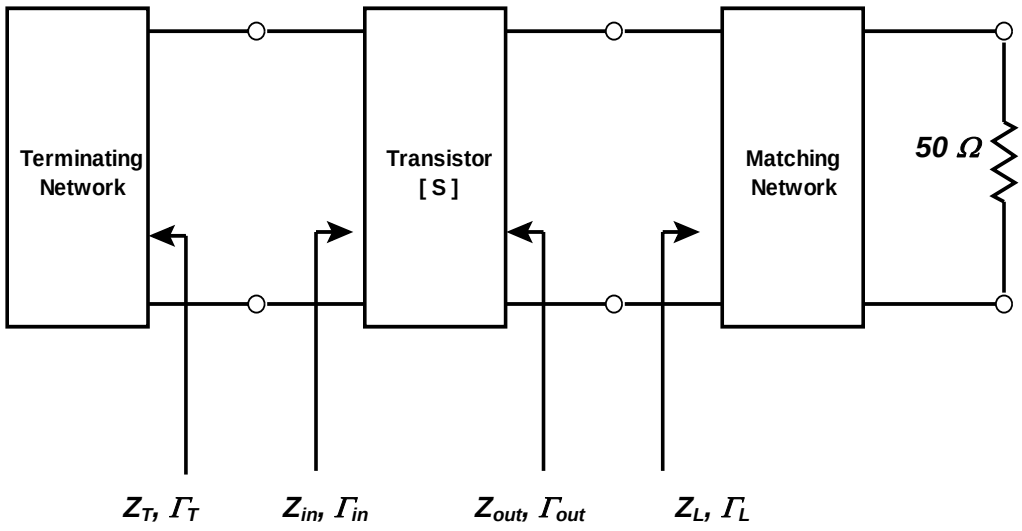


Figure 5.2: Two-port transistor oscillator circuit

reflection coefficients at the output of the transistor and the input of the matching network.

If the device is stable (i.e. $K > 1$), then the leads of common port (the base in our case) of the utilized active device need to be connected to an open or short circuited transmission line, rather than to be connected to the ground right away. In other words, the base would need to be loaded with either an inductive or a capacitive load.

Satisfying the above conditions at the input and output ports will guarantee oscillation. Reactive loading of the base port needs to be optimized for each case to produce the highest negative resistance of the device when looking into the output terminal at the collector side. Meanwhile, the emitter port is connected to a passive resonator such as an open- or short-circuited transmission line to select the operating

resonant frequency. Meanwhile, at the output side (the collector in this case), a simple one-section-matching network may be required to maximize the output power of the oscillator. Practically the load impedance is based on the following rule of thumb approximation

$$Z_{out} = R_{out} + jX_{out} \tag{5.6}$$

$$Z_L = -\frac{R_{out}}{3} - jX_{out} \tag{5.7}$$

where Z_{out} is the transistor output impedance, Z_L is load impedance.

5.1.2 Principle for reconfigurability

Fig. 5.3 shows a proposed configuration schematic addressing different operating wireless frequencies. The frequency agility can be achieved by tuning the capacitor C, the inductor L and $\lambda/4$ dc-feeds. In reality, microstrip lines have been used to realize capacitors and inductors rather than lumped elements, therefore frequency reconfigurability can be easily realized by changing the length of the microstrip lines based on the designed frequencies. In order to successfully switch among different frequency bands, the first step is to find the length of resonant elements and $\lambda/4$ dc-feeds for each service. This can be done by the single-service design. Second, the number of switches and their locations need to be properly determined based on the information in the first step. Finally, the circuit needs to be optimized and to take the effects of the switches and idled microstrip lines into account. This step is very important because without optimization, designed frequencies could be shifted up, down or gone.

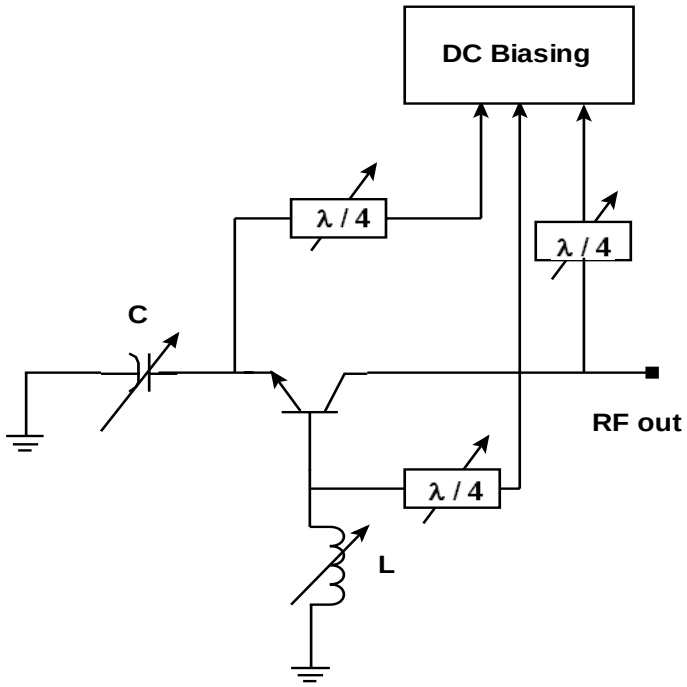


Figure 5.3: A proposed reconfigurable oscillator operating at different frequencies

5.2 Strategy for reconfigurable oscillator design

The single-service design would play an important role for fulfilling a reconfigurable multi-service design. By tracking the topology of matching and dc biasing circuitries of the individual service, the common parts of all designed services will be clearly identified. Therefore, first, design individual oscillators called single-service design. Second, design a reconfigurable oscillator named multi-service design based on the information from the single-service design. Third, modify the design and take MEMS parasitic effects and idled-microstrip-line coupling effects into account. For the

feasibility study of building a reconfigurable oscillator, it is only necessary to validate the operation at the designed frequency at current stage.

5.3 Implementation

Similar to the LNA designs addressed in Chapter 4, for the reconfigurable oscillator, the shared parts should include the transistor, the matching network and dc biasing circuits. Here transistor AT-41411 has been utilized for all the oscillator designs with dc biasing set at V_{ce} = 8V and I_c = 10 mA on the same FR4 substrate with permittivity of 4.4 and thickness of 62 mil for all cases. Same as the previous LNA designs, ADS has been used to finalize the design of these oscillators. Since an oscillator is a nonlinear block, nonlinear S-parameter and Harmonic Balance simulations have been used here, which are different from the small-signal simulation used in LNA designs. The procedures of all the designs in this chapter are summarized as:

1. Bias the transistor at I_{ce} = 10mA with V_{ce} = 8V.
2. Select the transistor configuration so that it can oscillate at all designed frequencies. Here the common-base configuration is chosen to enhance the negative resistance looking into the emitter and collector.
3. Add a small inductor L between the base and the ground to enhance the magnitude of S_{11} and S_{22} so that it can work over a wide temperature range.
4. Introduce a capacitor C on the emitter port as a resonant load and terminate the output using a 50-ohm load.

5. Use the S-parameter simulation with the “osctest’ block (part of ADS Simulation Library) to check the circuit output of the closed loop-magnitude and phase over the frequency range defined by the Oscport block. Then tune the value of the capacitor C and the inductor L to achieve both more-than-1 magnitude and zero phase at the required frequency, i.e. achieve oscillation.
6. Replace S-parameter simulation by Harmonic Balance simulation to predict output power spectrum and phase noise performance. Tweak the circuit again to get high output power and good phase noise at the same time.
7. Replace the tuning capacitor C, shunt inductor L and DC Feeds by micro-strip lines.
8. Re-run Harmonic Balance simulation and re-optimize the circuit.

For all the designs in this chapter, Agilent E4405B spectrum analyzer has been used to measure the output power and phase noise.

5.3.1 Single-service design

In this section, oscillators designed at the discrete frequencies will be presented including 850 MHz, 1850 MHz and 2350 MHz, which are specified for services GSM900, DECT or UMTS, and WLAN 802.11b/g or Zigbee respectively. Even though these three frequencies are not located exactly within the frequency ranges indicated in Table 4.1 except for DECT, they can be shifted back to those ranges in the future design.

Simulated and measured output powers for each service are going to be illustrated and discussed in detail. As an example, a measured phase noise performance will be presented at 850MHz.

5.3.1.1 Oscillator operating at 850MHz

Following the oscillator design steps mentioned above, an oscillator operating at 850MHz has been designed, fabricated, and tested. Fig. 5.4 illustrates the ADS schematic diagram including the biasing circuitry. The board realization has been presented in Fig. 5.5. In the schematic diagram, meander lines have been used here to replace straight lines to save the board real-estate area without performance degradation.

Figs. 5.6 and 5.7 show the simulated performances in terms of output power and phase noise for the single-service design at 850 MHz. Markers m1, m2 and m3 are related to the 1^{st}, 2^{nd} and 3^{rd} harmonic components, and the marker 4 indicates the phase noise at 3 MHz offset. The measured output power and phase noise are illustrated in Figs. 5.8 and 5.9 respectively. The simulated output power of 8.8dBm can be observed at the 1^{st} harmonic component, while the measured output power can reach 13.2dBm at the output of the real board, which is much better than the simulated one. The outcomes differ due to the limited accuracy of the large signal model of the commercial device at this relatively low frequency.

Regarding the phase noise performance at 3MHz offset, the simulated value is -134.2dBc/Hz, while the measured one is -123dBc/Hz, which is 11 dB higher than the simulated result. Here the simulated phase noise could not be believed due to the same

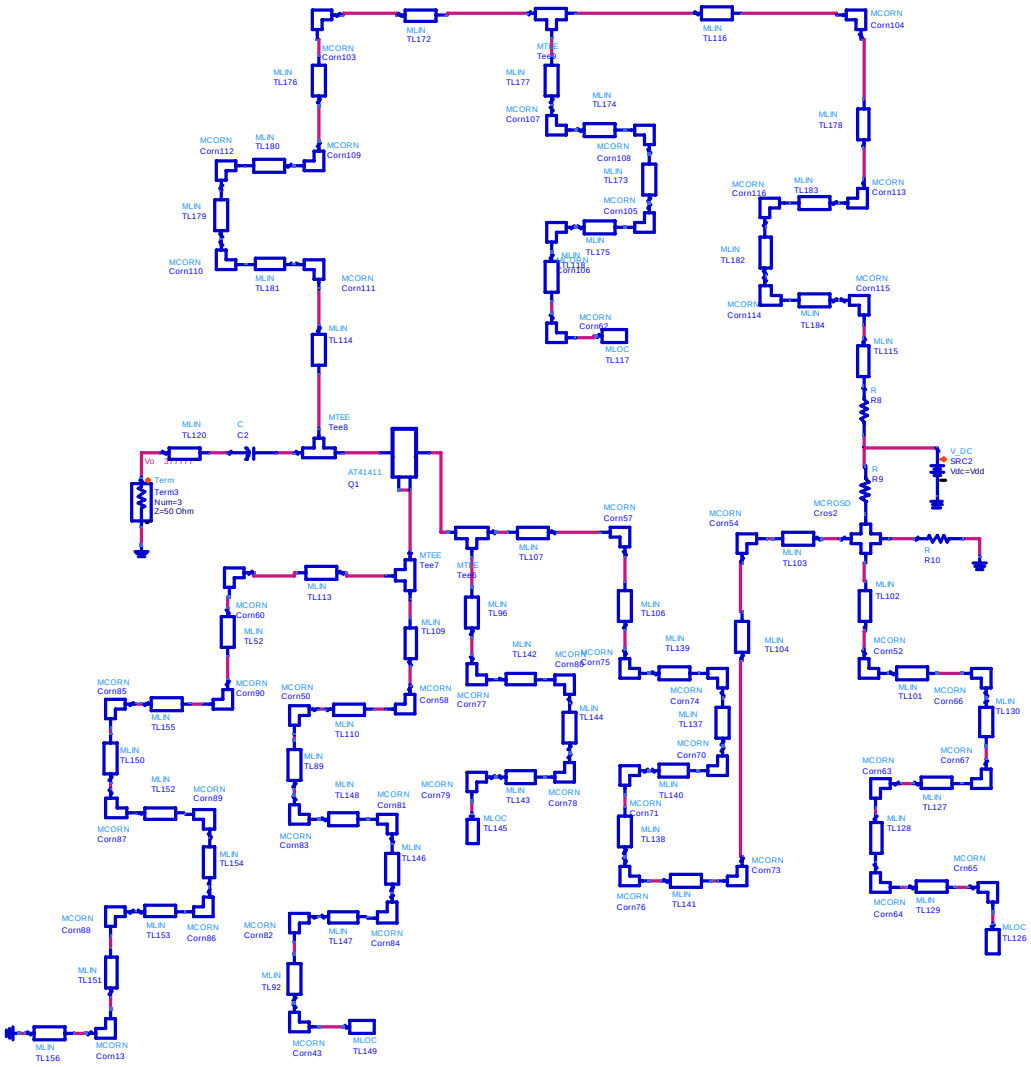


Figure 5.4: Schematic diagram of single-service oscillator at 850MHz

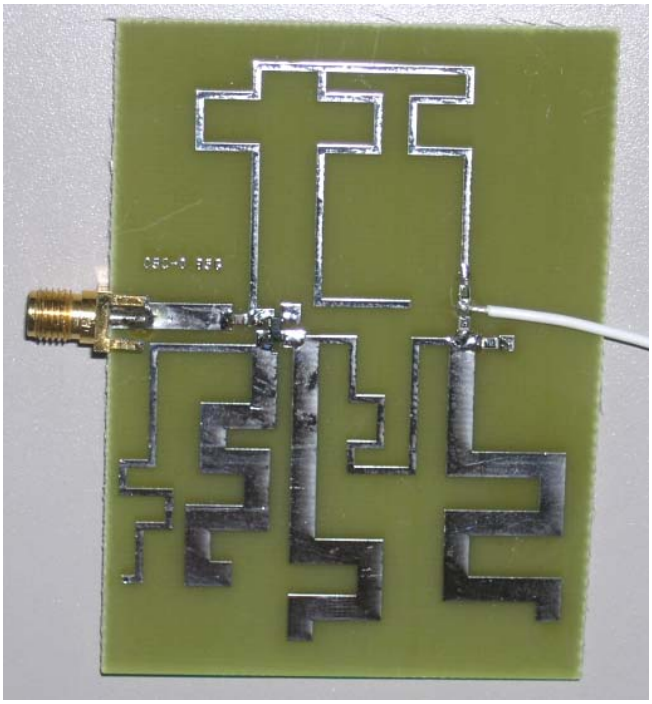


Figure 5.5: PCB of single-service oscillator at 850MHz

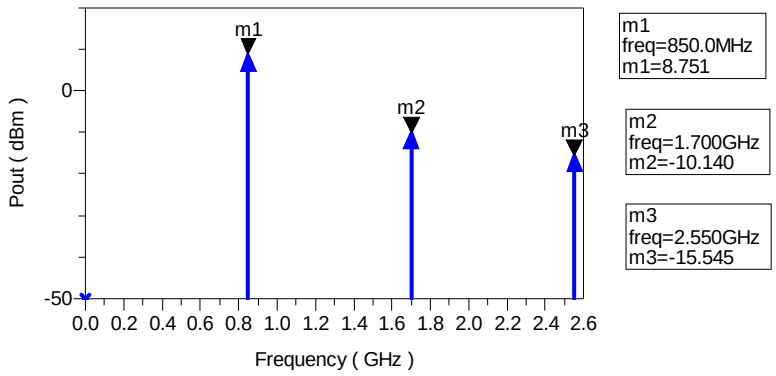


Figure 5.6: Simulated output power of single-service oscillator at 850MHz

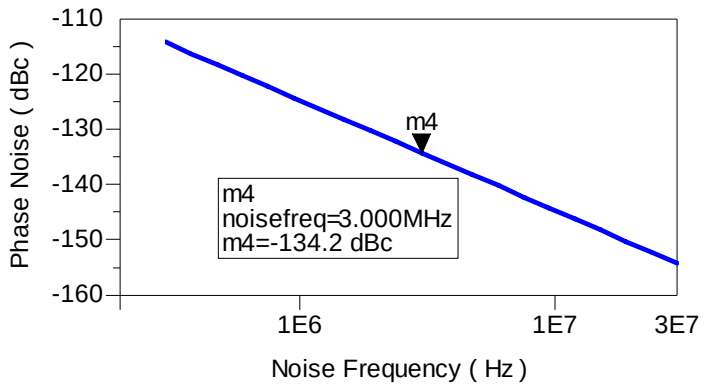


Figure 5.7: Simulated phase noise of single-service oscillator at 850MHz

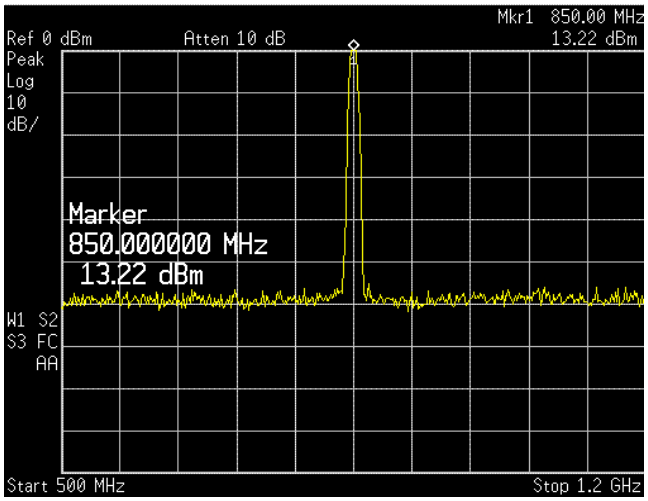


Figure 5.8: Measured output power of single-service oscillator at 850MHz

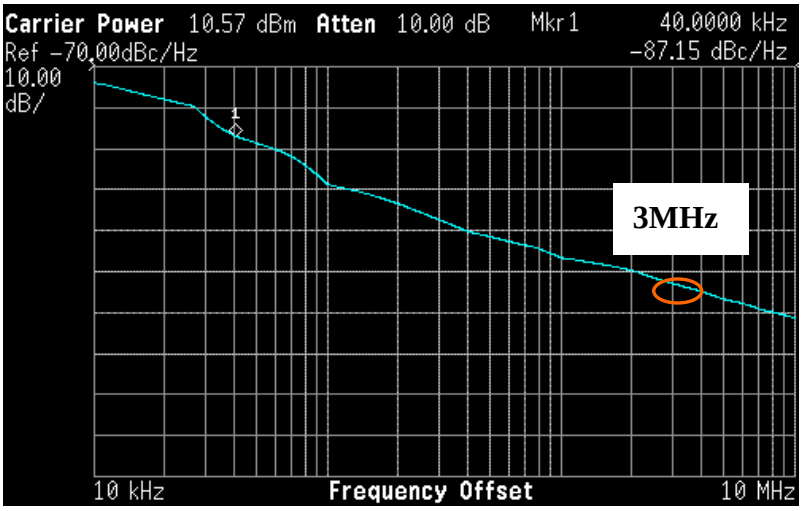


Figure 5.9: Measured phase noise of single-service oscillator at 850MHz

reason for the inaccurate simulated output power. Compared to the phase noise performance required by GSM900, that is -141dBc/Hz at 3MHz offset, the measured result is 18 dB higher, but can be improved and met by using PLL.

5.3.1.2 Oscillator operating at 1.85GHz

Repeating the same design steps, as previously mentioned, an oscillator operating at 1.85 GHz has been designed for the service of either DECT or UMTS. Figs. 5.10 and 5.11 demonstrate the ADS schematic diagram and the board realization. Same as the oscillator design at 850MHz, meander lines have again been used to replace straight lines to save the board area. No performance degradation has been observed. Compared to the PCB shown in Fig.5.5, the board area for this design has been largely shrunk due to the

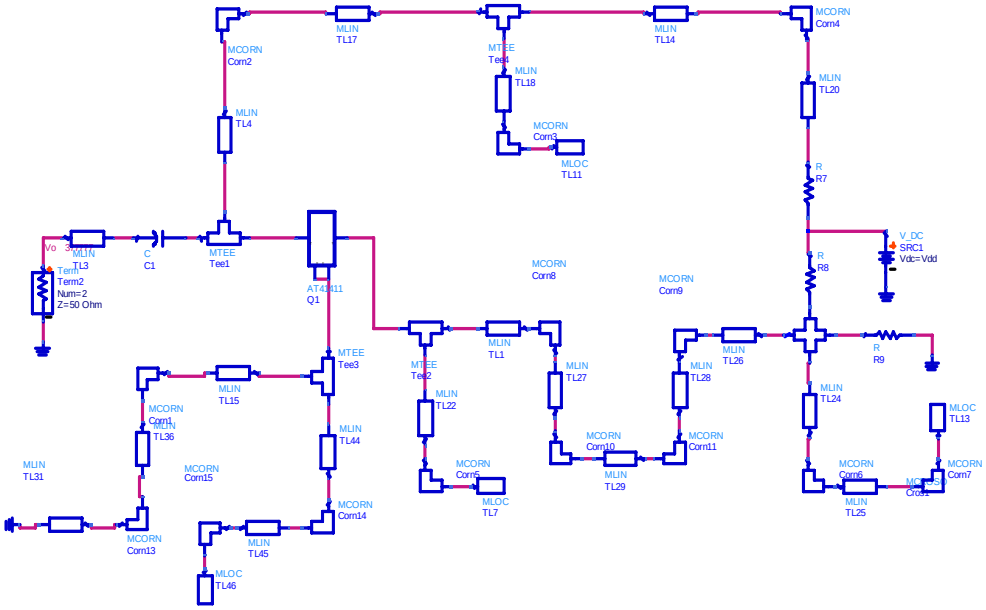


Figure 5.10: Schematic diagram of single-service oscillator at 1.85 GHz.

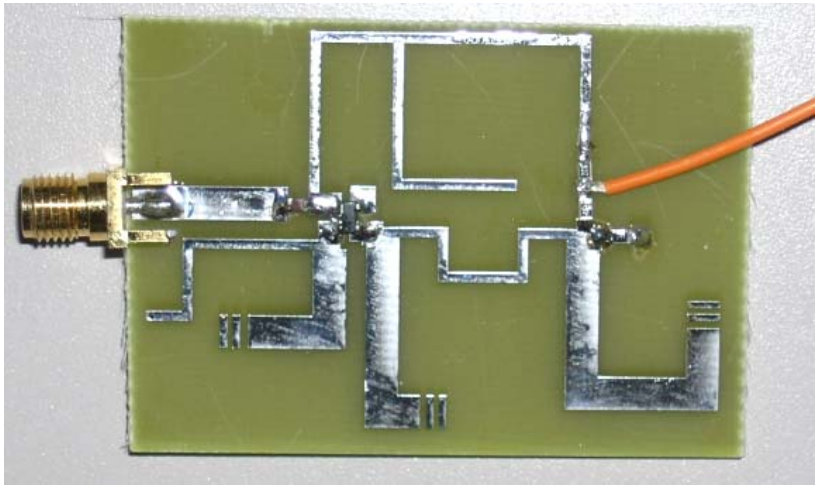


Figure 5.11: PCB of single-service oscillator at 1.85GHz.

higher designed frequency. Normally, the higher the designed frequency, the smaller the board area requires.

The simulated output power and phase noise as well as the measured output power of the single-service oscillator design at 1.85GHz are illustrated in Figs. 5.12 to 5.14. In the simulated output power diagram, markers m1 to m3 indicate the harmonic components from 1st to 3rd respectively. The simulated output power of 16.6dBm can be achieved at the designed frequency, while the measured output power is 12.6dBm, which is around 4 dB lower than the simulated one. The drop in the real output power is related to the loss of the measuring cable used.

For the phase noise performance, the simulated result is -131.7dBc/Hz and -144.9dBc/Hz at 2.19MHz and 10MHz frequency offset respectively which can meet the phase noise requirement of -96dBc/Hz set by DECT and -132dBc/Hz for UMTS.

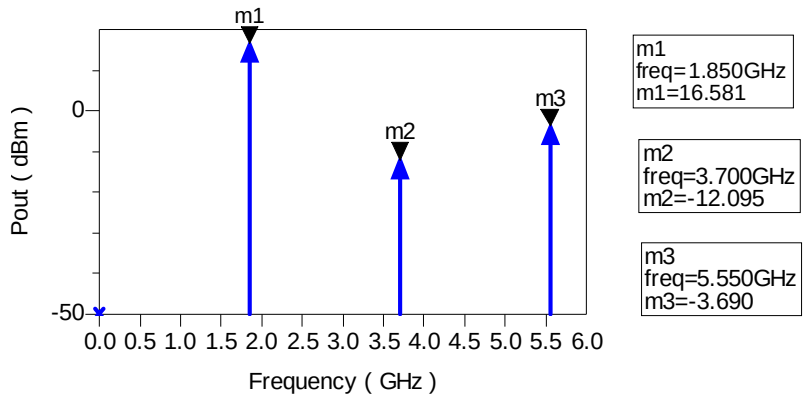


Figure 5.12: Simulated output power of single-service oscillator at 1.85 GHz

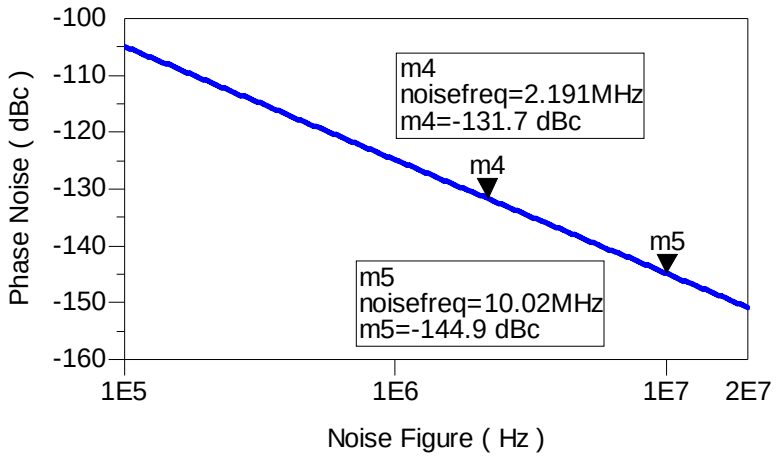


Figure 5.13: Simulated phase noise of single-service oscillator at 1.85 GHz

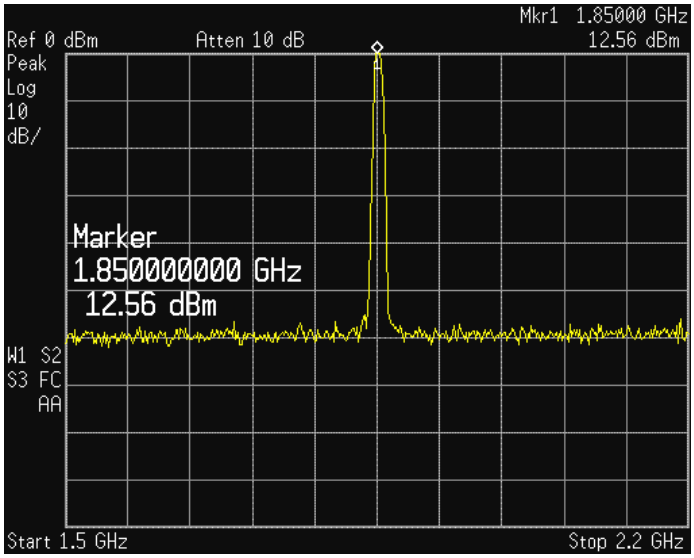


Figure 5.14: Measured output power of single-service oscillator at 1.85GHz

5.3.1.3 Oscillator operating at 2.35GHz

Again, following the same design procedure an oscillator operating at 2.35 GHz has been designed and fabricated. Figs. 5.15 and 5.16 represent the ADS schematic diagram and the board realization. Same as the previous two oscillator designs, meander lines are also introduced here to replace straight lines to minimize the board area. Since the designed frequency here is the highest of the three, only three microstrip lines are meandered in this design.

The simulated results and the measured output power at the required frequency of 2.35 GHz are illustrated in Figs. 5.17 to 5.19. At the designed frequency, the simulated output power as high as 16.2dBm can be obtained, while an output power of 13.7dBm is practically achieved. The slight output power drop is due to the same reason mentioned in the previous sub-section 5.3.1.2. The simulated phase noise here is -114dBc/Hz at 1MHz offset, which can satisfy the phase noise requirements set by the standards WLAN and Zigbee.

5.3.2 Multi-service design

In the previous section, three individual oscillators for three different services have been presented. By observing their schematic diagrams and PCB layouts, the following elements can be shared: the transistor, open stubs as capacitors, open stub as an inductor and $\lambda/4$ dc-feed. Since the previous single-service designs have been already adjusted to ease the multi-service design, no further adjustment in the simulation is

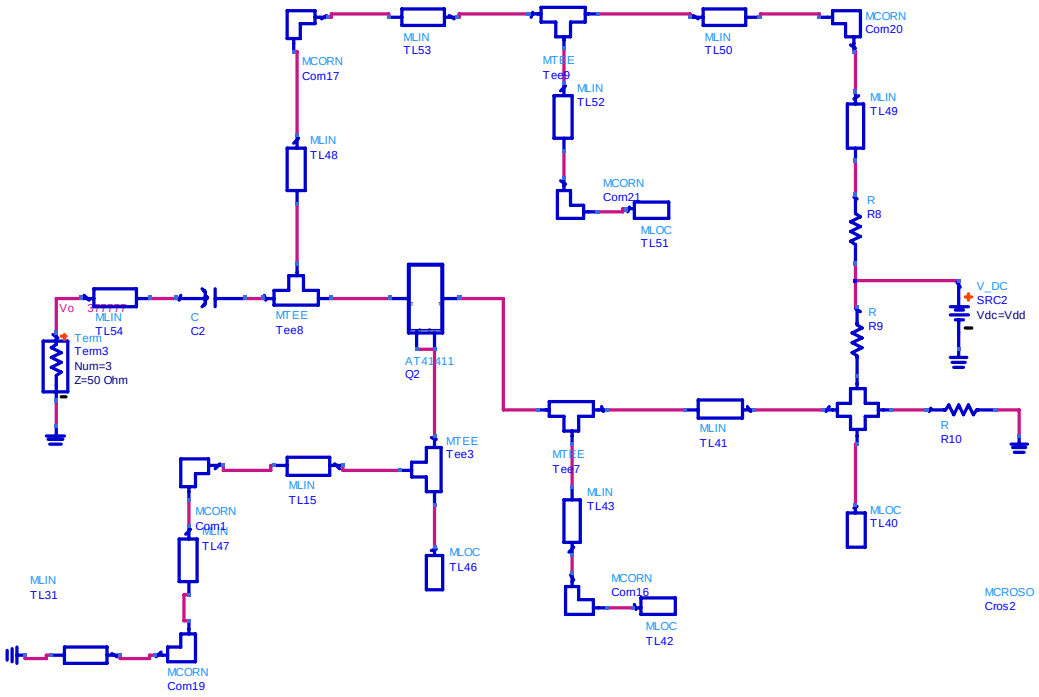


Figure 5.15: Schematic diagram of single-service oscillator at 2.35 GHz

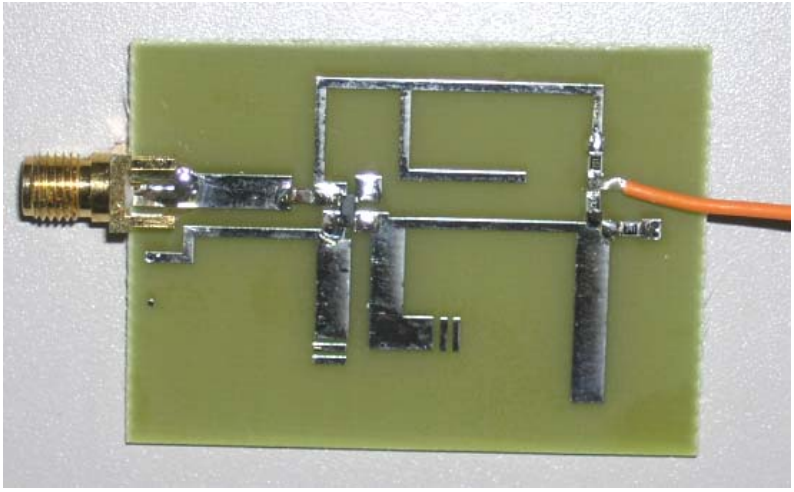


Figure 5.16: PCB of single-service oscillator at 2.35GHz

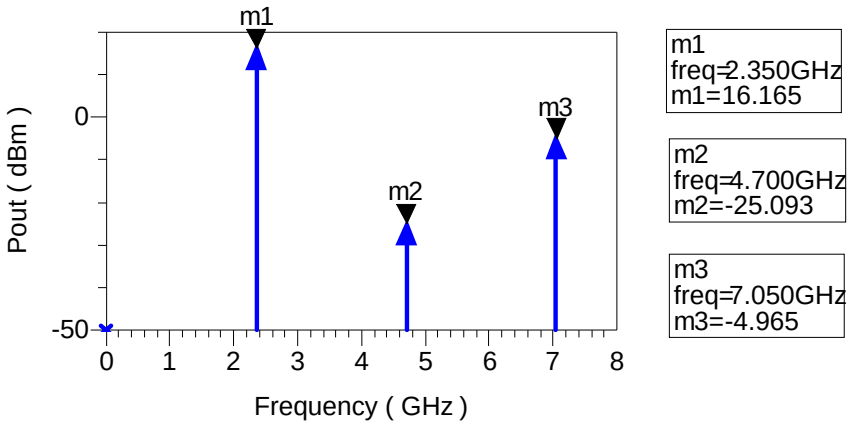


Figure 5.17: Simulated output power of single-service oscillator at 2.35 GHz

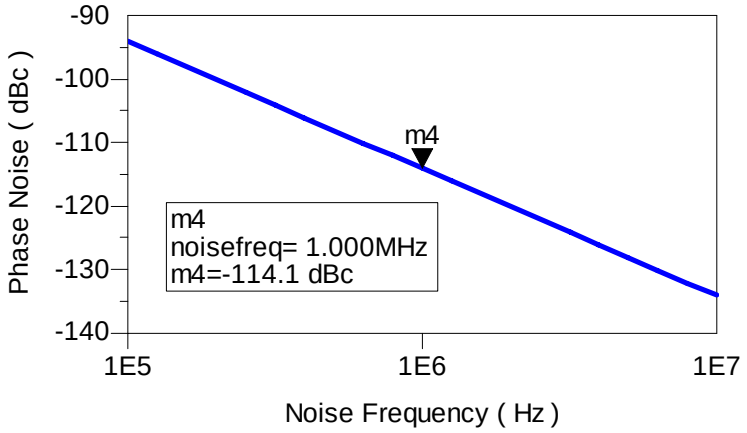


Figure 5.18: Simulated phase noise of single-service oscillator at 2.35 GHz

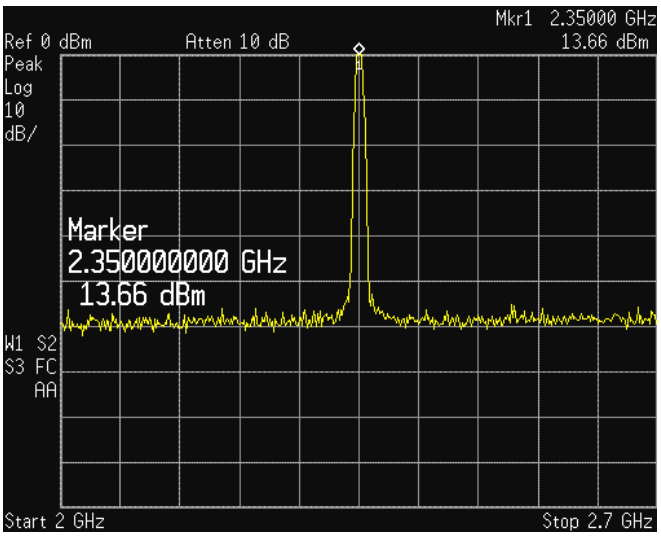


Figure 5.19: Measured output power of single-service oscillator at 2.35GHz

needed here. By using switches the oscillators operating one at a time can be realized while consuming no more board area than the single-service oscillator at 850MHz. As a result, a significant real-estate area has been achieved. In this stage, hard-wire connections rather than switches have been used to make reconfiguration.

Figures 5.20, 5.21 and 5.22 show the board implementations of the multi-service oscillator configured at 850 MHz, 1.85 GHz and 2.35 GHz respectively. From the PCB pictures, more hard wires have been used for the design configured at 850MHz. This means more switches will be used when switching to 850 MHz. The measured output powers for the multi-service design configured at three different frequencies are illustrated in Figures 5.23 to 5.25 respectively. A comparison between simulated and measured output powers both for the single-service and the multi-service designs is summarized in Table 5.3.

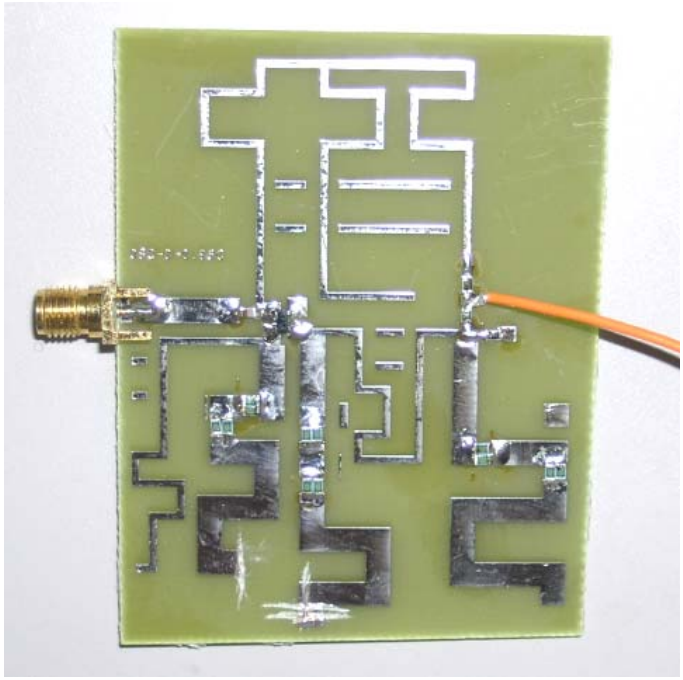


Figure 5.20: PCB of multi-service oscillator configured at 850MHz

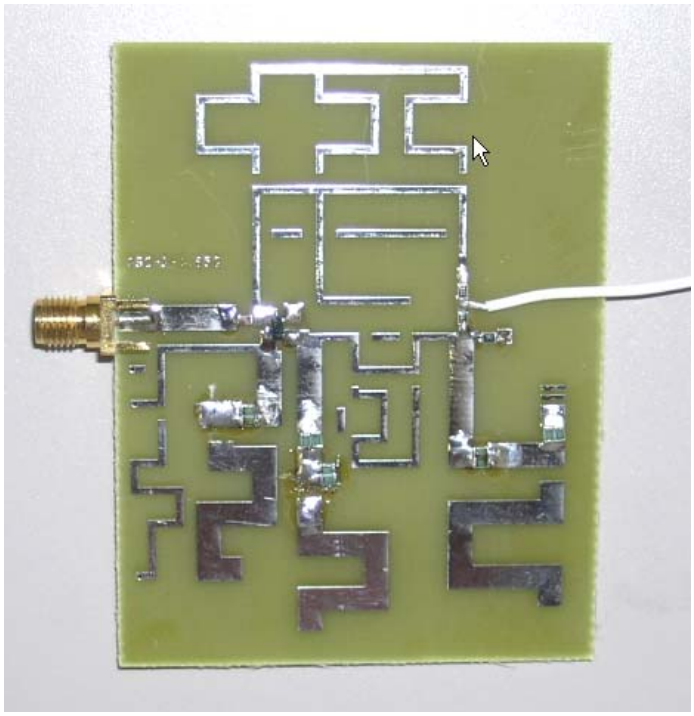


Figure 5.21: PCB of multi-service oscillator configured at 1.85GHz

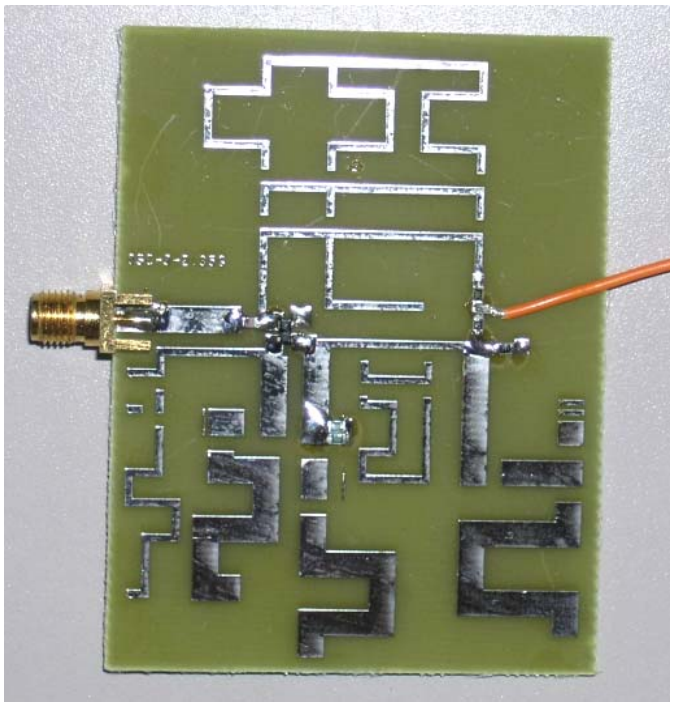


Figure 5.22: PCB of multi-service oscillator configured at 2.35GHz

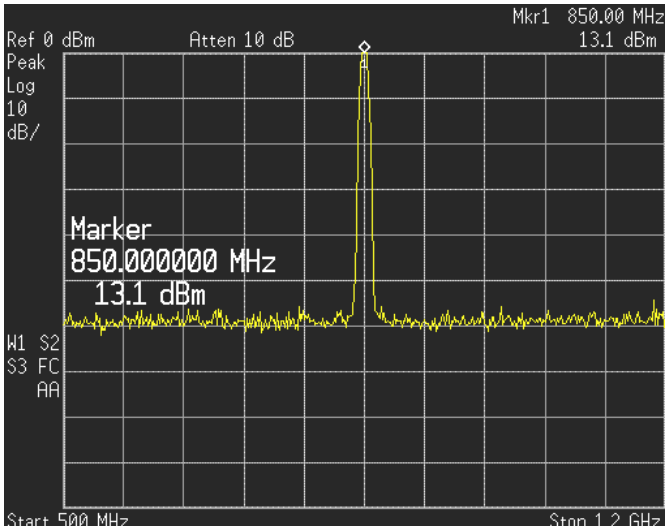


Figure 5.23: Measured output power of multi-service oscillator at 850MHz

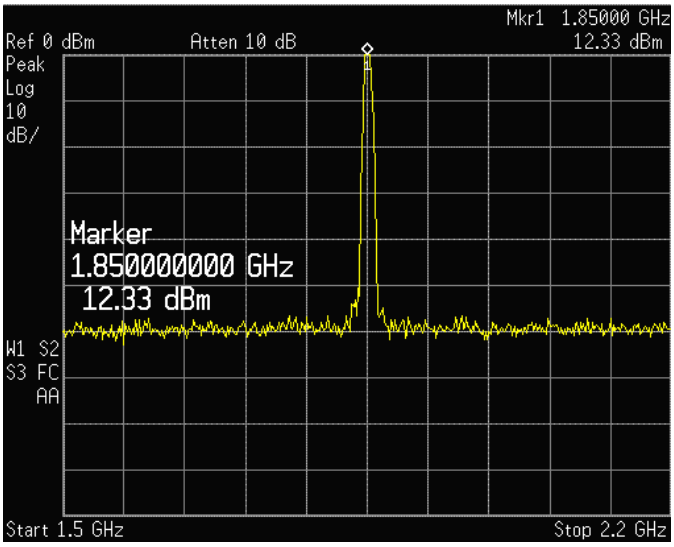


Figure 5.24: Measured output power of multi-service oscillator at 1.85GHz

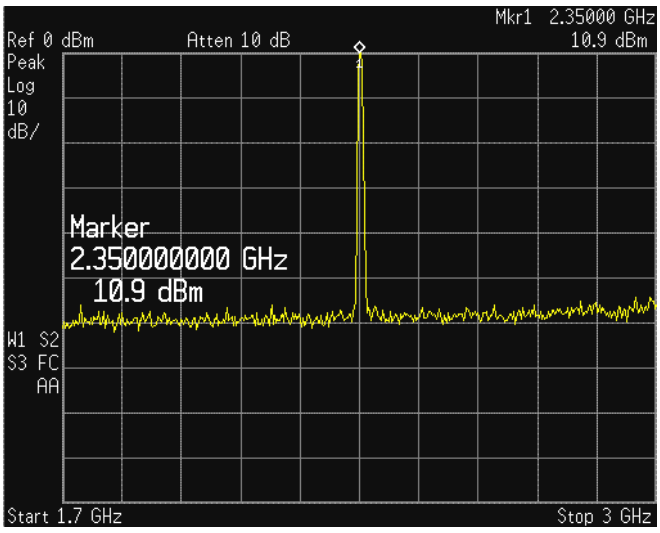


Figure 5.25: Measured output power of multi-service oscillator at 2.35GHz

Table 5.3: Comparison of the simulated and measured output power for single-service and multi-service designs

Designed Frequency	Simulation (dBm)	Single-service (dBm)	Multi-service (dBm)
850 MHz	8.75	13.22	13.1
1.85 GHz	16.6	12.56	12.33
2.35 GHz	16.16	13.66	10.9

From this table, at the designed frequencies of 850 MHz and 1.85 GHz , measured output power performances of the multi-service design are very close to those of the single-service design, which means no output power degradation due to the effect of the hard wires and the standby ‘parasitic’ microstrip lines used for other configurations in the multi-service design. For the designed frequency of 2.35 GHz, the measured output power for multi-service design is 10.9dBm, 2.7 dB lower than that of the single-service design. This means that there is some degradation due to hard wires used and idle microstrip lines. These effects need to be taken into account and the design could be re-optimized.

Based on the comparison of the simulated and measured results for both the single- and multi-service designs, it can be concluded that the three different services can be realized using the reconfigurable multi-service design without significant degradation of output power and phase noise performances. Board area has been greatly reduced due to the switches (hard wires currently) used in the multi-service design.

5.3.3 Oscillator design using MEMS

In the previous section, a multi-service design has been realized using hard-wired connection rather than switches. Switches should eventually replace these hard wires. However, there are many switches that can be used such as PIN diodes, GaAs switches and MEMS. Here MEMS is chosen to be used a switch due to its unique advantage of extra low power consumption. Also the MEMS switches consume less die area than active switches do when they are integrated on the same silicon substrate based on the current silicon technology. Fig. 5.26 illustrates the schematic diagram of an oscillator operating at 1.85 GHz using a MEMS switch and its dc biasing circuitry has been highlighted in the schematic diagram. In this design, the length of microstrip lines used as a shunt inductor, a tuning capacitor as well as $\lambda/4$ dc feed have been adjusted to compensate the effect of the MEMS switch when it is on. When the MEMS switch is off, no oscillation can be observed at the output port.

Figs. 5.27 and 5.28 show the simulated output power and phase noise for the oscillator using a MEMS switch at 1.85 GHz. Table 5.4 lists the simulated results of the oscillators both with and without MEMS switch at 1.85 GHz. From Table 5.4, it can be seen that the output power at the 1^{st} harmonic component with MEMS is 1.6 dB lower than that without MEMS, and the output power at 2^{nd} harmonic component with MEMS is -1.07 dBm, which is worse than that without MEMS. For the phase noise, it is well satisfied.

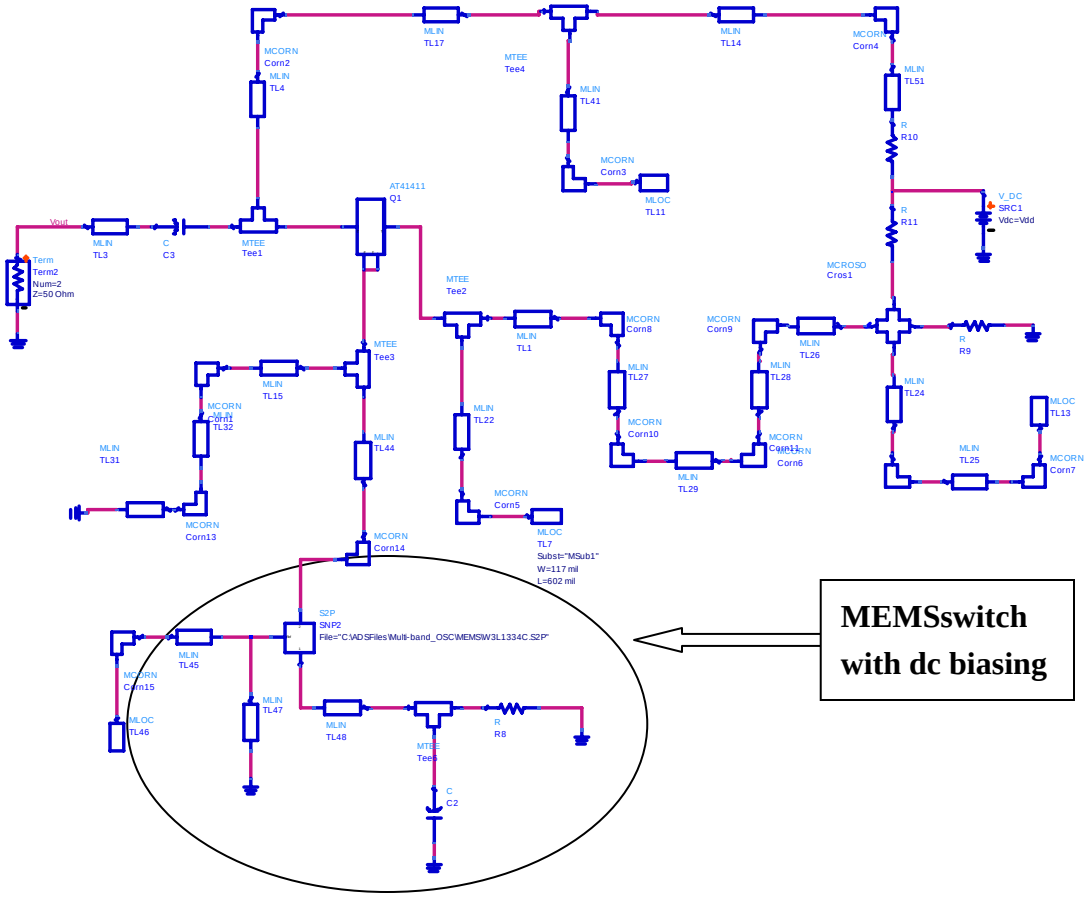


Figure 5.26: Schematic diagram of oscillator at 1.85 GHz using MEMS

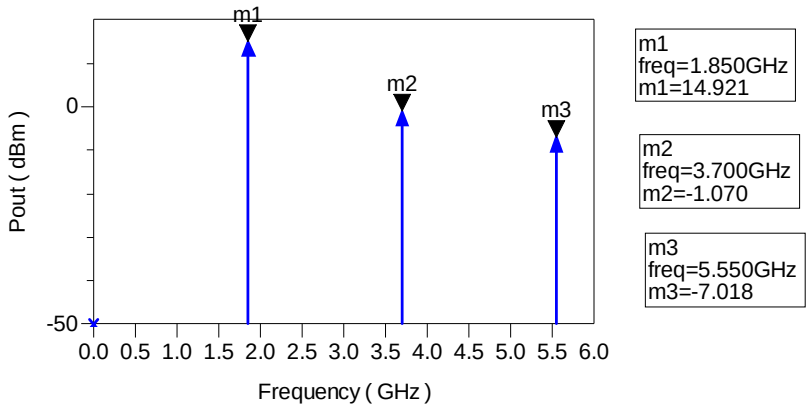


Figure 5.27: Simulated output power of oscillator at 1.85 GHz using MEMS

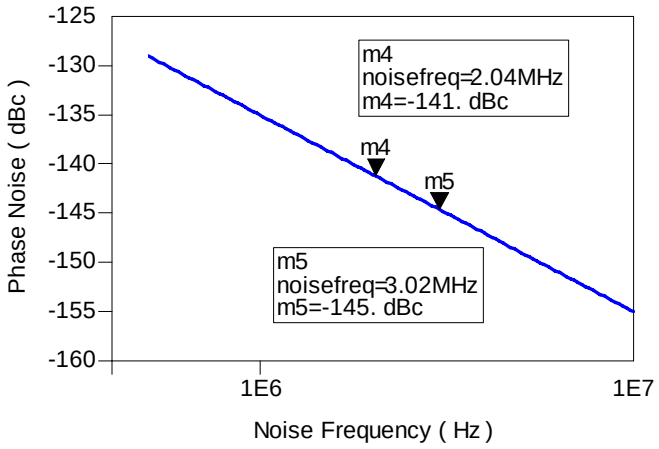


Figure 5.28: Simulated phase noise of oscillator at 1.85 GHz using MEMS

Table 5.4: Comparison of the output power of the 1st and 2nd harmonic components for an oscillator operating at 1.85 GHz with and without MEMS

	Output power 1st harmonic (dBm)	Output power 2nd. harmonic (dBm)
Without MEMS	16.58	- 12.1
With MEMS	14.92	-1.07

5.4 Conclusions

Based on the analysis of the previous designs from single- to multi-service and to the service with a MEMS switch, it can be concluded that the multi-service design using hard wires as switches can achieve very similar output power levels as the single-service design while consumes no larger board area than the single-service designed at the lowest frequency. MEMS can be used as a switch replacing the hard wires for the multi-service structure with a little performance degradation. However, MEMS need to be integrated on the same CMOS silicon substrate with low resistivity.

6
Conclusions and Future Work

Future wireless communication calls for the need of a universal RF terminal which can provide easy access to the available services at any time and at any place. In this thesis, different wireless services have been surveyed with the emphasis on the receiver specifications and optimal receiver architectures including GSM, DECT, UMTS, WLAN and Bluetooth using CMOS technology. Based on the detailed analysis for these services, a fully integrated universal multi-standard receiver has been addressed, as well as its RF front-end specifications. The principle approach to this novel receiver is to minimize the redundant components without performance degradation. This can be realized by using reconfigurable building blocks such as filters, LNAs, mixers, VCOs and gain blocks. An LNA with tunable gain, a mixer with tunable IIP2 and a VCO with continuous tuning range have been introduced. In order to realize frequency reconfigurability as well as longer battery life, a high-quality switch is needed. There are many switches available on the market including active switches and MEMS. Their performances related to the area, power consumption and insertion loss have been compared. At the current study stage, it is focused on the feasibility of reconfigurable multi-standard multi-band RF front ends. As an example, a multi-service LNA and a multi-service oscillator which can be switched among three frequency bands have been designed, fabricated and tested. A MEMS switch has been employed into the LNA design and its effect has been addressed based on the real measurement results. The

effect of MEMS on oscillator has also been discussed here based on the simulation results. Upon the current efforts, it is concluded that

1) Some receivers that do not operate at the same time can be combined into one receiver by using reconfigurable structure, such as GSM, DECT, UMTS, and WLAN.
2) Some services that cannot be combined need their own separate receivers, such as Bluetooth.
3) GPS service is different and might require updates from time to time.
4) Lumped element design up to 5 GHz is not an optimum design. All distributed element designs at 5 GHz or up are preferred, lumped element designs are only preferred at low frequency such as 800 MHz, while hybrid circuits are optimum for the frequency range from 1.6GHz to 2.4GHz.
5) Use of the constant-width input and output lines and the switchable stubs is the optimum topology for reconfigurable circuits addressed here.
6) Use of MEMS needs to change the circuit layouts. Moreover, MEMS needs to be packaged. Currently, a commercially packaged MEMS has been used. Upon silicon integration methods of hermetically sealed packages, the whole circuits need to be developed on the same die.
7) Oscillators are currently using PLL to improve their performance. Better performance can be achieved using dielectric resonators, but they are expensive and bulky. In case of developing reconfigurable oscillators, it may be worthy to develop multi-band dielectric resonator (DR) puck for reconfigurable multi-

band operation.

8) Reconfigurable RF front ends with MEMS are definitely of better efficiency. Their response speed is not an issue here. DC consumption, weight, cost, and real estate are the major design concerns.
9) Simple switchable LNAs could have good pass band characteristics but may not be able to control out of band performance. Use of more complex topologies could provide more freedom to control out of band performance including reducing the stringent requirements of tunable filters.
10) Eventually, it needs to integrate reconfigurable antennas, control circuits, RF front end, or base band on the same chip. Tunable filters requirements can be exemplified and much fewer sections would be used.

Based on the research so far, for the future study, it is suggested that efforts need be to put on the development of MEMS on low resistive silicon (10ohm.cm to 20ohm.cm) rather than highly resistive silicon (2000ohm.cm), active filters, light-weight, multi-band dielectric resonators, and integrated receivers including the filters and antennas using MEMS.

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Vita

Yongping Han was born in Shanghai, China on May 14, 1970. She took part in many competitions in Mathematics and Physics during high school. She started her undergraduate study in Tongji University in September 1988, and received her Bachelor Degree in Electrical Engineering in July 1993. One month later, that is August 1993, she entered the SHANGHAI G. YEAN ELECTRONICS CO., LTD. as a hardware design engineer. During that time she successfully improved the hardware and the supporting code for the test instrument for 3.5 inch floppy disk. In June 1995, she joined TÜV Product Service (Shanghai) Ltd. as a test engineer, and received the title of Senior Engineer in year 2000. From March 2002 to July 2003, she was working for TÜV Rheinland (Shanghai) Ltd. as a test engineer and was assigned as a Technical Certifier by TÜV Rheinland Berlin-Brandenburg Group in 2002. She started her graduate study in University of Tennessee, Knoxville in August 2003, and was a research assistant in microwave circuits for wireless communication. She will receive a Master of Science degree in Electrical Engineering in spring 2006. Yongping Han has many hobbies such as singing, jogging, table tennis, badminton and volleyball. In the Spring Festival 2005, she performed a song on the stage, and her performance was reported by the Daily Beacon.