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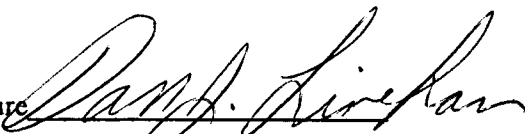
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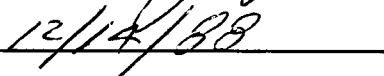
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AN APPLICATION SPECIFIC DESIGN OF A
SELF-DIAGNOSING ENCODER COUNTER

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Daniel John Linehan

May 1989

To Uncle Louie, Aunt Rosemary, my parents, John and Dorothy Linehan, and my wife, Lisa.

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ABSTRACT

Advancements in integrated circuit design and fabrication have provided a means by which more reliable and maintainable electronic equipment can be manufactured with less design effort. An encoder counter (a device often used in machine process control) was designed, fabricated, and tested using these advanced technologies. This Application Specific Integrated Circuit (ASIC) design included a self-diagnosing semicustom controller chip, and two Programmable Logic Devices (PLD's). The semicustom chip was constructed with a schematic capture Computer Aided Design (CAD) program utilizing predefined logic devices (standard cells), and was fabricated through Metal Oxide Semiconductor Implementation Service (MOSIS). A hardware and software interface were also implemented for initial testing purposes. The entire design process was then evaluated with respect to the performance of the CAD tools, and to the reliability and maintainability of the encoder counter.

Reliability was enhanced by at least a factor of two over a more traditional approach using SSI and MSI parts since the increased integration of this ASIC design reduced both the total chip count and the complexity of the printed circuit board layout. The self-diagnosing circuitry improved maintainability by at least a factor of three over a design without such capability since, after a failure has occurred, less troubleshooting time will be required. The CAD tools proved to be effective in reducing the design effort since both the semicustom chip and the PLDs were fully simulated before a hardware commitment was made. However, two limitations, which have since been addressed, were imposed on this ASIC design. First, the semicustom chip had to be built exclusively with small scale circuits since more advanced devices were not yet incorporated in the standard cell library. Second, fundamental-mode sequential circuit techniques could not be utilized due to simulation constraints of the CAD software. Methods have recently been devised to accurately simulate circuits designed with such techniques.

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CHAPTER I

INTRODUCTION

Presently, conventional position processors are designed with small and medium scale integrated circuits and include little self-diagnosing capability. Advancements in the design and fabrication of integrated circuits can improve upon current position processor designs in several ways. Reliability can be enhanced since increased integration can reduce both the chip count and the printed circuit board complexity of the position processor. In addition, ASICs can be designed to incorporate self-testing functions so that an improvement in maintainability can be achieved. The self-diagnosing position processor design presented in this paper utilizes these advanced technologies in an effort to improve both maintainability and reliability. This chapter will describe the specifications of this processor and Chapter II will discuss the hardware design.

The position processor, shown in Figure 1.1, is a very important part of a typical servo motor control system. It performs the function of displaying the actual position in an understandable format and relaying this data to a position compensation network. A position feedback unit (in this case, an optical incremental encoder) is used as the input to the processor. This electromechanical device, which converts motor shaft displacement into electrical signals, consists of a glass wafer with alternating translucent and etched opaque lines. One side of the disk contains a light source and the other a light sensor. The sensor output is electronically conditioned to produce TTL logic levels^[1]. These output signals, shown in Figure 1.2, consist of two square waveforms ninety degrees out of phase with respect to one another. The number of high-to-low (or low-to-high) transitions of each waveform per revolution determines the encoder resolution with the leading waveform governing the direction of travel. The encoder may also produce a "marker" pulse, active only once per revolution, that is used to zero the position processor (commonly called an encoder counter). The zero pulse, as well as the A and B signals, are all utilized by this specific

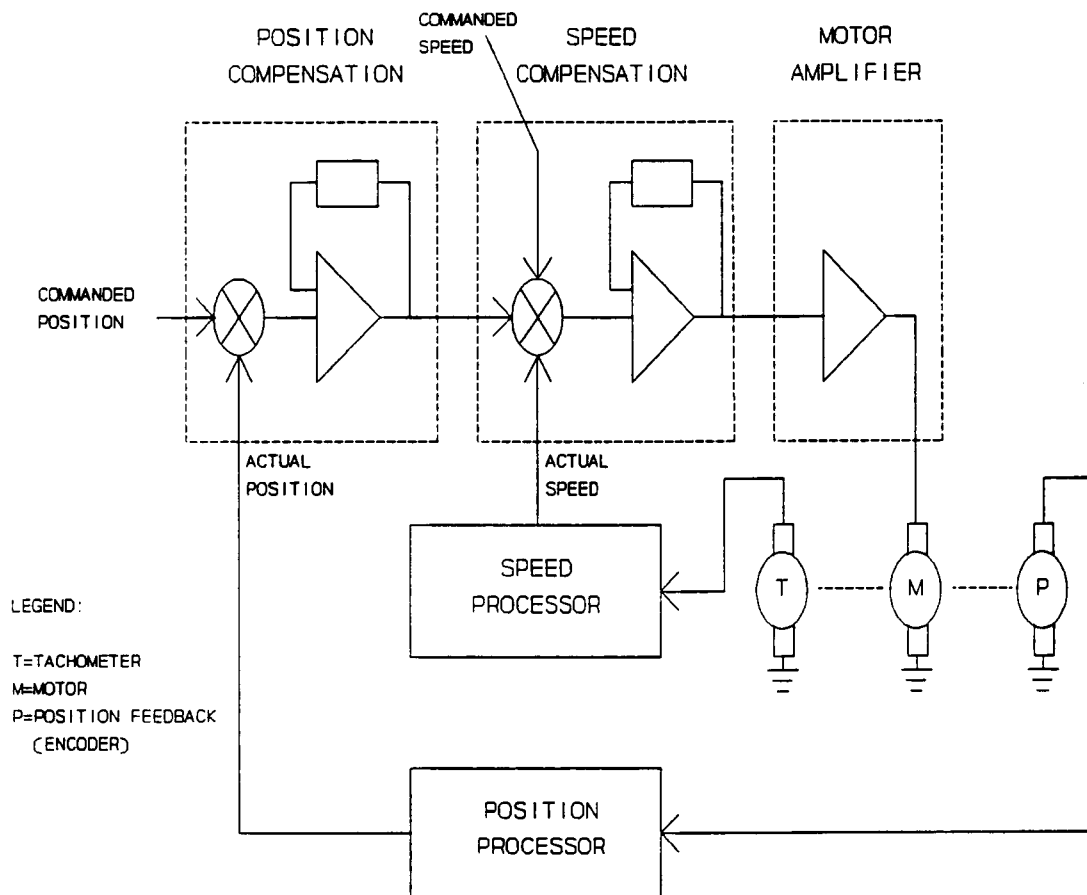


Figure 1.1. Basic servo block diagram.

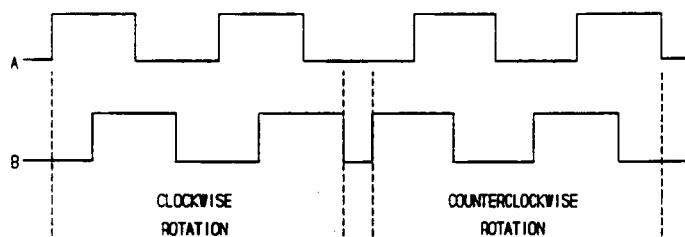


Figure 1.2. Encoder output waveforms.

encoder counter. The output of the counter is then compared to the commanded position creating an error signal. The compensation network produces motor movement until the position error is zero. In this design, the counter data sent to the compensator is in the form of complementary Binary Coded Decimal (BCD).

A basic block diagram of the position processor, shown in Figure 1.3, can now be constructed from the previous specification. This unit consists of an input signal processor, a set of up/down counters, an output data processor, and a display. The input section converts each transition of either the A or B waveforms produced by the encoder into up/down pulses suitable for the counter circuitry. The output section processes the counter data in a format acceptable to both the display and the output data bus. In addition to the basic position processor logic, three types of self-diagnosing circuitry, two static and one dynamic, were added as an aid in troubleshooting the encoder counter during field use. The intent of these circuits was to eliminate possible encoder and position compensator problems and to diagnose counter malfunctions. While present encoder counter designs perform well, they include little or no self-testing circuitry. This capability can reduce the time needed to troubleshoot not only the counter, but also the encoder and compensator. The next chapter will describe in greater detail the encoder counter design implemented in this paper.

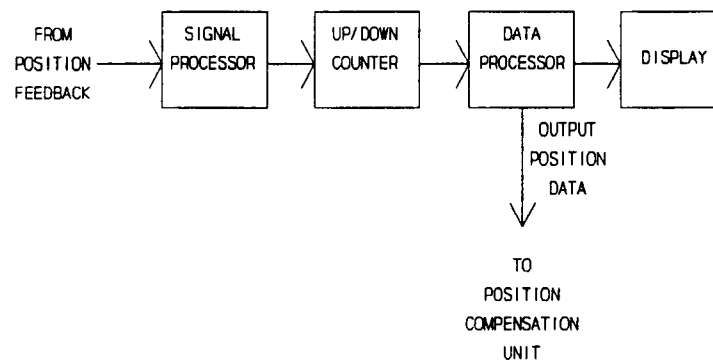


Figure 1.3. Position processor block diagram.

CHAPTER II

DESIGN HIERARCHY

The first decision made in designing the encoder counter concerned system partitioning, influenced by such factors as speed of operation, cost of fabrication, and complexity of the printed circuit board design. By integrating as much of the counter into a single semicustom LSI chip, this partitioning criteria was, in two ways, significantly optimized. First, capacitance and wire length delays associated with off-chip signal routing were reduced since fewer peripheral circuits were required^[2]. The length of lines running between chips on a printed circuit board are much greater than that running between cells inside a chip and, therefore, have a greater effect on system speed. And second, a diminished circuit board design complexity was achieved because increased integration also reduced the number of Integrated Circuits (ICs). Metal Oxide Semiconductor Implementation Service (MOSIS) was used to fabricate the semicustom chip designed for this project. MOSIS, sponsored jointly by the Defense Advanced Research Projects Agency (DARPA) and the National Science Foundation (NSF), provides this low cost prototype service by combining several designs onto one silicon wafer and contracting the actual fabrication to an outside vendor^[3].

The encoder counter block diagram of Figure 2.1 shows the final system partition indicating the three main components. The semicustom LSI controller chip performs the basic encoder counter and the advanced self-diagnosing functions. This chip consists of three finite state machines, several two- and four-bit counters, and the necessary "glue" logic. The output latch, which consists of two PLDs, provides inverted BCD encoder data for the position compensation unit. The display includes both the decimal LED patterns and the BCD-to-seven segment decoding logic. The inverting latch, display, and semicustom controller chip will be discussed in greater detail in the next sections.

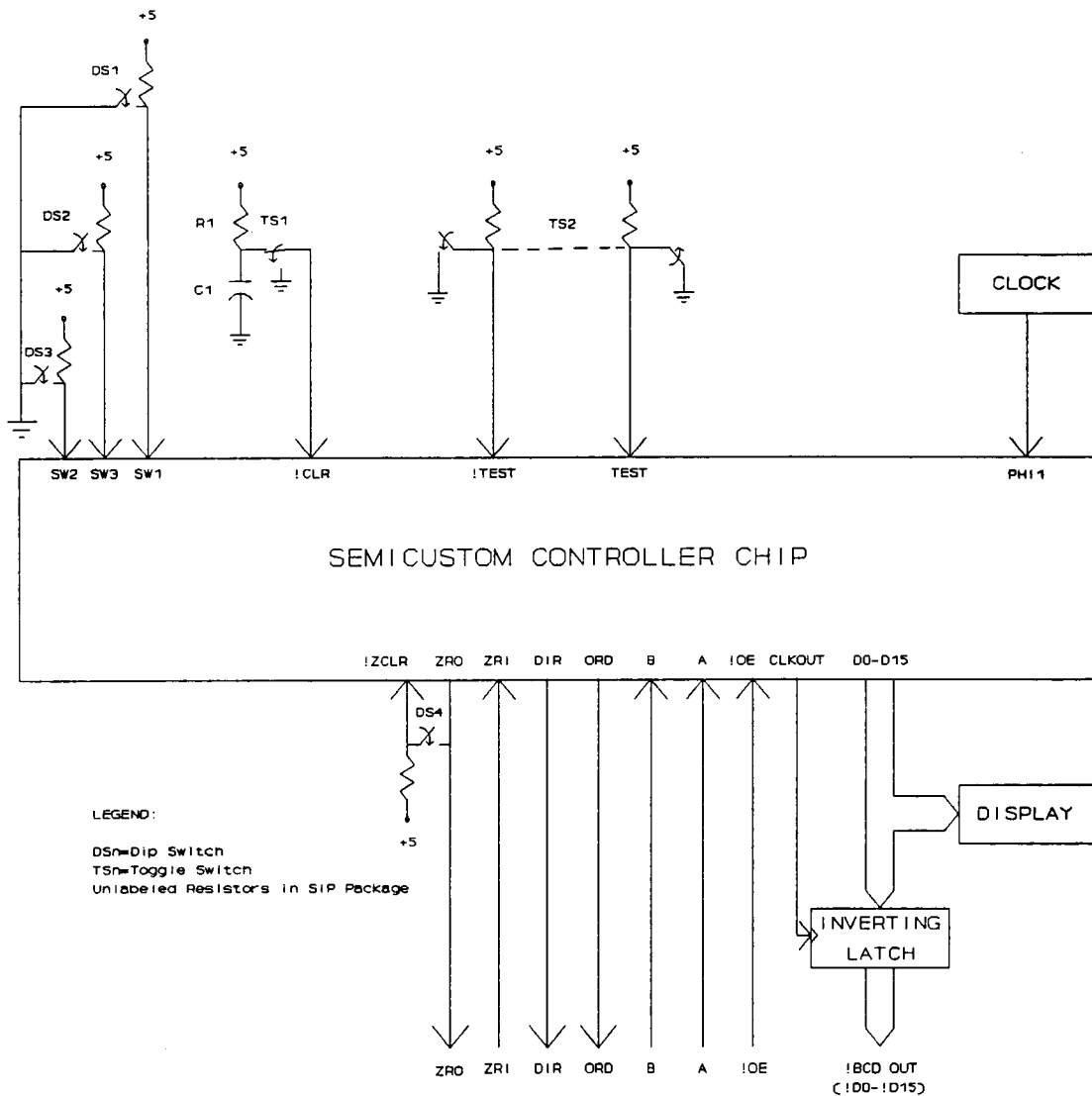


Figure 21. Encoder counter block diagram.

Output Latch and Display

Both the display and the output latch share a single input data bus, reducing the number of Input/Output (I/O) pins needed by the semicustom controller chip and minimizing the printed circuit board design complexity. The following paragraphs discuss the circuitry associated with the latch and display, respectively.

The specific PLDs used to form the output latch were 16R8 Programmable Array Logic (PAL) devices, of which one is shown in Figure 2.2. This PLD was chosen since it contained the necessary output inversion required by the position compensator. In addition, the design effort was simplified since these programmable devices provided internal wire routing capabilities, reducing the complexity of the printed circuit board design. Both PALs were programmed exactly alike simplifying field troubleshooting and repair while only slightly increasing the complexity of the printed circuit board design. The functional diagram of Figure 2.3 shows the configuration of one of the PAL devices.

The display was designed for six-digit accuracy and utilized Hewlett Packard 5800-7300 numeric indicators with on-board BCD-to-seven segment decoding. Since only a 0.025 degree resolution was required by the two least significant display digits, a form of data compression was

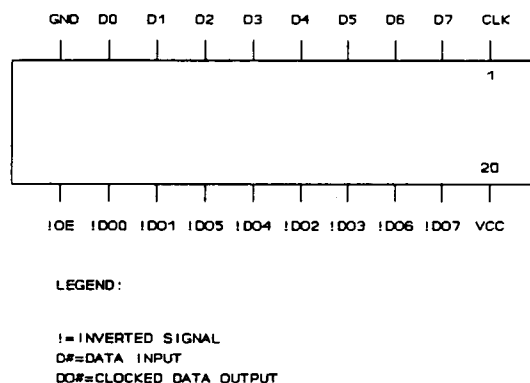


Figure 2.2. PAL pinout.

used so that only two bits of information are needed. For example, with D1,D0 equal to "1,0", the display would read "xxx.x50" degrees. Actual pinouts for both the display and output latch circuitry are shown in Figures A.2 and A.1, respectively. Figures A.4 and A.5 show the main (front and back) circuit board layouts, respectively, while Figure A.6 shows the component locations.

Semicustom Integrated Circuit

As has been previously stated, the semicustom controller chip, shown functionally in Figure 2.4, includes both the basic encoder counter and advanced self-diagnosing circuitry. The entire IC was designed with a personal computer-based schematic capture program utilizing basic predefined logic devices (standard cells). The following paragraphs give a fundamental overview of this chip with the details of the basic counter and self-diagnosing circuitry discussed in respective sections.

In normal operation, the input Finite State Machine (FSM) produces a pulse for each transition of either the A or B input from the encoder via the input selector. The self-clocking counter, initially set to all zeros, simply counts the UP/DOWN pulses from the input FSM (as long as the !ZLCR signal from the encoder is not active) developing a maximum count of "359.975" as seen by the display. The output of this circuit is then sent to the display and latching PALs through the bus selector. To accommodate active low or high A, B, or ZRO signals from the encoder, data selectors, configured by SW2 and SW1, are incorporated in the semicustom controller. In addition, !ZCLR may be inhibited with SW4.

The diagnostic mode of operation is initiated when a transition occurs at the TEST input of the control FSM. Each of three tests are executed sequentially and are active only after the momentary test switch has been depressed and then released. The first two (static) diagnostics are intended to determine if either a portion of the display or the output latch has failed. The control FSM, after sensing the initiation of the first diagnostic, instructs the bus selector to output data from the static test logic. The PAL outputs are valid only after CLKOUT from the semicustom

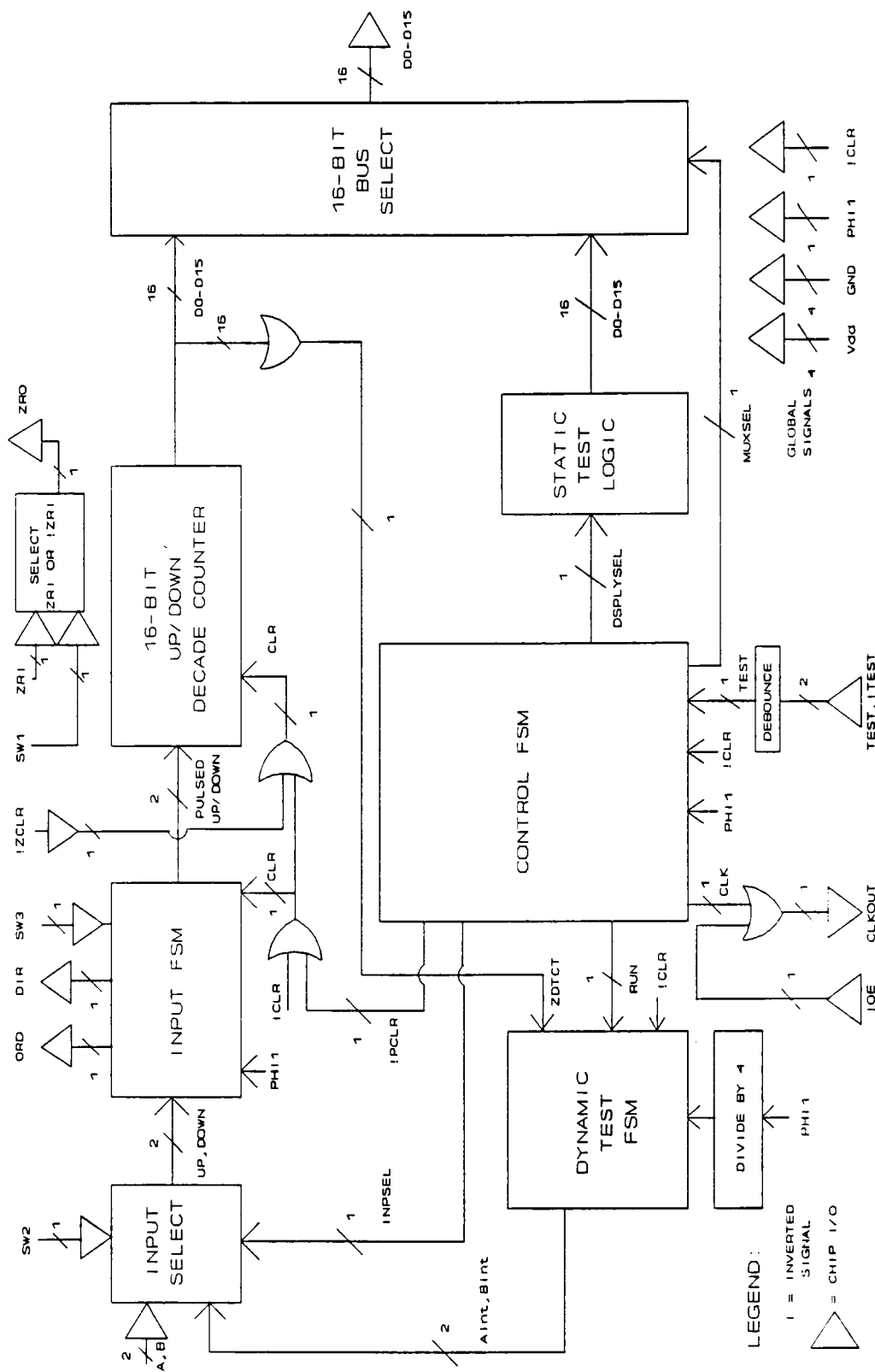


Figure 2.4. Semicustom chip functional block diagram.

chip has been pulsed. Each of the two unique static tests are distinguished by the DSPLYSEL signal from the control FSM. The third and final diagnostic is a dynamic test intended to determine whether a semicustom chip failure has occurred. When this test has been initiated, internal A and B (A_{int} and B_{int}) signals generated by the dynamic test FSM are routed to the input FSM, processed by the up/down counters, and sent to the display and latches via the bus selector. The dynamic test FSM, with its clock slowed to exhaustively test the basic counter circuitry, begins cycling A_{int} and B_{int} to produce a positive count when RUN becomes active. The phasing of these two signals reverses once a zero crossing is detected and ZDTCT becomes active. Once this signal becomes active again, the dynamic test is concluded and the entire semicustom controller is halted until a reset ($!CLR$) occurs.

The semicustom IC, whose pinout is shown in Figure A.3, also develops three other special signals. The ORD signal produces a positive pulse for each up or down pulse developed by the input FSM. Direction is sensed by the DIR line, active low or high via SW3. The output latches are clocked by either an internal signal from the control FSM (CLK) or by an external output enable ($!OE$). For this particular design, each of these are required signals.

Basic Encoder Counter

The input FSM and the set of up/down counters form the basic encoder counter. An FSM flowchart and schematic of the input level-mode sequential circuit are shown in Figures 2.5 and 2.6, respectively. Positive UP pulses are produced during input transitions with A leading B, and positive DOWN pulses are produced during input transitions with A lagging B. Fundamental-mode techniques, which offer faster circuit operation, were first pursued in designing this circuit since simultaneous transitions of A and B were not allowed, but limitations in the simulation software forced a more traditional approach. A method, available after the completion of this project, has recently been devised to accurately simulate fundamental-mode design.

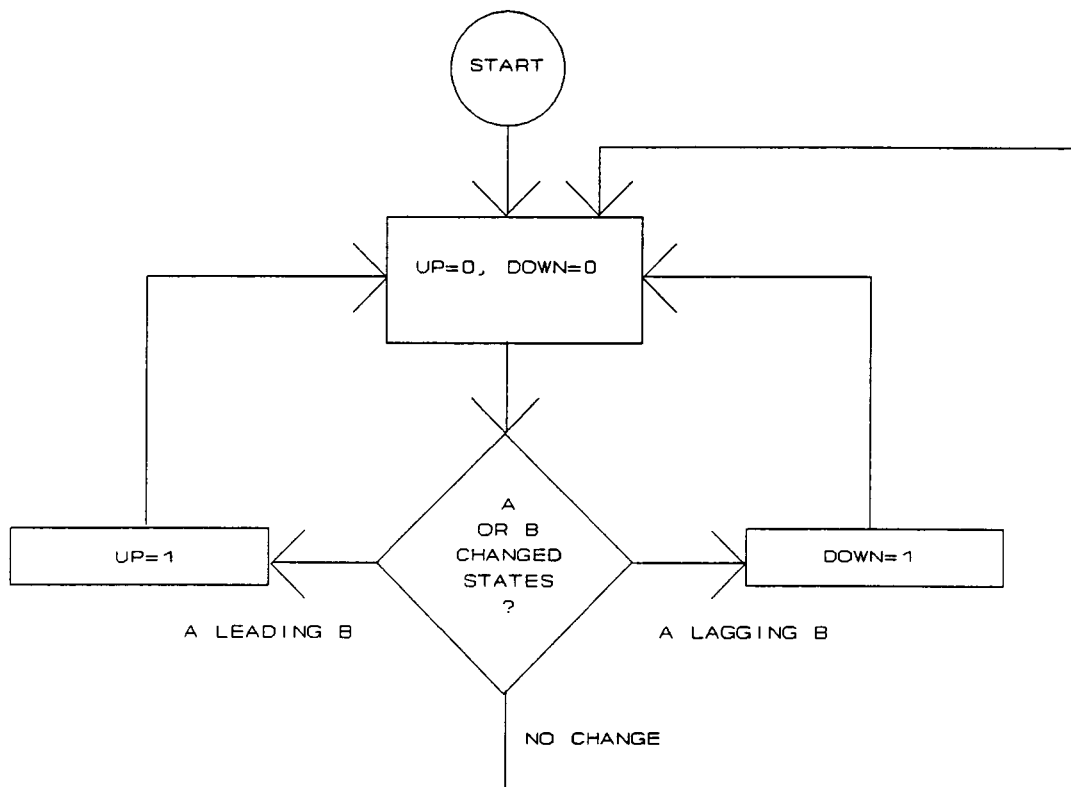


Figure 2.5. Input FSM flowchart.

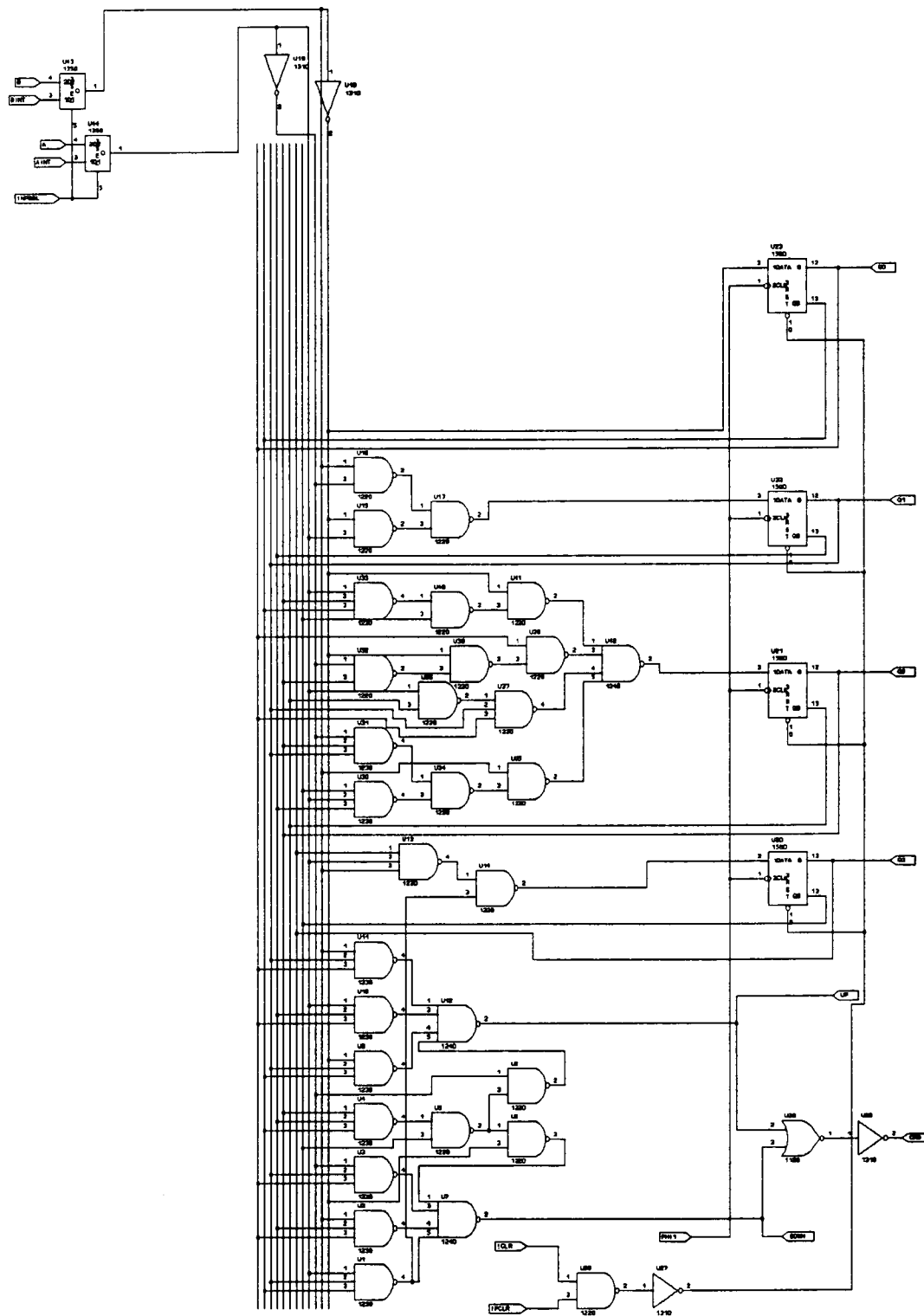


Figure 2.6. Input FSM schematic.

The up/down counter unit, shown functionally in Figure 2.7, consists of a pair of two-bit binary and three four-bit decimal counters. The two least significant display digits require a two-bit counter since a resolution of only "0.025" degrees are needed. Bits D0 and D1 are used to display these two digits. The most significant display digit also only requires a two-bit counter since its maximum value is "3". Data bits D14 and D15 are used to display this digit. The same two-bit binary up/down counter design was utilized for both the two least significant and the most significant display digits. The display digits immediately to the left and right of the decimal point require four-bit decimal up/down counters since any decimal value can occur. Schematics for both the two-bit binary and four-bit decimal up/down counters are shown in Figures 2.8 and 2.9, respectively. The second most significant counter requires special consideration since, under two conditions, it could produce incorrect values. First, with all counter digits equal to "0", a "5" must be displayed in this position after the next DOWN pulse has occurred. Second, with the counter at its maximum value of "359.975", a "0" must be displayed in the second most significant display position after the next occurrence of an UP pulse. The logic to handle these special cases is shown functionally in Figure 2.7 and schematically in Figure 2.10.

Added time was spent on the design of these counters since each was created with small scale standard cells (nand and nor gates). Counters as well as other medium scale devices, not available during the design phase of the semicustom chip, have since been added to the library.

Self-Diagnosing Circuitry

ASIC designs fall into a unique category when testability becomes an issue. The need for self-testing ICs increases as the number of internal circuit nodes available for observation decreases. Traditional fault detection methods based on an ad hoc approach, such as signature analysis, depend on the access of many such nodes^[4]. The added cost of increased pin count and, more importantly, increased circuit area (required for the associated signal routing) to provide nodal accessibility is

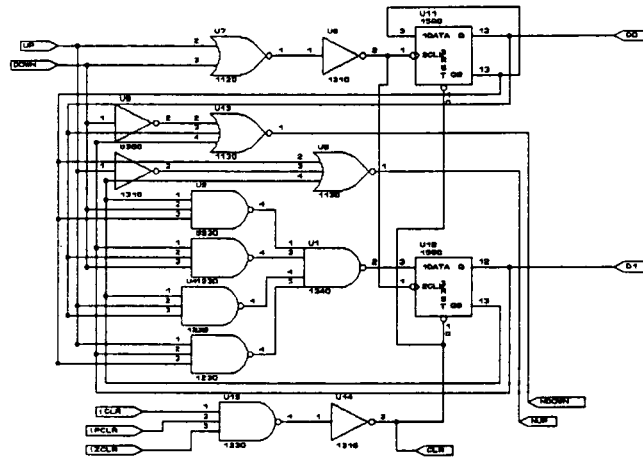


Figure 2.8. Two-bit up/down counter schematic.

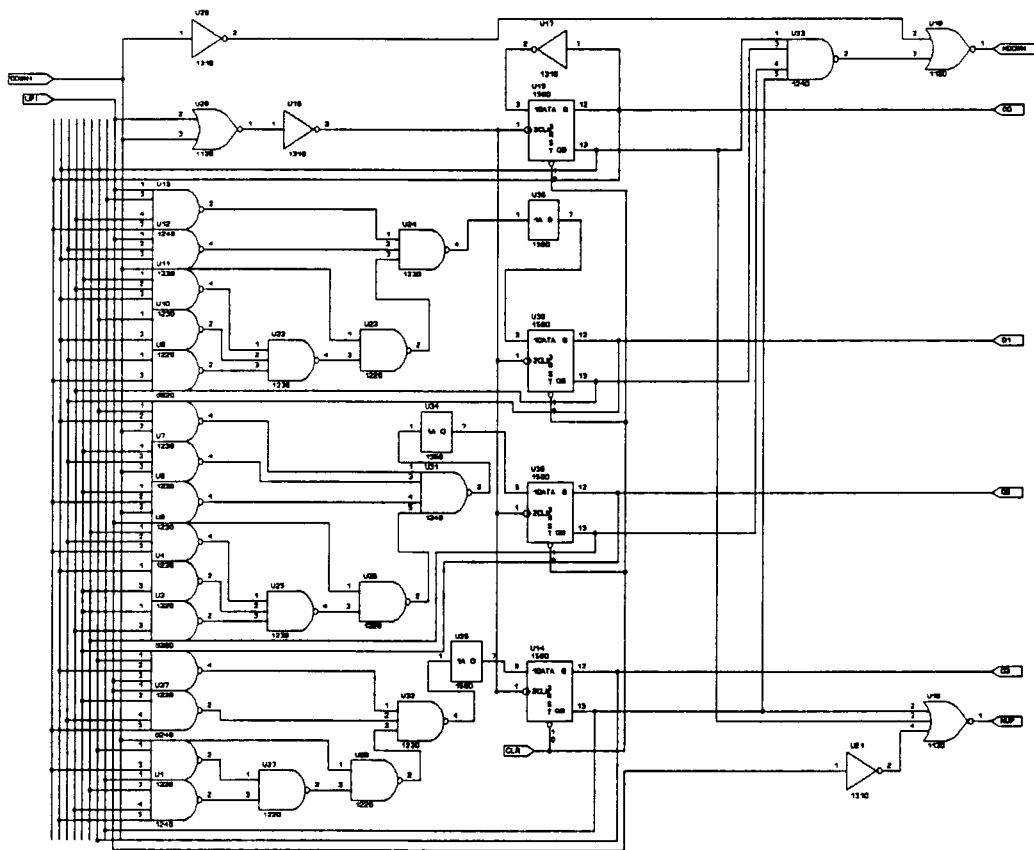
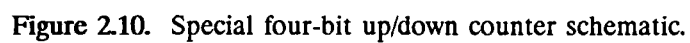


Figure 2.9. Four-bit up/down counter schematic.



prohibitive. In addition, many application specific designs, like the encoder counter presented in this paper, are not intended for mass fabrication and, therefore, do not lend themselves to structured approaches such as the Built-In Logic Block Observation (BILBO) method^[5]. For these reasons, a self-diagnosing scheme was designed into the LSI controller to provide functional testing of both the semicustom chip and its peripheral circuits. As has been stated, two static tests were implemented to provide functional testing of the display and output latch circuitry and one dynamic diagnostic was implemented to provide functional testing of the semicustom controller. The following paragraphs describe in detail this self-testing circuitry.

Two FSMs and several logic circuits form the testing portion of the semicustom controller chip. In normal operation, the control FSM, whose flowchart is shown in Figure 2.11, allows the A, B, and ZRI signals from the encoder to pass through the input selector, the input FSM, the counter circuitry, and the output bus selector. After the occurrence of a low-to-high transition on the TEST input of the semicustom controller, data from the display select logic is routed through the bus selector with MUXSEL. In addition, the input selector passes A_{int} and B_{int} from the test FSM to the input FSM with INPSEL. When the TEST input returns low, the next clock cycle validates the first static diagnostic. The second time that TEST switches to a logic "1" state, the DSPLYSEL line goes high. When TEST returns low, the next clock cycle validates the second static diagnostic. These two tests were designed to detect display and output latch stuck-at faults. A timing diagram and schematic of the control FSM are shown in Figures 2.12 and 2.13, respectively.

The final dynamic diagnostic is initiated the third time a transition from low-to-high occurs at the TEST input of the control FSM. The bus selector is then instructed to route data from the up/down counters to its output. When TEST makes a transition back to a logic "0", the next clock cycle activates RUN and control is passed on to the test FSM. This circuit, whose timing diagram and FSM flowchart are shown in Figures 2.14 and 2.15, respectively, cycles A_{int} and B_{int} so that UP pulses are produced by the input FSM. After all data from the counters has reached its maximum

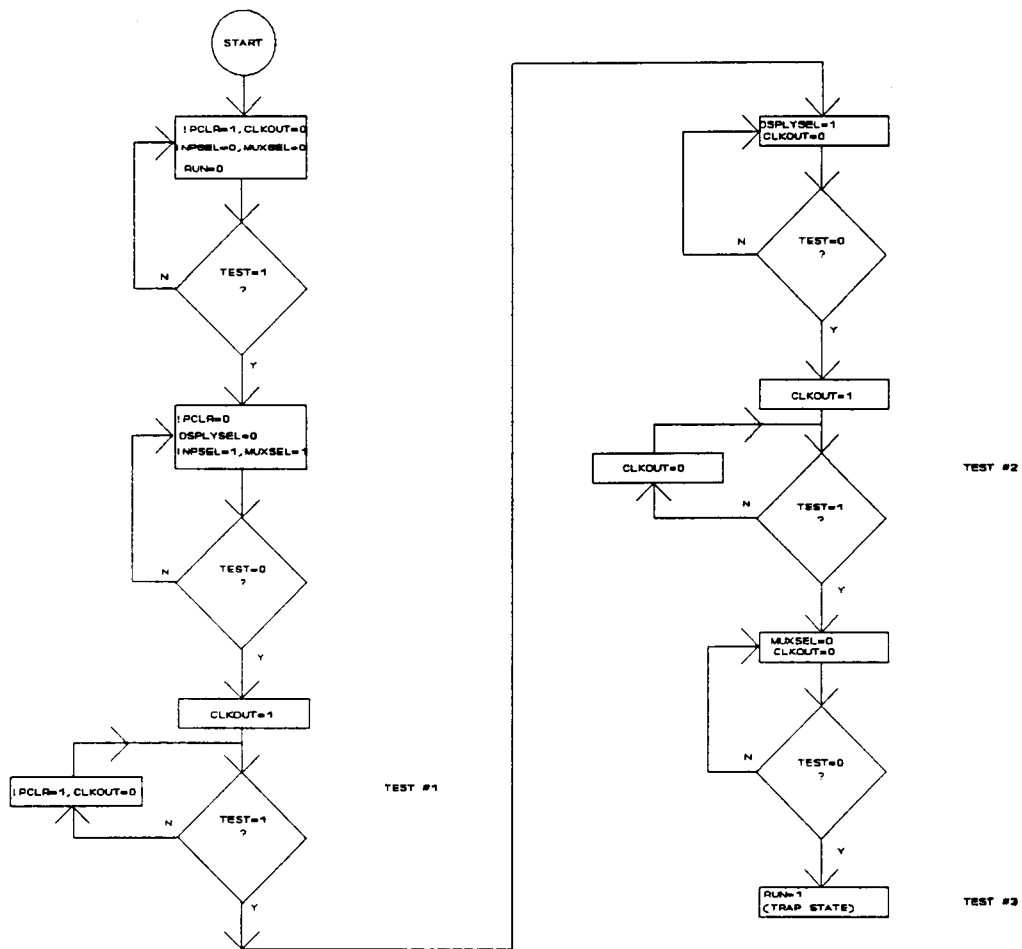


Figure 2.11. Control FSM flowchart.

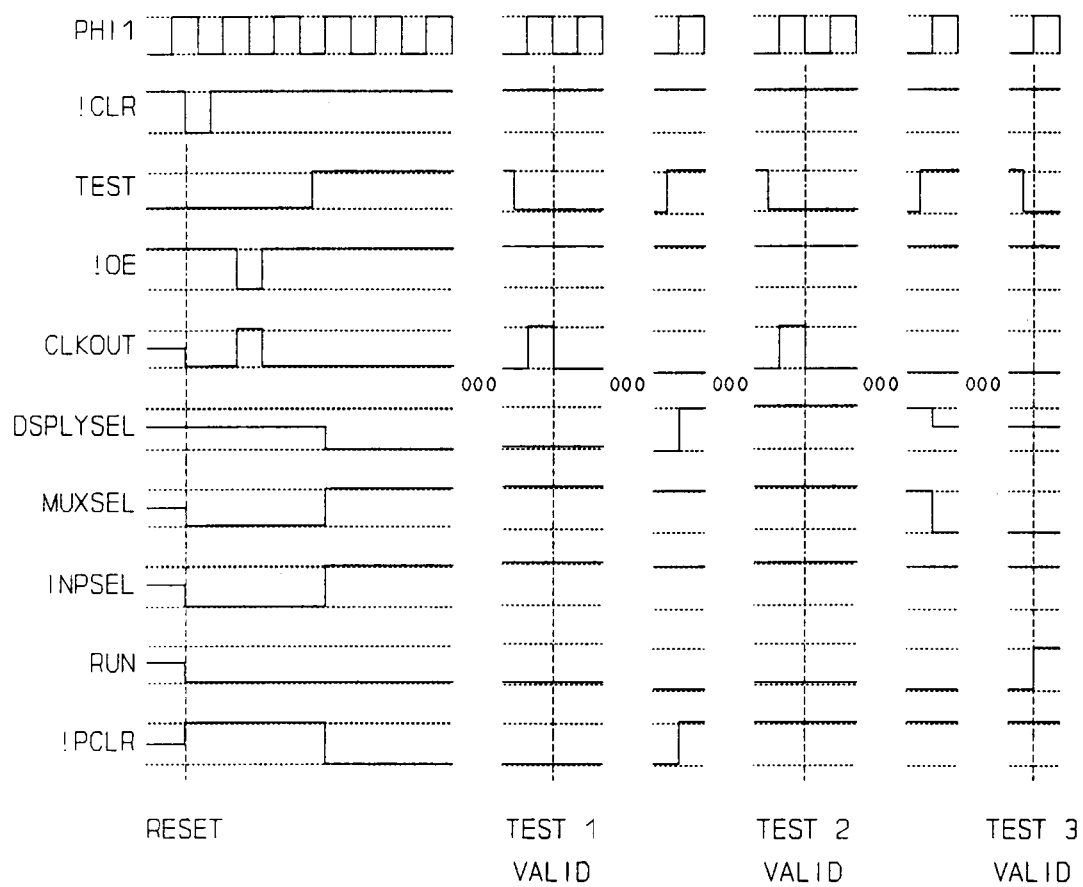


Figure 2.12. Control FSM timing diagram.

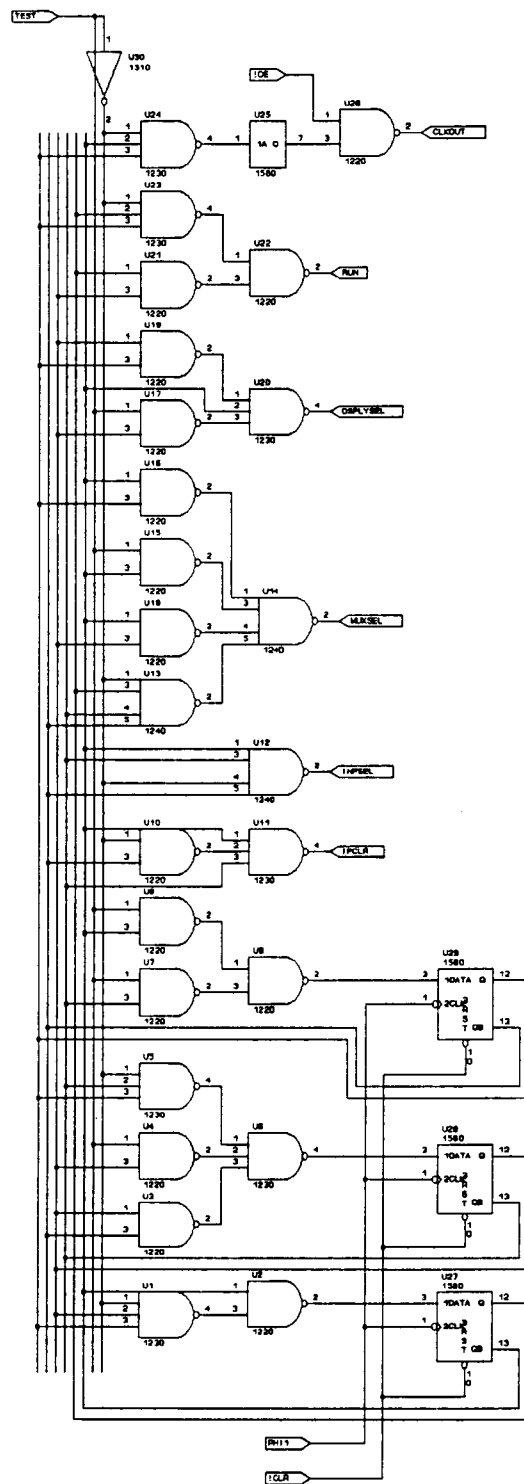
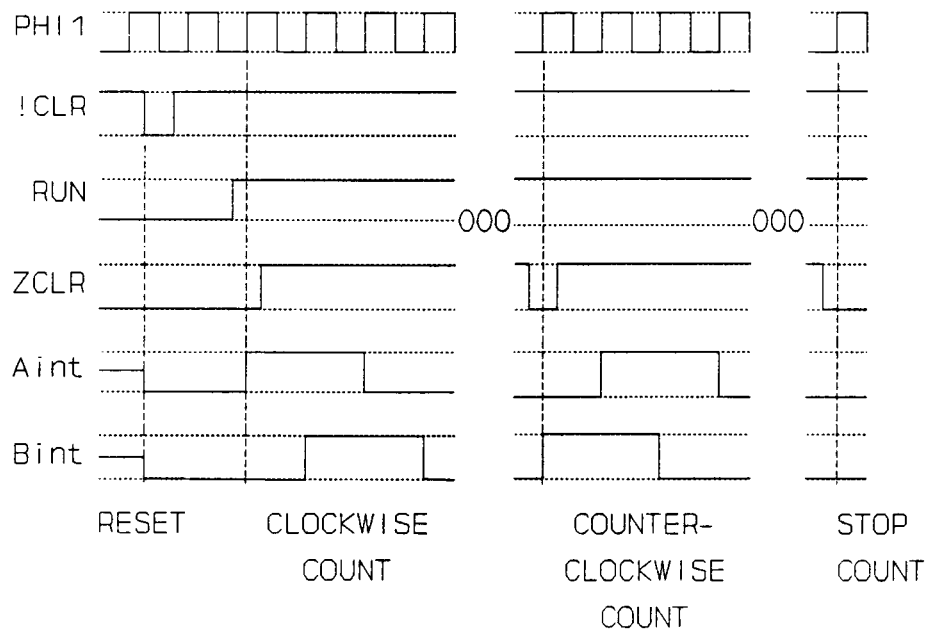


Figure 2.13. Control FSM schematic.



LEGEND:

— =UNKNOWN STATE

Figure 2.14. Test FSM timing diagram.

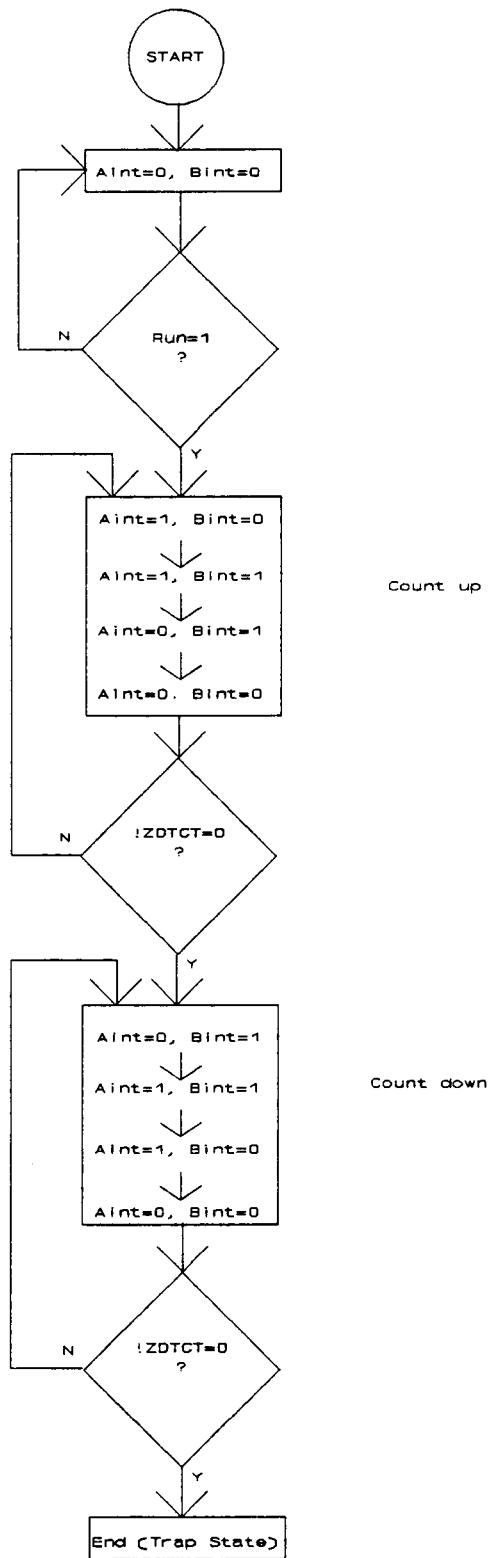


Figure 2.15. Test FSM flowchart.

count and has returned to zero, The ZDTCT line from the zero detect logic becomes active and the test FSM reverses the phasing of A_{int} and B_{int} so that DOWN pulses are produced by the input FSM. Once the counter data has again returned to zero and ZDTCT becomes active, both the test FSM, whose schematic is shown in Figure 2.16, and the control FSM are halted. A reset on !CLR will place these two circuits back in normal operation.

The ASIC encoder counter design described should increase reliability by at least a factor of two over a more conventional design using SSI and MSI circuits for two reasons. First, the increased integration associated with ASICs will reduce total chip count by at least a factor of ten. Assuming that the failure rate of the semicustom chip is equivalent to that of a small or medium scale IC, an enhanced reliability is achieved since fewer ICs will reduce the system failure rate. Second, the increased integration will also decrease the complexity of the printed circuit board design. A typical encoder counter will require two or three separate circuit boards to mount the required small and medium scale ICs. The design presented in this paper increases reliability since only one circuit board is needed to contain all the required ICs.

With the exception of the required "glue" logic, the entire encoder counter design has been described. Figures 2.17 and 2.18 show respective circuit diagrams for the display and multiplexer, and the zero detect "glue" logic. A complete semicustom chip schematic is shown in Figure A.9. In addition, the appendix also shows a complete interconnection list (Table A.1) and the design for the interconnecting printed circuit board (Figures A.7 and A.8). Chapter III will discuss the hardware and software interface used in the initial testing of the encoder counter. This chapter will also discuss system maintainability and outline a plan for field troubleshooting utilizing the self-diagnosing capabilities of this counter.

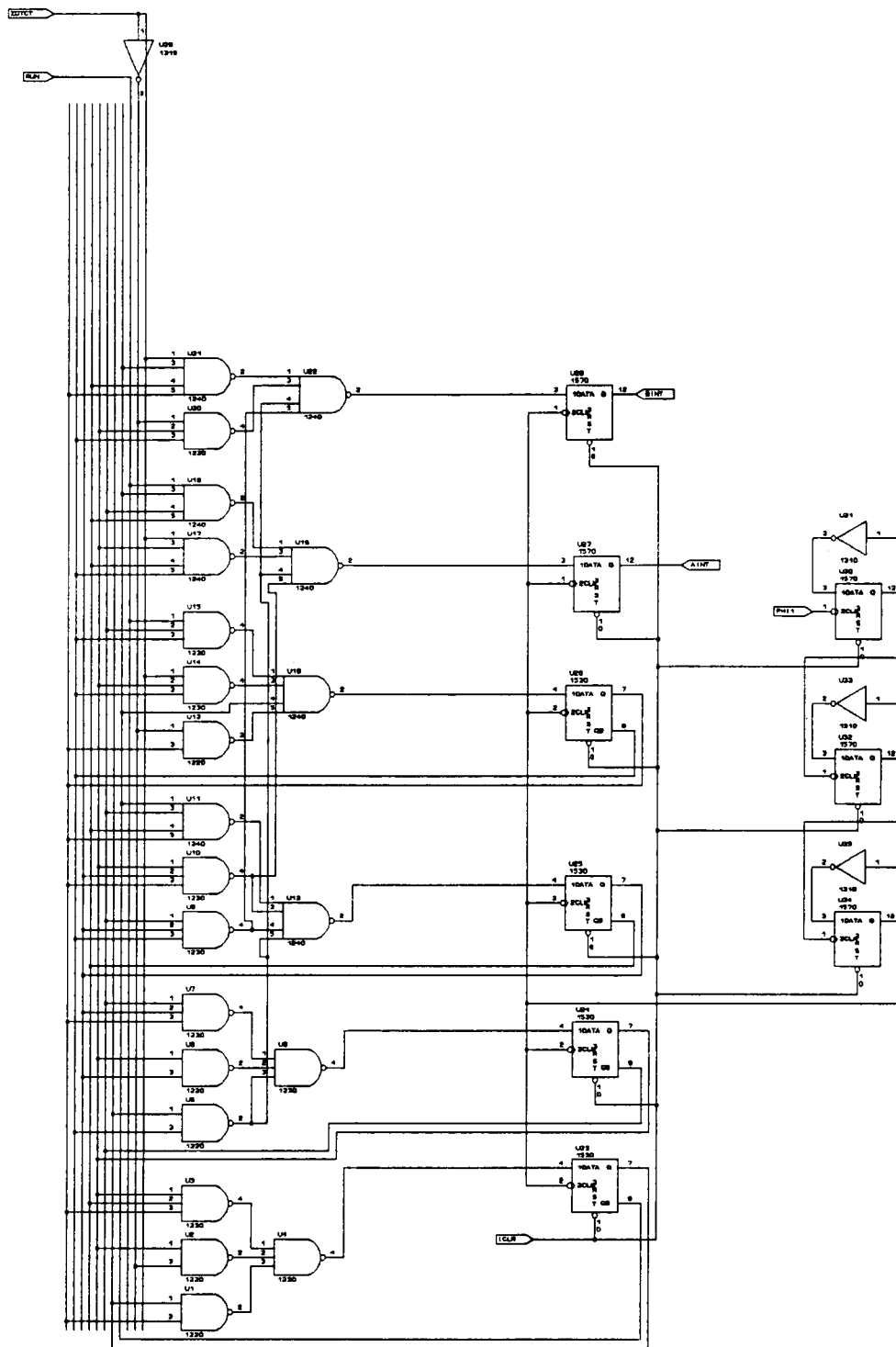


Figure 2.16. Test FSM schematic.

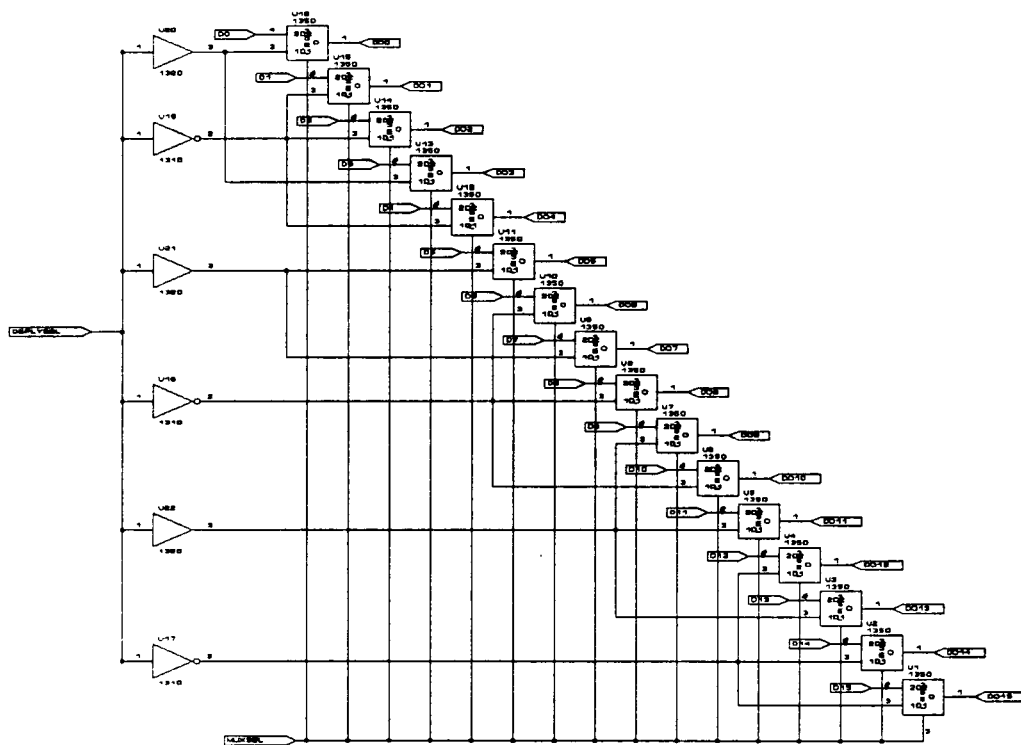


Figure 2.17. Display and multiplexer logic schematic.

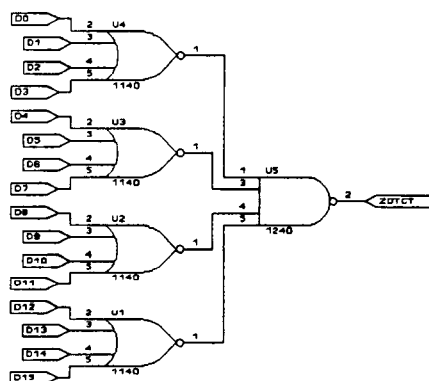


Figure 2.18. Zero detect logic schematic.

CHAPTER III

TESTABILITY

Increased integration of semicustom ICs has forced the designer to become more involved in the maintainability of his or her design. Separate test engineers cannot be expected to develop effective hardware and software testing interfaces after a design with limited nodal accessibility has been fabricated. Systems including LSI circuits must, therefore, be designed for testability. Furthermore, maintainability must also be considered so that these systems can be repaired in the field^[6]. An attempt was made to design the circuit presented in this paper for testability by developing a hardware and software interface used for initial testing purposes. In addition, self-diagnosing circuitry was incorporated in the semicustom chip in an effort to enhance system maintainability. The interface for initial circuit testing and a plan for field troubleshooting are discussed in the following paragraphs, respectively.

Initial Testing

The encoder counter was initially tested by interfacing it to the system bus of an IBM PC-compatible computer via a JDR Microdevices printed circuit board containing one 8255 Programmable Peripheral Interface (PPI) chip. This hardware and software interface was designed to test the functionality of the basic encoder counter. The hardware shown in Figure 3.1 performs the functions of both the encoder (by transmitting the A, B, and ZRI signals) and the compensator (by observing the complimentary BCD signals and by latching the output PALs with !OE). The compiled BASIC program, whose flowchart is shown in Figure 3.2, was written to simulate both encoder directions and can send ZRI signals to and receive and process BCD information from the encoder counter. A listing of this BASIC program is given in the appendix.

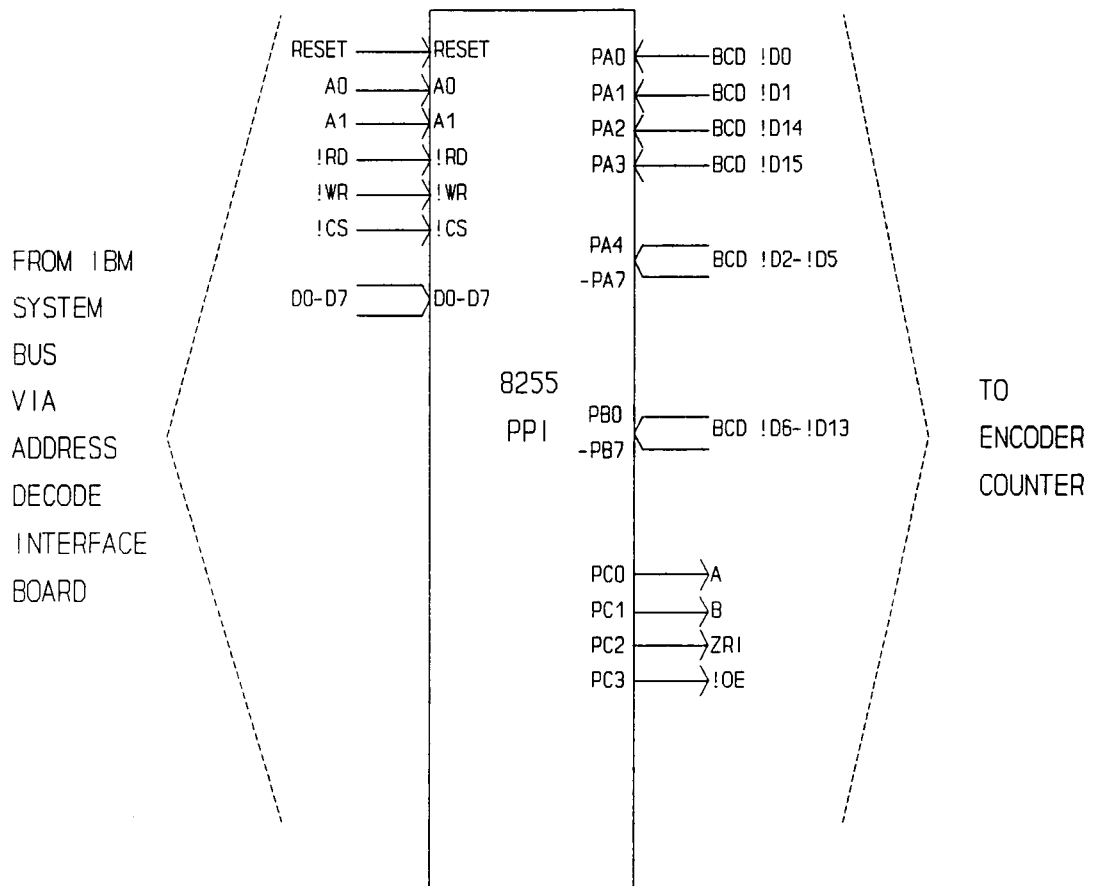


Figure 3.1. Encoder counter test interface diagram.

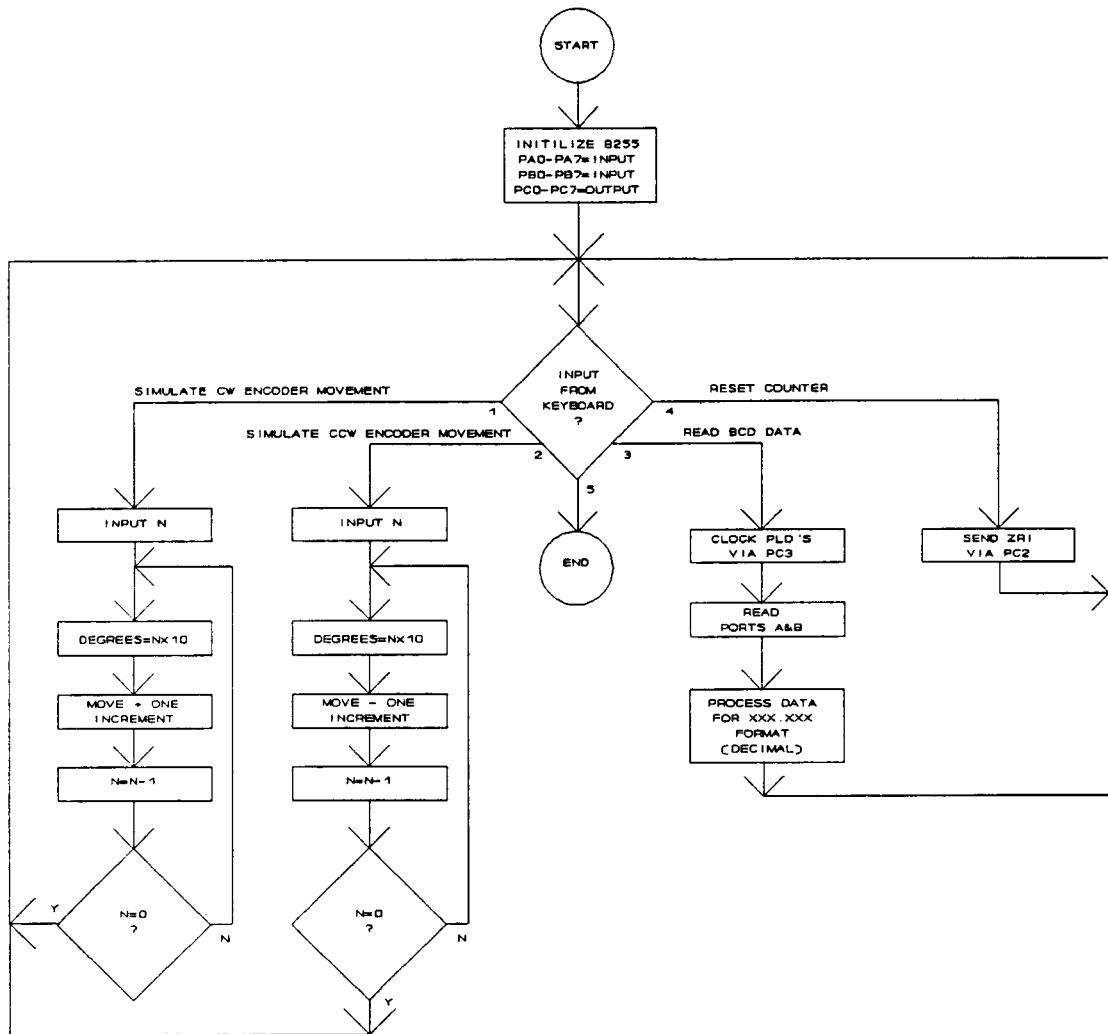


Figure 3.2. Test interface program flowchart.

Field Troubleshooting

Current encoder counters designed with SSI and MSI parts include little self-testing circuitry since the total number of ICs and the complexity of the printed circuit board design increases with this added functionality. However, by integrating self-diagnosing capability in a semicustom chip, system maintainability is enhanced without the added increase in chip count and printed circuit board complexity. The design presented in this paper includes such capability and should increase maintainability by at least a factor of three over a design without such circuitry since the three unique diagnostics incorporated in the semicustom IC will reduce the time needed to troubleshoot the display, the output latch, and the basic encoder counter functions. In addition, troubleshooting information about the encoder and position compensator (as well as the associated cabling) may be gained after the completion of these three self-tests.

The flowchart of Figure 3.3 presents a systematic approach to troubleshooting the encoder counter utilizing all three of the self-diagnostics. After the completion of the first two static tests (designed to detect stuck-at faults), display and output PLDs failures, if any, can be diagnosed and their faulty components replaced. The dynamic diagnostic (which exhaustively tests the input FSM, the counters, and the output multiplexer) is then initiated to detect faults associated with the basic encoder counter function of the semicustom IC. If this test fails, the semicustom chip must be replaced. If all three diagnostics perform correctly, but a positioning problem still exists, the basic encoder counter is functioning correctly and encoder or compensator failures are then suspected.

Both the initial testing hardware and software interface and the self-diagnosing circuitry were developed to ensure testability and maintainability of the encoder counter design. The troubleshooting flowchart will aid in reducing the time required to repair this counter once a problem has been detected. Chapter IV will assess the performance of the CAD tools and Chapter V will discuss the test results of this encoder counter design.

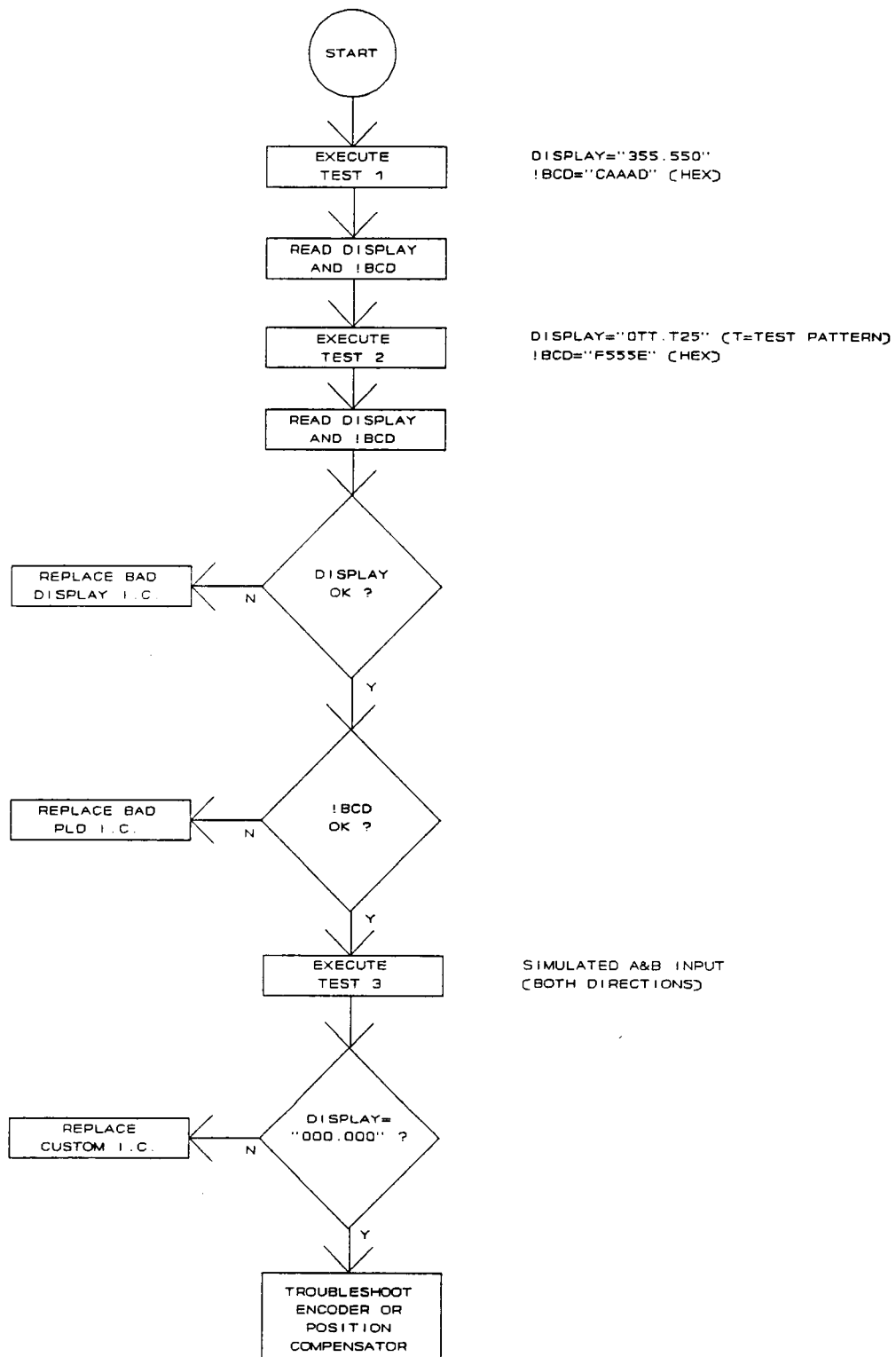


Figure 3.3. Field troubleshooting flowchart.

CHAPTER IV

EVALUATION OF COMPUTER AIDED DESIGN TOOLS

As has been stated, the standard cell implementation of the semicustom controller chip utilized CAD tools extensively for its design and simulation. A schematic representation of this IC was entered and simulated on a personal computer. This design process is analogous to that of a traditional approach using off-the-shelf components since the standard cell library contains similar devices. However, because of increased integration, an enhancement in system speed and a reduction in size and power dissipation are gained in a semicustom design.

The next step in the design process involved schematic-level simulation using a personal computer. After satisfactory results were achieved, the functional netlist was then transferred to a mainframe computer for cell placement and signal routing. This process, similar to that of designing a conventional printed circuit board, was done automatically by utilizing TimberWolf^[7]. This program can be used for standard cell, custom, and gate array designs, and can reduce to a minimum topology the area required by the cells and their interconnections since the iterative algorithm used in TimberWolf searches for the best possible fit. In addition, the designer is given the flexibility of constraining the number of rows and columns of cells, as well as the relative location of the I/O signals. However, the TimberWolf algorithm, which is NP-complete since there are no definitive solutions, may require several iterations for cell placement and signal routing^[8]. The topology of the semicustom chip is shown in Figure 4.1.

After switch-level simulation on a mainframe computer, the complete semicustom chip design was submitted to MOSIS for fabrication. The entire CAD process, shown in Figure 4.2, helped to reduce the design effort since this IC was fully tested before fabrication, and since the TimberWolf algorithm provided automatic cell placement and signal routing with little human

intervention. The next chapter will discuss the test results of the encoder counter design implemented in this thesis.

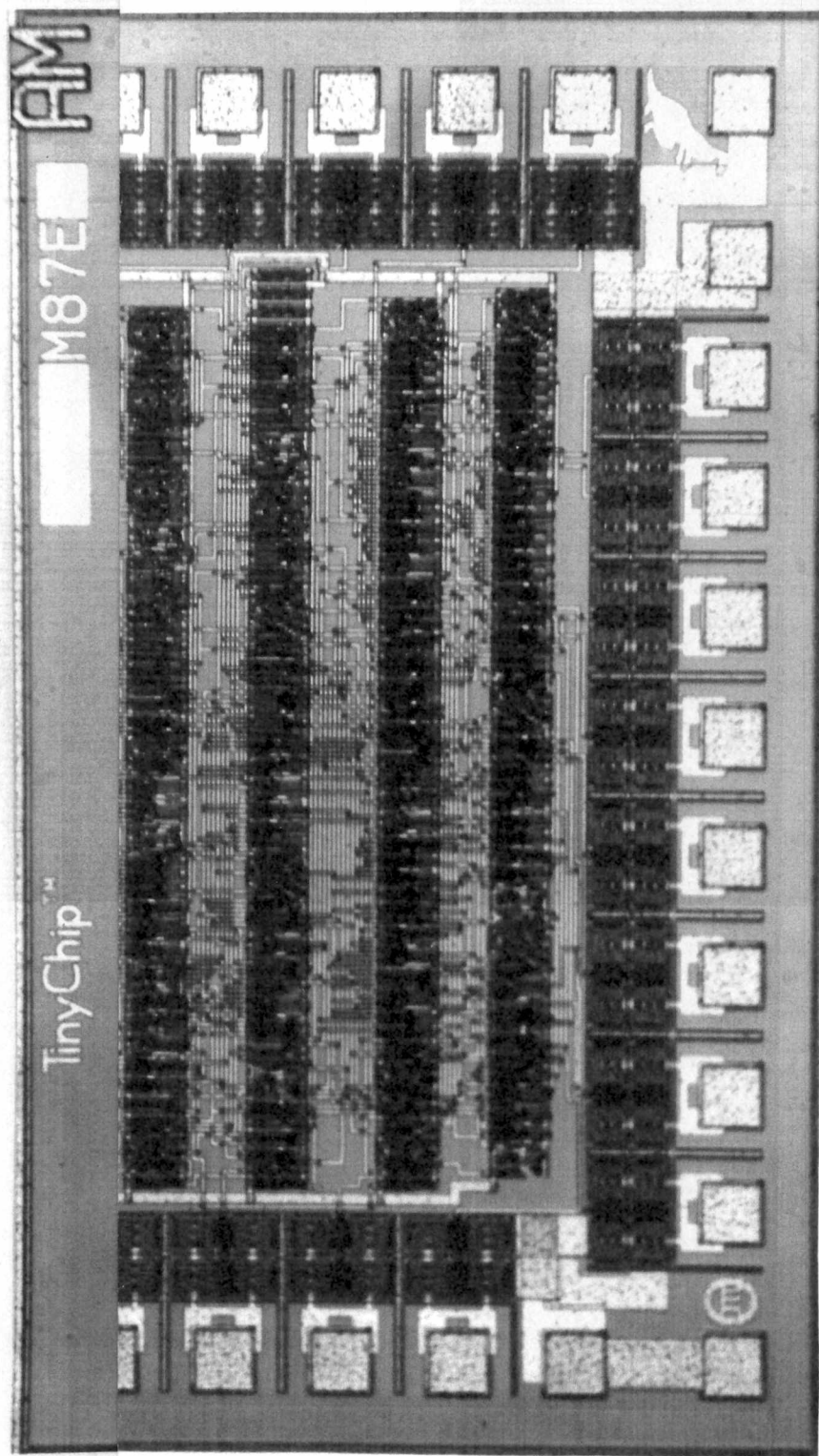


Figure 4.1. Semicustom chip physical layout.

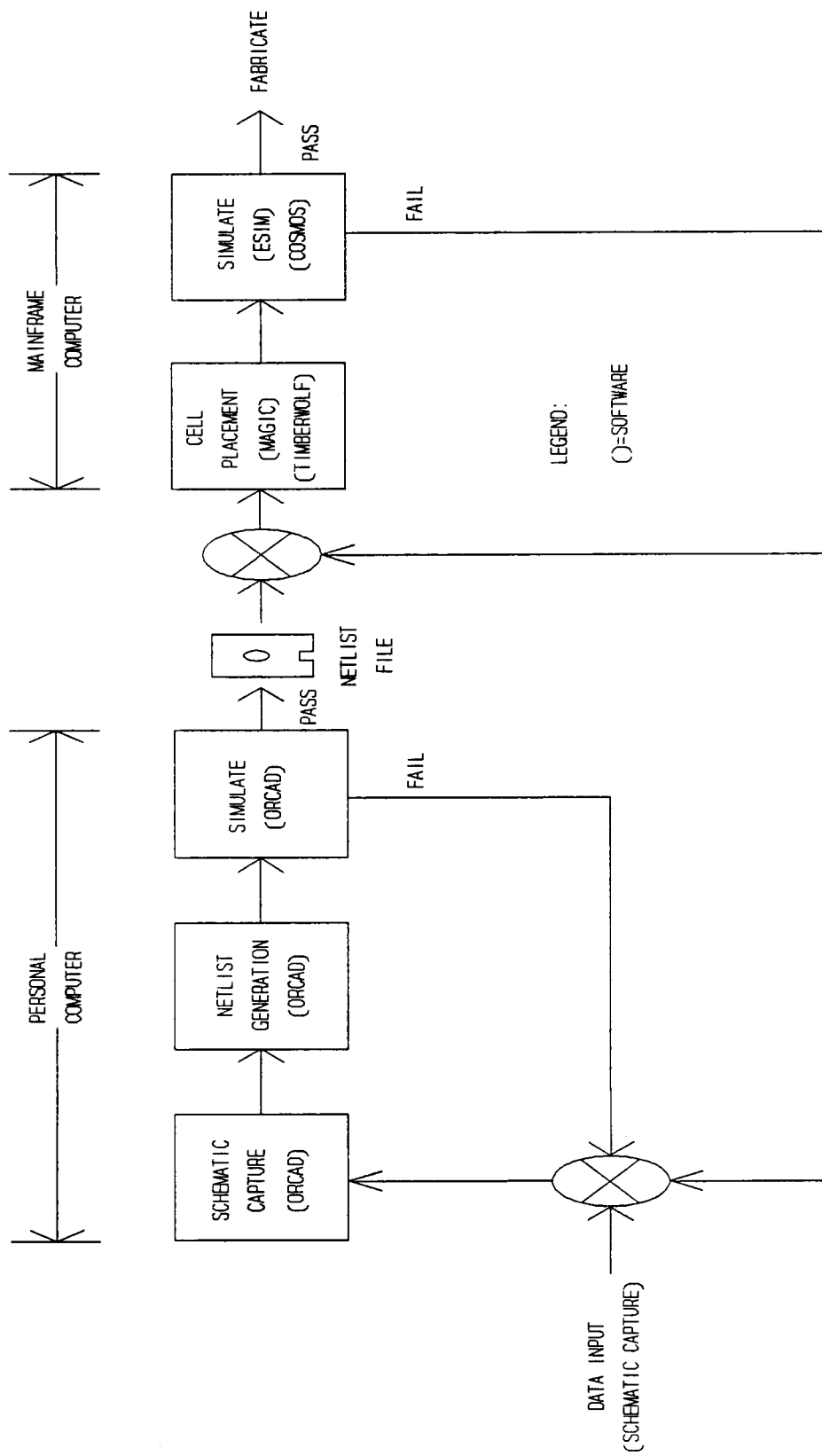


Figure 4.2. ASIC design process flow diagram.

CHAPTER V

TEST RESULTS

Favorable results were achieved during the initial testing of this encoder counter design. One modification was required, though, in order for the basic counter to function properly when attached to the hardware and software interface. The A and B inputs from the encoder had to be synchronized with the negative edge of the system clock to eliminate race conditions associated with the input level-mode FSM portion of the semicustom chip. With these inputs latched, the basic encoder counter circuitry performed accurately at a maximum clock speed of approximately 12 MHz and required approximately 510 mA. In addition, reliable counter operation was achieved with A and B transition occurring at up to 6 MHz. A standard encoder can provide reliable operation with A and B transitions occurring at up to 20 KHz.

Of the four semicustom chips fabricated, three performed both the basic encoder counter functions and the static diagnostics accurately at the maximum clock speed. The failure of the fourth semicustom IC is most likely associated with the fabrication process. The dynamic diagnostic, however, failed to function at any clock speed using any of the four semicustom chips. Since both the control and input FSMs, and the input select logic operated correctly under all other conditions, this failure is attributed to a dynamic test FSM design error. The simulation tools, however, did not detect any circuit malfunctions. One possible reason for the failure of these tools to discover this problem is due to the fact that simulation was performed using 3 μ m rules, while the semicustom chip was fabricated at a 2 μ m process. Therefore, an accurate simulation was not achieved since circuit and routing delays for a 3 μ m process are larger than that for a 2 μ m process. Definitive conclusions concerning this failure are further hampered since, after chip fabrication, neither the interior nor the I/O signals of the test FSM could be interrogated. Closing remarks are given in Chapter VI.

CHAPTER VI

CONCLUSIONS

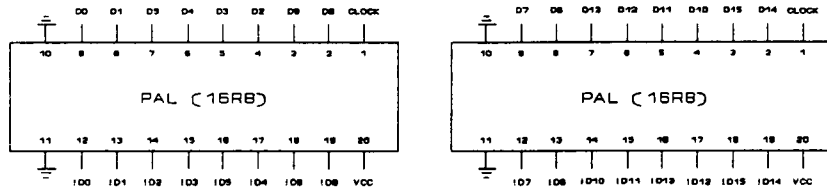
The design, fabrication, and testing of an application specific encoder counter with self-diagnosing capability has been discussed. This ASIC design included a semicustom IC, which contained the basic counter and self-testing circuitry and was designed with standard cells, and two PLDs, used for output latching. With the addition of circuitry to synchronize the encoder output signals to the system clock, this counter design (with the exception of the dynamic diagnostic) performed well at clock speeds of up to 12 MHz. Design errors associated with the dynamic test FSM are suspected as the cause of the dynamic diagnostic failure. System reliability is enhanced by at least a factor of two over present designs since the increased integration will reduce both the total chip count and the printed circuit board complexity. In addition, system maintainability will be increased by at least a factor of two over current designs since the self-diagnosing functions will reduce the time required for troubleshooting and repair. However, a further enhancement in maintainability would be achieved with the correct operation of the dynamic diagnostic.

Advancements in integrated circuit design and fabrication have reduced the effort associated with ASIC development. A schematic of a circuit can now be entered on a PC and fully simulated before a hardware commitment is made. Other types of ASIC technologies, such as gate arrays, also lend themselves to this design process. Recently, user-programmable gate arrays have been developed so that design changes can be implemented even after a hardware commitment is made without the added fabrication costs⁹. Each of these technologies, though, requires a design approach different from that of a circuit constructed with discrete ICs since the area required by and the time delays associated with the signals passing between cells are more devastating than that of the circuit elements themselves. For this reason, a new approach must be developed, based not on the cost of the individual cells but, rather, on the cost of routing signals between these cells¹⁰.

BIBLIOGRAPHY

- [1] Electro-Craft Corporation, DC Motors * Speed Controls * Servo Systems, 5th ed., pp. 7-1 to 7-11, 1980.
- [2] Bouldin, Donald W., *Electrical Engineering 6910 classroom notes*, Ferris Hall, The University of Tennessee, Knoxville (Fall 1985).
- [3] Tomovich, Christine, "MOSIS - A Gateway to Silicon", *IEEE Circuits and Devices*, Vol. 4, No. 2, pp. 22-23 (March 1988).
- [4] Williams, Thomas W., Kenneth P. Parker, "Design for Testability - A Survey", *Proceedings of the IEEE*, Vol. 71, No. 1, pp. 98-103 (January 1983).
- [5] Williams, pp. 104-110.
- [6] Bassak, Gil, "Testing VLSI Circuits", *Electronic Design*, pp. 140-152 (November 1984).
- [7] Sechien, Carl, Alberto Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package", *IEEE Journal of Solid-State Circuits*, Vol. 20, No. 2, pp. 510-522 (April 1985).
- [8] Brady, H. Nelson, John Banks, "Automatic Placement and Routing Techniques for Gate Array and Standard Cell Designs", *Proceedings of the IEEE*, Vol. 25, No. 6, pp. 797-806 (June 1987).
- [9] Freeman, Ross, "User-Programmable Gate Arrays", *IEEE Spectrum*, pp. 32-35 (December 1988).
- [10] Sutherland, Ivan E., Carver A. Mead, "Microelectronics and Computer Science", *Scientific American*, pp. 110-121 (September 1977).

APPENDIX



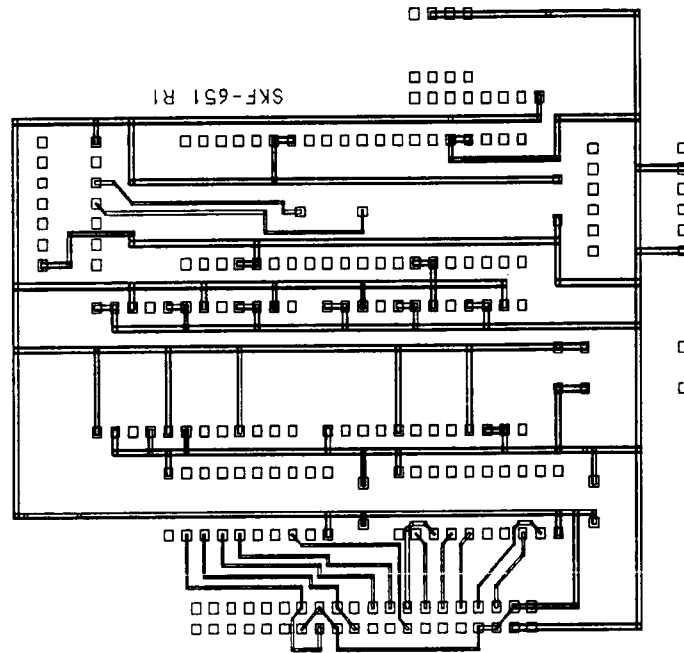


Figure A.4. Main circuit board layout (front).

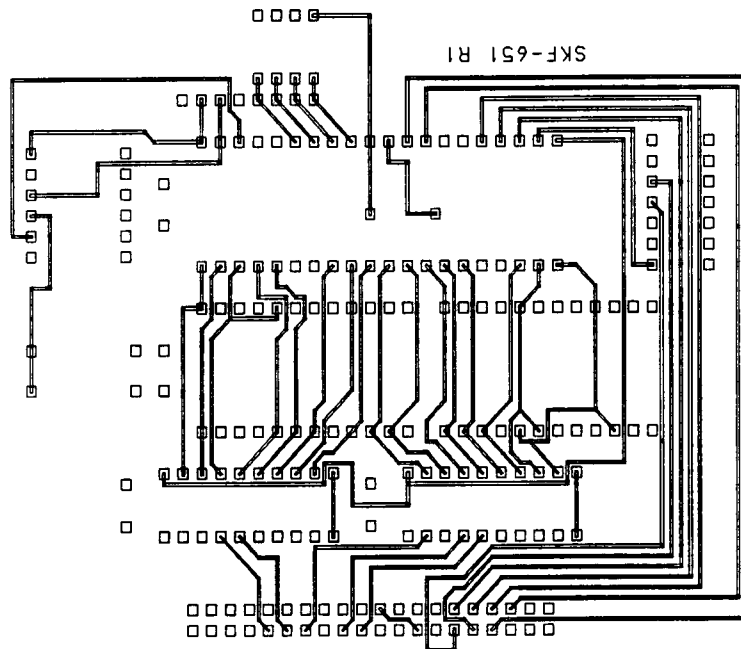
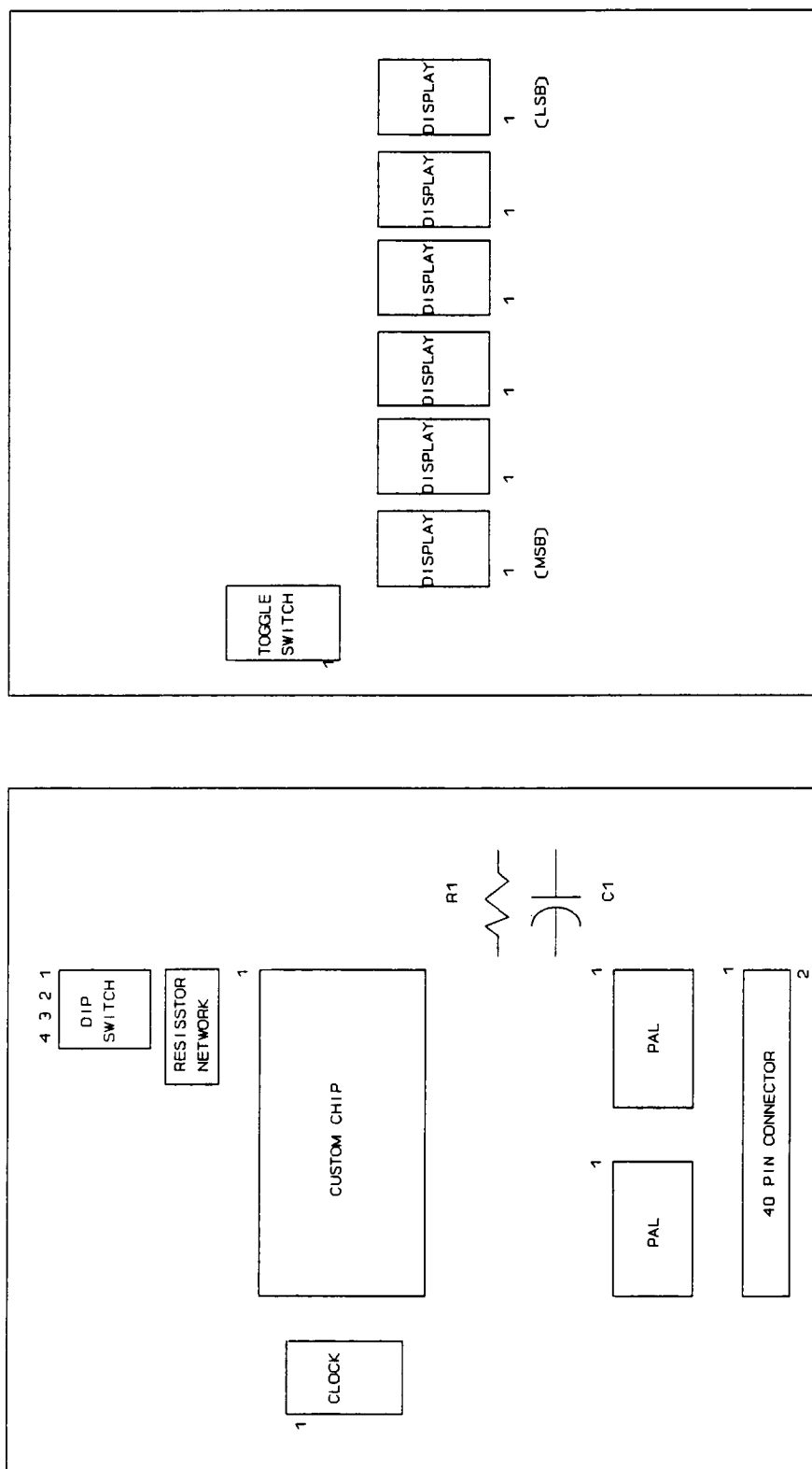


Figure A.5. Main circuit board layout (back).



FRONT

BACK

Figure A.6. Component location.

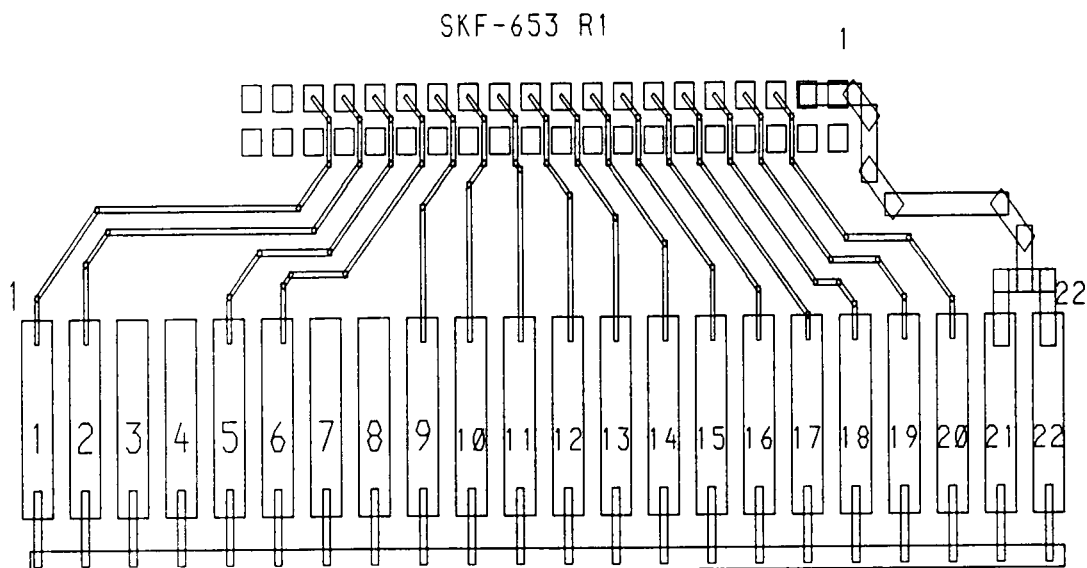


Figure A.7. Extender circuit board layout (front).

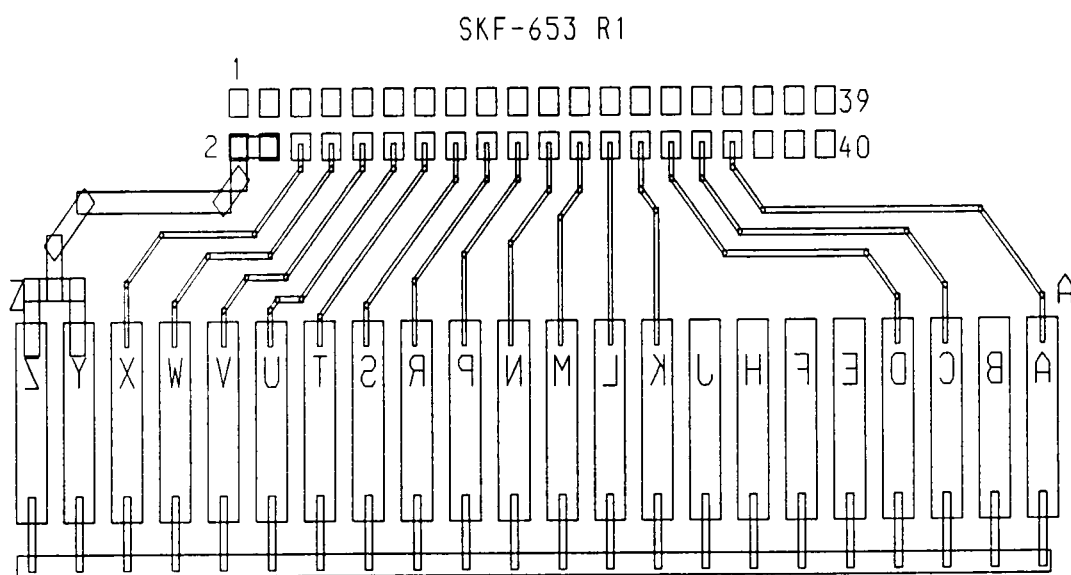


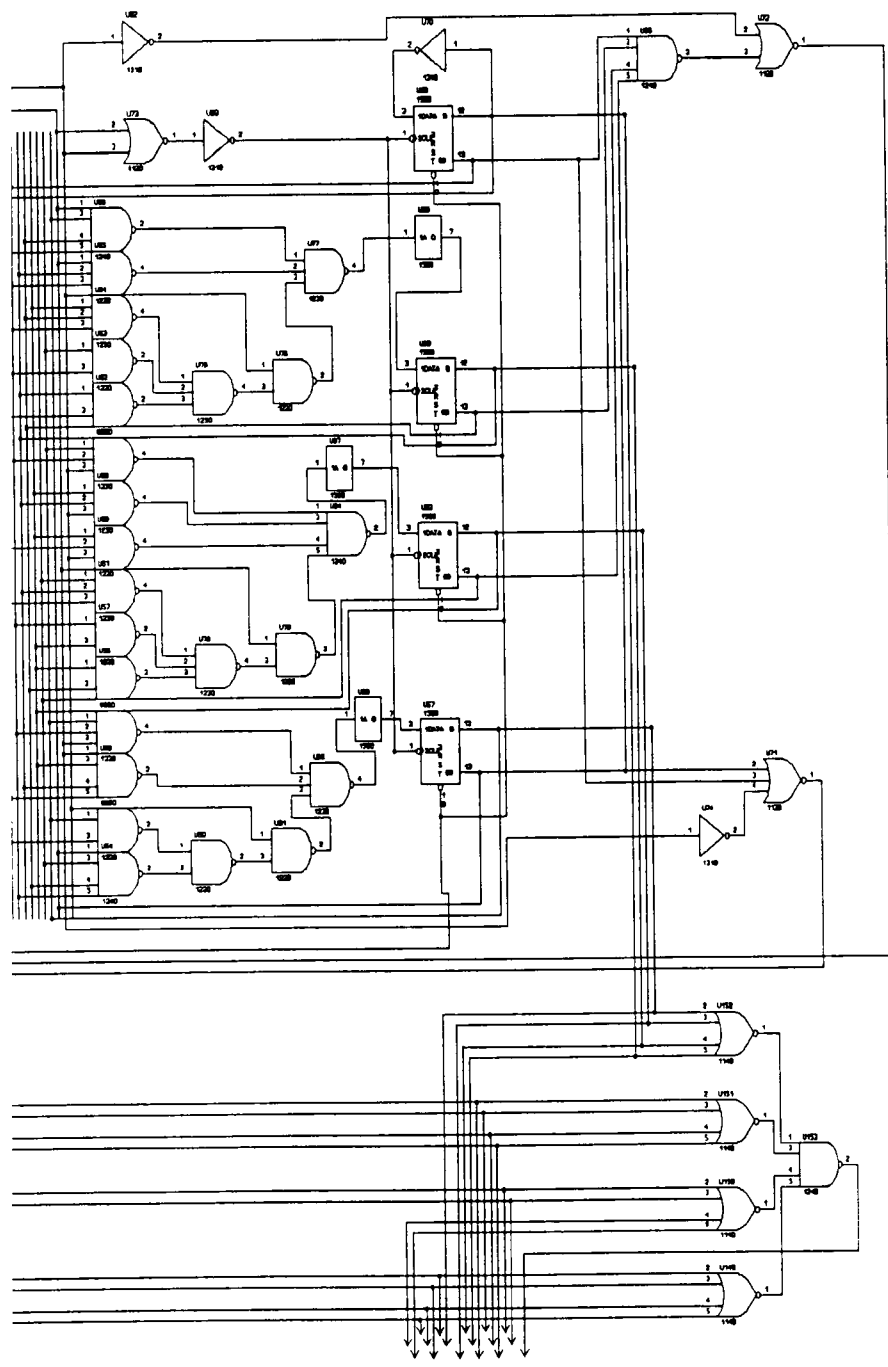
Figure A.8. Extender circuit board layout (back).

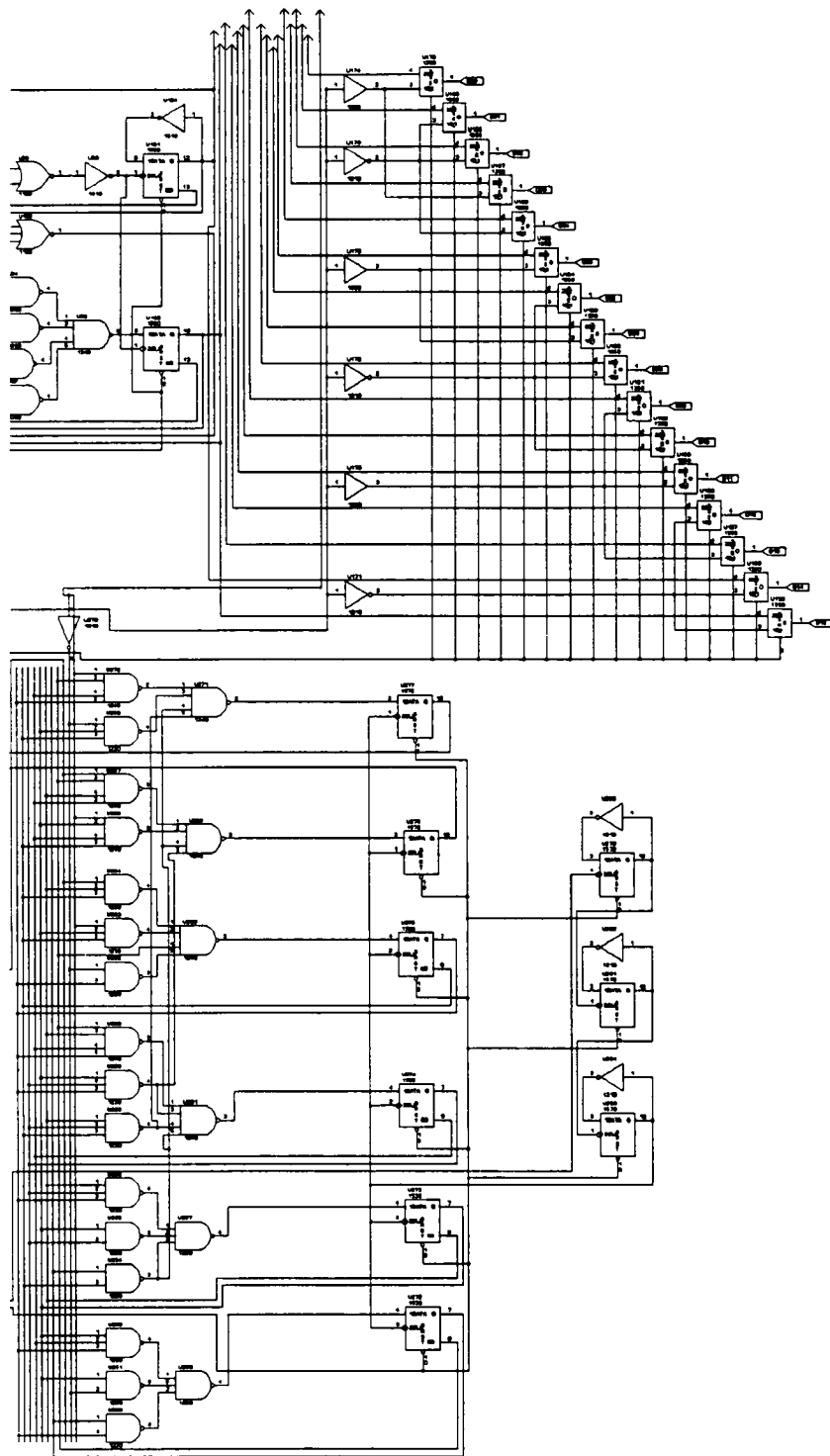
Table A.1. Interconnection List.

<u>44 PIN EDGE CONNECTOR</u>	<u>40 PIN CONNECTOR</u>	<u>DESCRIPTION</u>
1	35	ORD OUTPUT
2	33	CCW OUTPUT
3	NC	N/A
4	NC	N/A
5	31	A INPUT
6	29	B INPUT
7	NC	N/A
8	NC	N/A
9	27	BCD D0 OUTPUT
10	25	VCC
11	23	BCD D1 OUTPUT
12	21	BCD D0 OUTPUT
13	19	BCD D2 OUTPUT
14	17	BCD D3 OUTPUT
15	15	BCD D6 OUTPUT
16	13	BCD D7 OUTPUT
17	11	BCD D10 OUTPUT
18	9	BCD D11 OUTPUT
19	7	BCD D14 OUTPUT
20	5	BCD D15 OUTPUT
21	3	VCC
22	1	VCC
A	34	IOE INPUT
B	NC	N/A
C	32	ZRI INPUT
D	30	ZRO OUTPUT
E	NC	N/A
F	NC	N/A
H	NC	N/A
J	NC	N/A
K	28	VCC
L	26	BCD D0 OUTPUT
M	24	VCC
N	22	BCD D1 OUTPUT
P	20	BCD D5 OUTPUT
R	18	BCD D4 OUTPUT
S	16	BCD D9 OUTPUT
T	14	BCD D8 OUTPUT
U	12	BCD D13 OUTPUT
V	10	BCD D12 OUTPUT
W	8	VCC
X	6	VCC
Y	4	GND
Z	2	GND

BASIC Program Listing

<pre> 10 OUT &H303,&H92 20 OUT &H302,&H8 30 CLS 40 PRINT"1-MOVE POSITIVE DEGREES" 50 PRINT"2-MOVE NEGATIVE DEGREES" 60 PRINT"3-READ BCD PORT" 70 PRINT"4-SEND ZRI" 80 PRINT"5-EXIT TO DOS" 90 AS=INKEY\$ 100 IF AS="" GOTO 90 110 IF AS="1" GOTO 170 120 IF AS="2" GOTO 320 130 IF AS="3" GOTO 470 140 IF AS="4" GOTO 730 150 IF AS="5" THEN SYSTEM 160 GOTO 90 170 CLS 180 PRINT"ENTER N AS A WHOLE, POSITIVE NUMBER." 190 PRINT"N=1 WILL CAUSE .1 DEGREE MOVE." 200 INPUT N 210 OUT &H302,&H9 220 FOR D=1 TO 50:NEXT D 230 OUT &H302,&HB 240 FOR D=1 TO 50:NEXT D 250 OUT &H302,&HA 260 FOR D=1 TO 50:NEXT D 270 OUT &H302,&H8 280 FOR D=1 TO 50:NEXT D 290 IF N=1 GOTO 30 300 N=N-1 310 GOTO 210 320 CLS 330 PRINT"ENTER N AS A WHOLE, POSITIVE NUMBER." 340 PRINT"N=1 WILL CAUSE .1 DEGREE MOVE." 350 INPUT N 360 OUT &H302,&HA 370 FOR D=1 TO 50:NEXT D 380 OUT &H302,&HB 390 FOR D=1 TO 50:NEXT D 400 OUT &H302,&H9 410 FOR D=1 TO 50:NEXT D 420 OUT &H302,&H8 430 FOR D=1 TO 50:NEXT D 440 IF N=1 GOTO 30 450 N=N-1 460 GOTO 360 470 CLS 480 OUT &H302,&H0 490 FOR D=1 TO 50:NEXT D 500 OUT &H302,&H8 510 A=INP(&H300) 520 B=INP(&H301) 530 ALO=(A AND 15) XOR 15 540 AHI=(A AND 240)/16 XOR 15 550 BLO=(B AND 15) XOR 15 560 BHI=(B AND 240)/16 XOR 15 570 ALOW=ALO AND 3 580 MSB=(ALO AND 12)/4 590 IF ALOW=0 THEN LSB=0 600 IF ALOW=1 THEN LSB=25 610 IF ALOW=2 THEN LSB=50 620 IF ALOW=3 THEN LSB=75 630 MSB=MSB*100 640 BHI=BHI*10 650 AHI=AH*1 660 LSB=LSB*.001 670 IF (BHI=100) AND (BLO=10) AND (AHI=1) AND (LSB=.025) GOTO 710 680 BCD=MSB+BHI+BLO+AH*1+LSB 690 PRINT"BCD OUT =","BCD,"DEGREES" 700 GOTO 40 710 PRINT "BCD OUT = 088.825 DEGREES." 720 GOTO 40 730 OUT &H302,&HC 740 FOR D=1 TO 50:NEXT D 750 OUT &H302,&H8 760 GOTO 30 </pre>	<pre> INITIALIZE 8255 PIA IOE ACTIVE LOW 'A=1, B=0 'A=1, B=1 'A=0, B=1 'A=0, B=0 'A=0, B=1 'A=1, B=1 'A=1, B=0 'A=0, B=0 SEND IOE TO PLD'S 'READ DATA 'FROM PLD'S SEPARATE, INVERT, AND NORMALIZE BCD DATA EACH CHANGE IN A OR B CAUSES .025 CHANGE IN BCD OUTPUT 'WEIGHT 'VARIABLES 'SO THAT OUTPUT 'IS xxx.xxx SEND SIMULATED ZRI TO ASIC CHIP </pre>
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VITA

Daniel John Linehan was born in Littleton, Colorado on August 28, 1960 and raised in Fort Wayne, Indiana. He attended Paul Harding High School in Fort Wayne and graduated in 1979. That fall, he entered The University of Tennessee, Knoxville and graduated December 1983 with a Bachelor of Science in Electrical Engineering with Honors.

Mr. Linehan entered The Graduate School of The University of Tennessee, Knoxville in March 1984. After two quarters of study, he accepted employment with Martin Marietta Energy Systems in Oak Ridge, Tennessee as a production support engineer. He received the Master of Science in Electrical Engineering in May 1989. The author is a member of the Institute of Electrical and Electronics Engineers and is an Engineer-in-Training.