Design of High Power Density Three-Level Inverter for Aircraft Application

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Abstract

For more electric transportation applications, power density of the power electronic converters becomes the key issue because of the limited space and carrier capability. This dissertation studies three-level converter in aircraft application. The research focuses on design of high power density three-level inverter emphasizing on passive reduction through novel modulation and control, paralleling and interleaving strategy, filter modeling and design optimization.

First, understanding harmonic characteristics in a power converter is critical for passive design and reduction. Harmonic calculation models of three-level neutral point clamped inverter with space vector modulation are developed. The impact of interleaving angle on dc and ac side harmonics and EMI harmonics is comprehensively studied considering multiple impact factors and optimal interleaving angle ranges to reduce these harmonics is derived.

Second, low frequency circulating currents need to be suppressed in paralleled inverters. To increase inverter system power density, a space vector modulation is proposed for paralleled three-level inverters to reduce common-mode voltage and switching loss in addition to suppress the low frequency circulating current.

Third, high frequency circulating currents are suppressed by coupled inductors in parallel interleaved inverters. To reduce the coupled inductor size and weight, carrier based PWM method to achieve minimum flux for coupled inductor in interleaved three-level inverters is proposed.

Fourth, to reduce the required EMI filter, one approach is reducing EMI noise. The inverter and filter topology for common-mode noise reduction in three-level inverter is investigated. Fourth-leg topology is applied to three-level inverter for common-mode noise reduction. An impedance balancing circuit filter topology is proposed to reduce both dc and ac side common-mode noise for

motor drive system.

Fifth, to reduce the required EMI filter, another approach is filter design optimization. Spectrum concept is introduced for CM inductor saturation analysis and design optimization. CM inductor flux density model is developed and multiple impact factors are investigated. An improved CM filter design procedure is proposed to avoid over-design or under-design of CM inductor.

Last, design and demonstration of a 1 MW three-level inverter with cryogenic cooling is presented which provides guidance for high power three-level inverter design and cryogenic power converter design.

Table of Contents

1. Introduction 1

1.1 Application Background 1

1.2 Multilevel Topology and Modulation 5

1.3 EMI Noise and EMI Filters 9

1.4 Literature Review 11

1.4.1 Space Vector Selection for Three-Level Inverter 11

1.4.2 Harmonic Reduction through Parallel Interleaving 18

1.4.3 Circulating Current Reduction in Paralleled Inverters 19

1.4.4 EMI Noise Reduction Methods 20

1.4.5 EMI Filter Modeling and Design Optimization 29

1.5 Research Challenges 30

1.6 Dissertation Organization 31

2. Harmonic Modeling and Interleaving Angle Optimization to Reduce Harmonics for Paralleled Three-Level Inverters 34

2.1 Analytical Model for Harmonic Calculation of Three-Level SVM 34

2.1.1 Three-Level SVM 34

2.1.2 Analytical Model for AC Voltage Harmonic 37

2.1.3 Analytical Model for DC Side Current Harmonic of NPC Inverter 42

2.2 Impact of Interleaving on AC Voltage and DC side Current Harmonics 46

2.2.1 Impact of Interleaving Angle on AC Voltage WTHD 46

2.2.2 Impact of Interleaving Angle on DC-link Capacitor RMS Current 47

2.3 Impact of Switching Frequency and Interleaving on EMI Harmonics 49

2.3.1 Relationship between Switching Frequency and EMI Filter Corner Frequency. 50

2.3.2 Impact of Interleaving on EMI Filter Corner Frequency 55
2.4 Experimental Results..... 58
2.4.1 Analytical Model Verification..... 60
2.4.2 Impact of Interleaving on AC Voltage and DC Side Current Harmonics..... 63
2.4.3 Impact of Interleaving on EMI Harmonics 69
2.5 Conclusion..... 72
3. Space Vector Modulation to Reduce Circulating Current, CM Voltage, and Switching Loss for Paralleled Three-Level Inverters 74
3.1 Conventional Modulation Methods for Three-Level Inverter 74
3.1.1 NTSV and PDPWM 76
3.1.2 LMSZVM and PODPWM..... 78
3.1.3 CMR Modulation 80
3.2 Proposed Space Vector Modulation..... 81
3.2.1 Optimal Fourth Space Vector..... 81
3.2.2 Discuss on Neutral Point Voltage Balance..... 93
3.3 Simulation and Experimental Results 96
3.3.1 Simulation Results..... 96
3.3.2 Experimental Results..... 101
3.4 Conclusion..... 108
4. Coupled Inductor Flux Minimization for Parallel Interleaved Three-Level Inverters 109
4.1 Modulation for Coupled Inductor Flux Linkage Reduction..... 110
4.1.1 Flux Linkage of Coupled Inductor 110
4.1.2 Optimal Zero Sequence Offset 114
4.1.3 Discuss on Neutral Point Voltage Balance..... 122

4.2 Modulation Methods Comparison 124
4.2.1 General Method for Circulating Current Prediction 124
4.2.2 Modulation Comparison 125
4.3 Simulation and Experimental Results 131
4.3.1 Simulation Results 131
4.3.2 Experimental Results 134
4.4 Conclusion 140
5. Inverter and Filter Topology to Reduce CM Noise for Three-Level Inverter 141
5.1 Three-Level Fourth-leg Topology 141
5.1.1 Topology and Modulation 141
5.1.2 Experimental Results 146
5.1.3 Discuss on Alternative Fourth-leg Filter Structure 149
5.2 Impedance Balancing Filter Topology 152
5.2.1 Existing Impedance Balancing Circuit for DC side CM Noise Reduction 152
5.2.2 Analysis of Motor Drive with Input and Output CM Filters 155
5.2.3 Proposed Impedance Balancing Circuit 157
5.2.4 Noise Attenuation Performance Modeling and Analysis 162
5.3 Experimental Results and Analysis 167
5.3.1 Impedance Balancing Circuit Design to Reduce Only AC side CM Noise 168
5.3.2 Impedance Balancing Circuit Design to Reduce both AC and DC Sides CM Noise 170
5.3.3 Comparison to the Conventional CM Filter 173
5.4 Conclusion 176
6. CM Inductor Modeling, Analysis, and Design Optimization for Three-Level Inverter 178

6.1 Spectrum Concept for CM Inductor Design Optimization 178
6.1.1 Spectrum Concept Analysis 178
6.1.2 Experimental Verification 183
6.2 CM Inductor Flux Density Modeling and Analysis 187
6.2.1 Basic Model 187
6.2.2 Impact of Modulation Index 193
6.2.3 Impact of Dead Time 196
6.2.4 Impact of Neutral Point Voltage Variation 199
6.2.5 Impact of CM Inductance 205
6.3 Improved CM Filter Design Procedure 209
6.4 Verification 212
6.5 Conclusion 217
7. Design and Demonstration of a MW Three-Level Inverter with Cryogenic Cooling . 219
7.1 Power Devices and Magnetics Characterization at Cryogenic Temperature 220
7.1.1 Power Devices Characterization 220
7.1.2 Magnetics Characterization 225
7.2 MW Three-Level Inverter System Design 231
7.2.1 Power Module Selection and Paralleling Strategy 231
7.2.2 Switching Loop Analysis and Busbar Design 234
7.2.3 Controller Design 237
7.2.4 Filter Design 237
7.2.5 Cooling System Integration 240
7.3 MW Three-Level Inverter System Testing 242
7.3.1 Hardware 242

7.3.2 Function Verification 244
7.3.3 Cryogenic Temperature Testing 247
7.4 Conclusion 249
8. Conclusion and Future Work 250
8.1 Conclusion 250
8.2 Publication List 253
8.3 Future Work 258
References 260
Vita 283

List of Tables

Table 2-1. Double Fourier Integral Limits of NTSV in Region 3 (Sector I, II, II)..... 39

Table 2-2. Double Fourier Integral Limits of NTSV in Region 2 (Sector I, II, III) 40

Table 2-3. Double Fourier Integral Limits of NTSV in Region 1 (Sector I, II, II)..... 41

Table 2-4. Comparison of Main Components of AC Phase Voltage..... 61

Table 2-5. Comparison of Main Components of DC Input Currents. 63

Table 2-6. Line Voltage WTHD at Different Modulation Index and Interleaving Angles 64

Table 2-7. DC-link Capacitor High Frequency Current RMS Value with Different Modulation Index and Interleaving Angles (PF=1)..... 65

Table 2-8. DC-link Capacitor High Frequency Current RMS Value with Different Modulation Index and Interleaving Angles (PF=0)..... 69

Table 3-1. CMV Levels of Different Switching States..... 76

Table 3-2. PWM Sequences of Proposed Modulation (Sector I)..... 88

Table 3-3. Impact of k on AZSV at Different Sectors..... 90

Table 3-4. Impact of k on NP Voltage at Different Sectors 96

Table 3-5. Parameters for Simulation and Experiment..... 97

Table 3-6. Devices Loss Comparison 99

Table 3-7. Current THD Comparison 99

Table 4-1. The Optimal Zero Sequence Offset Candidates $V0$ and the Corresponding H 117

Table 4-2. Duration Time and Slope of Each Segment of the Circulating Current..... 125

Table 4-3. Parameters for Simulation and Experiments 131

Table 5-1. Main Parameters of the Inverter 146

Table 6-1. Double Fourier Integral Limits of Basic PDPWM..... 191

Table 6-2. Inverter System Main Parameters 193

Table 6-3. Double Fourier Integral Limits of Basic PDPWM Considering Dead Time 197

Table 6-4. Phase Voltage and CM Voltage Main Components at M=1 198

Table 6-5. Phase Voltage and CM Voltage Main Components at M=0.4 198

Table 6-6. Averaged Neutral Point Current in a Fundamental Cycle 201

Table 6-7. Main Components of Phase Voltage and CM Voltage without NP Voltage Variation (M=1, Vdc=300 V, Io=20 A) 204

Table 6-8. Main Components of Phase Voltage and CM Voltage with NP Voltage Variation (M=1, Vdc=300 V, Io=20 A) 204

Table 6-9. CM Inductor Design Results with Improved CM Filter Design Procedure 216

Table 6-10. CM Inductor Design Results with Conventional CM Filter Design Procedure 216

List of Figures

Fig. 1-1. Evolution of MEA [227]. 2

Fig. 1-2. Example of an aircraft electric network with power converters [227]. 2

Fig. 1-3. Notional power system configuration [1]. 3

Fig. 1-4. Inverter System boundary and interfaces [1]. 3

Fig. 1-6. Classification of multilevel converter topologies. 5

Fig. 1-7. Subdivisions of NPC and FC topologies. 6

Fig. 1-8. Subdivisions of cascaded topologies. 6

Fig. 1-9. Classification of modulation strategies for multilevel converter. 7

Fig. 1-10. EMI noise propagation path in a power inverter system. 10

Fig. 1-11 EMI standards in DO-160. 10

Fig. 1-12. Circuit and space vector diagram for three-level NPC inverter [32]. 12

Fig. 1-13. Circuit diagram for vectors and the influence on NP voltage [32]. 13

Fig. 1-14. Space vector hexagon and voltage reference for 60° DPWM. 16

Fig. 1-15. Two methods for CM voltage reduction. 17

Fig. 1-16. EMI filter corner frequency versus switching frequency [101]. 21

Fig. 1-17. Gate logic and CM voltage for (a) SVPWM, (b) DPWM (clamped to positive bus), (c) DPWM (clamped to negative bus), (d) AZSPWM, (e) NSPWM. 23

Fig. 1-18. Implementation of feedforward CM noise voltage cancellation [117]. 24

Fig. 1-19. Implementation of feedforward CM noise current cancellation [117]. 25

Fig. 1-20. Comparison of the measured CM noise [117]. 25

Fig. 1-21. Four leg two-level inverter with second order filter and motor load [145]. 27

Fig. 1-22. Filter topology- connecting ac and dc mid-point [137]. 28

Fig. 1-23. Filter topology - impedance balancing circuit in motor drive system [141]. 28

Fig. 2-1. Vectors of NTSV and the PWM sequences of sector I. 35

Fig. 2-2. Two sub-sector boundary angles in sector I, (a) region 2, (b) region 3. 36

Fig. 2-3. (a) Three-level PD PWM carrier waveform, (b) the unit cell contour plot. 37

Fig. 2-4. Switching pattern and current path of a three-level active NPC. 43

Fig. 2-5. Dc side current spectrum of a two-level inverter with SVM when PF=1. 45

Fig. 2-6. Dc side current spectrum of a three level NPC inverter with NTSV when PF=1, (a) positive/negative line current, (b) neutral line current. 45

Fig. 2-7. Ac side line to line voltage WTHD versus interleaving angle ($f0 = 400\ Hz, fc = 20\ kHz$). 47

Fig. 2-8. Dc side dc-link capacitor ripple current RMS value versus interleaving angle ($f0 = 400\ Hz, fc = 20\ kHz$), (a) PF=1, (b) PF=0. 49

Fig. 2-9. (a) LISN used in DO-160 standards, (b) CM equivalent circuit. 50

Fig. 2-10. Flow chart to determine the noise peak frequency. 52

Fig. 2-11. Calculated corner frequency versus switching frequency, (a) single stage LC filter, and (b) two stage LC filter. 54

Fig. 2-12. Design results of ac side CM filter corner frequency versus switching frequency, (a) single stage LC filter, and (b) two stage LC filter applied. 54

Fig. 2-13. EMI filter corner frequency versus interleaving angle ($fs = 70\ kHz$), (a) CM filter, (b) DM filter. 57

Fig. 2-14. The 3rd, 4th, 5th and 6th carrier harmonics gain versus interleaving angle. 58

Fig. 2-15. Circuit schematic Circuit schematic of two paralleled three-level ANPC inverters. 59

Fig. 2-16. Experiment platform of two paralleled three-level ANPC inverters. 59

Fig. 2-17. Ac side output voltage and current. 61

Fig. 2-18. Spectrum of ac side phase output voltage, (a) tested results, (b) calculation results with developed models. 61

Fig. 2-19. DC side input currents. (a) From top to bottom: output phase current ia, input positive

line current ip, input neutral line current $ineu$, input negative line current in, (b) zoom in figures of (a) showing switching cycle waveforms. 62

Fig. 2-20. Spectrum of dc side positive line current, (a) tested results, (b) calculation results with developed models..... 62

Fig. 2-21. Spectrum of dc side neutral line current, (a) tested results, (b) calculation results with developed models..... 63

Fig. 2-22. Ac side voltage waveforms at M=0.9. From top to bottom: line to line voltage measured at load input, line to line voltage of inverter #1, and phase output current, (a) 0° interleaving angle, (b) 90° interleaving angle..... 64

Fig. 2-23. Spectrum of line voltage at M=0.9, (a) 0° interleaving angle, (b) 90° interleaving angle. 64

Fig. 2-24. Dc side current waveforms at M=0.9 and PF=1. From top to bottom: output phase current ia, input positive line current of inverter #1 $ip1$, input positive line current of inverter #2 $ip2$, and total input positive line current ip, (a) 0° interleaving angle, (b) zoom in figures of (a) showing switching cycle waveforms, (c) 180° interleaving angle, (d) zoom in figures of (c) showing switching cycle waveforms. 66

Fig. 2-25. Spectrum of the positive line current ip at M=0.9 and PF=1, (a) 0° interleaving angle, (b) 180° interleaving angle. 67

Fig. 2-26. Dc side current waveforms at M=0.9 and PF=0. From top to bottom: output phase current ia, input positive line current of inverter #1 $ip1$, input positive line current of inverter #2 $ip2$, and total input positive line current ip, (a) 0° interleaving angle, (b) zoom in figures of (a) showing switching cycle waveforms, (c) 90° interleaving angle, (d) zoom in figures of (c) showing switching cycle waveforms..... 68

Fig. 2-27. Spectrum of the positive line current ip at M=0.9 and PF=0, (a) 0° interleaving angle, (b) 90° interleaving angle..... 69

Fig. 2-28. Measured ac side CM noise at different interleaving angles and their comparison with 0° interleaving angle, (a) 60° interleaving angle, (b) 180° interleaving angle. 70

Fig. 2-29. Measured ac side DM noise at different interleaving angles and their comparison with

0° interleaving angle, (a) 60° interleaving angle, (b) 180° interleaving angle. 71

Fig. 2-30. EMI filter corner frequency versus interleaving angles, (a) CM filter, (b) DM filter.. 72

Fig. 3-1. Paralleled three-level active NPC inverters. 75

Fig. 3-2. Space vectors of three-level inverter. 75

Fig. 3-3. (a) PWM sequences of NTSV, (b) PWM sequences of carrier based PDPWM. 77

Fig. 3-4. (a) Vectors of LMSZVM in sector I, (b) PWM sequences of LMSZVM, (c) PWM sequences of carrier based PODPWM. 79

Fig. 3-5. (a) Vectors of CMR modulation in sector I, (b) PWM sequences of CMR in sector I subsector 2. 80

Fig. 3-6. Comparison of CMR modulation (left) and the proposed modulation (right) in sector I, (a) subsector 2, (b) subsector 3, (c) subsector 4, and (d) subsector 1. 88

Fig. 3-7. ZSCC control block diagram..... 91

Fig. 3-8. Flow chart to combine proposed modulation and control. 92

Fig. 3-9. NP in the three-level inverter. 94

Fig. 3-10. CMV level comparison, (a) with conventional NTSV modulation, (b) with the proposed modulation. 97

Fig. 3-11. Phase output voltage comparison - conventional NTSV modulation, CMR modulation and the proposed modulation. 99

Fig. 3-12. Phase output currents and ZSCC with unequal current reference, $I1\_ref = 4\,A$, $I2\_ref = 8\,A$, (a) with CMR modulation, (b) with proposed modulation. 100

Fig. 3-13. Voltages of the two dc-link capacitors. 101

Fig. 3-14. Three phases output voltage and CMV. 102

Fig. 3-15. Three phases output voltage and CMV. 102

Fig. 3-16. Experiment waveforms when PWM mismatch exists among two paralleled inverters, (a) without control, (b) with proposed modulation and control strategy..... 103

Fig. 3-17. Experiment waveforms of the phase output voltage, (a) ZSCC is small and within the

limit, (b) ZSCC may exceed the limit. 105

Fig. 3-18. Experiment waveforms when two paralleled inverters have unequal current reference, $I1\_ref = 4\,A$, $I2\_ref = 8\,A$, $Lc1 = Lc2 = 250\,uH$, (a) with CMR modulation, (b) with the proposed modulation. 106

Fig. 3-19. Experiment waveforms when two paralleled inverters have unequal output inductance, $I1\_ref = I2\_ref = 6\,A$, $Lc1 = 450\,uH$, $Lc2 = 250\,uH$ (a) with CMR modulation, (b) with proposed modulation. 107

Fig. 4-1. Parallel interleaved three-level active NPC inverters. 109

Fig. 4-2. Phase-neutral voltage and circulating current patterns, (a) $D < 1/2$, (b) $D \geq 1/2$. ... 111

Fig. 4-3. Carrier based PDPWM implementation for a three-level inverter, (a) reference $VX *> 0$, (b) reference $VX *< 0$. 113

Fig. 4-4. Flow chart to determine the optimal zero sequence offset $Vopt$. 119

Fig. 4-5. The optimal zero sequence offset $Vopt$ when modulation index M=0.4, (a) $V0 > 0$, (b) $V0 < 0$, (c) $V0$ has no limit. 120

Fig. 4-6. The optimal zero sequence offset $Vopt$ at different modulation indexes. 121

Fig. 4-7. NP in the three-level NPC inverter. 122

Fig. 4-8. Flowchart for NP voltage balance control with the proposed modulation. 124

Fig. 4-9. The reference (black solid line) and zero sequence offset (red dash line) of different PWM methods at modulation index M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation. 126

Fig. 4-10. Calculated circulating currents with different PWM methods at modulation index M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation. 127

Fig. 4-11. Maximum flux linkage comparison with different modulation methods. 129

Fig. 4-12. Loss and THD comparison of different modulation methods at different modulation indexes, (a) devices conduction loss, (b) devices switching loss, (c) inductor winding loss, (d) inductor core loss, (e) current THD. 130

Fig. 4-13. Waveforms with the proposed modulation. From top to bottom: line voltage and phase

voltage of one inverter, total output current..... 132

Fig. 4-14. Voltages of the two dc-link capacitors. 132

Fig. 4-15. Simulation results of circulating currents with different PWM methods at modulation index M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation. 133

Fig. 4-16. Waveforms with the proposed modulation. From top to bottom: line voltage, phase voltage of inverter 1, total output current. 134

Fig. 4-17. Voltages of the two dc-link capacitors. 135

Fig. 4-18. (a) Output currents (Ia1 and Ia2) of two interleaved inverters and circulating current (Icir) at M=0.8, (b) Zoom in waveforms. 135

Fig. 4-19. (a) Output currents (Ia1 and Ia2) of two interleaved inverters and circulating current (Icir) at M=0.4, (b) Zoom in waveforms. 136

Fig. 4-20. Circulating currents with different PWM methods at M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation. 137

Fig. 4-21. Maximum circulating currents with different modulation methods..... 139

Fig. 4-22. Output current THD with different modulation methods..... 139

Fig. 5-1. Three-level active NPC inverter with the fourth-leg..... 142

Fig. 5-2. Space vectors for a two-level inverter. 142

Fig. 5-4. Space vector arrangement for three main phase legs and the fourth-leg in sector I, (a) subsector 1, (b) subsector 2, (c) subsector 3, (d) subsector 4. 144

Fig. 5-5. Insertion gain amplitude versus frequency..... 145

Fig. 5-6. The three-level active NPC inverter. 146

Fig. 5-7. Inverter output line to line voltage and three phase currents. 147

Fig. 5-8. (a) Three phase output voltage, their summation, and the fourth-leg output voltage, (b) zoom in waveforms. 147

Fig. 5-9. Tested CM noise comparison w/ and w/o the fourth-leg. 148

Fig. 5-10. (a) Fourth-leg connected to three main phases through a CMT, (b) simplified CM

equivalent circuit. 150

Fig. 5-11. (a) Proposed fourth-leg connected filter, (b) simplified CM equivalent circuit. 152

Fig. 5-12. Dc side impedance balancing circuit. 154

Fig. 5-13. Simplified equivalent CM circuit. 154

Fig. 5-14. Improvement of the dc side impedance balancing circuit. 154

Fig. 5-15. Dc-fed motor drive system with input and output EMI filters. 156

Fig. 5-16. CM equivalent circuit with one stage LC filter at both the dc and ac sides. 156

Fig. 5-17. Proposed impedance balancing circuit. 158

Fig. 5-18. (a) CM equivalent circuit. (b) Simplified CM equivalent circuit. 158

Fig. 5-19. (a) LISN CM current conduction path w/o impedance balancing circuit; (b) LISN CM current conduction path w/ impedance balancing circuit; (c) LISN CM current conduction path considering the impedance bridge is not perfectly balanced. 161

Fig. 5-20. CM equivalent circuit considering power stage parasitic capacitance. 162

Fig. 5-21. Simplified CM equivalent circuit. 164

Fig. 5-22. Insertion gain curve. 166

Fig. 5-23. (a) Insertion gain curves at different ac side power stage parasitic capacitances. (b) Insertion gain curves at different dc side power stage parasitic capacitances. 166

Fig. 5-24. Inverter platform and voltage/current waveforms. 167

Fig. 5-25. CM EMI noise with and without the impedance balancing circuit at n=1, (a) ac side, (b) dc side. 169

Fig. 5-26. CM EMI noise with and without the impedance balancing circuit at n=4, (a) ac side, (b) dc side. 171

Fig. 5-27. CM EMI noise with and without the impedance balancing circuit at n=4, (a) ac side, (b) dc side. 172

Fig. 5-28. CM EMI noise comparison: with 500 uH inductor and impedance balancing circuit, and with the increased 3.43 mH CM inductor, (a) ac side. (b) dc side. 174

Fig. 5-29. Loss of the 500 uH CM inductor, auxiliary inductor and the 3.43 mH inductor. 176

Fig. 6-1. CM inductor CM current spectrum. 179

Fig. 6-2. LC filter corner frequency position and damping. 181

Fig. 6-3. (a) Connecting ac and dc midpoint CM filter structure in dc-fed motor drives. (b) Proposed notch filter structure. 182

Fig. 6-4. CM voltage spectrum comparison: conventional SVPWM scheme versus CMR scheme. 184

Fig. 6-5. EMI CM noise spectrum with impedance resonances well damped. 185

Fig. 6-6. Time domain waveform and related CM inductor CM current spectrum with CFB. .. 186

Fig. 6-7. Time domain waveform and related CM inductor CM current spectrum with notch filter. 186

Fig. 6-8. Three-level inverter with dc side EMI filter system. 187

Fig. 6-9. Flux density in a CM inductor. 188

Fig. 6-10. Simplified CM equivalent circuit. 190

Fig. 6-11. (a) Three-level PDPWM carrier waveform, (b) the unit cell contour plot. 191

Fig. 6-12. CM inductor flux density versus modulation index. 194

Fig. 6-13. CM inductor flux density with NTSV modulation. 194

Fig. 6-14. CM inductor flux density versus modulation index for motor with fun load. 195

Fig. 6-15. Phase output voltage of a three-level inverter considering dead time. 197

Fig. 6-16. Impact of dead time on CM inductor maximum flux density. 197

Fig. 6-17. Simplified CM equivalent circuit considering NP voltage variation. 200

Fig. 6-18. Impact of NP voltage variation on CM inductor maximum flux density. 205

Fig. 6-19. A typical CM impedance of the studied three-level inverter system. 206

Fig. 6-20. Relative position of the CM impedance resonance frequency and switching frequency, (a) $fres > fsw$, (b) $fres < fsw$. 207

Fig. 6-21. Impact of CM inductance on CM inductor maximum flux density. 208

Fig. 6-22. Impact of CM inductance on CM inductor maximum flux density when switching frequency is 20 kHz. 209

Fig. 6-23. Improved CM filter design procedure. 211

Fig. 6-24. CM current of the CM inductor at different modulation index, (a) M=0.7, (b) M=1. 213

Fig. 6-25. CM current of the CM inductor with different dead time at M=1, (a) dead time is 2% of switching period, (b) dead time is 10% of switching period. 213

Fig. 6-26. CM current of the CM inductor with different dead time at M=0.4, (a) dead time is 2% of switching period, (b) dead time is 10% of switching period. 213

Fig. 6-27. Voltages of the two dc-link capacitors. 214

Fig. 6-28. CM current of the CM inductor with NP voltage variation. 214

Fig. 6-29. CM current of the CM inductor with different CM inductor value when switching frequency is 60 kHz. (a) CM inductor value is 600 uH, (b) CM inductor value is 2.5 mH. 215

Fig. 6-30. CM current of the CM inductor with different CM inductor value when switching frequency is 20 kHz. (a) CM inductor value is 600 uH, (b) CM inductor value is 2.5 mH. 215

Fig. 6-31. Simulation results of the dc side CM noises of the two design cases. 216

Fig. 7-1. Performance of two Si MOSFET candidates at cryogenic temperature. 221

Fig. 7-2. Performance of three SiC MOSFET candidates at cryogenic temperature. 222

Fig. 7-3. Performance of 65V GaN HEMT at cryogenic temperature. 224

Fig. 7-4. Ferrite N87 characteristics under operating point 0.1 T and 100 kHz. 226

Fig. 7-5. Ferrite N87 temperature dependent characteristics under different frequencies. 226

Fig. 7-6. Vitroperm 500F characteristics under operating point 0.5 T and 20 kHz. 227

Fig. 7-7. Vitroperm 500F temperature dependent characteristics under different frequencies. . 227

Fig. 7-8. Ferrite N87 saturation flux density dependence on temperature. 228

Fig. 7-9. Vitroperm 500F saturation flux density dependence on temperature. 229

Fig. 7-10. Ferrite N87 B-H curve dependence on temp. with magnetization curve highlighted.230

Fig. 7-11. Ferrite N87 permeability dependence on temperature at 20 kHz. 230

Fig. 7-12. Vitroperm 500F B-H curve dependence on temp. with magnetization curve highlighted. 230

Fig. 7-13. Vitroperm 500F permeability dependence on temperature at 20 kHz. 231

Fig. 7-14. Wolfspeed 900 V/ 800 A high current power module. 232

Fig. 7-15. On-state resistance versus temperature. 233

Fig. 7-16. Breakdown voltage versus temperature. 233

Fig. 7-17. Switching transient waveforms. 233

Fig. 7-18. Switching loss versus load. 234

Fig. 7-19. A single phase of the three-level ANPC inverter with parasitic inductance. 235

Fig. 7-20. Operation principle of the three-level ANPC inverter. 235

Fig. 7-21. Laminated busbar design for a single phase of three-level ANPC inverter. 236

Fig. 7-22. Measure impedance of the busbar. 237

Fig. 7-23. Function diagram of DSP. 238

Fig. 7-24. Function diagram of FPGA. 238

Fig. 7-25. Housing design of the coupled inductor. 239

Fig. 7-26. Housing design of the CM inductor. 240

Fig. 7-27. Cooling of the inverter system. 241

Fig. 7-28. Inverter system integration. 241

Fig. 7-29. A single phase of the three-level ANPC inverter prototype. 242

Fig. 7-30. Controller hardware. 243

Fig. 7-31. Coupled inductor with 3D printing housing. 243

Fig. 7-32. CM inductor with 3D printing housing. 243

Fig. 7-33. The inverter system. 244
Fig. 7-34. Pulse test – output voltage and current waveforms. 244
Fig. 7-35. Pulse test – switching transient waveforms 245
Fig. 7-36. Continuous power test – output voltage and current waveforms. 245
Fig. 7-37. Phase voltages of two 60° interleaved inverters 246
Fig. 7-38. CM EMI noise comparison with 0° and 60° interleaving angles. 246
Fig. 7-39. Output currents of two paralleled inverters. 246
Fig. 7-40. Power stage cooling concept. 247
Fig. 7-41. Cooling system setup. 248
Fig. 7-42. Voltage and current waveforms. 248

1. Introduction

1.1 Application Background

Electrical power is utilized more and more in transportation applications. In aircraft applications, the trend is more electric aircraft (MEA) in last a few decades. Different from conventional aircraft where several types of energy including mechanical, electrical, hydraulic, and pneumatic energy are used, MEA replaces the major parts driven by nonelectric power with pure electrical systems. This can eliminate the heavy and costly nonelectric components, and thus bring various benefits in efficiency, weight, maintenance costs, reliability, and emissions. The electric power rating keeps increasing as large aircraft is developing towards MEA as shown in Fig. 1-1 [227]. Electrical system in aircraft covers power generation to power distribution, energy storage for emergency power supply or electrical loads. All these are realized through power converters such as inverters, rectifiers, and choppers. Power converters are the key units to process the electrical power. Fig. 1-2 [227] shows an example of an aircraft electric network with industrial power converters. Power converters has also been utilized for propulsion purpose. As envisioned by NASA and Boeing, high power inverters (5 to 20 MW) will be a key enabler for future aircraft based hybrid electric or electric propulsion [1]. One notional diagram of a hybrid system using a combination of a turbine-driven generator and a battery for the energy source is shown in Fig. 1-3 [1], and the notional inverter system boundary is shown in Fig. 1- 4 [1].

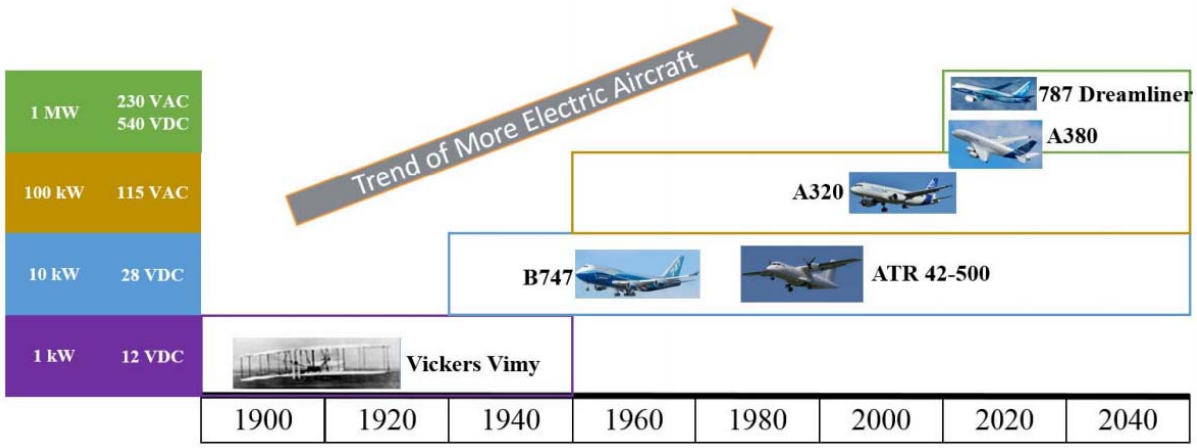


Fig. 1-1. Evolution of MEA [227].

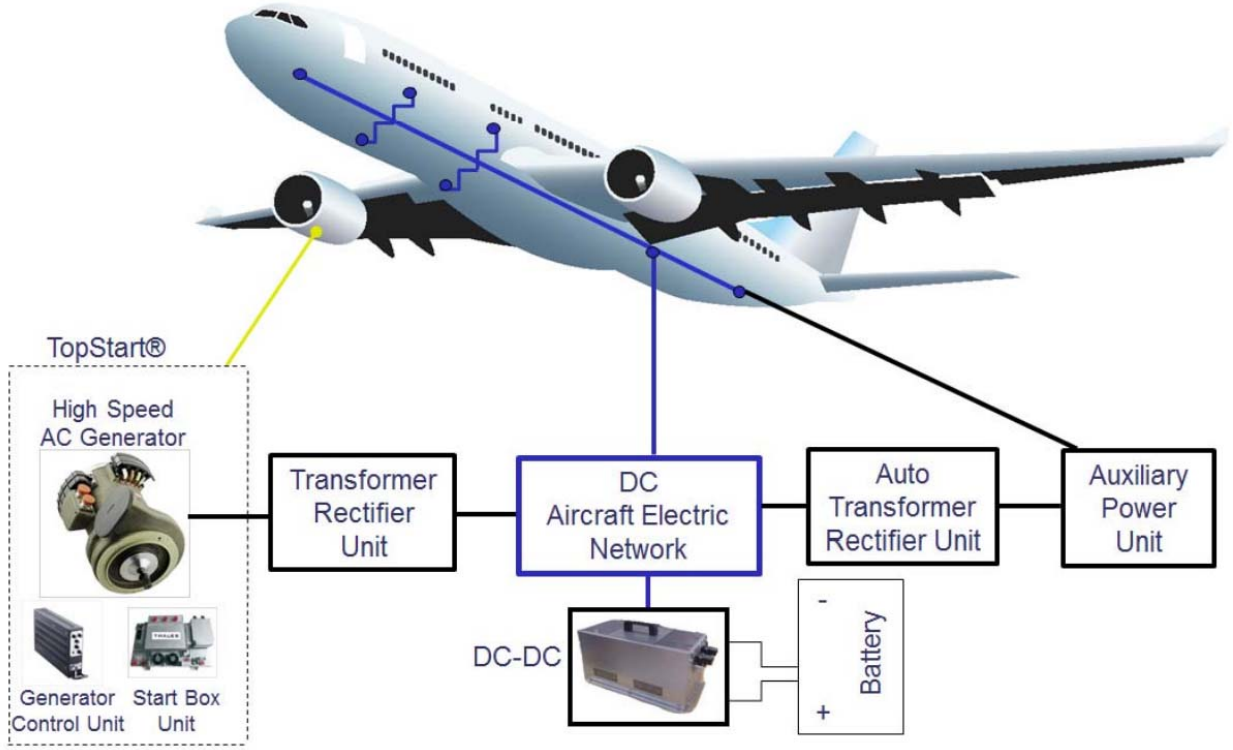


Fig. 1-2. Example of an aircraft electric network with power converters [227].

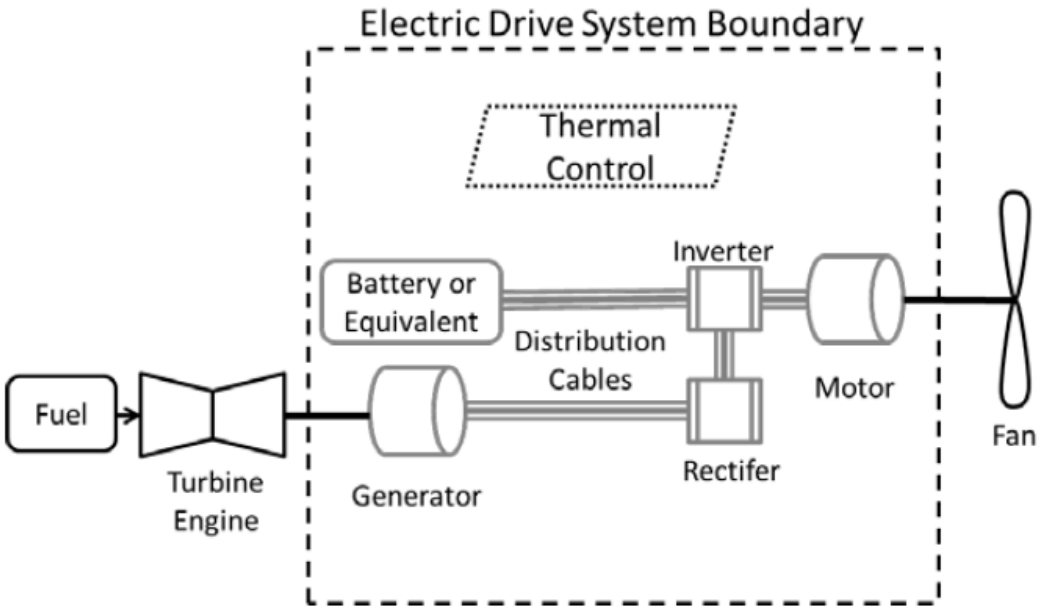


Fig. 1-3. Notional power system configuration [1].

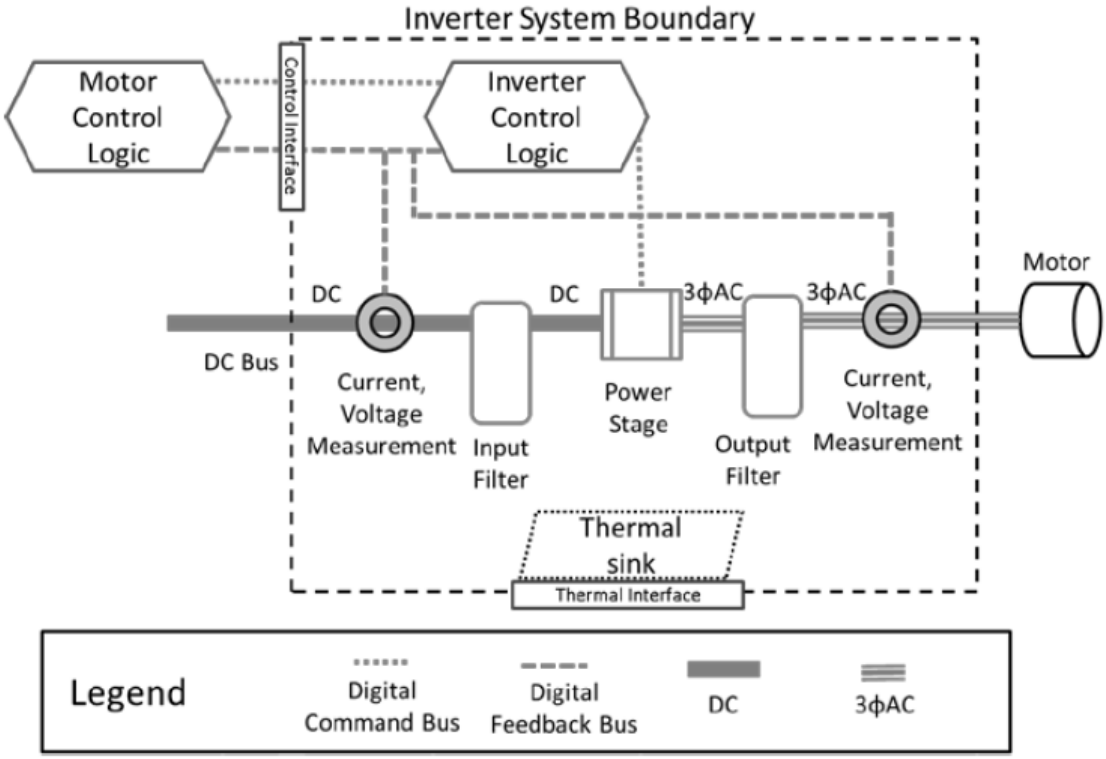


Fig. 1-4. Inverter System boundary and interfaces [1].

For aircraft applications [2-3], power density becomes the key issue because of the limited space and carrier capability. The introduction of fast switching power semiconductor devices has greatly improved the efficiency, size, and weight of the power converters. However, the switching actions of power converters generate harmonics which need to be suppressed to meet power quality (PQ) and electromagnetic compatibility (EMC) requirements. Passive components are inserted into power converter systems to suppress undesired harmonics. Fig. 1-5 shows a typical inverter fed motor drive for aircraft propulsion. Passive filters such as dc and ac side EMI filters, dc-link capacitors, and coupled inductors for paralleled inverters are inserted to the inverter system. The passives largely increase the power electronics size and weight [4-6]. For a motor drive system with EMI filter added to both ac and dc sides, the filters usually take more than 50% of the total system weight [26-27] and become the main barrier for achieving high power density of the inverter fed motor drive in aircraft applications. It is a big challenge for power electronics to design and integrate the power converters and filters together to achieve high power density.

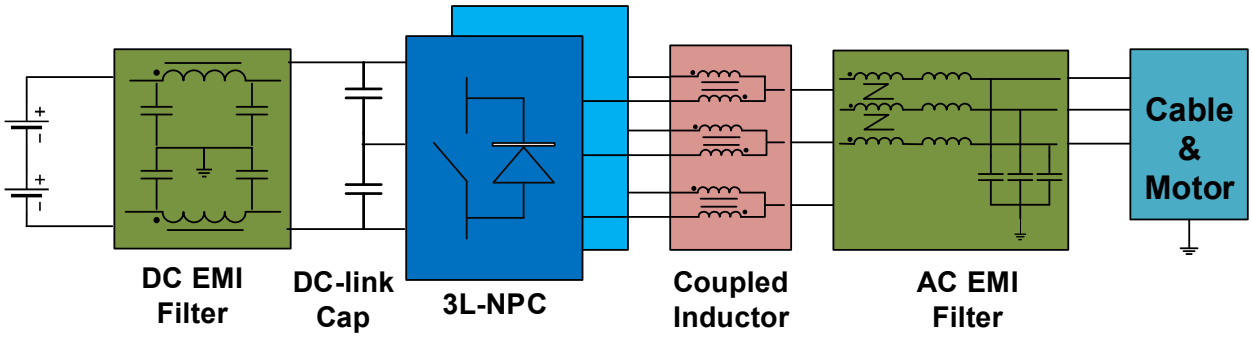


Fig. 1-5. Inverter fed motor drive system for aircraft propulsion.

1.2 Multilevel Topology and Modulation

Multilevel converters have several advantages when compared to two-level converters, and are promising to achieve higher power density [7-11]. First, each switch has smaller voltage stress, and low rated devices with low loss can be used. Second, the switching noise and EMI emission are reduced due to the smaller dv/dt. Third, the output voltage/current has lower harmonics.

Because of the advantages of multilevel converters, this topology has been evolving for decades and numerous variations has been invented [12-18]. In general, there are four major categories for the multilevel converter family as shown in Fig. 1-6. The first and second categories, flying capacitor (FC) and the neutral point clamped (NPC) converter, were invented in early 1980's as shown in Fig. 1-7. The cascade topology as the third category is first reported in 1980's as well as shown in Fig. 1-8. Then, within the last three decades, it has been widely used in high power applications. This evolved in 2000's when the modular multilevel converter (MMC) topology was proposed for even higher voltage and power rating. The fourth category of hybrid topology is a combination and mixture of the other three categories.

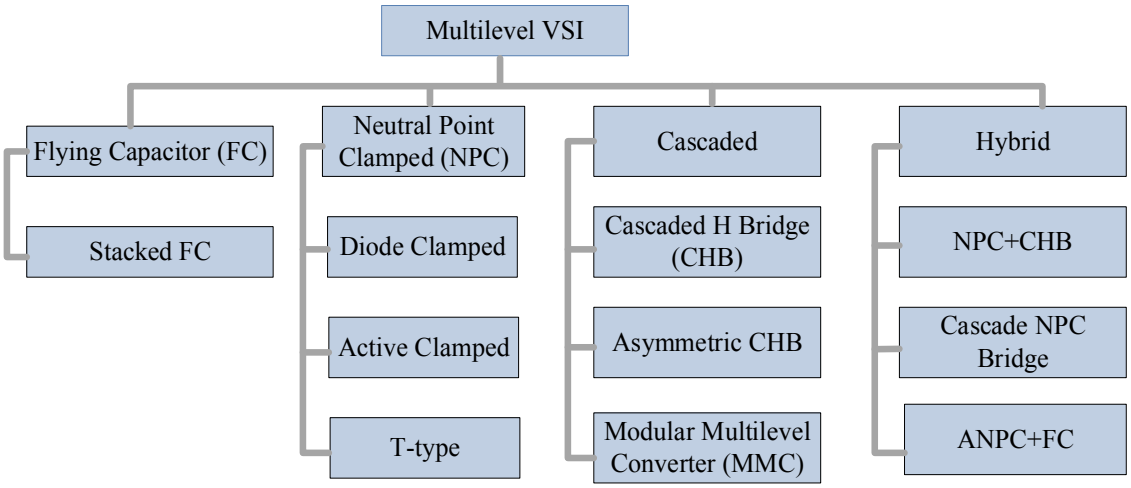
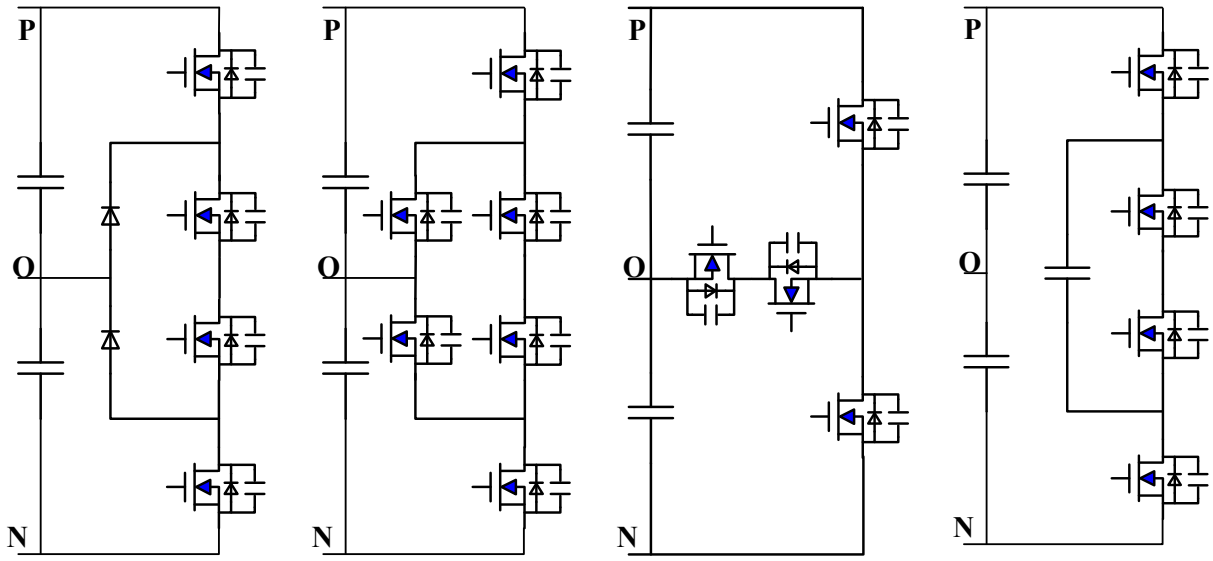
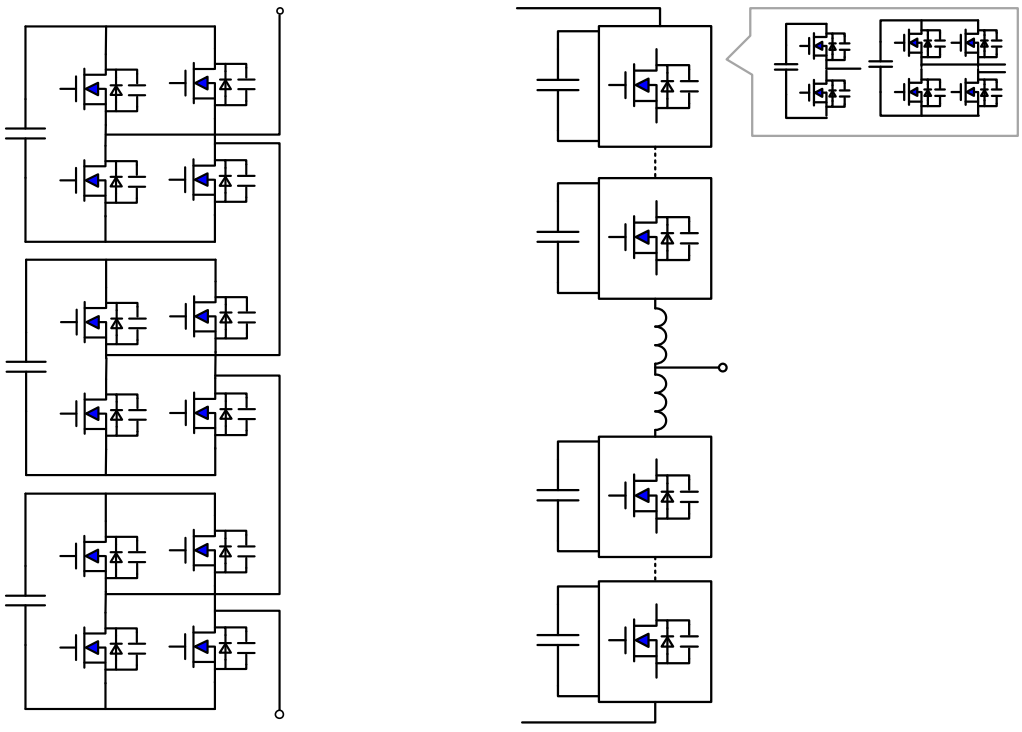


Fig. 1-6. Classification of multilevel converter topologies.



(a) DNPC (b) ANPC (c) T-type (d) Flying Capacitor

Fig. 1-7. Subdivisions of NPC and FC topologies.



(a) CHB (b) MMC

Fig. 1-8. Subdivisions of cascaded topologies.

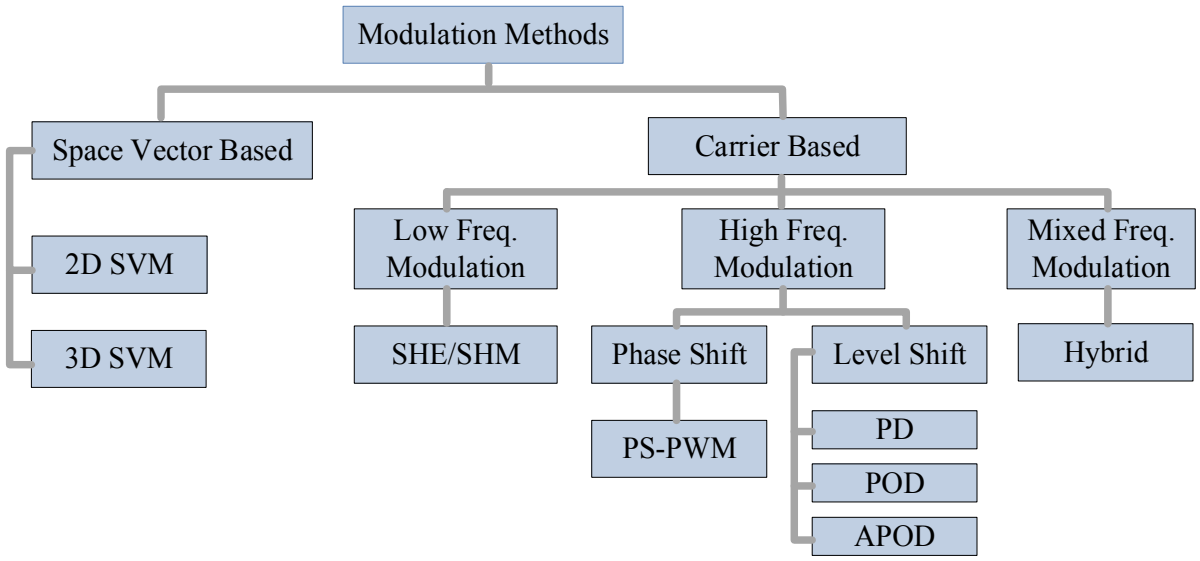


Fig. 1-9. Classification of modulation strategies for multilevel converter.

The modulation is tightly connected with the topology for multilevel converters, and it largely determines the system performance. The categories of the modulation strategies are shown in Fig. 1-9. There are two major groups of modulations. One is the space vector based and the other is carrier based.

Space vector modulation is based on three-phase systems [21-22]. The different switching states for the three-phase multilevel converter can be mapped to a space vector hexagon. The voltage reference can also be mapped to the hexagon, and it can be synthesized in various manners by the space vectors, or the switching status. For a three-level converter, each phase leg has three switching states, and the three-phase system has 27 switching states, which corresponds to 19 space vectors in the hexagon. There are redundant switching states for some vectors, which can be used as freedom to achieve certain control objectives. For a converter with higher level, there will be a large number of space vectors. The higher level provides more redundant switching states for control freedom. But it also has higher computation cost for the reference voltage locating and the

vector selection from a large number of candidates. For this reason, the SVM is not realistic for implementation when the level goes high. But it is extremely suitable for three-level NPC topology since the calculation is not complex.

Low frequency modulation is based on staircase synthesis [23]. Sinusoidal voltage waveform can be represented by stacking multiple two-level square waves. Hence, this modulation is usually applied to cascaded topology with high level number.

Carrier based high frequency modulation is classified to two categories. One is the phase shifted modulation and the other one is level shifted modulation [23-24]. For the phase shift (PS) modulation, the carrier for each cell has a phase shift with other carriers. The specific phase shift angle is 180° divided by the module numbers. All the modules in a phase leg have the same switching pattern. The switching frequency and switching loss for each module is therefore naturally balanced. Another benefit for this modulation is the high equivalent switching frequency at the output, which equals to the switching frequency for each carrier times the cell numbers. The more cells in the phase leg, the higher switching frequency and lower THD at its output. Consequently, the phase shift method is especially suitable for CHB and MMC topology.

Another carrier based method is the level shifted modulation. The carrier waves shift their level with respect to the reference wave. There are three types of level shifting methods: phase disposition (PD), phase opposite disposition (POD), and alternative phase opposite disposition (APOD). For the PD method, all the carriers are in the same phases. For POD method, all the positive carriers are in phase with each other, so does the negative carriers. But the positive and negative carriers are in phase opposite with each other. For APOD method, all the carriers are in phase opposite with each other. The level shift modulation generates different switching frequency and switching pattern for different cell. The inner cells have lower switching frequency and

switching loss than the outer cells. The switching pattern and loss distribution is influenced by the modulation index. From the THD point of view, the level shift modulation has higher THD than the phase shift modulation. The THD comparison for all the carrier based high frequency modulation gives the following sequence for THD from low to high: PS<PD<APOD<POD. The level shift method is not as advantageous as the phase shift method for the cascade topology. But it is often used on the NPC topology since it has unbalanced loss and switching pattern for each device. Each carrier modulates one switch in the phase leg. It is a simple way to modulate one NPC phase leg compared with SVM method.

The mixed frequency modulation is the mixture of low frequency and high frequency modulation [25]. The concept is to use different switching frequencies for different cells in the system according to their voltage ratings. Therefore, it is suitable for hybrid multilevel topologies.

1.3 EMI Noise and EMI Filters

The generation of EMI noise is an inherent problem of power converters. During the modulation and switching, other than the energy generated at needed frequency, different harmonics will also be generated at different frequencies that can interfere with other equipment through the physical connections and become conducted EMI noise. Fig. 1-10 shows the noise propagation in a power inverter system. The power inverter (DUT) is used to process the energy from source to load. The source could be a dc power supply, dc voltage bus or an active front end, and the load could be a motor or grid, or RL load. The line impedance stabilization network (LISN) is required to measure and compare the EMI noise per all conducted emissions standards. To analyze the EMI noise and design EMI filters, the conducted emissions can be separated into two types: common-mode (CM) and differential mode (DM). The CM noise flows in the same direction and then returns through a

common ground. The DM noise flows between the power ports of the converters.

In aircraft applications, the EMI noise can be harmful to other electronics systems on the aircraft such as the communication, navigation and surveillance systems. EMI emissions is limited by specified regulations to protect these systems. Fig. 1-11 shows the dc and ac side EMI limits defined in DO-160 standards for different categories of equipment.

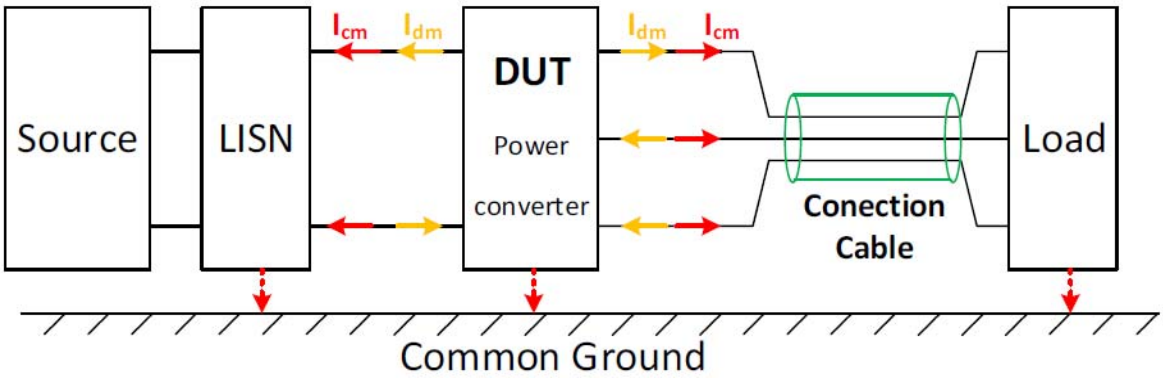


Fig. 1-10. EMI noise propagation path in a power inverter system.

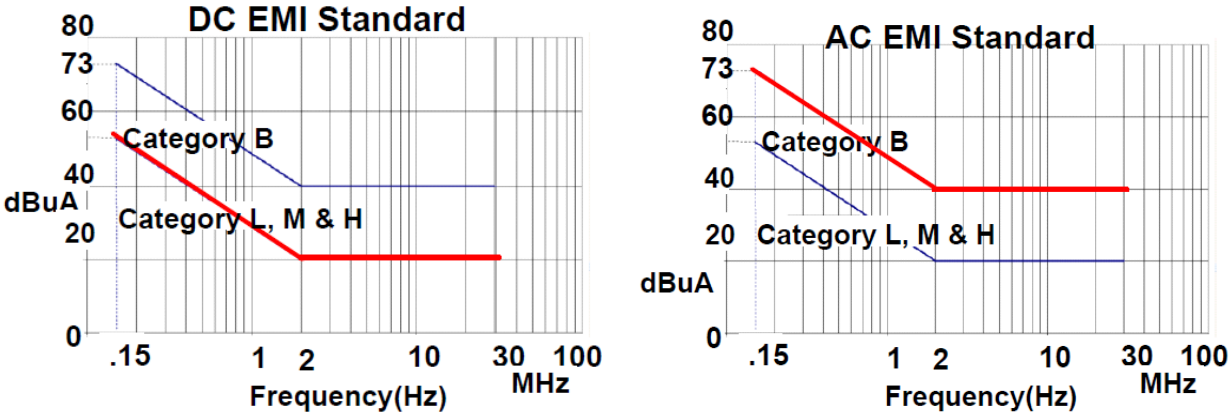


Fig. 1-11. EMI standards in DO-160.

EMI filters are usually added to the inverter system to suppress the EMI noise and thus to meet EMI standards. Typical EMI filters have one or several stages of inductors and capacitors to create the impedance mismatch between the power converter and load/source to block or bypass EMI noise. In conventional EMI filter design, the CM filter and DM filter are designed separately according to the CM and DM bare noise [28]. Typical LC filters are selected. Assuming ideal inductors and capacitors are used without influence from parasitic components, the attenuation performance of one stage LC filter features a slope of 40 dB/dec. The bare noise of either CM or DM needs to be measured and compared with standard at first. The part of noise higher than the EMI standards is the part of noise requiring attenuation. Based on the required attenuation, LC filter corner frequency can be determined.

1.4 Literature Review

1.4.1 Space Vector Selection for Three-Level Inverter

For the three-level inverter, each phase leg is equivalent to a 1 pole triple-throw switch that connects to the positive, negative or neutral dc bus. As shown in Fig. 1-12 [32], there are a total of 27 switching states, corresponding to 19 space vectors. Among them, there are six long vectors, six medium vectors, six small vectors and one zero vector. The small and zero vectors have redundant switching states. For the space vector modulation method, the selection of the redundant switching states is the key to achieve different control objectives such as the neutral point (NP) voltage balance [29-34], switching loss reduction [35-36], or common-mode noise reduction [37-42].

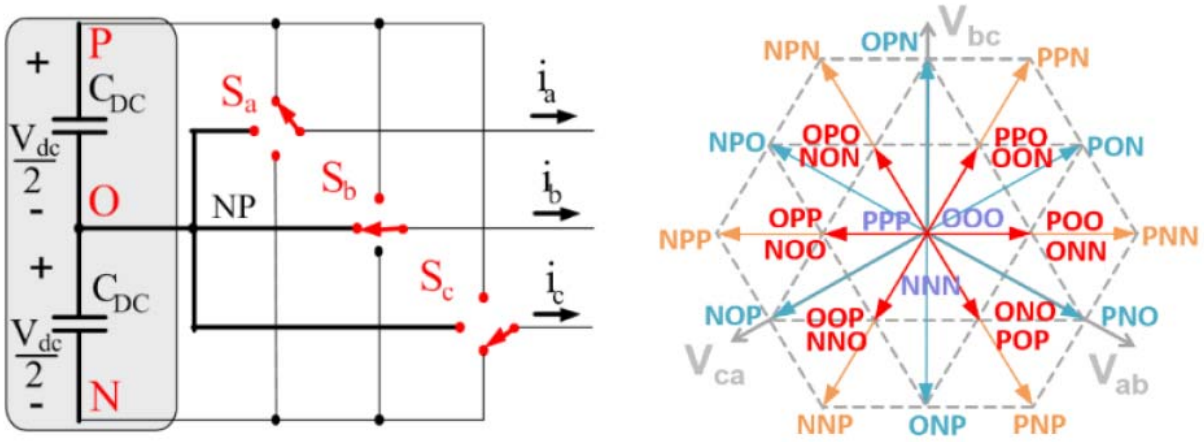


Fig. 1-12. Circuit and space vector diagram for three-level NPC inverter [32].

The principle to achieve the three control objectives by selecting the redundant switching states in three-level modulation is illustrated as follows:

(1) Neutral point voltage balance

For the neutral point clamped (NPC) converter, the dc link is separated by several capacitors, each of which provides one output voltage level. For the three-level NPC converter, the two capacitor voltages must be balanced. Otherwise, the output voltage is distorted and harmonics are increased. The NP balance can be achieved by modulation method. The four types of vectors have different influence on neutral point voltage. By defining the neutral point voltage imbalance as the difference between the bottom and top cell capacitor voltage $\Delta V = V_{ON} - V_{PO}$, the influence of different vectors can be analyzed as shown in Fig. 1-13.

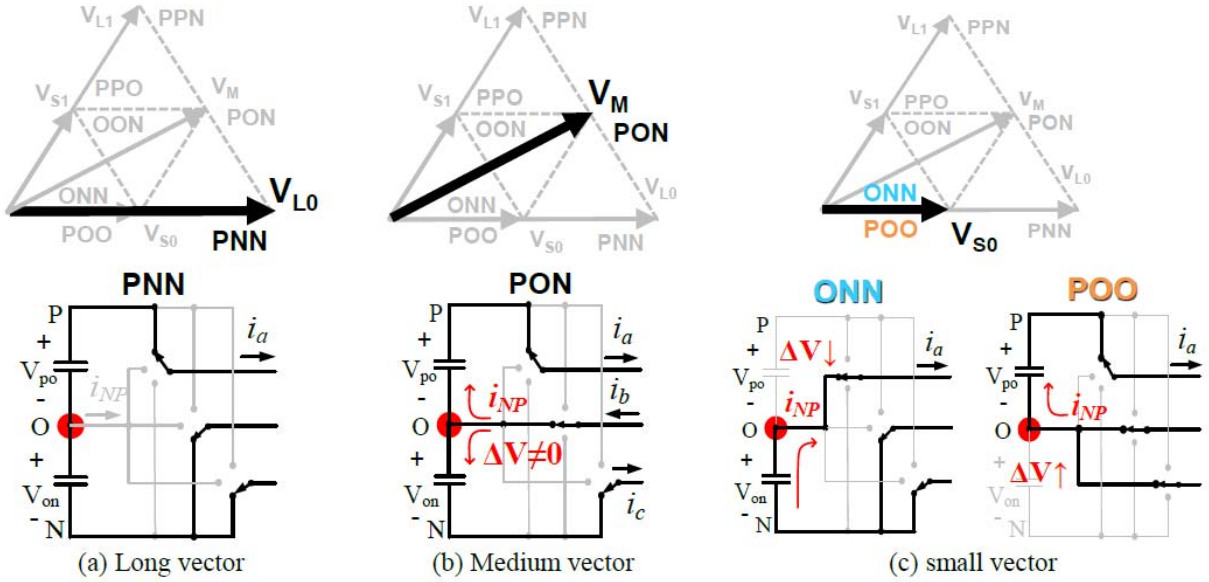


Fig. 1-13. Circuit diagram for vectors and the influence on NP voltage [32].

The analysis takes the first sector as an example. For the long vectors in Fig. 1-13(a), both the top and bottom capacitors are connected in the circuit. There is no neutral current so the two capacitors are charged or discharged by the same current. Consequently, the long vectors do not create any neutral point voltage imbalance. For the medium vector in Fig. 1-13(b), the top and bottom capacitors are connected in the circuit as well. However, there is neutral current in the circuit, and the two dc capacitors are charged or discharged by different current. The medium vectors create imbalance and are the source for the neutral point voltage variation. For the small vectors in Fig. 1-13(c), the two switching states for the small vector connect different dc-link capacitors in the circuit but with the same charging or discharging phase current. If phase current is more than zero, vector ONN reduces V_{ON} and increases ΔV while POO reduces V_{PO} and decreases ΔV. If the phase current is less than zero, the result is just the opposite. Hence, the two switching states for one small vector have an opposite influence on the neutral point voltage and

this is the basis to balance the neutral point voltage.

There are three approaches to select the small vectors for NP balance. The passive balancing method alternately uses the two switching states in a pair in each switching cycle. Since the influence of the two states are opposite, the neutral point voltage can be balanced naturally. This method does not need to sense the neutral point voltage and phase current. Also it does not cause extra switching events and related loss in the switching cycle. But the balancing result largely relies on the power factor. Also, it can only work under a balanced three-phase system and the balancing result is poor under system dynamics.

The active balance scheme uses both switching states for the small vector in each switching cycle. The control objective is to achieve a zero neutral point charge in one switching cycle so that ΔV returns to the initial value after the switching cycle. For each small vector, the two switching states are used with different duty cycle to achieve zero NP charge. The charge is calculated by sensing the phase current and knowing the duty cycle of each vector. The active scheme has good balancing result within one switching cycle. However, it uses both two switching states for each small vector in the switching cycle. The transition between the two switching states inevitably introduces extra switching events.

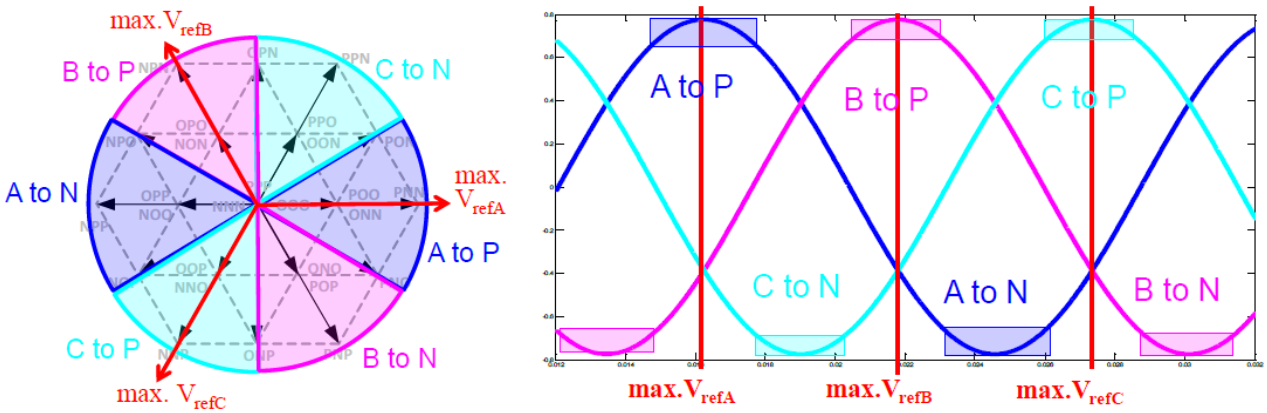
Compared with the active balance scheme which uses both switching states and tries to balance NP voltage in every switching cycle, the hysteresis balance scheme balances the NP voltage in two or more switching cycles by using only one switching state for the small vector in each switching cycle. The selected small vector moves the neutral point voltage to the opposite direction of the imbalance. In each switching cycle, the neutral point voltage ΔV is sensed together with the three-phase current. The switching state for the small vector is selected based on ΔV and the phase current direction. If ΔV is positive at the beginning of the switching cycle, the switching state is

selected to decrease the NP voltage. In the next switching cycle, if ΔV is reduced to a negative value, then the other switching state for the same small vector is used to increase NP voltage. If one cycle is not enough to control the NP voltage, this method will use the same switching state continuously for several cycles to control the NP voltage. This method is robust to the system dynamics because it has neutral voltage feedback. The NP balancing result is not as good as that of the active scheme since the neutral point voltage is controlled back and forth around zero. The NP voltage also has a strong harmonic component at half of the switching frequency. But this method can still achieve NP balance within several switching cycles. It has the benefit of having the least switching events because it only uses one switching state in each switching cycle.

(2) Switching loss reduction

The basic principle for this control objective is to clamp the phase leg for a certain period of time, so that the phase leg with the largest current can avoid switching. Thus, switching loss can be reduced. There are some variations on the clamping methods, and they are similar to the DPWM for the two-level converter. The phase leg can be clamped for 60° or 30° in a line cycle. Each leg can be clamped to positive, negative or neutral dc bus.

The most commonly used DPWM method for both two-level and three-level converter is the 60° DPWM that clamps each phase leg for 60° around its voltage reference peak. This method can avoid the phase leg switching in the vicinity of its maximum voltage reference. The space vector hexagon division for this method is shown in Fig. 1-14(a). The hexagon is equally divided into six sectors. Each sector is center aligned to the peak or valley of the phase leg reference voltage as shown in Fig. 1-14(b). The shaded areas on the voltage reference waveform are the clamped period. By properly selecting the switching states for the small vector, each phase leg is clamped to P or N in consecutive 60° area.



(a) Space vector hexagon division (b) Clamped voltage reference area

Fig. 1-14. Space vector hexagon and voltage reference for 60° DPWM.

(3) Common-mode voltage reduction

Besides the NP voltage ripple and switching loss, the common mode voltage can also be reduced or even eliminated by the redundant small vector selection. For the three-phase system, the CM voltage is defined as one third of the summation of the three phase output voltage. The CM voltage generated by the different types of vectors can be calculated. The long vectors generate $\pm 1/6\ V_{dc}$ CM voltage. The medium vectors generate no CM voltage. For the small vectors, the two switching states generate different CM voltage. They give either $\pm 1/6\ V_{dc}$ or $\pm 1/3\ V_{dc}$ CM voltage. For the zero vectors, they generate either $\pm 1/2\ V_{dc}$ or zero CM voltage.

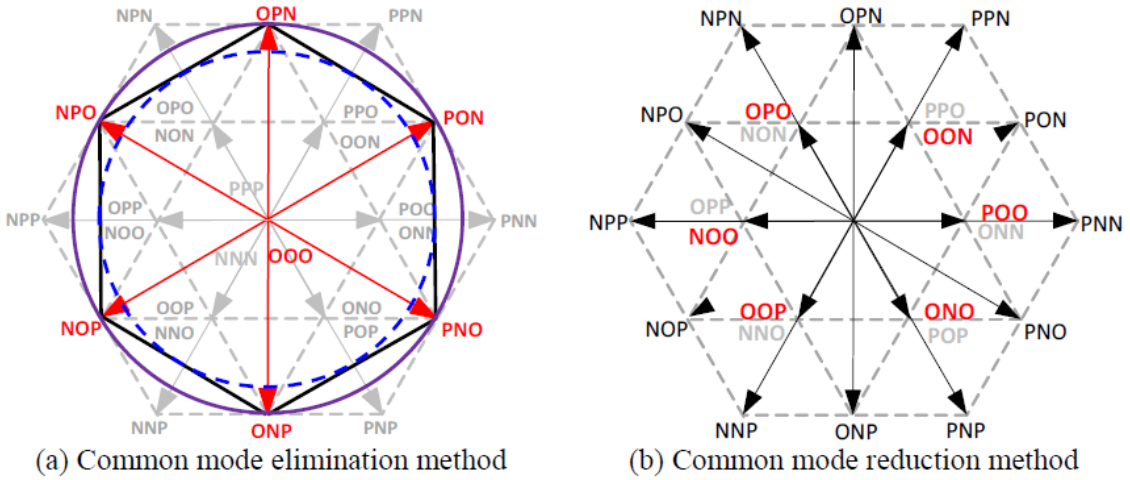


Fig. 1-15. Two methods for CM voltage reduction.

There are two modulations to reduce CM voltage. The CM elimination method (CME) can totally avoid CM noise generated by the modulation. It only uses the medium vectors and the zero vector OOO since they do not generate any CM voltage. The vector diagram for this method is shown in Fig. 1-15 (a). By using only the medium and zero vectors, this method can totally eliminate the CM voltage. However, the dc link voltage utilization rate is reduced. The radius for the reference vector is reduced from 1 to$\sqrt{3}/2$. This method also loses the benefit of the nearest three vectors. Each phase leg has more switching events and higher switching loss associated with the switching. Additionally, due to the influence of the dead-time, the CM noise cannot be totally eliminated. Another method is the CM reduction method (CMR). This method uses the nearest three vectors to synthesize the reference, and the switching state of small vectors with smaller CM voltage $\pm 1/6\, V_{dc}$ is selected as shown in Fig. 1-15(b). This method reduces the CM voltage amplitude by half and also has the benefit of reduced switching loss compared to continuous PWM method.

1.4.2 Harmonic Reduction through Parallel Interleaving

The use of paralleled three-phase PWM converters dates back to the late 1980s in motor drive and uninterruptable power supply (UPS) applications [43-44]. By phase shifting the carriers of the paralleled converters, i.e. interleaving, the total voltage and current ripple at the ac terminal due to PWM switching can be reduced. As a result, the size and weight of passive components such as the dc-link capacitors and EMI filters can be reduced.

The time domain analysis shows that ripple current cancellation effect exists when interleaving is applied [45-46]. However, the analysis in time domain lacks insight. It is difficult to investigate the impact of interleaving angle on harmonics reduction, especially if there are more than two converters in the paralleling system. As a result, conventional symmetric interleaving is used, in which the carrier waves of each converter are phase shifted by 1/N switching cycle for N paralleled converters.

Frequency domain analysis is more effective for understanding the harmonics characteristics. Harmonics generated by PWM can be determined using double Fourier integral analysis. Much study has been conducted on the harmonics analysis of two-level and three-level converters [47-52]. Frequency domain analysis has also been used to investigate the impact of interleaving on paralleled converter systems [53-65]. The output harmonics cancellation effect of interleaving N converters has been theoretically confirmed. Impact of interleaving on harmonic voltages and currents on the ac and dc side of paralleled converters are analyzed. The impact of the non-conventional asymmetric interleaving is also discussed.

1.4.3 Circulating Current Reduction in Paralleled Inverters

Circulating current issue exists for paralleled three phase converters due to the hardware and control difference between paralleled converters. The circulating current can be classified into two groups by frequency. One is the low frequency components related to fundamental frequency, which can be limited by control. The other one is the high frequency components related to switching frequency, which is out of the control bandwidth and can only be limited by passive components.

Much research has been conducted on circulating current suppression, both in control and passive components. The conventional method is to use separate power supplies [44], [66-68], or isolated transformer [45], [69-72]. Adding additional power supplies or the line-frequency transformer make the paralleling converter system bulky and expensive. Another method of passive components is to use coupled inductor and CM inductor to provide high impedance in the loop to suppress circulating current [73-77]. However, this method is not effective to suppress the low frequency circulating current.

Control methods need to be used for suppressing the low frequency circulating current [78-91]. [78-81] mainly focus on the circulating current on the d-q axis, which is also called load sharing control. The control of zero sequence circulating current (ZSCC) on the zero axis are discussed in [82-85] for two-level inverters. Ye et al. [83] proposed a method to control the low frequency ZSCC by adjusting the dwell time of zero space vectors. Furthering this study, the dead-beat control was proposed to improve the performance of ZSCC control [88]. With a similar concept, the ZSCC is controlled by adjusting the injected zero sequence signal to the modulation for the carrier based pulse width modulation (PWM) [89-92]. Nonlinear control methods were also proposed to reduce ZSCC [93-94], however, this algorithm was too complicated to be implemented

in practical applications.

The method to control the low frequency ZSCC is to adjust the averaged zero-sequence voltage (AZSV) generated by the paralleled inverters. This method is also applied to ZSCC suppression in paralleled three-level inverters. In [95], the ZSCC of paralleled T-type inverters is modeled, a proportional-integral (PI) controller and a modified LCL filter are applied to reduce low frequency and high frequency ZSCCs, respectively. In [96], ZSCC suppression of paralleled three-level T-type inverters with three-limb inductors was discussed. The periodical ZSCC jumps was observed and eliminated, and the grid voltage feedforward control is adopted to eliminate starting current jumps. In [97], the deadbeat control is also applied to three-level inverters to achieve better control performance when the paralleled inverters have different parameters. In [98], a large, medium, small and zero vector modulation (LMSZVM) method is proposed which reduce the ZSCC and the common-mode voltage (CMV) simultaneously. This modulation method is equivalent to the phase opposition disposition PWM (PODPWM) for carrier based PWM [99]-[100].

1.4.4 EMI Noise Reduction Methods

EMI filters are inserted in power converters to provide enough EMI noise attenuation and thus pass EMI standards. EMI filters usually take more than 50% of the total inverter system size and weight in aircraft motor drive system where both dc and ac side need to pass EMI standards. Generally, two approaches can be considered for EMI filter size and weight reduction. The first approach is to reduce the EMI noise in the power converter system. The second approach is to optimize EMI filter design. In this section, the advanced method for EMI noise reduction are reviewed and briefly illustrated.

(1) Switching frequency selection

Switching frequency is a key design parameter for power converters. Generally, increasing switching frequency will reduce passive components weight and increase switching device power loss. Therefore, for a specific application, there would be an optimal switching frequency. When considering the EMI filter, the relationship between the switching frequency and the filter may not be linear due to the noise spectrum and the standard requirement. Fig. 1-16 shows the required filter corner frequency (a two-stage filter with 80 dB attenuation is assumed) versus the switching frequency based on the DO-160 standards [101]. The non-linear relationship indicates that higher switching frequency does not necessarily lead to higher filter corner frequency. A higher corner frequency is desirable since it indicates a smaller filter. There are some preferred switching frequencies (such as 40 kHz, 140 kHz or above 500 kHz) as can be seen in Fig. 1-16. Some literature [102-103] pointed out that the weight of an inductor is not only determined by the inductor value but also related with the volt-second on the inductor. Switching frequency selection needs to avoid amplifying the volt-second on the CM or DM inductor.

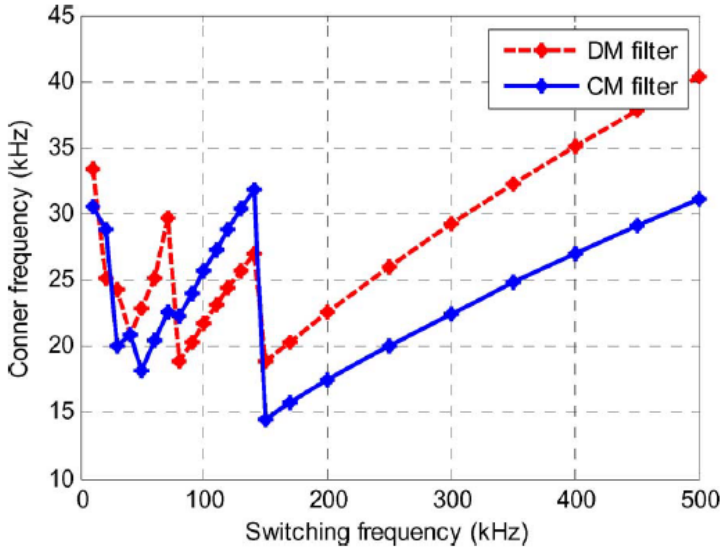


Fig. 1-16. EMI filter corner frequency versus switching frequency [101].

In addition to selecting an optimized fixed switching frequency, random PWM (RPWM) can be used to further reduce EMI noise. The principle of RPWM is to spread the energy concentrated around the harmonics of the switching frequency to a wider frequency range to reduce the EMI noise peak [104-111].

(2) Modulation method

Modulation schemes determine the noise source of the conducted EMI. Many efforts have been made on modulation scheme optimization for CM noise reduction.

For two-level inverters, the main idea is reducing the CM voltage from $Vdc/2$ to $Vdc/6$ through avoiding zero vectors. Among these modulation schemes, the active zero state pulse width modulation (AZSPWM) and near state pulse width modulation (NSPWM) are usually preferred [112] – [115]. AZSPWM is a variation for SVPWM but inverses the aligment of the medium-length duty and reduces the CM voltage peak to be ±Vdc/6. Similarly, NSPWM is a variation for DPWM and reduces both the switching loss and CM voltage, but it could not work with a low modulation index. Fig. 1-17 shows the four typical PWM methods' gate logic and the corresponding CM voltage.

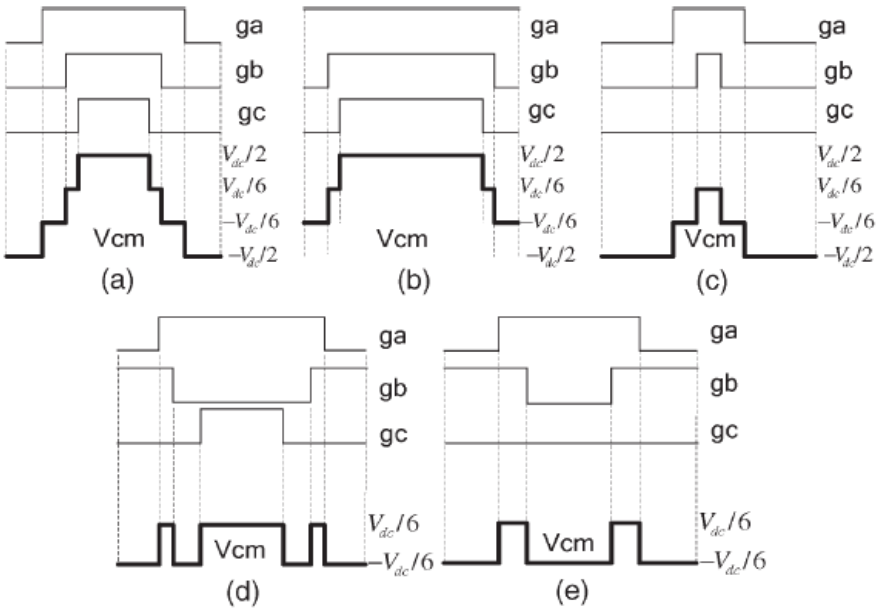


Fig. 1-17. Gate logic and CM voltage for (a) SVPWM, (b) DPWM (clamped to positive bus), (c) DPWM (clamped to negative bus), (d) AZSPWM, (e) NSPWM.

For three-level three phase inverters, the two modulation method to reduce CM voltage and CM noise – CME and CMR methods – are illustrated in section 1.41 [37-42].

(3) Active/hybrid filters

Active/hybrid filter is a promising alternative of the bulky passive filter. Active filters are mainly based on the detection-injection concept where the raw noise, either voltage or current, is sensed using direction detection circuitry, then a reversed noise, either current or voltage, is injected back to ensure the output line current is less noisy. Usually the active filter reduces low frequency EMI noise, and the passive filter reduces high frequency EMI noise. The total size and weight of active filter and passive filters could be much smaller than a conventional passive EMI filter. A considerable amount of research has been conducted on active/hybrid filters in different applications such as dc-dc converters, motor drives and electric vehicles [116-134]. In [120], four

basic circuit configurations for current cancellation were classified and compared. In [121], a generalized analysis of active EMI filter topologies was conducted. The converter insertion loss and stability issues were discussed in [129-131]. Hybrid EMI filters were evaluated and implemented in motor drive systems [122-126]. Digital active filters were applied to a micro-inverter module and a dc/dc converter in [127-128]. DM active filter was used in boost power factor correction ac-dc converters [134].

Fig. 1-18 and Fig. 1-19 show the implementation of CM active filters [117]. In Fig. 1-18, the voltage between the neutral point and the dc bus is sensed using resistors and injected to the dc side through a CM transformer. There is a disadvantage for the CM noise voltage cancellation in high voltage applications. The transformer's primary side inductor cannot be small to avoid large magnetizing current. Then the inductance of the secondary side will be large due to the high turn ratio of the voltage transformer. So the voltage transformer's weight/size will be big.

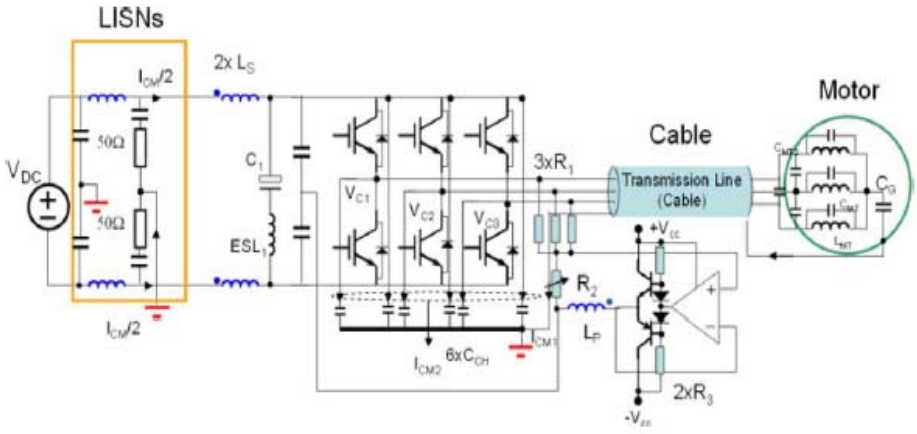


Fig. 1-18. Implementation of feedforward CM noise voltage cancellation [117].

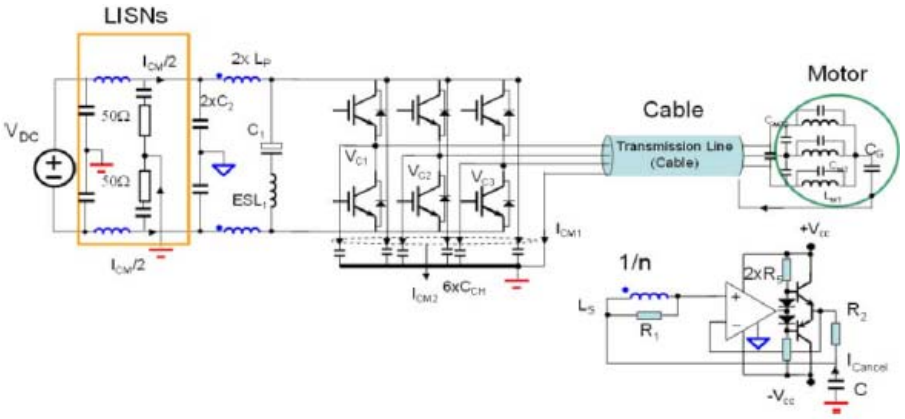


Fig. 1-19. Implementation of feedforward CM noise current cancellation [117].

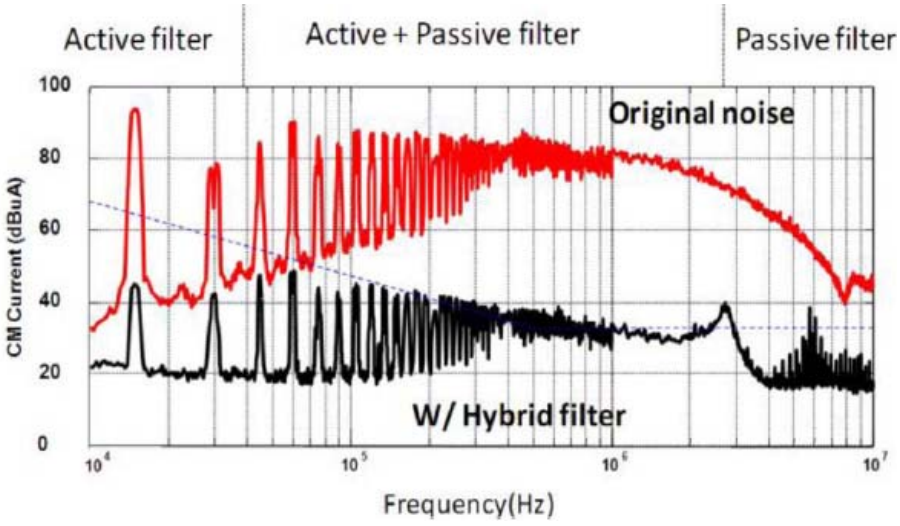


Fig. 1-20. Comparison of the measured CM noise [117].

In Fig. 1-19, a current transformer is used to sense CM noise current on the dc bus. The cancellation current is then injected to the common ground via injection capacitor. The transformer's primary winding has only one turn. Hence, the current transformer's weight and size is much smaller than that of the voltage transformer. Passive filter is usually used together with the active filter to reduce high frequency noise and to reduce the di/dt of the CM current so that active filter can work properly. Fig. 1-20 shows the measured CM noise using hybrid filter with

current feedforward cancellation [117]. Around 50 dB attenuation is achieved by the active filter at the first noise peak.

(4) Special inverter and filter topology

Some special inverter topologies were proposed for CM voltage and CM noise reduction in previous literature such as four phase-leg inverters and balanced inverters [142-151]. The fourth-leg topology was first used by Julian et al. [145] to reduce CMV and CM noise. A fourth-leg and a fourth phase LC filter are inserted into the two-level inverter as shown in Fig. 1-21. The zero vector is not used in the modulation to achieve zero CMV. Compared to two-level inverters, little attention has been paid to the fourth-leg for three-level inverters. An auxiliary leg is added to the NPC inverter to produce the compensating voltage for CMV reduction through a four-winding transformer in [149]. However, an additional dc source and a CM transformer are required. A multi-level fourth-arm circuitry is used and connected to the induction motor neutral point through an isolation capacitor to eliminate the bearing current in NPC inverter based motor drive in [150]. The CMV reduction of four-leg T-type grid-tied inverter is illustrated in [151]. However, the PWM method is carrier based, and the control strategy cannot achieve zero CMV.

Some special filter topologies are proposed for motor drive applications. The CM noise in the dc and ac side of a dc-fed motor drive system are coupled, which makes the filter design more complicated. Adding EMI filter on one side will change the propagation impedance and EMI noise level on both sides. However, on the other hand, it provides the opportunity to use connecting ac and dc filetr topology to supress EMI noise. One method is connecting the ac and dc mid-point. A filter topology which connectes the ac DM capacitor mid-point and the dc link capacitor mid-point in motor drive system was propoaed in [135-138]. The influence of this method on EMI noise reduction is analyzed in [137]. Fig. 1-22 shows the filter topology [137]. This method confines the

CM noise within the converter and supresses both ac and dc side CM noise.

Another method is using impedance balancing technique. In [139], an impedance balancing circuit is presented to reduce CM EMI noise of dc-dc converters by creating a balanced impedance bridge around the CM voltage source of the converter. This method is then applied to single-phase boost PFC converters [140]. The impedance balancing circuit was first introduced to dc-fed motor drive system in [141]. An impedance bridge is formed by adding a Lr-Rr-Cr branch from the inverter ac output to dc input as shown in Fig. 1-23 [141]. In the EMI frequency range, the impedance of Rr, Cr is much smaller than Lr, impedance Cx is much smaller than Lcm, motor CM impedance is modeled as capacitance $C1$, and device parasitic impedance is modeled as $C2$, so the CM current in LISN branch is zero if equation $Lr/Lcm = C1/C2$ is met. The impedance balancing circuit can effectively reduce CM noise in the low EMI frequency range. However, the high frequency CM noise reduction performance is limited due to the impact of parasitics of the components in the impedance balance bridge. Moreover, this topology is only suitable for motor drive system where only dc side needs EMI filters.

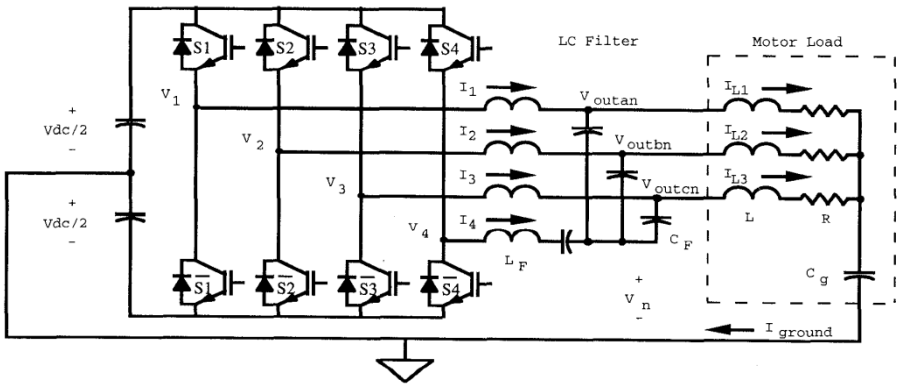


Fig. 1-21. Four leg two-level inverter with second order filter and motor load [145].

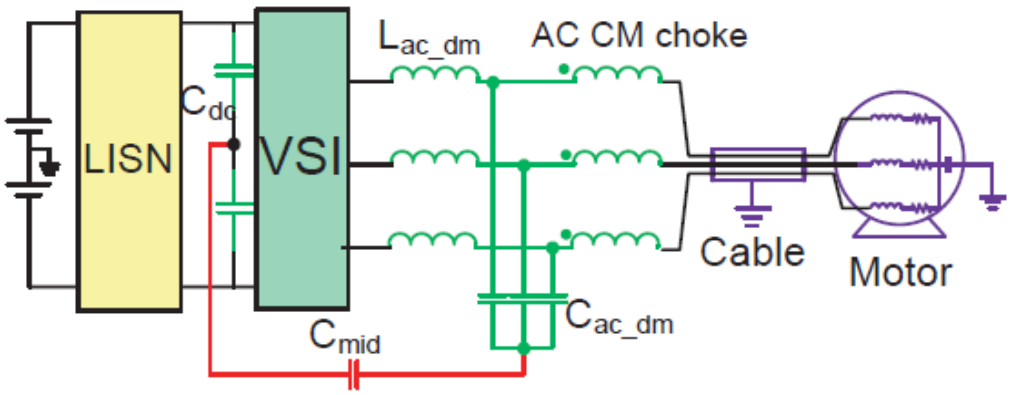


Fig. 1-22. Filter topology - connecting ac and dc mid-points [137].

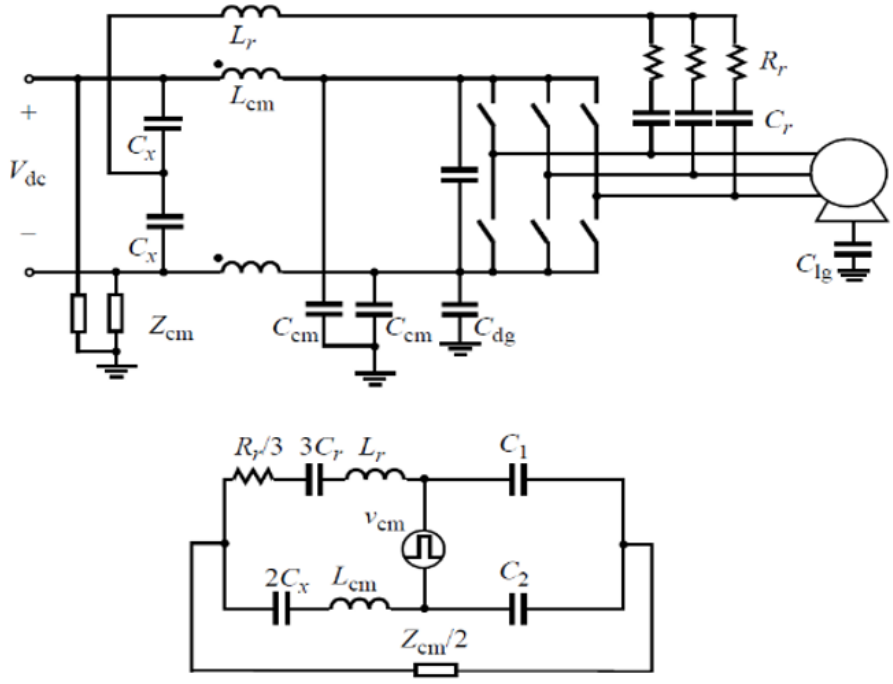


Fig. 1-23. Filter topology - impedance balancing circuit in motor drive system [141].

1.4.5 EMI Filter Modeling and Design Optimization

As discussed in last section, the second approach for EMI filter size and weight reduction is filter design optimization. In this section, the EMI filter modeling and design optimization are reviewed and briefly illustrated.

Design of EMI filters for power converters has been traditionally done using trial and error methods which cannot ensure the optimal EMI filter design. However, over the last few decades, several modeling methodologies have been published for extracting EMI models of power converters.

For the noise source modeling, the subintervals of switching actions were considered in [152], and [155] simplified the switching devices as equivalent voltage and current sources. [152] further approximated the source impedance using impedance masking concept. The unterminated behavior model was applied in [153-154]. The impact of dv/dt switching speed on EMI were investigated theoretically and experimentally in IGBT, SiC, GaN converters [156-160]. Generally, this impact is above tens of MHz, mainly in radiated noise range.

For the passive EMI filters modeling, several efforts have been made in literature from modeling of the inductor's parasitic capacitance [161-165], impedance characteristics and equivalent circuit considering the frequency-dependent behavior [161, 166-172] and current-dependent flux density nonlinearity [169, 173-177] of magnetic cores, and thermal resistance [178-179]. Inductive coupling and capacitive coupling of passive components in a multi-components filter are considered as key factors degrading filter performance. However, theoretical modeling is difficult due to the invisible and multi-branch coupling path strongly related to component geometry and dimensions. The finite element method (FEM), method of moments (MOM), finite difference time domain (FDTD), and partial element equivalent circuit (PEEC) based solutions are

presented to predict coupling impedance [180-182].

Parasitic reduction techniques and winding scheme techniques to improve filter high frequency attenuation performance were explored. In [183-187], equivalent parallel capacitance cancellation for CM choke and DM inductor was illustrated. In [188-189], PCB trace length was controlled to form a negative coupling inductance to offset the ESL of capacitor branch. In [186, 190], inductive coupling mitigation for two stage DM capacitors by adding an extra opposite winding on a film capacitor were presented. The winding schemes' impact on parasitic capacitance of inductor and its optimization were reported in [163-165, 191-197].

EMI filter design considerations for dc-fed motor drive system were illustrated in [198-204]. Design optimization on CM and DM inductor physical implementation were also investigated where all design variables such as winding turns, wire size, core material and geometry, flux density, and temperature rise are controllable to find the optimized result in terms of efficiency, size, weight and cost [204-215].

1.5 Research Challenges

From literature review results, significant effort has been made on increasing inverter system power density through modulation and control methods, paralleling and interleaving topology, EMI modeling and filter design optimization. However, there are still a lot of unknown knowledge and unsolved issues and for design of high power density three-level inverter fed motor drive. The main challenges are summarized as follows.

(1) Understanding the harmonic characteristics in power inverters is critical for passives design and reduction. However, there is still a lack of analytical models to analyze different harmonics (dc and ac side harmonics, EMI harmonics) in three-level NPC inverters with space vector

modulation. How interleaving angle impacts these harmonics and how to optimize interleaving angle to reduce these harmonics for three-level inverters are also unknown.

(2) Paralleling and interleaving two-level converters and associated circulating current suppression methods are well studied. However, knowledge regarding paralleling and interleaving three-level inverters has not been fully explored. Modulation methods to achieve multiple control objectives in addition to circulating current control for paralleled three-level inverter have not been investigated. Coupled inductor flux minimization and design optimization for interleaved three-level inverters are not studied.

(3) EMI noise reduction methods for three-level inverter and for motor drive systems that requires both dc input side and ac output side EMI filters has not been fully explored. Comprehensive CM inductor flux modeling, analysis and filter design optimization for three-level inverter has not been conducted.

Addressing these issues, this dissertation will propose new method and provide new knowledge on modulation and control, paralleling and interleaving strategy, EMI noise reduction and filter design optimization for three-level inverters, aiming at increasing the power density of three-level inverter for aircraft application.

1.6 Dissertation Organization

The dissertation is organized as follows:

Chapter 1 introduces the application backgrounds of this research and reviews the research activities in the corresponding areas including modulation methods for three-level inverters, harmonics and circulating current reduction in paralleled and interleaved inverters, EMI noise

reduction and EMI filter modeling and design optimization.

Chapter 2 presents the modeling and reduction of harmonics in paralleled three-level inverters. Analytical harmonic calculation models for three-level NPC inverter with space vector modulation are developed. The optimal interleaving angle ranges to reduce the ac and dc side harmonics and EMI harmonics considering multiple impact factors for parallel interleaved three-level inverters are thoroughly studied.

Chapter 3 investigates circulating current control and reduction in paralleled three-level inverters. A space vector modulation which reduces the circulating current, common-mode voltage, and switching loss simultaneously for paralleled three-level inverters is proposed.

Chapter 4 analyzes the flux linkage of coupled inductor in parallel interleaved three-level inverters. Carrier based PWM method to achieve minimum flux linkage for the coupled inductor is proposed.

Chapter 5 studies the inverter and filter topology for CM EMI noise reduction for a three-level inverter. First, the fourth-leg inverter topology is applied to three-level inverter to reduce CM noise. Second, an impedance balancing circuit filter topology is proposed to reduce both the dc and ac side CM noise for an inverter-fed motor drive.

Chapter 6 presents the modeling and design optimization of CM inductor in a three-level inverter. First, the spectrum concept is introduced for CM inductor analysis and optimization. Second, CM inductor flux density model considering multiple impact factors is developed, and an improved filter design procedure is proposed to CM inductor over-design and under-design.

Chapter 7 presents the design and demonstration of a MW three-level inverter with cryogenic cooling. Power device and magnetics characterization at cryogenic temperature, inverter system

design to fit cryogenic cooling and achieve high power density, MW inverter prototype and cryogenic cooling system building and testing results are demonstrated.

Chapter 8 presents the conclusion and future work.

2. Harmonic Modeling and Interleaving Angle Optimization to Reduce Harmonics for Paralleled Three-Level Inverters

Compared with two-level converters, three-level converters have reduced voltage stress for devices, lower output current harmonics, and reduced EMI noise. Paralleling three-level converters is gaining popularity as it allows higher power rating or an increase in system reliability. In addition, by phase-shifting the carriers of the paralleled converters, i.e. interleaving, the switching frequency harmonics can be reduced, as a result, the size and weight of passive components such as the dc-link capacitors and EMI filters can be reduced. This chapter presents the modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level NPC inverters with SVM. The analytical models for harmonics calculation of three-level NPC inverter with SVM are developed. The impact of interleaving angle on ac and dc side harmonics and EMI harmonics are comprehensively studied and optimal interleaving angle ranges to reduce these harmonics are derived consider multiple impact factors.

2.1 Analytical Model for Harmonic Calculation of Three-Level SVM

2.1.1 Three-Level SVM

The popular three-level SVM – NTSV scheme – is shown in Fig. 2-1. The NTSV scheme uses all the redundant switching states of small vectors as shown in Fig. 2-1. Fig. 2-1 also shows the PWM sequences of NTSV in all subsectors of sector I. NTSV will be used as an example to develop analytical models and to conduct harmonic analysis in this chapter.

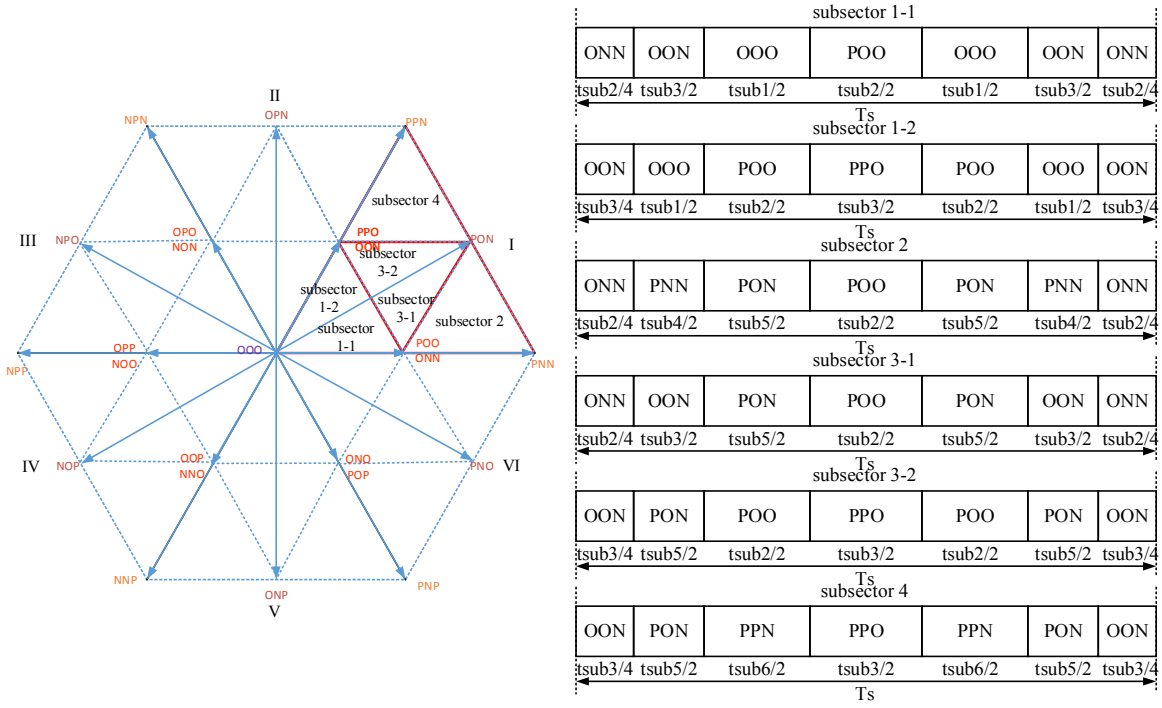


Fig. 2-1. Vectors of NTSV and the PWM sequences of sector I.

Different from two-level SVM, the sector is determined by both the reference angle and amplitude for three-level SVM. To better illustrate the harmonic calculation of three-level SVM, here three regions are defined as (2-1) based on the modulation index range.

$$\text{region 1: } M \le \frac{1}{\sqrt{3}}; \text{region 2: } \frac{1}{\sqrt{3}} < M \le \frac{2}{3}; \text{region 3: } \frac{2}{3} < M \le \frac{2}{\sqrt{3}} \qquad (2-1)$$

M is the modulation index which is defined as

$$M = V_{phase}/(V_{dc}/2) \qquad (2-2)$$

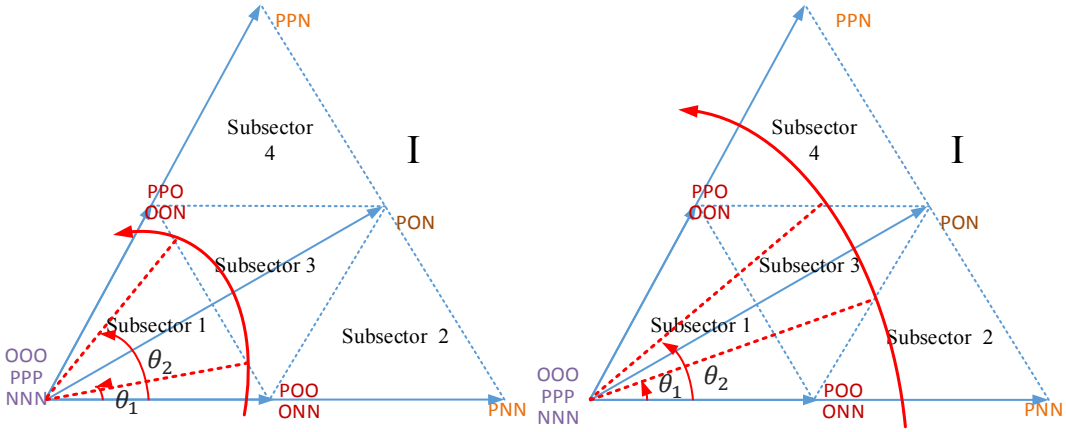


Fig. 2-2. Two sub-sector boundary angles in sector I, (a) region 2, (b) region 3.

The voltage reference will go through a full circle for a fundamental period. When the reference is in region 1, it will only go through subsector 1 of sector I. When the reference is in region 2, it will go through sector I from subsector 1 to subsector 3 and then back to subsector 1. When the reference is in region 3, it will go through sector I from subsector 2 to subsector 3 and then to subsector 4. The cases in other sectors are the same. In both region 2 and region 3, the reference will go through different subsectors. For calculation purpose, two subsector boundary angles are defined as θ_1 and θ_2 as shown in Fig. 2-2. When in region 2, the boundary angles are calculated as (2-3). When in region 3, the boundary angles are calculated as (2-4).

$$\theta_1 = arcsin\frac{1}{\sqrt{3}M} - \frac{\pi}{3}, \qquad \theta_2 = \frac{2\pi}{3} - arcsin\frac{1}{\sqrt{3}M} \tag{2-3}$$

$$\theta_1 = \frac{\pi}{3} - arcsin\frac{1}{\sqrt{3}M}, \qquad \theta_2 = arcsin\frac{1}{\sqrt{3}M} \tag{2-4}$$

2.1.2 Analytical Model for AC Voltage Harmonic

The spectrum of pulse width modulated phase leg voltage can be expressed as (2-5).

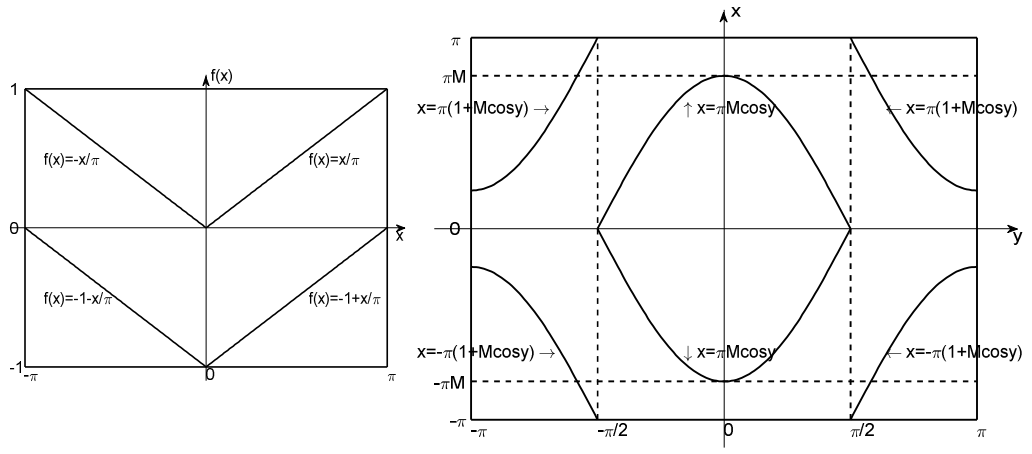
$$f(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{on}\cos(ny) + B_{on}\sin(ny)]$$

$$+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty} [A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)], x = \omega_c t, y = \omega_0 t$$

$$C_{mn} = A_{mn} + jB_{mn},\ A_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\cos(mx+ny)\,dxdy$$

$$B_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\sin(mx+ny)\,dxdy \qquad (2-5)$$

Here, *m* and *n* are the carrier baseband integer indices, respectively. The carrier and fundamental angular frequency are represented by ω_c andω_0, respectively.



(a) (b)

Fig. 2-3. (a) Three-level PD PWM carrier waveform, (b) the unit cell contour plot.

For carrier based PWM, Fig. 2-3(a) shows the three-level phase disposition (PD) PWM carrier waveform, and the unit cell contour plot is shown in Fig. 2-3(b) when the sinusoidal reference is $f(y) = Mcosy$. Then, the harmonic coefficient C_{mn} can be determined as (2-6).

$$C_{mn} = \frac{1}{2\pi^2}\left[\int_{-\pi}^{-\frac{\pi}{2}}\int_{-\pi}^{-\pi(1+Mcosy)}\left(-\frac{V_{dc}}{2}\right)e^{j(mx+ny)}dxdy + \int_{-\pi}^{-\frac{\pi}{2}}\int_{\pi(1+Mcosy)}^{\pi}\left(-\frac{V_{dc}}{2}\right)e^{j(mx+ny)}dxdy\right.$$
$$+\int_{\frac{\pi}{2}}^{\pi}\int_{-\pi}^{-\pi(1+Mcosy)}\left(-\frac{V_{dc}}{2}\right)e^{j(mx+ny)}dxdy + \int_{\frac{\pi}{2}}^{\pi}\int_{\pi(1+Mcosy)}^{\pi}\left(-\frac{V_{dc}}{2}\right)e^{j(mx+ny)}dxdy$$
$$\left.+\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\int_{-\pi Mcosy}^{\pi Mcosy}\left(\frac{V_{dc}}{2}\right)e^{j(mx+ny)}dxdy\right] \qquad (2-6)$$

SVM is functionally equivalent to carrier based PWM. The basic idea to derive the analytical solution for three-level SVM is to re-define the integral limits in (2-6) by taking account of the fact that the reference is no longer the pure sinusoidal but is now made up of several segments across a full fundamental cycle.

For NTSV scheme shown in Fig. 2-1, in sector I subsector 2, the equivalent reference is the average of the applied vector volt-second, and is calculated as (2-7). Then the inner integral limits can be determined as (2-8). The integral limits in other subsectors can be determined similarly.

$$V_{ref} = \frac{\sqrt{3}}{2}Mcos\left(y - \frac{\pi}{6}\right) \qquad (2-7)$$

$$x_r = -\pi(\frac{\sqrt{3}}{2}Mcos\left(y - \frac{\pi}{6}\right)), x_f = \pi(\frac{\sqrt{3}}{2}Mcos\left(y - \frac{\pi}{6}\right)) \qquad (2-8)$$

Table 2-1. Double Fourier Integral Limits of NTSV in Region 3 (Sector I, II, II)

y_s	y_e	x_r	x_f	$f(x,y)$
0	θ_1	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
θ_1	$\frac{\pi}{6}$	$-\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{6}$	θ_2	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
θ_2	$\frac{\pi}{3}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}$	$\frac{\pi}{3}+\theta_1$	$-\pi(\frac{3}{2}Mcosy)$	$\pi(\frac{3}{2}Mcosy)$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}+\theta_1$	$\frac{\pi}{2}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{2}$	$\frac{\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{\pi}{3}+\theta_2$	$\frac{2\pi}{3}$	$-\pi$	$-\pi(1+\frac{3}{2}Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{2\pi}{3}$	$\frac{2\pi}{3}+\theta_1$	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	π	
$\frac{2\pi}{3}+\theta_1$	$\frac{5\pi}{6}$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{5\pi}{6}$	$\frac{2\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	π	
$\frac{2\pi}{3}\pm\theta_2$	π	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$

Table 2-2. Double Fourier Integral Limits of NTSV in Region 2 (Sector I, II, III)

y_s	y_e	x_r	x_f	$f(x,y)$
0	θ_1	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
θ_1	$\frac{\pi}{6}$	$-\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\pi(\frac{3}{2}Mcosy-\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{6}$	θ_2	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
θ_2	$\frac{\pi}{3}$	$-\pi(\frac{3}{2}Mcosy)$	$\pi(\frac{3}{2}Mcosy)$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}$	$\frac{\pi}{3}+\theta_1$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}+\theta_1$	$\frac{\pi}{2}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right)+\frac{1}{2})$	$\frac{V_{dc}}{2}$
$\frac{\pi}{2}$	$\frac{\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{\pi}{3}+\theta_2$	$\frac{2\pi}{3}$	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{2\pi}{3}$	$\frac{2\pi}{3}+\theta_1$	$-\pi$	$-\pi(1+\frac{3}{2}Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{2\pi}{3}+\theta_1$	$\frac{5\pi}{6}$	$-\pi$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right)+\frac{1}{2})$	π	
$\frac{5\pi}{6}$	$\frac{2\pi}{3}+\theta_2$	$-\pi$	$-\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	$-\frac{V_{dc}}{2}$
		$\pi(\frac{3}{2}Mcosy+\frac{3}{2})$	π	
$\frac{2\pi}{3}+\theta_2$	π	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	π	

Table 2-3. Double Fourier Integral Limits of NTSV in Region 1 (Sector I, II, II)

y_s	y_e	x_r	x_f	$f(x,y)$
0	$\frac{\pi}{6}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{6}$	$\frac{\pi}{3}$	$-\pi(\frac{3}{2}Mcosy)$	$\pi(\frac{3}{2}Mcosy)$	$\frac{V_{dc}}{2}$
$\frac{\pi}{3}$	$\frac{\pi}{2}$	$-\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\pi(\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$\frac{V_{dc}}{2}$
$\frac{\pi}{2}$	$\frac{2\pi}{3}$	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y+\frac{\pi}{6}\right))$	π	
$\frac{2\pi}{3}$	$\frac{5\pi}{6}$	$-\pi$	$-\pi(1+\frac{3}{2}Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{3}{2}Mcosy)$	π	
$\frac{5\pi}{6}$	π	$-\pi$	$-\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	$-\frac{V_{dc}}{2}$
		$\pi(1+\frac{\sqrt{3}}{2}Mcos\left(y-\frac{\pi}{6}\right))$	π	

For different regions, as the reference will go through different subsectors, the equivalent reference and double Fourier integral limits will be different. Table 2-1 summarizes the integral limits of sector I, sector II, and sector III in region 3. The integral limits for region 2 and region 1 are shown in Table 2-2 and 2-3 [216-218].

Dead-time will impact the harmonics amplitude. As the dead-time t_d is small in the studied system (2% of the switching periodT_{sw}), its impact on harmonics is very small and can be neglected. For applications where dead-time is relatively large and needs to be considered, the inner integral limits shown in Table 3-1 should be modified by adding a term $2\pi t_d/T_{sw}$ on the rising or falling edge according to the polarity of output current. For simplicity, dead-time effect is shown in the models.

2.1.3 Analytical Model for DC Side Current Harmonic of NPC Inverter

Fig. 2-4 depicts the switching pattern and the current paths of the two dc-link capacitors of a three-level active NPC inverter. The positive line current $i_p(t)$ of a three-level NPC inverter is a combination of ac output currents and the uppermost switchS_{1H}. The ac output current can be considered as sinusoidal if THD is small. Hence, the frequency domain expression of switched current of phase A in the dc side can be derived as (2-9). Here, s_{1H-a} represents the switching function of the uppermost switch S_{1H-a}. I_0 and $\emptyset$ are the amplitude of the phase output current and the power factor angle, respectively.

The harmonic coefficient of switching function s_{1H-a} is expressed as C_{mn-1a}. According to the switching pattern, the double Fourier integral limits of C_{mn-1a} is similar as the derived phase output voltage model in Table 2-1. The difference is that, the function $f(x,y)$ is equal to 1 instead of $V_{dc}/2$ for the positive half cycle, and $f(x,y)$ is equal to zero instead of $-V_{dc}/2$ for the negative half cycle. Then, C_{mn-1a} can be determined, which is asymmetric in a fundamental cycle. This actually causes the input current frequency domain characteristics to be quite different from two-level inverter case. As C_{mn-1a} is determined, transforming (2-9) back to the time domain, the Fourier series of switched current of phase A in dc side and harmonic coefficient C_{mn-a} are represented as (2-10).

$$I_{dc-a}(\omega) = s_{1H-a}(\omega) \otimes I_{0a}(\omega) = \frac{I_{0a}}{2}\left(e^{j\emptyset} s_{1H-a}(\omega-\omega_0) + e^{-j\emptyset} s_{1H-a}(\omega-\omega_0)\right) \quad (2-9)$$

$$I_{dc-a}(t) = \frac{A_{00-a}}{2} + \sum_{n=1}^{\infty}[A_{0n-a}\cos(ny) + B_{0n-a}\sin(ny)] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[A_{mn-a}\cos(mx+ny) + B_{mn-a}\sin(mx+ny)]$$

$$A_{00-a} = \frac{I_0}{2}(A_{01}cos\emptyset + B_{01}sin\emptyset)$$

$$A_{mn-a} = \frac{I_0}{2}\left[\left(A_{m,n-1-1a} + A_{m,n+1-1a}\right)cos\emptyset + \left(B_{m,n-1-1a} + B_{m,n+1-1a}\right)sin\emptyset\right]$$

$$B_{mn-a} = \frac{I_0}{2}\left[\left(B_{m,n-1-1a} + B_{m,n+1-1a}\right)cos\emptyset - \left(A_{m,n-1-1a} - A_{m,n+1-1a}\right)sin\emptyset\right] \quad (2-10)$$

The contribution of phase B and phase C switched currents to the dc side current can be calculated similarly. Then, the harmonic coefficient C_{mn} of $i_p(t)$ is derived by summing all three phases as (2-11). The harmonic spectrum of negative line current $i_n(t)$ is similar as $i_p(t)$ due to symmetry, and the neutral line current $i_{neu}(t)$ harmonics can be calculated based on (2-12).

$$I_{dc}(\omega) = s_{a1}(\omega)\otimes I_{0a}(\omega) + s_{b1}(\omega)\otimes I_{0b}(\omega) + s_{c1}(\omega)\otimes I_{0c}(\omega)$$

$$C_{mn} = C_{mn-a}\left(1 + 2\cos\left(n\frac{2\pi}{3}\right)\right) \quad (2-11)$$

$$i_{dc} - i_{c1}(t) = i_p(t), i_{c2}(t) - i_{dc} = i_n(t), i_{neu}(t) = i_{C1}(t) - i_{C2}(t) = -i_p(t) - i_n(t) \quad (2-12)$$

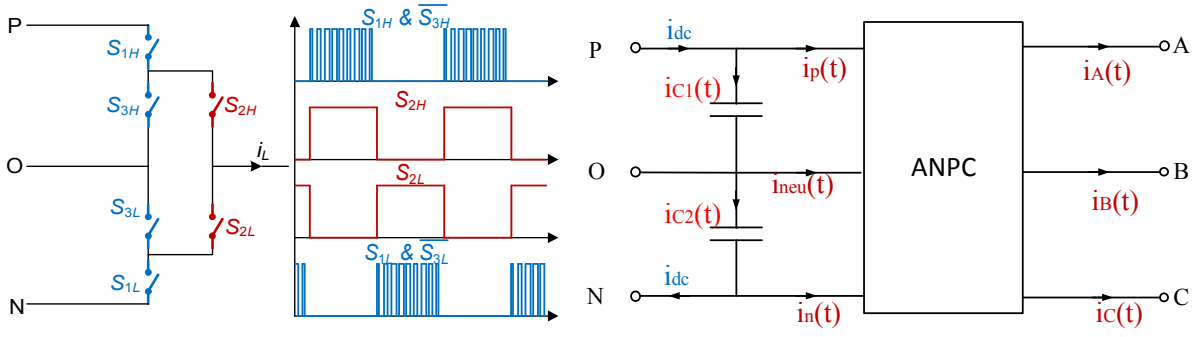


Fig. 2-4. Switching pattern and current path of a three-level active NPC.

To illustrate the difference of the dc side current harmonics between a three-level NPC inverter and a two-level inverter, the dc side current characteristics of the two-level inverter is briefly discussed. The dc side current spectrum of a two-level inverter with SVM is calculated, and the main components are shown in Fig. 2-5. The dc input current spectrum has the dc component, odd order carrier harmonic components such as $f_c \pm 3f_0$, $f_c \pm 9f_0$, and even order carrier harmonic components such as $2f_c$, $2f_c \pm 6f_0$. Since the 1st carrier harmonic does not exist, the 2nd carrier harmonic is the dominant component.

Then, based on the derived model, the dc side current spectrum of NPC converter is calculated and illustrated in Fig. 2-6. Fig. 2-6(a) shows the positive/negative line current spectrum, and Fig. 2-6(b) is the neutral line current spectrum. Unlike the spectrum of a two-level inverter, the positive/negative line current has dc component, third order harmonics, and $mf_c \pm 3nf_0$ carrier harmonics for both odd order and even order carrier harmonics. The neutral line current does not have dc component, but it has third harmonics, odd order carrier harmonic components such as f_c, $f_c \pm 6f_0$, and even order carrier harmonics components such as $2f_c \pm 3f_0$, $2f_c \pm 9f_0$. The third harmonic and all the carrier harmonics have doubled amplitude compared to the positive/negative line current harmonics. The 1st carrier harmonic is the dominant component. The difference of dc side current harmonic characteristics between a two-level inverter and a three-level NPC inverter is caused by the NPC structure. The existence of the neutral line actually decouples the positive line and negative line current. Thus, more sideband harmonics exist in the NPC inverter.

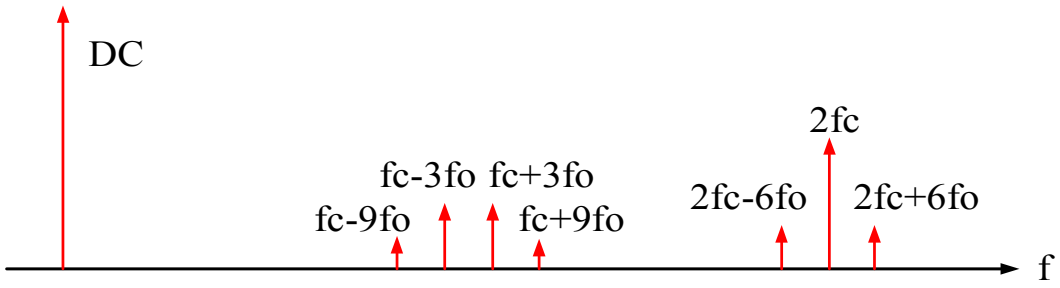


Fig. 2-5. Dc side current spectrum of a two-level inverter with SVM when PF=1.

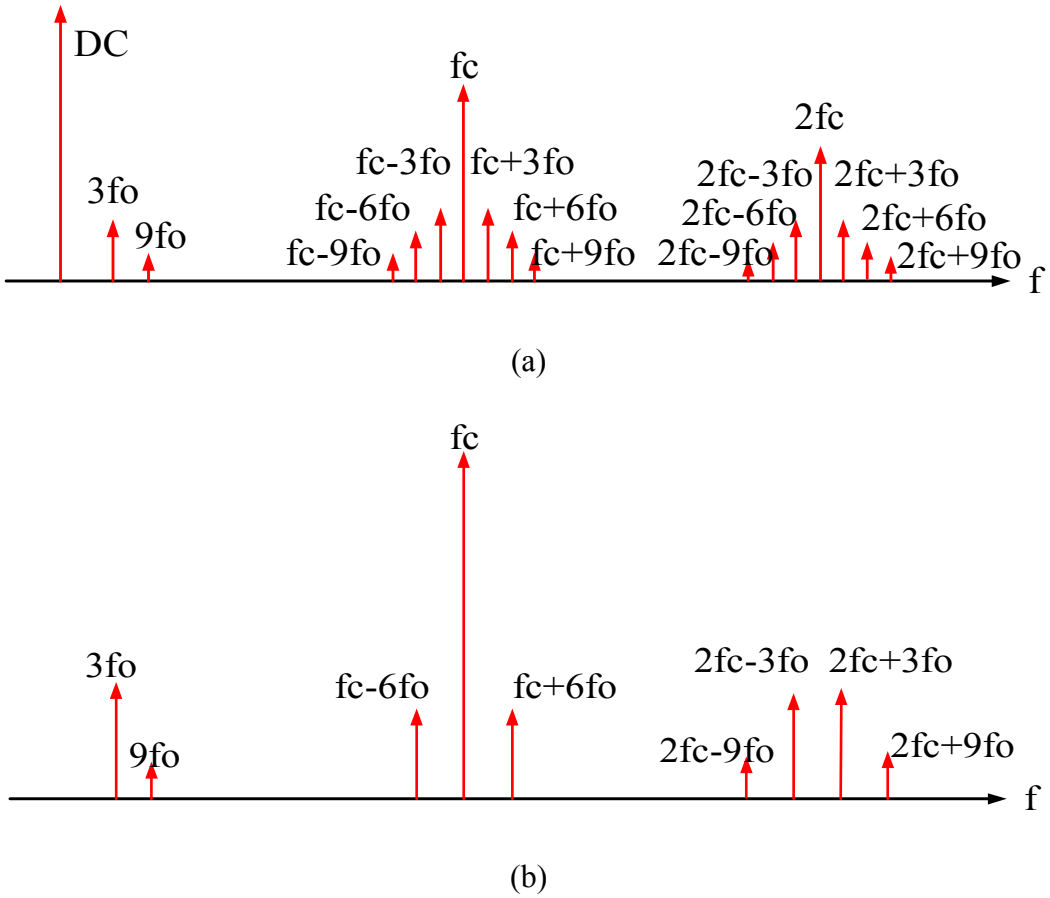


Fig. 2-6. Dc side current spectrum of a three level NPC inverter with NTSV when PF=1, (a) positive/negative line current, (b) neutral line current.

2.2 Impact of Interleaving on AC Voltage and DC side Current Harmonics

The impact of interleaving angle on ac side voltage and dc side current harmonics of parallel interleaved three-level NPC inverters is studied in this section. For two interleaved inverters, if the interleaving angle of inverter 2 is γ with respect to inverter 1, the harmonic amplitude of two interleaved inverters output can be determined as (2-13). From (2-13), it is obvious that interleaving can reduce the amplitude of the output harmonics.

$$C_{mn,avg} = \frac{1}{2}\left|(C_{mn,1} + C_{mn,2}e^{im\gamma})\right| = C_{mn}\left|\cos\left(\frac{m\gamma}{2}\right)\right| \qquad (2-13)$$

2.2.1 Impact of Interleaving Angle on AC Voltage WTHD

The weighted total harmonic distortion (WTHD) is a commonly used figure of merit to size the power filter requirements in the ac output side and is used for interleaving angle optimization. With the developed models, the ac side line voltage harmonics WTHD is calculated as a function of modulation index and interleaving angle. The results are shown in Fig. 2-7. From Fig. 2-7, interleaving angle range around 90° is optimal to minimize WTHD for different modulation indexes. As the dominant high frequency components in the line voltage are the 2nd carrier harmonic sidebands $2f_c \pm f_0$, 90° interleaving angle eliminate the 2nd carrier harmonic and sideband and thus significantly reduce WTHD.

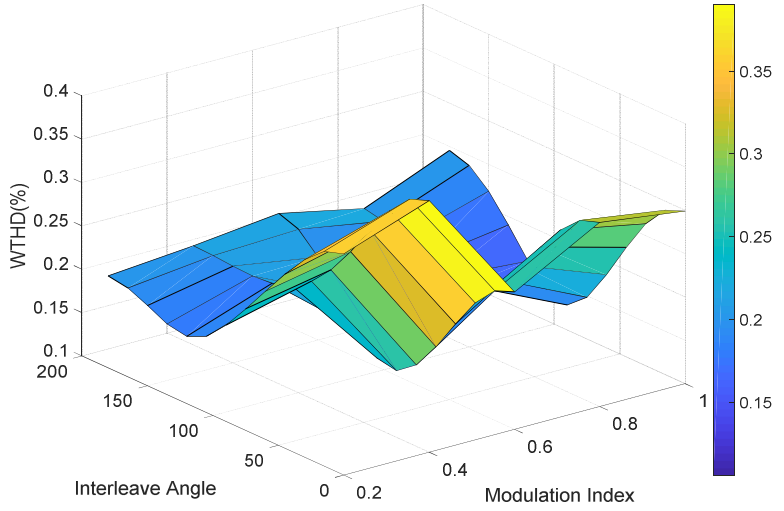


Fig. 2-7. Ac side line to line voltage WTHD versus interleaving angle ($f_0 = 400\,Hz, f_c = 20\,kHz$).

2.2.2 Impact of Interleaving Angle on DC-link Capacitor RMS Current

Based on the spectrum analysis, the dc side current of three-level NPC inverter has both low frequency and high frequency components. The low frequency components can be controlled if there is front-end converters, or closed-loop control, and is not impacted by interleaving angle. The high frequency components is the result of PWM switching and must be handled by dc-link capacitors. Dc-link capacitors are usually a weak point in the system and determine system reliability due to the thermal issues related to ripple current flowing through the capacitors. The capacitor high frequency ripple current rms value is used as the figure of merit for interleaving angle optimization. From Fig. 2-4(b) and relationship shown in (2-12), the high frequency harmonics in the positive/negative line will flow through the dc-link capacitor.

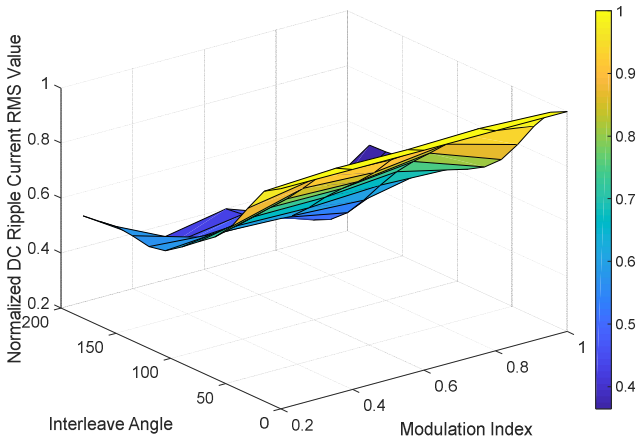
With the developed models in section 2.1 and (2-13), the normalized dc-link capacitor high

frequency ripple current rms value is calculated as a function of modulation index, interleaving angle, and power factor. The results are shown in Fig. 2-8. The optimal interleaving angle range for dc-link capacitor ripple current rms is highly dependent on power factor and modulation index. The results show different trends compared to the interleaved two-level inverters.

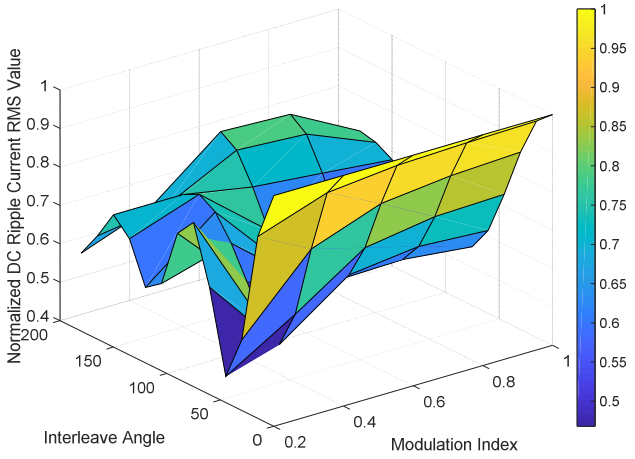
When the modulation index is high and power factor is high, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle range is around 180°. This can be expected as the 1st carrier harmonic exists and is the dominant high frequency component in the dc-link capacitor current, and 180° interleaving angle will totally eliminate the 1st carrier harmonic and its sidebands.

When the modulation index is high and power factor is low, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle range is around 90°. This is because the 2nd carrier harmonic sidebands become the dominant high frequency component, and 90° interleaving angle will eliminate the 2nd carrier harmonic and its sidebands.

When the modulation index is low (in region 1), the dc-link capacitor ripple current rms value shows a complicated variation trend when the interleaving angle varies. This is because both the 1st and 2nd and high order carrier harmonic sidebands are dominant in this case.



(a)



(b)

Fig. 2-8. Dc side dc-link capacitor ripple current RMS value versus interleaving angle ($f_0 = 400\ Hz, f_c = 20\ kHz$), (a) PF=1, (b) PF=0.

2.3 Impact of Switching Frequency and Interleaving on EMI Harmonics

EMI filters are required in power converters to suppress the EMI harmonics and thus pass EMI standards. The size and weight of an EMI filter can be indicated by EMI filter corner frequency. A higher EMI filter corner frequency usually indicates a smaller filter. The impact of switching

frequency and interleaving angle on EMI filter corner frequency are analytically derived in this section.

2.3.1 Relationship between Switching Frequency and EMI Filter Corner Frequency

As the harmonics of ac side output phase voltage is calculated above, the EMI noise source for both common-mode and differential-mode voltages can be determined as (2-14) and (2-15).

$$V_{CM} = \frac{V_A + V_B + V_C}{3} = \frac{1}{3}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} C_{mn}\cos(mx + ny)\left(1 + 2\cos\left(n\frac{2\pi}{3}\right)\right) \qquad (2-14)$$

$$V_{DM-A} = V_A - V_{CM} \qquad (2-15)$$

EMI filter corner frequency is actually determined by a certain EMI noise peak. The motor drive system in aircraft application is investigated. For CM noise, the motor CM impedance can be simply modeled as a capacitor. EMI noise currents need to meet DO-160 standards. The LISN schematic defined in DO-160 standards is shown in Fig. 2-9(a). The CM equivalent circuit for the CM noise propagation path is derived as shown in Fig. 2-9(b).

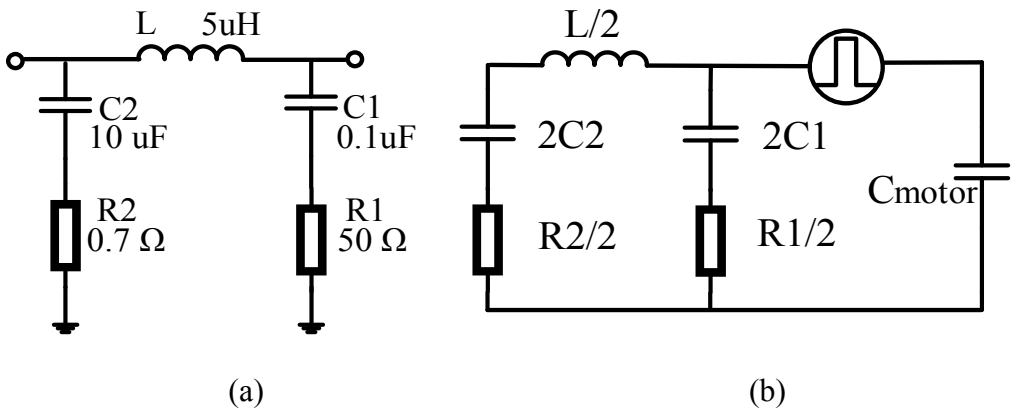


Fig. 2-9. (a) LISN used in DO-160 standards, (b) CM equivalent circuit.

As the EMI noise source and noise propagation path impedance are determined, and EMI standards are given, the required CM noise attenuation can be determined as (2-16).

$$I_{RA(f_{index})} = 20log_{10}\left(\frac{V_{CM(f_{index})} \times 10^6}{Z_{CM(f_{index})}}\right) - I_{std(f_{index})} + \text{Margin} \qquad (2-16)$$

where $I_{RA(f_{index})}$, $I_{std(f_{index})}$, $V_{CM(f_{index})}$, and $Z_{CM(f_{index})}$ are the noise current required attenuation, EMI standards defined noise current limit level, CM noise voltage, and CM noise propagation path impedance at a certain frequency f_{index}, respectively.

After the required noise attenuation is calculated and the EMI filter type is selected, the noise peak frequency f_{pk} which determines the EMI filter corner frequency can be identified with the flowchart shown in Fig. 2-10. Then, CM filter corner frequency can be calculated as (2-18). Here, the filter type is indicated by k (k=2 and k=4 represent single and two stage LC filters, respectively).

$$I_{RA(f_{index})} \geq k\left(20log_{10}(f_{index}) - 20log_{10}(f_{pk})\right) + I_{RA}(f_{pk}) \qquad (2-17)$$

$$log_{10}(f_c) = log_{10}(f_{pk}) + \frac{I_{std(f_{pk})} - 20log_{10}\left(\frac{V_{CM(f_{pk})}10^6}{Z_{CM(f_{pk})}}\right)}{20k} \qquad (2-18)$$

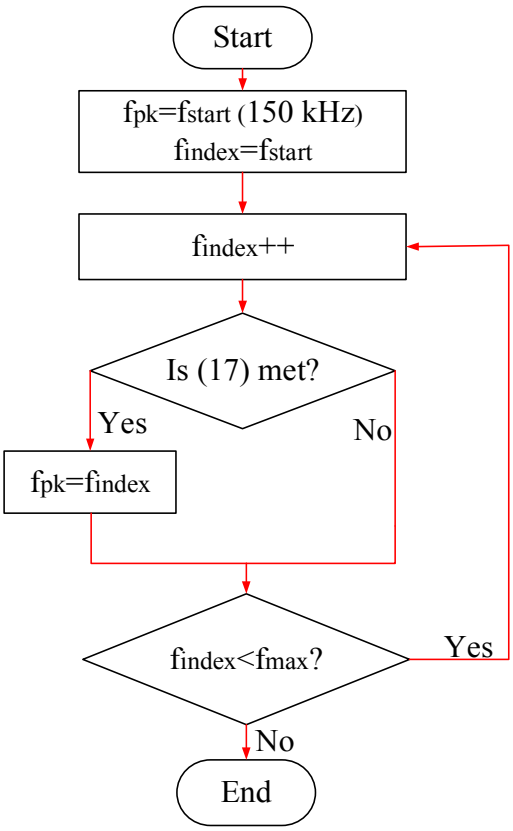


Fig. 2-10. Flow chart to determine the noise peak frequency.

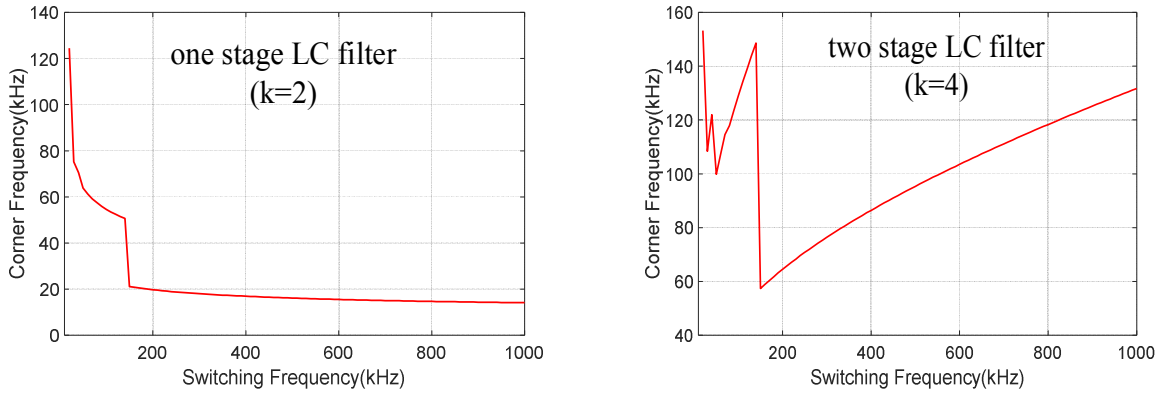
Then, the CM filter corner frequency f_c as a function of switching frequency f_s can be calculated. Fig. 2-11 shows a case study calculation results ($C_{motor} = 1\ nF$) when one stage LC filter and two stage LC filter are assumed. The DM filter corner frequency calculation is similar and is not repeated here.

Resonance may exist in the CM noise propagation path impedance if there is not enough damping. If the resonance frequency is close to the switching frequency or its multiples, it may become the noise peak frequency and largely impact the CM filter corner frequency. However, for a high density EMI filter design, it is better to damp the impedance resonance first and then design the EMI filter.

From Fig. 2-11, several findings are observed. When 20 kHz< f_s<150 kHz, f_c and f_s have a non-linear relationship, some preferred f_s exist such as 140 kHz. When 150 kHz< f_s<2 MHz, if single stage LC filter is applied, f_c has slight change as f_s increases. If two or multiple stage LC filters are applied, f_c increases fast as f_s increases. This findings provide a guideline for switching frequency and EMI filter type selection.

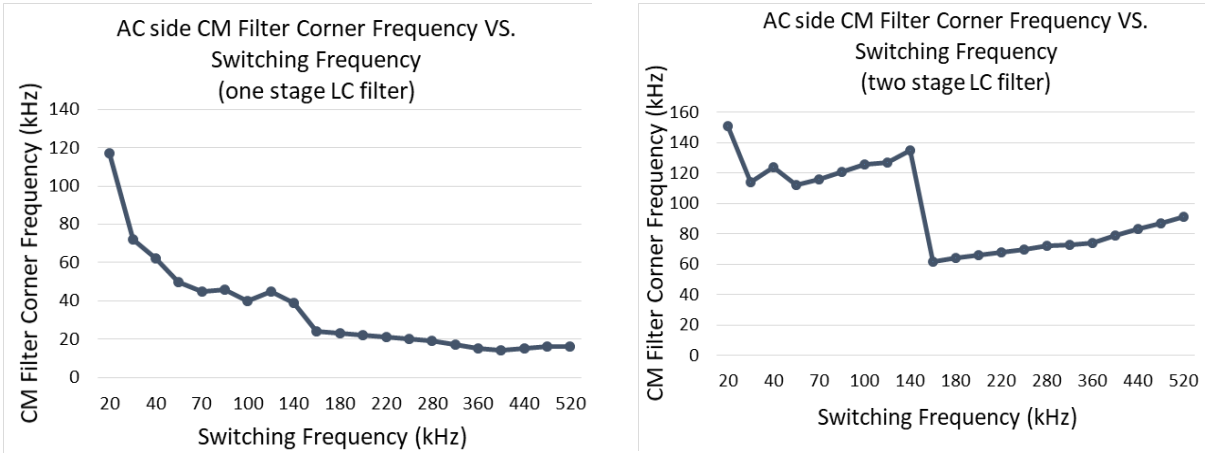
The non-linear relationship between f_c and f_s in the 20 kHz to 150 kHz range can be understood because the noise peak frequency and CM voltage harmonic amplitude are not changed linearly as switching frequency increases. The different trends of filter corner frequency between a single stage LC filter and a multiple stage filter when switching frequency is in the 150 kHz ~ 2 MHz range can also be explained. As switching frequency increases, the LC filter impedance increases, and the DO-160 EMI standard limit decreases at a slow rate of around 30 dB/dec. For single stage LC filter, the benefit gained from the increase of LC filter impedance is almost cancelled out by the decrease of the EMI standards limit. As a result, f_c has slight change as f_s increases. For multiple stage LC filter, the LC filter impedance increases much faster as switching frequency increases and outweighs the decrease of EMI standard limit. Thus, f_c increases fast as f_s increases.

MATLAB/SIMULINK simulations were conducted. CM filter corner frequency are determined for different switching frequencies as shown in Fig. 2-12. The trends how CM filter corner frequency varies with switching frequency match the calculation and conclusions above.



(a) (b)

Fig. 2-11. Calculated corner frequency versus switching frequency, (a) single stage LC filter, and (b) two stage LC filter.



(a) (b)

Fig. 2-12. Design results of ac side CM filter corner frequency versus switching frequency, (a) single stage LC filter, and (b) two stage LC filter applied.

2.3.2 Impact of Interleaving on EMI Filter Corner Frequency

According to (2-13), when symmetric interleaving ($\gamma = \pi$) is applied to two interleaved inverters,

$$C_{mn,avg} = C_{mn}\left|\cos\left(\frac{m\pi}{2}\right)\right| = \begin{cases} C_{mn}, & m\ is\ an\ even\ number \\ 0, & m\ is\ an\ odd\ number \end{cases} \quad (2-19)$$

When asymmetric interleaving ($\gamma \neq \pi$) is applied to two interleaved inverters,

$$C_{mn,avg} = C_{mn}\left|\cos\left(\frac{mr}{2}\right)\right| \leq C_{mn} \quad (2-20)$$

Hence, symmetric interleaving will eliminate the odd number carrier harmonics while keeping the even number carrier harmonics amplitude unchanged. Asymmetric interleaving could reduce the amplitude of all the harmonic components. When the objective is EMI noise and EMI filter reduction which is actually determined by certain harmonic peaks, asymmetric interleaving could be more effective.

As the CM and DM voltage harmonics calculation, noise propagation path impedance calculation, and the noise peak frequency f_{pk} identification are illustrated, the relationship between interleaving angle and CM filter corner frequency is calculated as (2-21). The relationship between interleaving angle and ac side DM filter corner frequency can be calculated similarly.

$$log_{10}(f_c) = log_{10}(f_{pk}) + \frac{I_{std(f_{pk})} - 20log_{10}\left(\frac{V_{CM(f_{pk})}\cos\left(\frac{m\gamma}{2}\right)10^6}{Z_{CM(f_{pk})}}\right)}{20 \cdot k} \quad (2-21)$$

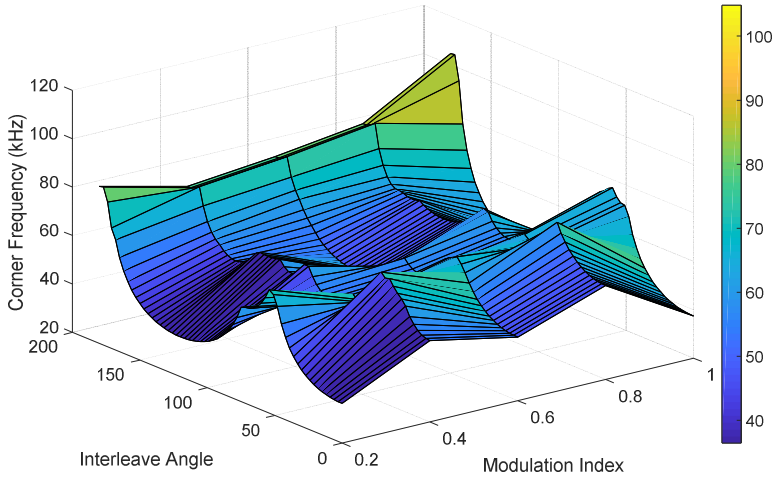
From (2-21), EMI filter corner frequency is a function of switching frequency, modulation index, interleaving angle, EMI filter type, and EMI noise propagation path impedance. Interleaving angle can be optimized to increase EMI filter corner frequency.

Whether the switching frequency is located in the EMI frequency range or not will influence the trend how EMI filter corner frequency varies as interleaving angle changes. Hence, two case studies are conducted.

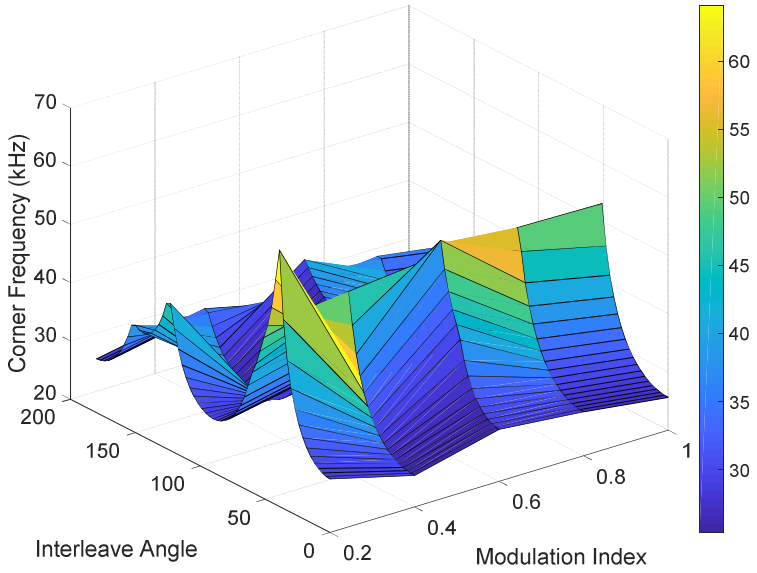
The first case is that switching frequency is f_s=70 kHz (<150 kHz). The CM and DM filter corner frequencies are calculated as a function of modulation index and interleaving angle. One stage filter is assumed (k=2). The results are shown in Fig. 2-13.

From Fig. 2-13(a), the CM filter corner frequency peak is achieved when interleaving angle is around 180°, and the second optimal interleaving angle range is 30°~90°. From Fig. 2-13(b), the DM filter corner frequency peak is obtained when interleaving angle is around 30°~60°, and the second optimal interleaving angle range is around 120°~180°.

In this case, the 1st and 2nd carrier harmonics are not in the EMI frequency range. Hence, the 3rd to 6th carrier harmonics are the potential candidates which may determine EMI filter corner frequency. For CM voltage harmonics, the 3rd and 5th harmonics are dominant, and 30°~60° and 150°~180° interleaving angle range are preferred for harmonics reduction according to Fig. 2-14. For DM voltage harmonics, the 4th and 6th harmonics are dominant, and 30°~60° and 90°~120° interleaving angle range are preferred for harmonics reduction.



(a)



(b)

Fig. 2-13. EMI filter corner frequency versus interleaving angle ($f_s = 70\ kHz$), (a) CM filter, (b) DM filter.

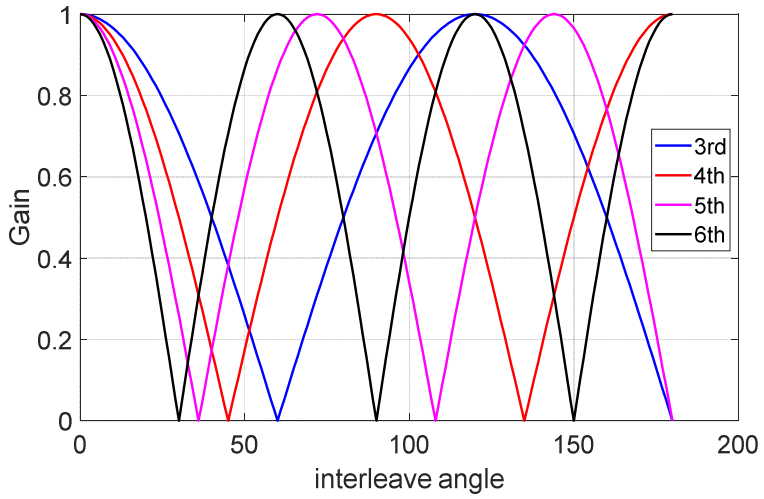


Fig. 2-14. The 3rd, 4th, 5th and 6th carrier harmonics gain versus interleaving angle.

The second case is that switching frequency is f_s=200 kHz (>150 kHz). In this case, the 1st and 2nd carrier harmonics are in the EMI frequency range. The analysis is similar. The CM and DM filter corner frequencies are also calculated, and the results show that the CM filter corner frequency peak is achieved when interleaving angle is around 180° while the DM filter corner frequency peak is achieved when interleaving angle is in the 90° ~150° range.

2.4 Experimental Results

Two three-level NPC inverters are constructed to verify the key points in aforementioned analysis. Fig. 2-15 shows the circuit schematic and Fig. 2-16 shows the experiment platform. The inverter is tested at 200 V dc bus voltage. The ac output fundamental frequency is 400 Hz and carrier frequency is 60 kHz. RL load (R=20 Ω, L=320 uH for each phase) is applied.

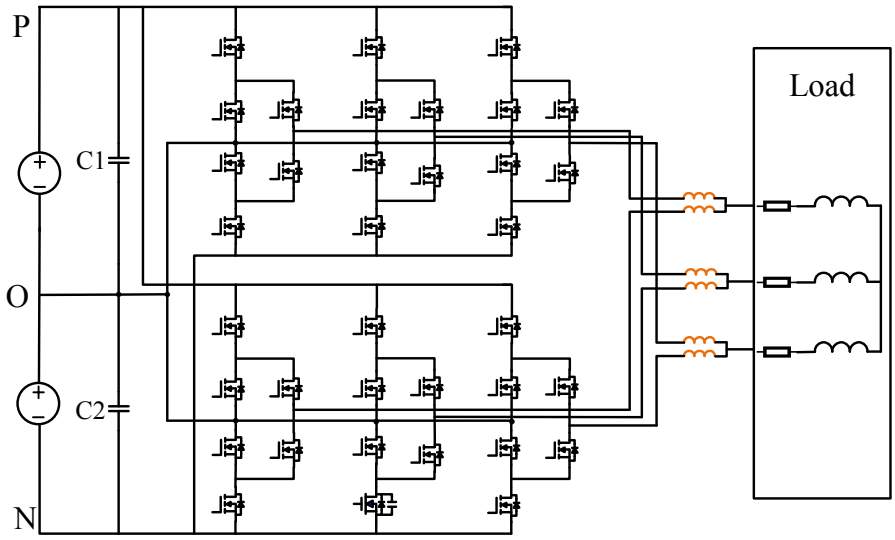


Fig. 2-15. Circuit schematic Circuit schematic of two paralleled three-level ANPC inverters.

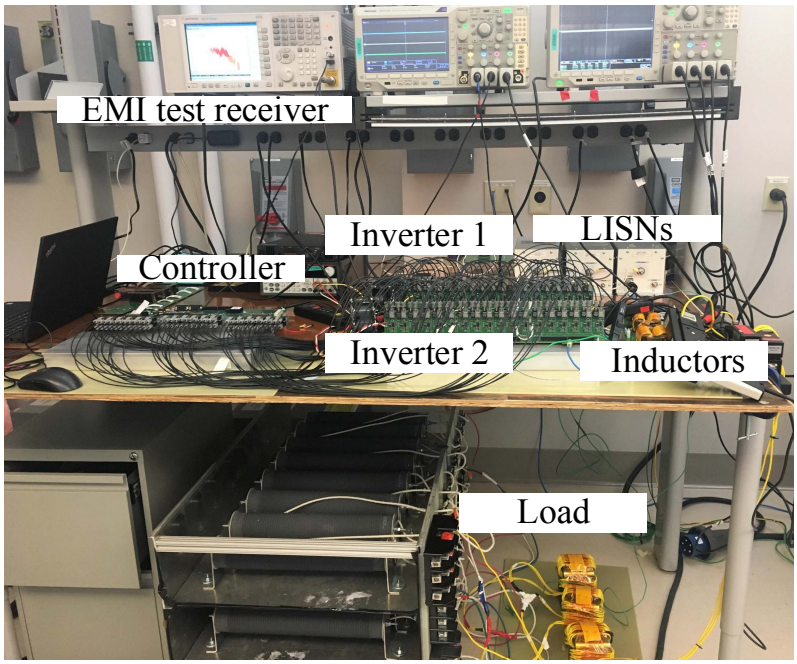


Fig. 2-16. Experiment platform of two paralleled three-level ANPC inverters.

2.4.1 Analytical Model Verification

Fig. 2-17 shows the ac side output voltages and current with modulation index *M*=0.9. Fig. 2-18(a) and Fig. 2-18(b) show the tested phase output voltage spectrum and the calculated spectrum with developed model, respectively. Table 2-4 summarizes the main components comparison between tested results and calculated results. The calculated harmonics frequency and amplitude match well with tested results.

Fig. 2-19 shows the dc side input currents waveforms including the positive line current i_p, neutral line current i_{neu}, and negative line current i_n. The definition of the currents are the same as shown in Fig. 2-4(b). Fig. 2-20(a) and Fig. 2-20(b) show the tested positive line current spectrum and the calculated spectrum with developed model, respectively. Fig. 2-21(a) and Fig. 2-21(b) show the tested neutral line current spectrum and calculated spectrum with developed model, respectively. The negative line current spectrum is the same as the positive line current.

Table 2-5 summarizes the main components value comparison between tested results and calculated results. The calculated harmonics frequency and amplitude match well with tested results, and verifies the aforementioned dc side current harmonic characteristics analysis.

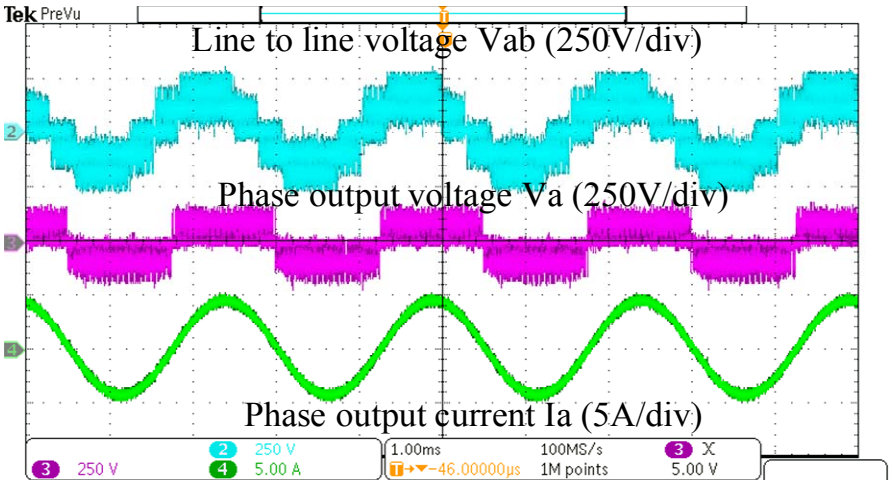
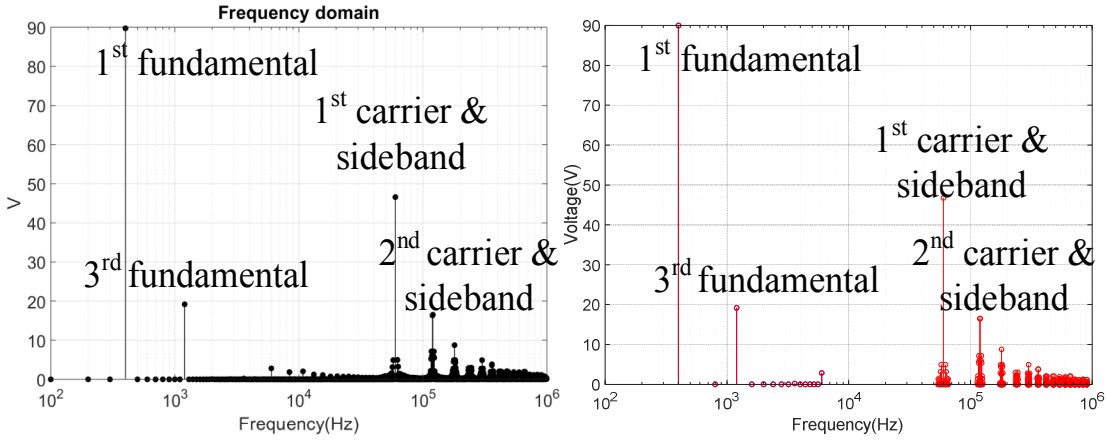


Fig. 2-17. Ac side output voltage and current.

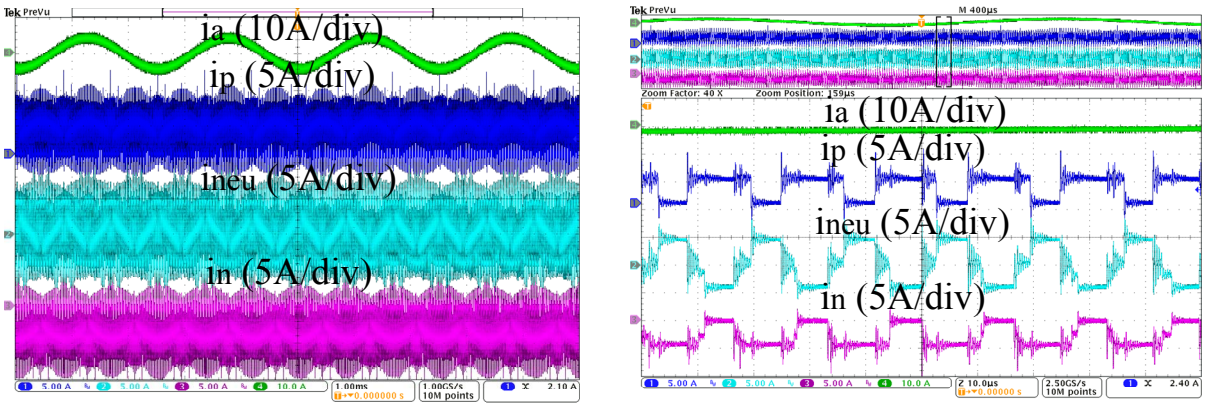


(a) (b)

Fig. 2-18. Spectrum of ac side phase output voltage, (a) tested results, (b) calculation results with developed models.

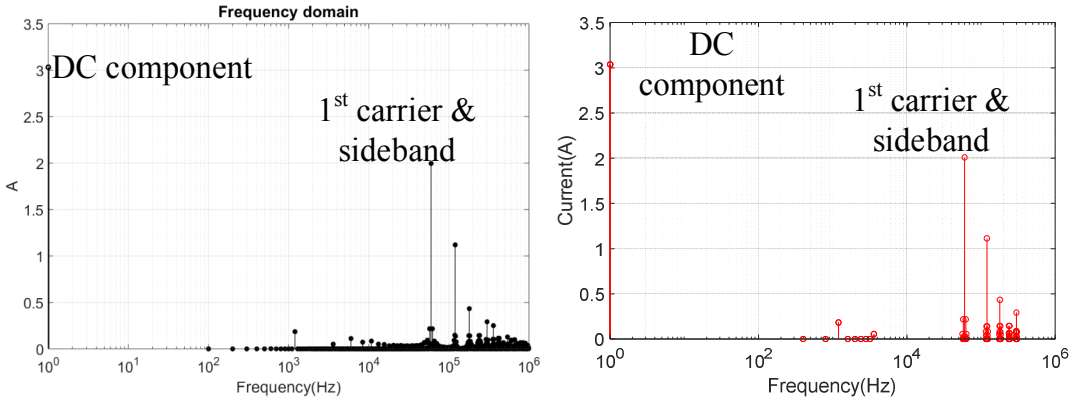
Table 2-4. Comparison of Main Components of AC Phase Voltage.

Harmonics/V	f_0	$3f_0$	f_c	$2f_c \pm f_0$	$2f_c \pm 3f_0$
Tested	89	18.7	46	16	1.1
Calculated	90	19.2	46.8	16.5	1.3



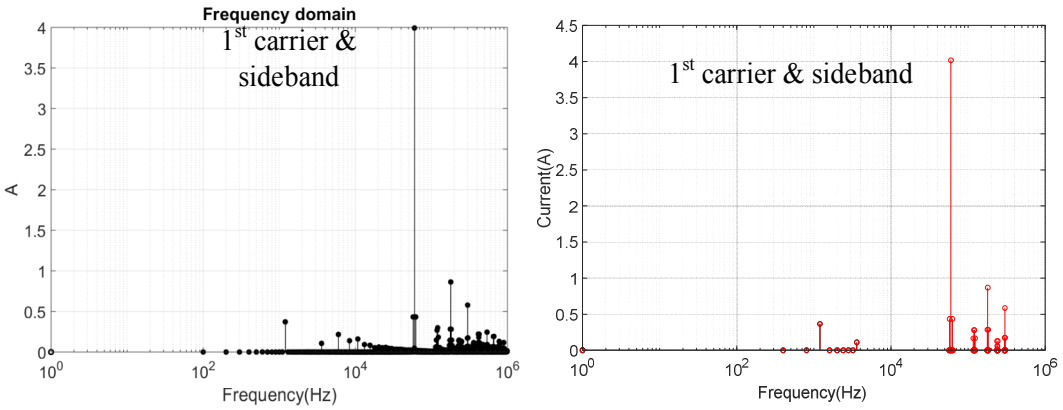
(a) (b)

Fig. 2-19. DC side input currents. (a) From top to bottom: output phase current i_a, input positive line current i_p, input neutral line current i_{neu}, input negative line current i_n, (b) zoom in figures of (a) showing switching cycle waveforms.



(a) (b)

Fig. 2-20. Spectrum of dc side positive line current, (a) tested results, (b) calculation results with developed models.



(a) (b)

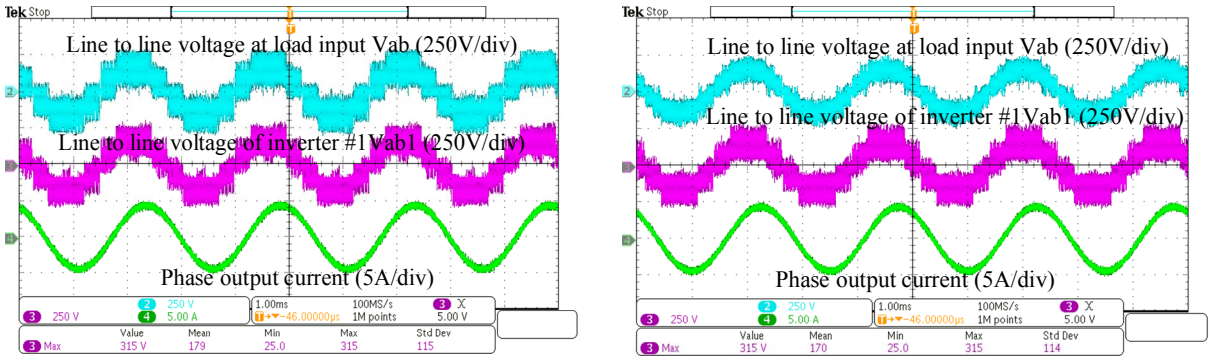
Fig. 2-21. Spectrum of dc side neutral line current, (a) tested results, (b) calculation results with developed models.

Table 2-5. Comparison of Main Components of DC Input Currents.

Harmonics/A	DC	$3f_0$	f_c	$f_c \pm 6f_0$	$2f_c$	$2f_c \pm 3f_0$
i_p tested	3.16	0.21	2.1	0.19	1.2	0.18
i_p calculated	3.02	0.18	2	0.22	1.1	0.15
i_{neu} tested	0	0.41	4.2	0.39	0	0.36
i_{neu} calculated	0	0.36	4.04	0.44	0	0.3

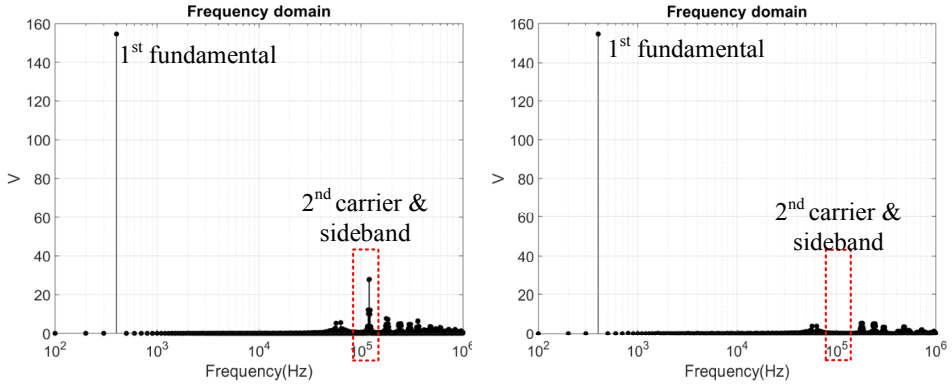
2.4.2 Impact of Interleaving on AC Voltage and DC Side Current Harmonics

The line voltage of paralleled inverters are measured with different modulation indexes and different interleaving angels. Fig. 2-22 shows line voltage waveforms with 0° and 90° interleaving angle, all at the condition M=0.9. Fig. 2-23 shows spectrum of line voltage. With 90° interleaving angle, the dominant components - second carrier frequency and sideband harmonics - are almost eliminated. Table 2-6 summarizes the WTHD of line voltage at different modulation indexes and interleaving angles. Minimum WTHD is achieved at around 90° interleaving angle.



(a) (b)

Fig. 2-22. Ac side voltage waveforms at M=0.9. From top to bottom: line to line voltage measured at load input, line to line voltage of inverter #1, and phase output current, (a) 0° interleaving angle, (b) 90° interleaving angle.



(a) (b)

Fig. 2-23. Spectrum of line voltage at M=0.9, (a) 0° interleaving angle, (b) 90° interleaving angle.

Table 2-6. Line Voltage WTHD at Different Modulation Index and Interleaving Angles

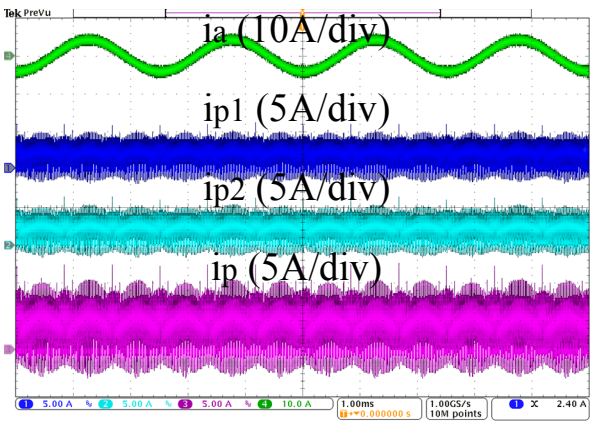
WTHD0 (%)	M=0.9	M=0.4
γ=0°	0.12	0.14
γ=90°	0.036	0.051
γ=180°	0.108	0.114

The dc side currents are measured with different modulation indexes, different interleaving angles, and different power factors. Fig. 2-24 shows the dc side input current waveforms with 0° and 180° interleaving angle, all at the condition M=0.9. As RL load (R=20 Ω, L=320 uH for each phase) is adopted, the power factor is nearly PF =1. In Fig. 2-24, ringing can be observed in the switching cycle PWM waveforms. This is because the leads between the dc-link cap and switch phase leg is purposely increased for measuring input current. However, the ringing frequency is above MHz and will not impact the switching frequency harmonic characteristics.

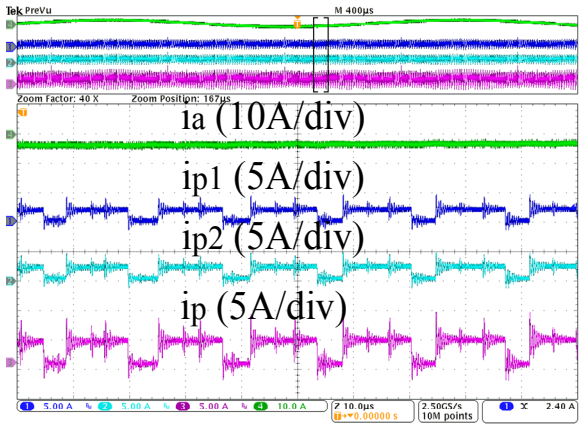
Fig. 2-25 shows the spectrum of positive line current harmonics. With 180° interleaving angle, the dominant components - the 1st carrier frequency and sideband harmonics - are eliminated. As the high frequency components of i_p will go through dc-link capacitor C1, around 180° interleaving angle eliminates the dominant high frequency components and achieves minimum RMS ripple current in capacitor C1.

Table 2-7. DC-link Capacitor High Frequency Current RMS Value with Different Modulation Index and Interleaving Angles (PF=1)

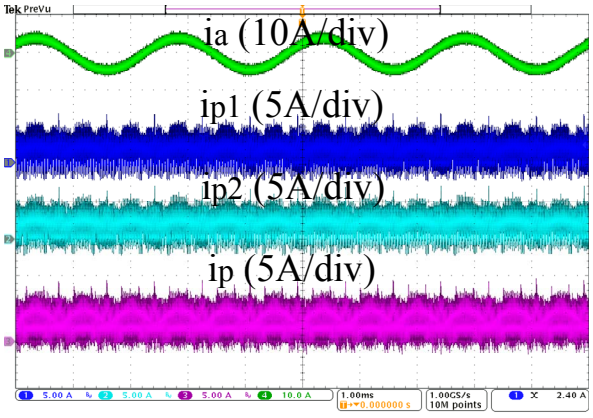
Capacitor high frequency current RMS (A)	M=0.9	M=0.4
γ=0°	1.76 (100%)	0.83(100%)
γ=90°	1.15 (65%)	0.51(61%)
γ=180°	0.79 (45%)	0.34 (41%)



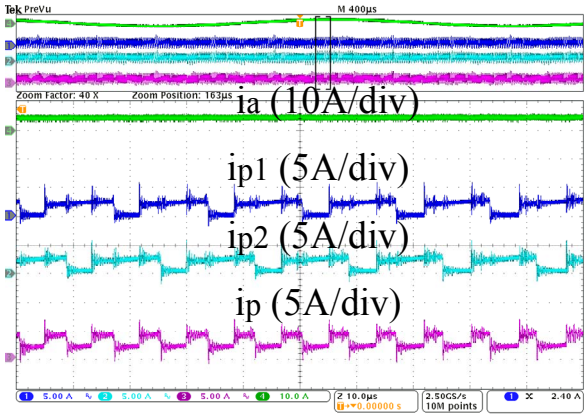
(a)



(b)

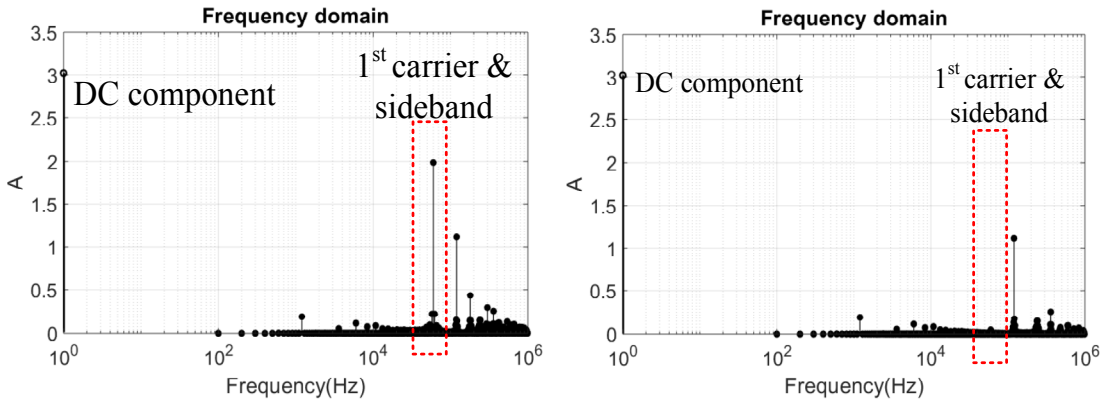


(c)



(d)

Fig. 2-24. Dc side current waveforms at M=0.9 and PF=1. From top to bottom: output phase current i_a, input positive line current of inverter #1 i_{p1}, input positive line current of inverter #2 i_{p2}, and total input positive line current i_p, (a) 0° interleaving angle, (b) zoom in figures of (a) showing switching cycle waveforms, (c) 180° interleaving angle, (d) zoom in figures of (c) showing switching cycle waveforms.



(a) (b)

Fig. 2-25. Spectrum of the positive line current i_p at M=0.9 and PF=1, (a) 0° interleaving angle, (b) 180° interleaving angle.

To verify the analysis with low power factor case, the RL load is changed to L load (R=0 Ω, L=320 uH for each phase), and the fundamental frequency is increased to 3 kHz and dc voltage reduced to 100 V to limit the output current level. In this case, the power factor is PF=0. Fig. 2-26 shows the dc side input current waveforms with 0° and 90° interleaving angle, all at the condition *M*=0.9. Fig. 2-27 shows the spectrum of positive line current harmonics. With 90° interleaving angle, the dominant components – the 2nd carrier frequency and sideband harmonics - are significantly reduced. It can be observed that the 2nd carrier and sideband harmonics are not eliminated. This is because that ratio between the carrier frequency and fundamental frequency (60 kHz/3 kHz) is low in this case and the sidebands of 1st carrier frequency harmonic overlap with the sidebands of the 2nd carrier frequency harmonic. Table 2-8 summarizes the dc-link capacitor high frequency current RMS value at different modulation indexes and interleaving angles, all at power factor PF=0. In this case, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle is around 90°. The trend matches previous conclusion.

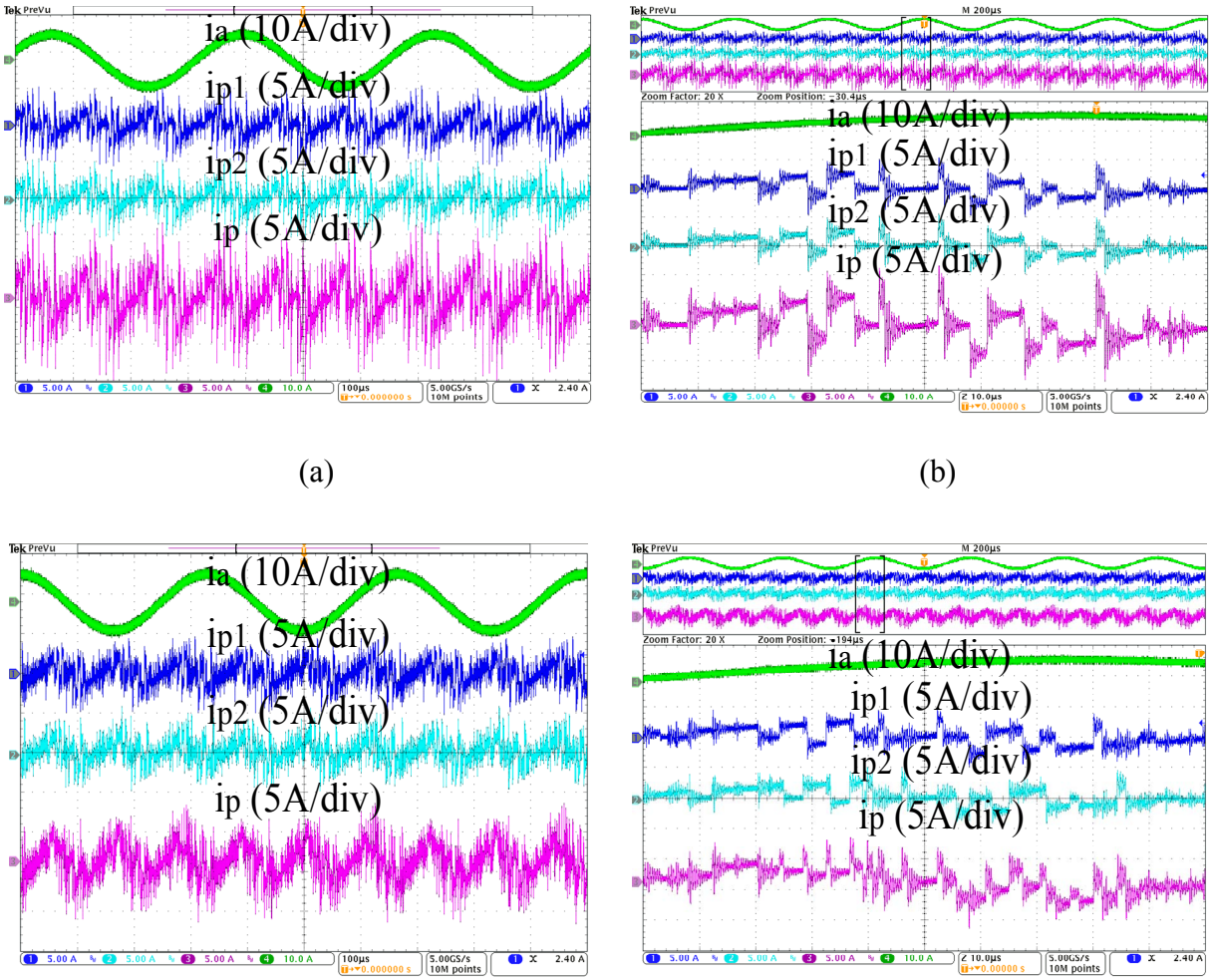
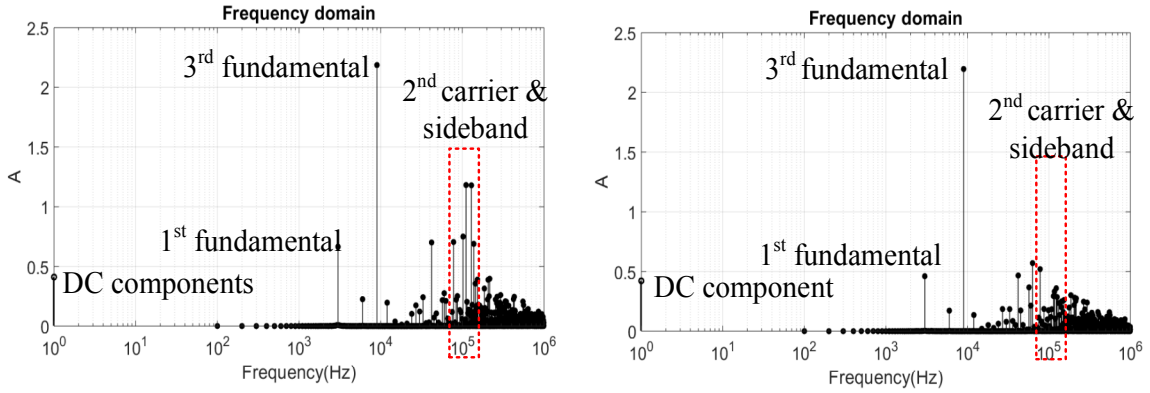


Fig. 2-26. Dc side current waveforms at M=0.9 and PF=0. From top to bottom: output phase current i_a, input positive line current of inverter #1 i_{p1}, input positive line current of inverter #2 i_{p2}, and total input positive line current i_p, (a) 0° interleaving angle, (b) zoom in figures of (a) showing switching cycle waveforms, (c) 90° interleaving angle, (d) zoom in figures of (c) showing switching cycle waveforms.



(a) (b)

Fig. 2-27. Spectrum of the positive line current i_p at M=0.9 and PF=0, (a) 0° interleaving angle, (b) 90° interleaving angle.

Table 2-8. DC-link Capacitor High Frequency Current RMS Value with Different Modulation Index and Interleaving Angles (PF=0)

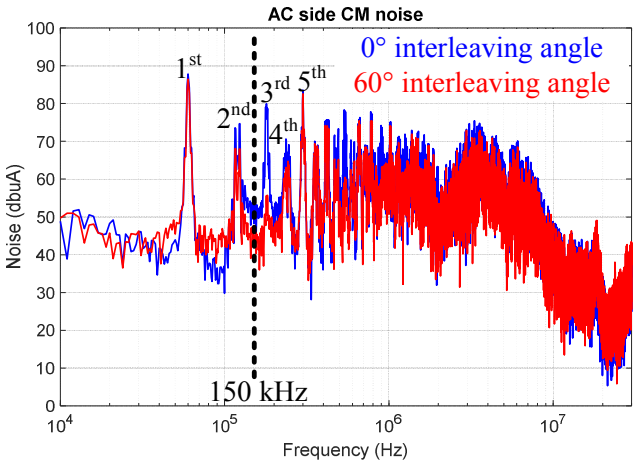
Capacitor high frequency current RMS (A)	M=0.9	M=0.4
γ=0°	2.04 (100%)	0.72(100%)
γ=90°	0.93 (46%)	0.38(51%)
γ=180°	1.65 (81%)	0.49 (68%)

2.4.3 Impact of Interleaving on EMI Harmonics

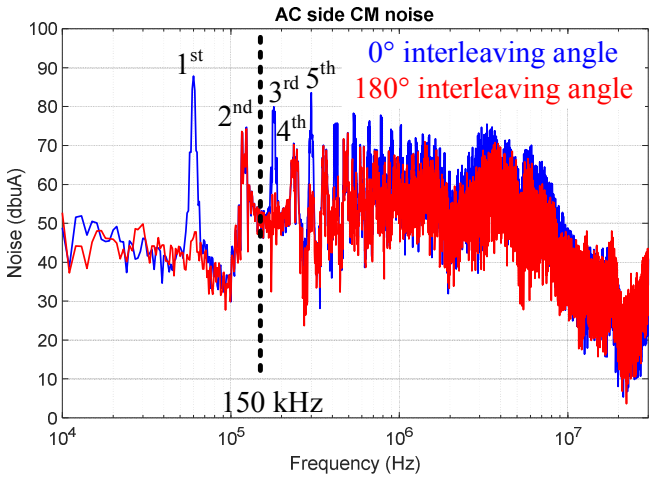
The EMI noise currents of the paralleled inverter system are measured with the EMI test receiver and RF probe following DO-160 standards. The operation condition is the same as previous. RL load is used. A 1nF capacitor and a 100 Ω damping resistor are added between the three phase RL load neutral point and ground to model the stray capacitance.

The EMI noise currents are measured at different interleaving angles. Fig. 2-28 and Fig. 2-29 show the measured ac side CM noise and DM noise at several typical interleaving angles and their

comparison with 0° interleaving angle, respectively. Different interleaving angles will reduce different carrier harmonics. For example, in Fig. 2-28 (a), the 60° interleaving angle eliminates the 3rd carrier harmonics and reduces the 2nd and 4th carrier harmonics by half.

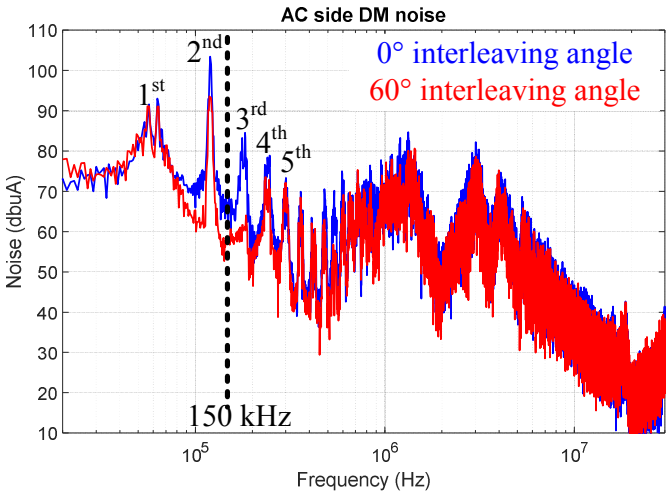


(a)

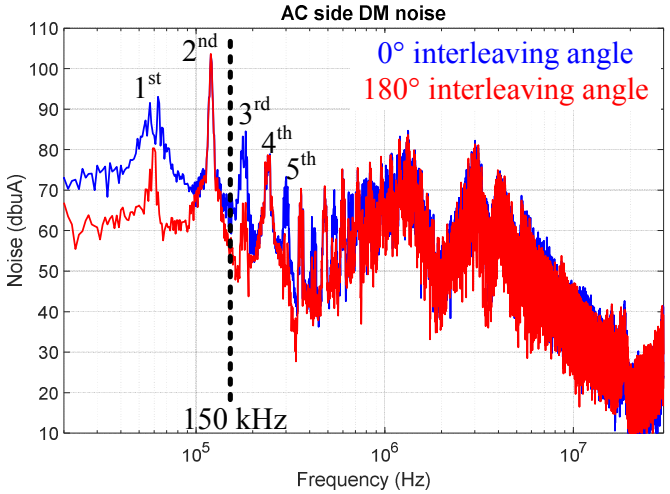


(b)

Fig. 2-28. Measured ac side CM noise at different interleaving angles and their comparison with 0° interleaving angle, (a) 60° interleaving angle, (b) 180° interleaving angle.

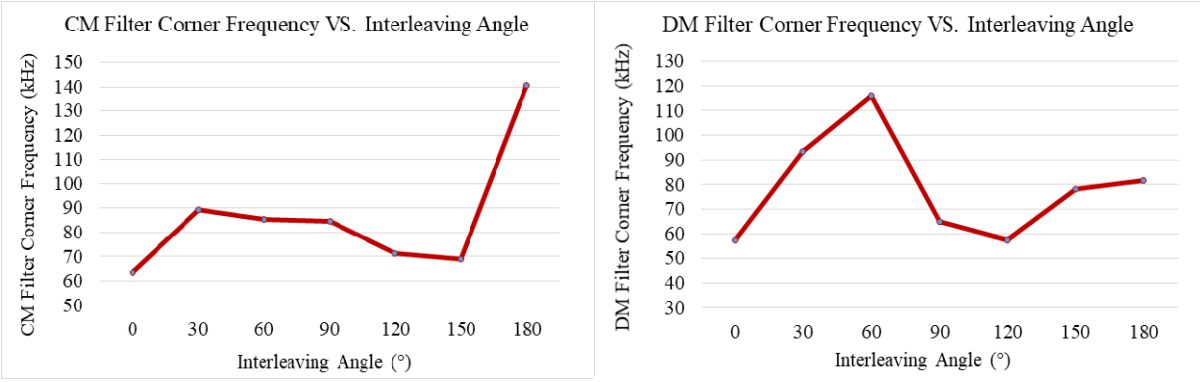


(a)



(b)

Fig. 2-29. Measured ac side DM noise at different interleaving angles and their comparison with 0° interleaving angle, (a) 60° interleaving angle, (b) 180° interleaving angle.



(a) (b)

Fig. 2-30. EMI filter corner frequency versus interleaving angles, (a) CM filter, (b) DM filter.

With the measured EMI bare noises, EMI filter corner frequency can be determined. Fig. 2-30 summarizes the CM filter corner frequency and DM filter corner frequency at different interleaving angles when one stage filter assumed. The trends match the conclusion in aforementioned analysis. With 60 kHz switching frequency, the CM filter corner frequency peak is achieved when interleaving angle is around 180°, and the second optimal interleaving angle range is 30°~90°. The DM filter corner frequency peak is obtained when interleaving angle range is around 30°~60°, and the second optimal interleaving angle range is around 120°~180°.

2.5 Conclusion

This chapter presents the modeling and reduction of harmonics in paralleled and interleaved three-level NPC inverters with SVM.

First, the analytical models for harmonics calculation of three-level NPC inverter with SVM are developed, and the unique dc current harmonics characteristic of NPC inverter are identified. Accuracy of the models are experimentally verified.

Second, the impact of interleaving angle on ac voltage and dc current harmonics are comprehensively studied. The optimal interleaving angle to reduce dc-link capacitor high frequency current ripple is derived and experimentally verified, which is highly dependent on power factor and modulation index and different from the two-level inverter case. For example, at high modulation index, optimal interleaving angle range is around 180° and around 90° for high power factor and low power factor, respectively. However, in two-level inverter, the conclusion is opposite - the optimal interleaving angle range is around 90° and around 180° for high power factor and low power factor, respectively.

Third, the impact of switching frequency and interleaving angle on EMI harmonics are analytically studied. The optimal interleaving angle ranges for CM and DM filter corner frequency are also derived and experimentally verified, which is highly dependent on switching frequency. For example, with 60 kHz switching frequency and impedance resonance well damped, around 180° and 30°~90° interleaving angle ranges are preferred for CM filter, and 30°~60° and 120°~180° interleaving angle ranges are preferred for DM filter.

3. Space Vector Modulation to Reduce Circulating Current, CM Voltage, and Switching Loss for Paralleled Three-Level Inverters

Circulating current exists when paralleled inverters have common dc and ac sides. Circulating current will distort the output currents, and degrade the paralleled inverter system performance. The low frequency circulating current can only be suppressed with control method. In addition to suppress the circulating current, reduce CMV and switching loss are also preferred to achieve high power density for the inverter system. The CMV generated by PWM switching actions may lead to problems such as the EMI noise, motor shaft voltage and bearing current in motor drive applications. Reducing CMV will reduce motor shaft voltage, reduce the required EMI filter, and increase system reliability and power density. Reducing converter switching loss leads to higher efficiency or smaller cooling system, and thus improves inverter system power density. However, conventional modulation and control method cannot achieve these control objectives in addition to suppress the low frequency circulating current.

To overcome this limit and furthering previous study, this chapter proposes a space vector modulation which is capable to reduce the low frequency ZSCC, CMV, and inverter switching loss simultaneously for paralleled three-level inverters.

3.1 Conventional Modulation Methods for Three-Level Inverter

Fig. 3-1 shows the paralleled three-level active NPC inverters topology. Fig. 3-2 shows the space vectors of the three-level NPC converter, where P, O, and N represents voltage outputs of $+V_{dc}/2$, 0, and $-V_{dc}/2$, respectively. There are total 27 switching states which grouped to 19

vectors including six long vectors, six medium vectors, six small vectors, and one zero vectors. The small and zero vectors have redundant switching states. The vector hexagon is divided into six sectors. Each of them is further divided into four small subsectors. The CMV is defined as

$$V_{CM} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \qquad (3-1)$$

where V_{ao}, V_{bo}, and V_{co} are inverter output voltages. The CMV levels of different switching state are summarized in Table 3-1.

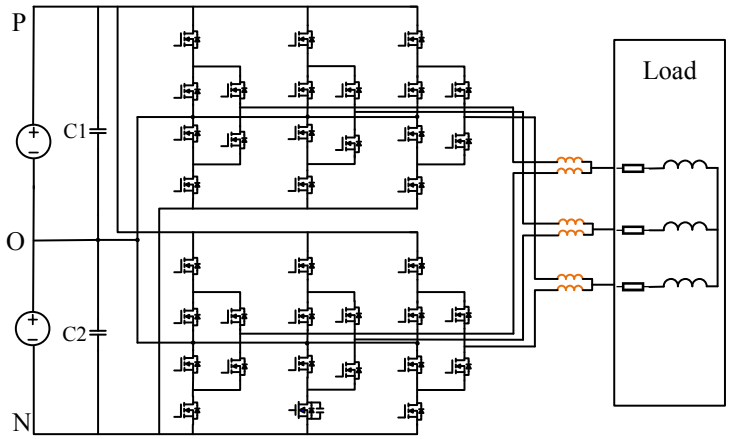


Fig. 3-1. Paralleled three-level active NPC inverters.

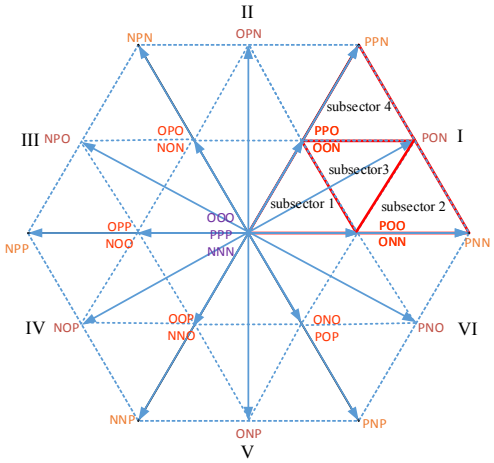


Fig. 3-2. Space vectors of three-level inverter.

Table 3-1. CMV Levels of Different Switching States

Vectors	Switching State	CMV Level
Large	PPN, NPP, PNP	$+V_{dc}/6$
	NPP, NNP, PNP	$-V_{dc}/6$
Medium	PON, OPN, NPO,	0
	NOP, ONP, PNO	
Small	POO, OPO, OOP	$+V_{dc}/6$
	OON, ONO, OON	$-V_{dc}/6$
	PPO, OPP, POP	$+V_{dc}/3$
	ONN, NON, NNO	$-V_{dc}/3$
Zero	OOO	0
	PPP	$+V_{dc}/2$
	NNN	$-V_{dc}/2$

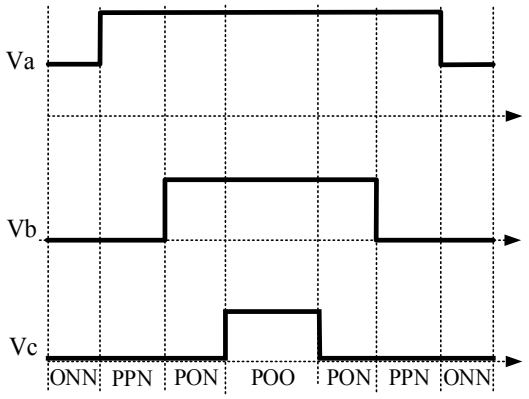
3.1.1 NTSV and PDPWM

The symmetric NTSV method uses the nearest three vectors in each subsector to synthesize the reference voltage, and both redundant switching states of the small vector are used. For example, in sector I subsector 2, the vectors POO/ONN, PON, and PNN are selected and the PWM sequences for three phases are shown as Fig. 3-3(a). The vectors for this modulation is equivalent to the carrier based phase deposition PWM (PDPWM), which use two carriers with phase deposition to synthesize the voltage reference as shown in Fig. 3-3(b). The modulation voltage reference are noted as V_a^*, V_b^*, and V_c^*.

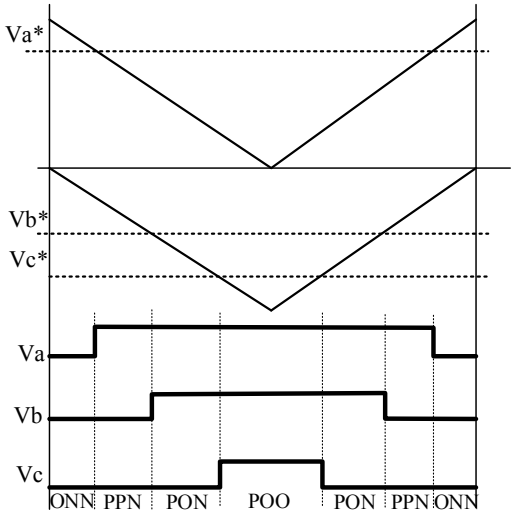
The key to achieve low frequency ZSCC control is that the modulation needs to have adjustable

AZSV in every switching cycle. For NTSV, the AZSV can be adjusted by adjusting the dwell time of the two redundant switching states of small vector (for example, POO/ONN). For PDPWM, adjusting the AZSV is realized by adjusting the injected zero-sequence voltage to the sinusoidal modulation reference.

In conclusion, the NTSV and PDPWM methods have the ZSCC control capability. However, the NTSV and PDPWM methods have a CMV amplitude of $V_{dc}/3$, and six switching actions in one switching cycle. Therefore, these modulations cannot reduce the CMV and switching loss.



(a)



(b)

Fig. 3-3. (a) PWM sequences of NTSV, (b) PWM sequences of carrier based PDPWM.

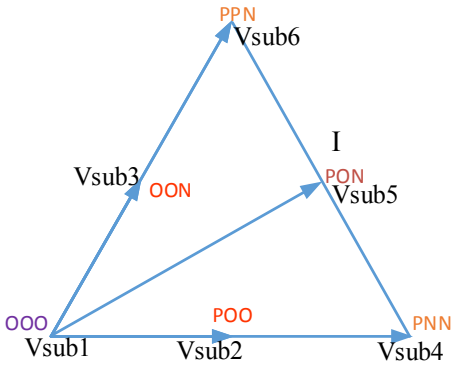
3.1.2 LMSZVM and PODPWM

The LMSZVM method uses large, medium, small, and zero vector in each sector to synthesize the voltage. Fig. 3-4(a) shows the vectors in sector I. The vectors for this modulation is actually equivalent to the carrier based phase opposite deposition PWM (PODPWM), which use two carriers with opposite deposition to synthesize the voltage reference as shown in Fig. 3-4(c). The switching state of the small vector which has lower CMV amplitude is selected (POO or OON for sector I). Thus, the CMV amplitude of this method is reduced to $V_{dc}/6$.

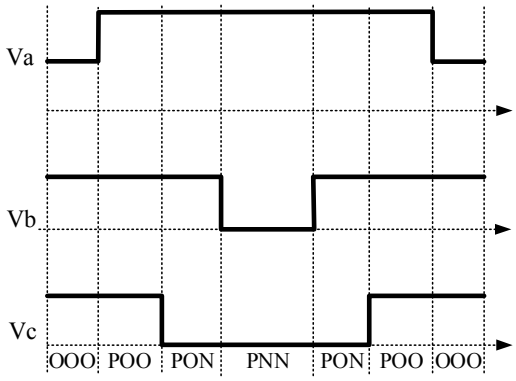
For LMSZVM, the AZSV can be adjusted by adjusting the dwell time of the small vector. Fig. 3-4(b) shows the PWM sequences of three phases in sector I when small vector POO is selected. Similarly, for PODPWM, adjusting the AZSV is realized by adjusting the injected zero-sequence voltage to the sinusoidal modulation reference.

The LMSZVM and PODPWM method does not further divide each sector into four subsectors like the regular three-level SVMs. Thus, it actually doesn't use the nearest three vectors. Also, this modulation has six switching actions in one switching cycle even in the case that the circulating current is very small and the dwell time of the small vector is zero.

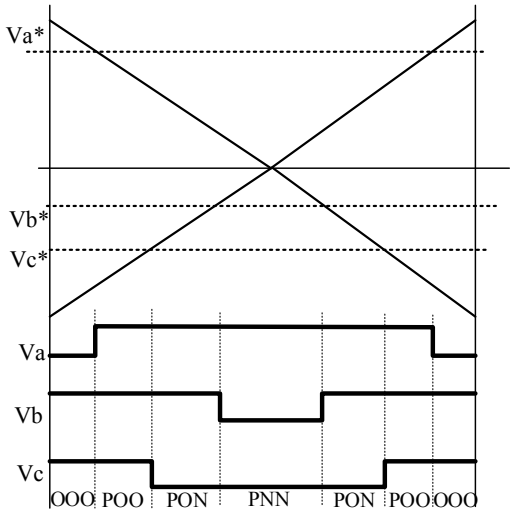
In conclusion, the LMSZVM and PODPWM method have the ZSCC control capability and reduced CMV. However, this modulation method cannot reduce switching loss.



(a)



(b)

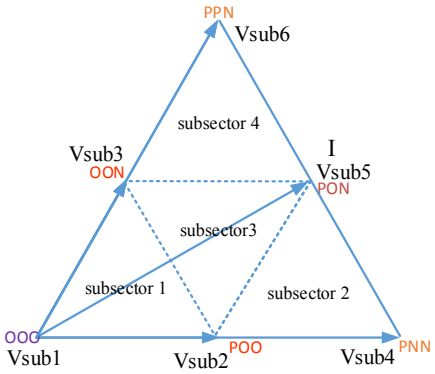


(c)

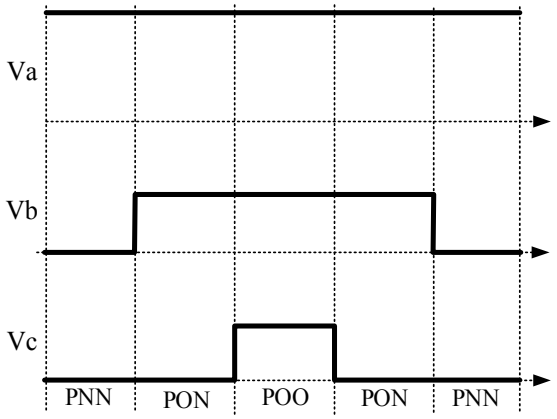
Fig. 3-4. (a) Vectors of LMSZVM in sector I, (b) PWM sequences of LMSZVM, (c) PWM sequences of carrier based PODPWM.

3.1.3 CMR Modulation

The CMR modulation uses the nearest three vectors in each subsector to synthesize the reference voltage, and the redundant switching sate of the small vector with lower CMV amplitude are used. Thus, the CMV amplitude of this modulation is also reduced to $V_{dc}/6$. Fig. 3-5(a) shows the vectors in sector I, and Fig. 3-5(b) shows the PWM sequences for three phases of sector I subsector 2. As shown in Fig. 3-5(b), there is always one phase clamped to P or O or N and there are four switching actions in one switching cycle.



(a)



(b)

Fig. 3-5. (a) Vectors of CMR modulation in sector I, (b) PWM sequences of CMR in sector I subsector 2.

The CMR modulation uses three vectors to synthesize the reference voltage and has no redundant switching state. When the reference voltage is determined, the dwell times of all the vectors used are fixed and the AZSV is fixed. Thus, CMR modulation loses the ZSCC control capability.

In conclusion, the CMR method has reduced CMV and reduced switching loss, but cannot control ZSCC.

3.2 Proposed Space Vector Modulation

By reviewing the conventional modulation methods in last section, CMR modulation can reduce CMV and switching loss and is preferred for motor drive in aircraft applications. However, CMR modulation does not have ZSCC control capability and cannot be applied to the paralleled three-level inverters for suppressing low frequency ZSCC. This section proposes a space vector modulation which modifies the CMR modulation and thus ZSCC control can be achieved.

3.2.1 Optimal Fourth Space Vector

The basic idea to obtain ZSCC control capability is to introduce a fourth space vector to the three existing vectors of CMR modulation. Adding a fourth vector creates a dimension of freedom and thus adjustable AZSV in each switching cycle can be achieved.

To better illustrate the selection of optimal fourth space vector, the dwell time calculation of the CMR modulation is briefly discussed. For the CMR modulation as shown in Fig. 5, take subsector 2 of sector I as an example, the dwell times of the three vectors can be calculated based on the volt-second balance principle as shown in (3-2).

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{sub2}}T_{sub2} + \overrightarrow{V_{sub4}}T_{sub4} + \overrightarrow{V_{sub5}}T_{sub5}$$

$$T_s = T_{sub2} + T_{sub4} + T_{sub5} \quad (3-2)$$

where $\overrightarrow{V_{sub2}}$ represents the vector POO, the labels for other vectors are shown in Fig. 5(a). The dwell times of the three vectors $\overrightarrow{V_{sub2}}$, $\overrightarrow{V_{sub4}}$, and $\overrightarrow{V_{sub5}}$ are denoted by T_{sub2}, T_{sub4}, and T_{sub5}, respectively. To simplify the calculation, three temporary constants t_x, t_y, t_z are defined as (3-3).

$$t_x = 2\sqrt{3}Msin\theta$$

$$t_y = 3Mcos\theta + \sqrt{3}Msin\theta$$

$$t_z = 3Mcos\theta - \sqrt{3}Msin\theta \quad (3-3)$$

where M is the modulation index, and θ represents the angle between the reference and d-axis.

Then, the vectors dwell times in subsector 2 sector I are denoted as (3-4). As the dwell times are fixed, AZSV is fixed and CMR modulation loses the ZSCC control capability.

$$T_{sub2} = (2 - t_y)T_s$$

$$T_{sub4} = (t_z - 1)T_s$$

$$T_{sub5} = t_x T_s \quad (3-4)$$

Based on the requirements, the optimal fourth vector needs to satisfy the following constraints: (a) the CMV amplitude of the fourth vector should be zero or $V_{dc}/6$; (b) the fourth vector should be not far away from the existing three vectors of CMR modulation in the vector plane; (c) after added, there should be no transition directly from P to N or N to P in each phase; (d) after added, the switching actions should be no more than six times in one switching cycle; (e) after added, the modulation should have adjustable AZSV in every switching cycle.

The optimal fourth vector for each subsector in sector I is investigated. For subsector 2 as shown in Fig. 3-5(a), the three existing vectors are POO, PON, and PNN. To meet constraint (a) and (b),

the fourth vector candidates could be OOO, OON, PPN, OPN, PNO, ONO, and PNP. Then, to meet constraint (c), the remaining vectors are OOO, OON, PNO, and ONO. Then, to meet constraint (d), the remaining vectors are OOO and PNO. Now the constraint (e) is investigated.

First, considering PNO is selected as the fourth vector. Based on the volt-second balance principle, (3-5) can be derived. The vector PNO and its dwell time are indicated as $\overrightarrow{V_{sub0}}$ and T_{sub0}, respectively.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{sub2}}T_{sub2} + \overrightarrow{V_{sub4}}T_{sub4} + \overrightarrow{V_{sub5}}T_{sub5} + \overrightarrow{V_{sub0}}T_{sub0}$$

$$T_s = T_{sub2} + T_{sub4} + T_{sub5} + T_{sub0} \quad (3-5)$$

There is non-unique solution for (3-5), and (3-6) can be derived.

$$T_{sub0} + T_{sub2} = (2 - t_y)T_s \quad (3-6)$$

Define a variable k so that

$$T_{sub0} = k(2 - t_y)T_s \quad (3-7)$$

Then, based on (3-5) and (3-7), the dwell time of other three vectors are calculated as (3-8).

$$T_{sub2} = (1 - k)(2 - t_y)T_s$$

$$T_{sub4} = (\mathrm{t}_z - 1 - k(2 - t_y))T_s$$

$$T_{sub5} = \left(\mathrm{t}_x + k(2 - t_y)\right)T_s \quad (3-8)$$

The variable k indicates the dwell time of the fourth vector $\overrightarrow{V_{sub0}}$ (PNO), from (3-8), when k changes, the dwell times of the other three vectors will also change.

The CMV level of $\overrightarrow{V_{sub2}}$, $\overrightarrow{V_{sub4}}$, $\overrightarrow{V_{sub5}}$, and $\overrightarrow{V_{sub0}}$ are $V_{dc}/6$, $-V_{dc}/6$, 0, and 0, respectively. The AZSV in subsector 2 can be expressed as (3-9).

$$AZSV_{subsector2} = \frac{V_{dc}\left(\frac{1}{6}T_{sub2} - \frac{1}{6}T_{sub4} + 0 \cdot T_{sub5} + 0 \cdot T_{sub0}\right)}{T_s} \quad (3-9)$$

Substituting (3-8) to (3-9), it can be derived that

$$AZSV_{subsector2} = \frac{V_{dc}(3 - t_y - t_z)}{6T_s} \quad (3-10)$$

From (3-10), the variable k is cancelled in the equation and AZSV is a constant, which means that adjustable AZSV and ZSCC control cannot be achieved.

Second, considering OOO is selected as the fourth vector. Similarly, (3-11) can be derived. The vector OOO and its dwell time are indicated as $\overrightarrow{V_{sub1}}$ and T_{sub1}, respectively.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{sub2}}T_{sub2} + \overrightarrow{V_{sub4}}T_{sub4} + \overrightarrow{V_{sub5}}T_{sub5} + \overrightarrow{V_{sub1}}T_{sub1}$$

$$T_s = T_{sub2} + T_{sub4} + T_{sub5} + T_{sub1} \quad (3-11)$$

There is non-unique solution for (3-11) and (3-12) can be derived.

$$2T_{sub1} + T_{sub2} = (2 - t_y)T_s \quad (3-12)$$

Define the variable k so that

$$T_{sub1} = k(1 - t_y/2)T_s \quad (3-13)$$

Then, dwell times of other three vectors are calculated as (3-14).

$$T_{sub2} = (1-k)(2 - t_y)T_s$$

$$T_{sub4} = \left(t_z - t_x - (1-k)(2 - t_y)\right)T_s/2$$

$$T_{sub5} = t_x T_s \quad (3-14)$$

From (3-14), when k changes, the dwell times of $\overrightarrow{V_{sub2}}$ and $\overrightarrow{V_{sub4}}$ will also change while the

dwell time of $\overrightarrow{V_{sub5}}$ is a constant.

The AZSV in subsector 2 with the fourth vector OOO is calculated as (3-15).

$$AZSV_{subsector2} = \frac{V_{dc}\left(3(1-k)\left(2-t_y\right)+t_x-t_z\right)}{12T_s} \qquad (3-15)$$

The variable k will impact the AZSV. When k increases AZSV decreases, adjustable AZSV and ZSCC control can be achieved in every switching cycle.

Therefore, the vector OOO is the only vector that can meet all the constraints and is the optimal fourth vector for subsector 2. The vector OOO is also the optimal vector for subsector 4 due to the symmetry.

For subsector 3, the three existing vectors are OON, PON, and POO. To meet constraint (a), (b) and (c), the fourth vector candidates could be OOO, PNN, PPN, OPN, and PNO. Then, to meet constraint (d), the remaining vectors are OOO, OPN, and PNO. Now the constraint (e) is investigated.

First, considering OPN is selected as the fourth vector. The relationship in (3-16) can be derived. The vector OPN and its dwell time are indicated as $\overrightarrow{V_{sub0}}$ and T_{sub0}, respectively.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{sub2}}T_{sub2} + \overrightarrow{V_{sub3}}T_{sub3} + \overrightarrow{V_{sub5}}T_{sub5} + \overrightarrow{V_{sub0}}T_{sub0}$$

$$T_s = T_{sub2} + T_{sub3} + T_{sub5} + T_{sub0} \qquad (3-16)$$

There is non-unique solution for (3-16) and (3-17) can be derived.

$$2T_{sub0} + T_{sub3} = (1-t_z)T_s \qquad (3-17)$$

Define a variable k so that

$$T_{sub0} = k(1-t_z)T_s/2 \qquad (3-18)$$

Then, dwell time of other three vectors are calculated as (4-19).

$$T_{sub3} = (1-k)(1-t_z)T_s$$

$$T_{sub2} = \left(3 - \mathrm{t}_x - \mathrm{t}_y - (1-k)(1-t_z)\right)T_s/2$$

$$T_{sub5} = \left(\mathrm{t}_y - 1\right)T_s \qquad (3-19)$$

The AZSV in subsector 3 with the fourth vector OPN is calculated as (3-20).

$$AZSV_{subsector3} = \frac{V_{dc}\left(3 - t_x - t_y - 3(1-k)(1-t_z\right)}{12T_s} \qquad (3-20)$$

From (3-20), the variable k will impact the AZSV, and adjustable AZSV and ZSCC control can be achieved in every switching cycle.

When vector PNO is selected as the fourth vector, the situation is similar as OPN due to the symmetry, ZSCC control can also be achieved.

Second, considering OOO is selected as the fourth vector. (3-21) can be derived.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{sub2}}T_{sub2} + \overrightarrow{V_{sub3}}T_{sub3} + \overrightarrow{V_{sub5}}T_{sub5} + \overrightarrow{V_{sub1}}T_{sub1}$$

$$T_s = T_{sub2} + T_{sub3} + T_{sub5} + T_{sub1} \qquad (3-21)$$

Based on (3-21), (3-22) can be derived.

$$T_{sub1} + T_{sub2} = (1-t_x)T_s \qquad (3-22)$$

Define a variable k so that

$$T_{sub1} = \mathrm{k}(1-t_x)T_s \qquad (3-23)$$

Then, dwell times of other three vectors are calculated as (3-24).

$$T_{sub2} = (1-k)(1-t_x)T_s$$

$$T_{sub3} = \left(\mathrm{t}_x - \mathrm{t}_z + (1-k)(1-t_x)\right)T_s$$

$$T_{sub5} = \left(\mathrm{t}_z - (1-k)(1-t_x)\right)T_s \qquad (3-24)$$

The AZSV in subsector 3 with the fourth vector OOO is calculated as (3-25)

$$AZSV_{subsector3} = \frac{V_{dc}(t_z - t_x)}{6T_s} \qquad (3-25)$$

Although variable k will impact dwell times of all the vectors, from (3-25), the variable k is cancelled and AZSV is a constant. Thus, adjustable AZSV and ZSCC control cannot be achieved.

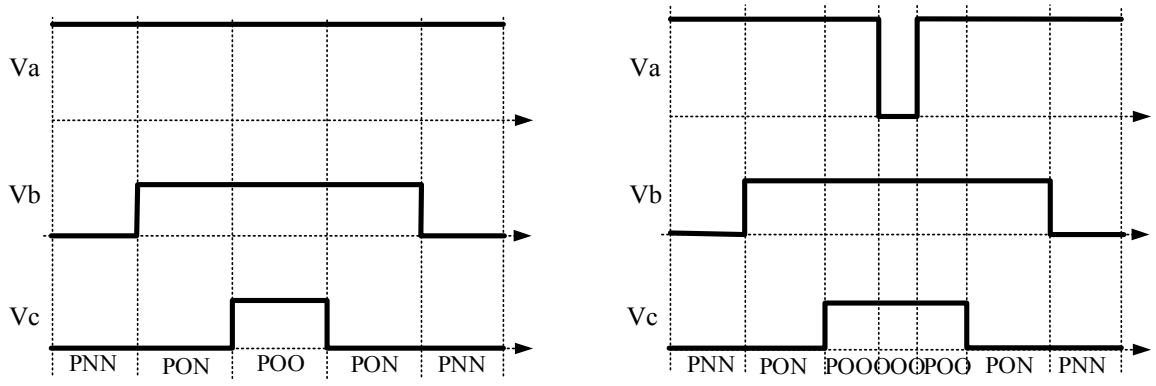
Therefore, the vector OPN and PNO are the only two vectors that can meet all the constraints and are the optimal fourth vectors for subsector 3. OPN and PNO are also the optimal vectors for subsector 1 due to the symmetry.

In conclusion, the optimal fourth vector for subsector 1 and subsector 3 is OPN or PNO, and the optimal fourth vector for subsector 2 and subsector 4 is OOO. Due to the symmetric, the optimal fourth vector for other sectors can be analyzed with the same procedure. It can be conclude that for subsector 2 and subsector 4 of all the six sectors, the optimal fourth vector is OOO. If OPN is selected as the optimal fourth vector for subsector 3 and subsector 1 of sector I, the optimal fourth vector will be NPO, NOP, ONP, PNO, and PON for subsector 3 and subsector 1 from sector II to sector VI.

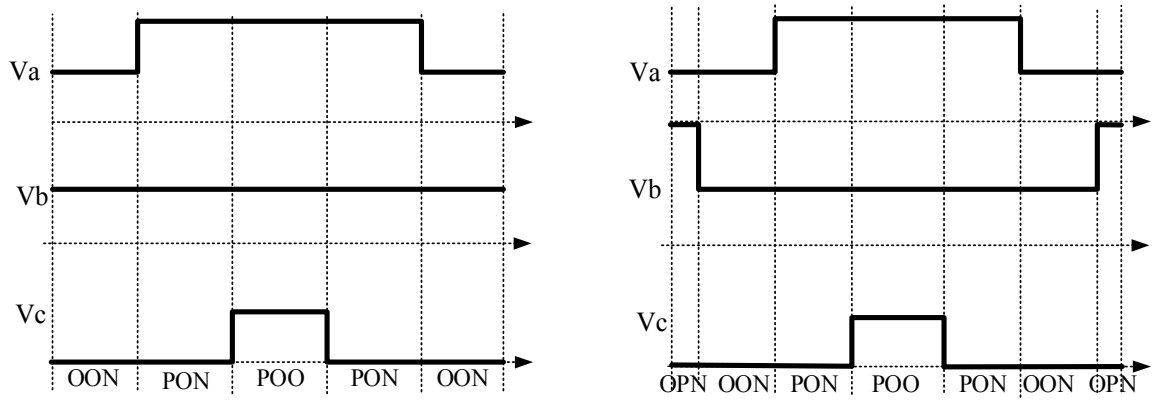
Table 3-2 lists the PWM sequences of the proposed modulation in sector I. The three phase voltages PWM pattern of the proposed modulation and its comparison to CMR modulation are shown in Fig. 3-6.

Table 3-2. PWM Sequences of Proposed Modulation (Sector I)

Subsector	PWM Sequences
2	PNN, PON, POO, OOO, POO, PON, PNN
3	OPN, OON, PON, POO, PON, OON, OPN
4	OOO, OON, PON, PPN, PON, OON, OOO
1	OPN, OON, OOO, POO, OOO, OON, OPN

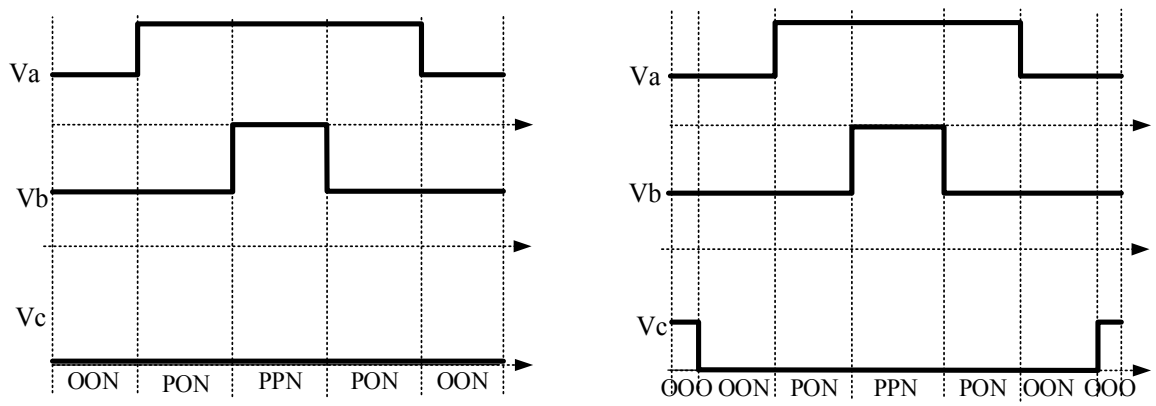


(a)

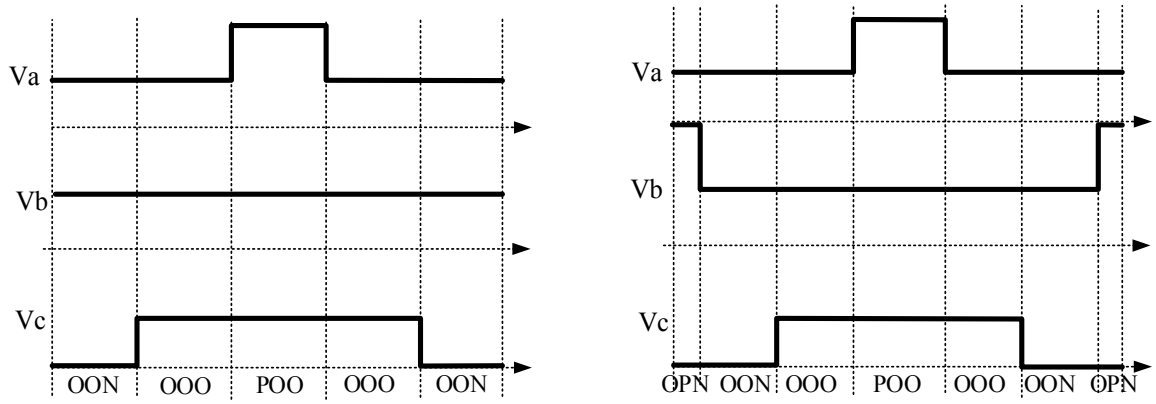


(b)

Fig. 3-6. Comparison of CMR modulation (left) and the proposed modulation (right) in sector I, (a) subsector 2, (b) subsector 3, (c) subsector 4, and (d) subsector 1.



(c)



(d)

Fig. 3-6. Continued.

The dwell time of the added fourth vector is a variable and can be regulated by the ZSCC control loop. From Fig. 3-6, the proposed modulation modifies the PWM pattern of the phase which is clamped to P or O or N in the CMR modulation, and does not change the PWM pattern of other two phases. The added fourth vector increase the switching actions from four to six times in one switching cycle. However, when the circulating current is small and within the limit value, the ZSCC control will not regulate and the dwell time of the fourth vector will be zero. The switching

action will still be four times in one switching cycle. When the circulating current is not small and the ZSCC control regulates, one inverter will have four switching actions and the other inverter will have six switching actions. Thus, switching loss will still be reduced. Controller Implementation

The dwell time of the fourth vector is indicated by the variable k, which has a linear relationship with AZSV. From (3-15), (3-20), (3-32), and (3-37), it can be conclude that the AZSV will decrease when k increases in subsector 2 while the AZSV will increase when k increases in subsector 1, subsector 3, and subsector 4 of sector I. The relationship between k and the AZSV in other sectors can be calculated with the same procedure. Table 3-3 summarizes how k impact the AZSV in all sectors.

The zero-axis current loop for paralleled inverters is a first-order system as discussed in previous literature. The ZSCC control block diagram is shown in Fig. 3-7. The ZSCC controller can be a PI controller or deadbeat controller. Assume the ZSCC controller output is variable c as shown in Fig. 3-7. To combine the proposed modulation and ZSCC closed loop control, the relationship between controller output c and variable k need to be established.

Table 3-3. Impact of k on AZSV at Different Sectors

sector	subsector	k	AZSV
I, III, V	2	↑	↓
	1, 3, 4	↑	↑
II, IV, VI	2	↑	↑
	1, 3, 4	↑	↓

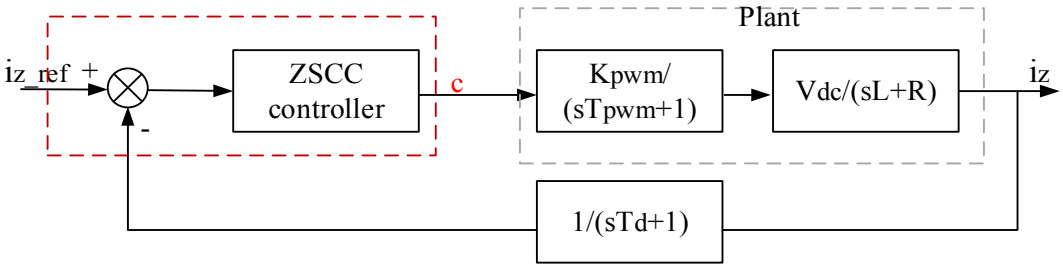


Fig. 3-7. ZSCC control block diagram.

As discussed, when the measured ZSCC i_z is small and within the limit i_{z_limit}, the ZSCC control is not required. Then, $k = 0$, the proposed modulation is the same as the CMR modulation. The total switching actions in one switching cycle for two converters reduce to eight times.

When the measured ZSCC i_z exceeds the limit i_{z_limit}, the ZSCC control works. When the ZSCC of one inverter is smaller than 0, which means that the AZSV of this inverter is smaller than another inverter. Then, the ZSCC controller output c of this inverter will increase to increase the AZSV, and the ZSCC will be regulated to approach zero. According to relationship between k and AZSV in table III, let $k = c$ if the reference is located in subsector 1, subsector 3, and subsector 4 of sector I, sector III, and sector V or in subsector 2 of sector II, sector IV, and sector VI. Then, k increases and AZSV increases, the control goal is achieved. Let $k = -c$ if the reference is located in subsector 2 of sector I, sector III, and sector V or in subsector 1, subsector 3, and subsector 4 of sector II, sector IV, and sector VI. Then, k decreases and AZSV increases, the control goal is achieved. When the ZSCC of one inverter is larger than 0, the analysis is similar.

In summary, let $k = c$ when the reference is located in subsectors that AZSV and k has a positive coefficient, and let $k = -c$ when the reference is located in subsectors that AZSV and k has a negative coefficient.

As c could be either larger than 0 or smaller than 0, but $0 \leq k \leq 1$ need to be satisfied based on its definition. Assuming at some time constant the ZSCC of inverter 1 is larger than 0 and thus controller output c is smaller than 0, the reference is located in the subsector that $k = c$. Then, k will be smaller than 0. In this case, let $k = 0$ for inverter 1, which means the PWM pattern of inverter 1 is the same of CMR modulation. However, the ZSCC is still controllable because at the same time the ZSCC of inverter 2 is smaller than 0 and thus controller output c is larger than 0. Then, k of inverter 2 will be larger than 0. The AZSV of inverter 2 will increase to regulate the ZSCC approaching 0.

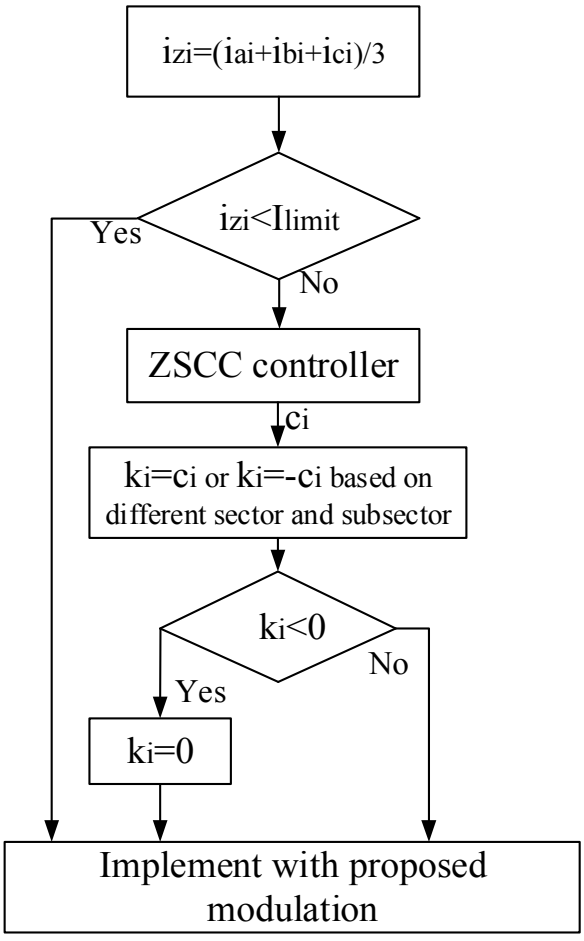


Fig. 3-8. Flow chart to combine proposed modulation and control.

Based on this analysis, Fig. 3-8 illustrates the flowchart to determine variable k of the proposed modulation. The index i as shown in Fig. 3-8 indicates the ith inverter. For two paralleled inverters, there is at least one inverter that keeps $k = 0$ when ZSCC control works. With proposed modulation and control, the switching actions of two inverters reduce to eight times or ten times from twelve times of the conventional modulation. For each inverter, it only needs the current information of its own and the current information of other inverters are not required. Therefore, the control strategy can be applied to multiple paralleled inverters.

3.2.2 Discuss on Neutral Point Voltage Balance

For motor drive in aircraft applications, the input dc source is three wire plus/minus configuration as shown in Fig. 3-1. Hence, the two capacitor voltages of three-level NPC inverter are forced to be balanced. No extra NP balancing control is needed. To not lose generality for other applications where the dc-link neutral point is floating, the NP voltage balance is briefly discussed in this section.

There is similarity between the ZSCC control and NP voltage balancing control of three-level NPC inverters. The NP voltage balance problem is thoroughly studied in previous literature. The essence of NP voltage balancing methods is the same as the ZSCC control methods – zero sequence adjusting. The control goal can be achieved by adjusting the injected zero-sequence voltage for carrier based PWM or adjusting the dwell time of redundant vectors for space vector based PWM. The difference between the ZSCC control and NP voltage balancing control is just that ZSCC is dependent on zero sequence voltage while NP voltage is dependent on zero sequence current. Previous literature has shown that modulation with ZSCC control capability can actually control the NP voltage.

How the proposed modulation impacts and controls the NP voltage balance is discussed in this section. For simplification, only the case that the output voltage and current has the same polarity is analyzed. When the load power factor is not unity there is a chance that the output voltage and current have different polarity. However, the analysis method is the same.

The NP voltage will be influenced when output current is connected to the NP point. As shown in Fig. 3-9, point O is the neutral point. If the averaged NP current $\overline{i_n}$ in a switching cycle is larger than zero, the lower capacitor is discharged and V_{c2} decreases. If $\overline{i_n}$ is smaller than zero, the lower capacitor is charged and V_{c2} increases. The impact of variable k on NP voltage V_{c2} is investigated using sector I as an example.

For subsector 2, vectors OOO and PNN will not impact the NP voltage, and vector PON dwell time is not impacted by variable *k* based on (3-14). Hence, variable *k* actually impacts the NP voltage by adjusting the dwell time of vector POO. Vector POO charges the lower capacitor and V_{c2} increases. Therefore, when variable k increases, T_{sub2} (dwell time of POO) decreases based on (3-14), then V_{c2} decreases.

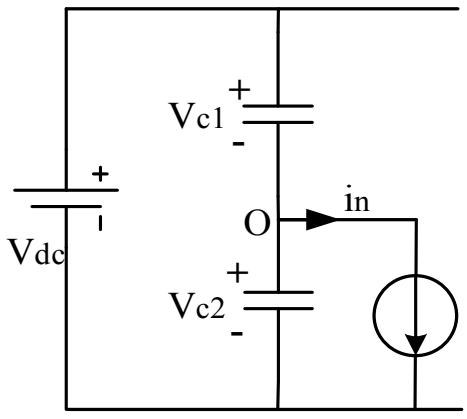


Fig. 3-9. NP in the three-level inverter.

For subsector 4, the analysis is similar to subsector 2. Variable k actually impacts the NP voltage by adjusting the dwell time of vector OON. When variable k increases, T_{sub3} (dwell time of OON) decreases, then V_{c2} increases.

For subsector 3, when variable k changes, the dwell times of vectors OPN, POO and OON will change while the dwell time of vector PON is not impacted based on (3-19). Thus, variable k impacts the NP voltage by adjusting the dwell times of OPN, POO and OON. The averaged NP current $\overline{i_n}$ is formed by (3-26).

$$\overline{i_n} = T_{sub0} i_a + T_{sub2}(-i_a) + T_{sub3}(-i_c) + T_{sub5} i_b \qquad (3-26)$$

where T_{sub0}, T_{sub2}, T_{sub3}, and T_{sub5} represents the dwell times of vectors OPN, POO, OON, and PON, respectively. The three phase output currents are indicated by i_a, i_b, and i_c.

Based on (3-19), (3-27) is derived.

$$T_{sub0} - T_{sub2} = \frac{t_x + t_y - t_z - 2}{2} \qquad (3-27)$$

The variable k is actually cancelled in (3-27). From (3-26) and (3-27), although variable k impacts the dwell times of OPN and POO, their influence on the NP voltage cancelled with each other. Hence, variable k actually impacts the NP voltage by adjusting the dwell time of vector OON. Vector OON discharges the lower capacitor and V_{c2} decreases. Therefore, when variable k increases, T_{sub3} decreases based on (3-19), then V_{c2} increases.

For subsector 1, the analysis is similar to subsector 3. Variable k actually impacts the NP voltage by adjusting the dwell time of vector OON. When variable k increases, T_{sub3} decreases, then V_{c2} increases.

Table 3-4. Impact of k on NP Voltage at Different Sectors

sector	subsector	k	NP Voltage V_{c2}
I, III, V	2	↑	↓
	1, 3, 4	↑	↑
II, IV, VI	2	↑	↑
	1, 3, 4	↑	↓

The variable k has a linear relationship with NP voltage. Table 4-4 summarizes how k impact the NP voltage in all sectors. The trend is the same as how k impact the AZSV. Both ZSCC control and NP voltage balance control can be settled with proposed modulation. When $i_z < 0$ and $V_{c2} - V_{dc}/2 < 0$ or When $i_z > 0$ and $V_{c2} - V_{dc}/2 > 0$, the ZSCC regulation is also helpful to balance the NP voltage. When $i_z < 0$ and $V_{c2} - V_{dc}/2 > 0$ or When $i_z > 0$ and $V_{c2} - V_{dc}/2 < 0$, the variable k can be selected by the relatively higher value comparing the ZSCC controller output and NP voltage balance controller output.

3.3 Simulation and Experimental Results

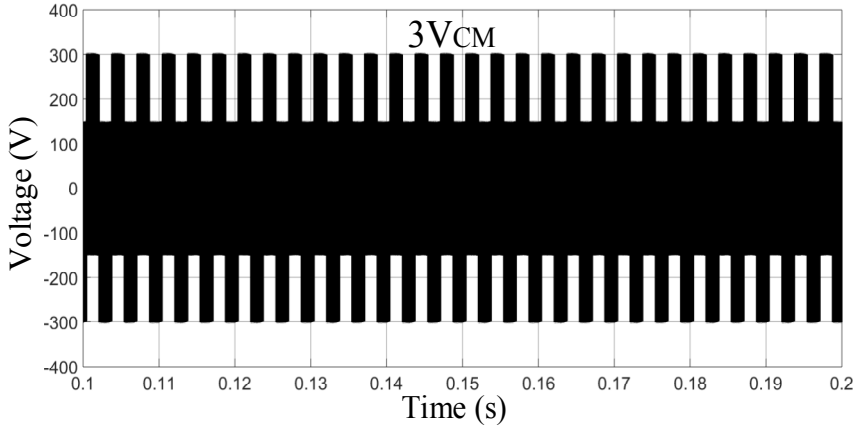
Simulation and experiments are conducted on two paralleled active NPC inverters to verify the theoretical analysis on the proposed modulation. The RL load is used for this study. Main parameters for the simulation and experiment are listed in Table 3-5.

3.3.1 Simulation Results

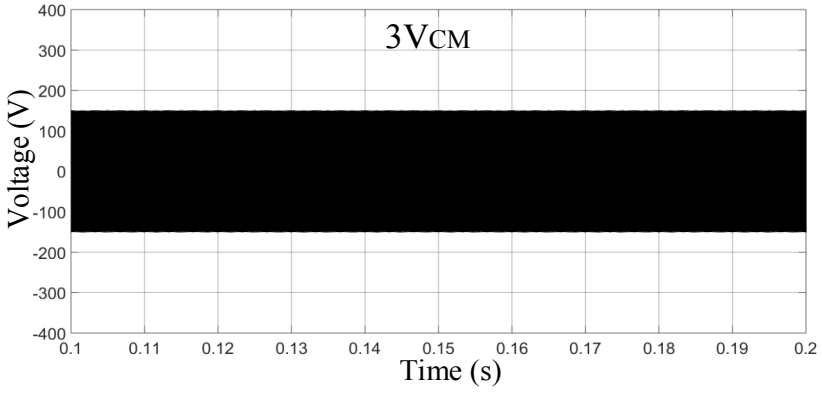
Fig. 3-10 shows the CMV comparison with NTSV modulation and the proposed modulation. CMV magnitude of the proposed modulation has been reduced to half of the NTSV modulation.

Table 3-5. Parameters for Simulation and Experiment

DC input voltage	300 V
Carrier frequency	60 kHz
Fundamental frequency	100 Hz
MOSFETs	Wolfspeed C3M0065100K
RL load	L=320 uH, R=10 Ω, each phase
Output inductor Lc	250 uH / 450 uH



(a)



(b)

Fig. 3-10. CMV level comparison, (a) with conventional NTSV modulation, (b) with the proposed modulation.

PWM mismatch is usually one of the factors causing asymmetry in paralleled inverters. In the simulation, the two inverters have different dead-time delay. Different modulation schemes including NTSV, CMR and proposed modulation are applied. The ZSCC can be suppressed with NTSV and proposed modulation.

Fig. 3-11 shows the phase output voltage comparison. The phase output voltage with proposed modulation has been clamped to P or O or N at some time, which indicates that the phase is clamped and has only four switching actions in one switching cycle at these time instants. Thus, the proposed modulation reduces switching loss compared to conventional NTSV method. The device loss with all the modulation are summarized in Table 3-6. From the results, the proposed modulation has smaller switching loss than NTSV and a little larger switching loss than CMR. The proposed modulation has smaller conduction loss than CMR due to smaller circulating current. Hence, the total loss of proposed modulation is almost equal to CMR modulation in this case. The output THD comparison with all the modulation schemes is summarized in Table 3-7. The THD of proposed modulation is higher than NTSV and almost the same as CMR.

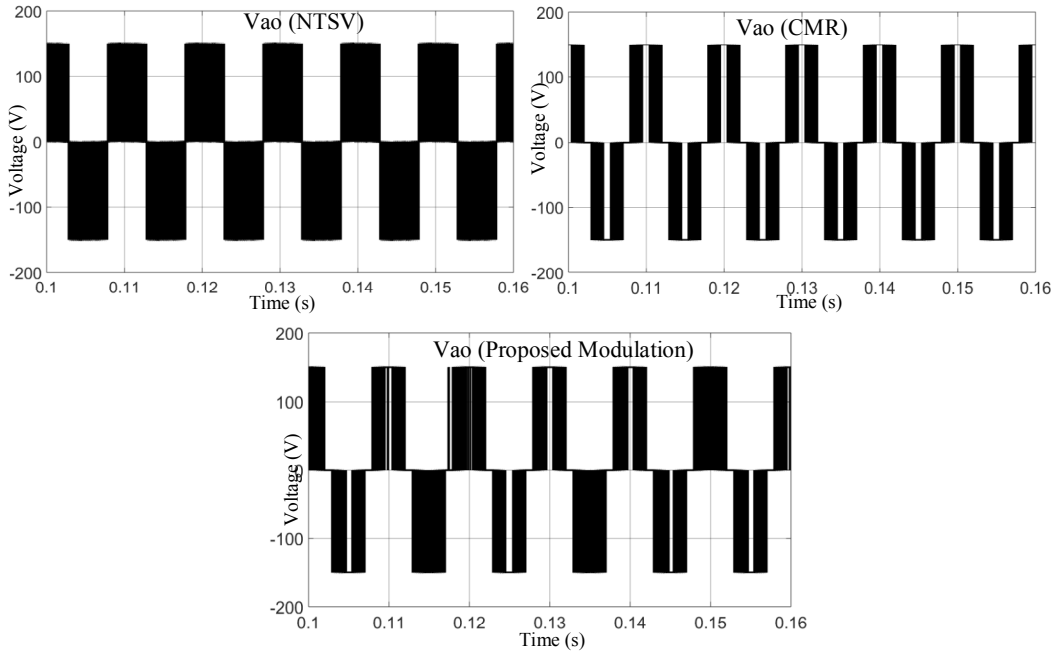


Fig. 3-11. Phase output voltage comparison - conventional NTSV modulation, CMR modulation and the proposed modulation.

Table 3-6. Devices Loss Comparison

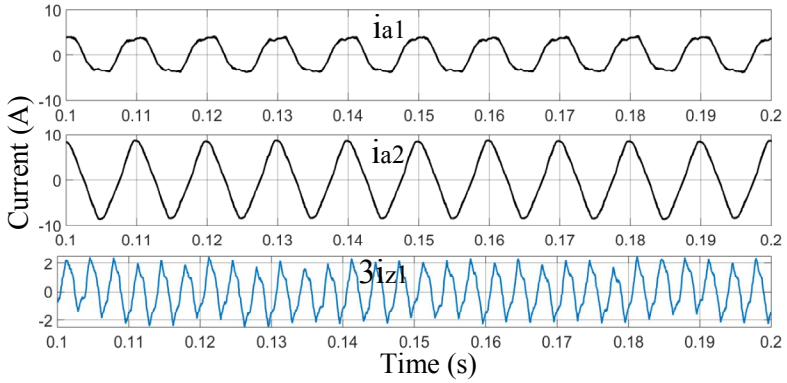
	conduction loss	switching loss	total loss
NTSV	12.5 W	7.6 W	20.1 W
CMR	13.3 W	4.6 W	17.9 W
Proposed mod.	12.7 W	5 W	17.7 W

Table 3-7. Current THD Comparison

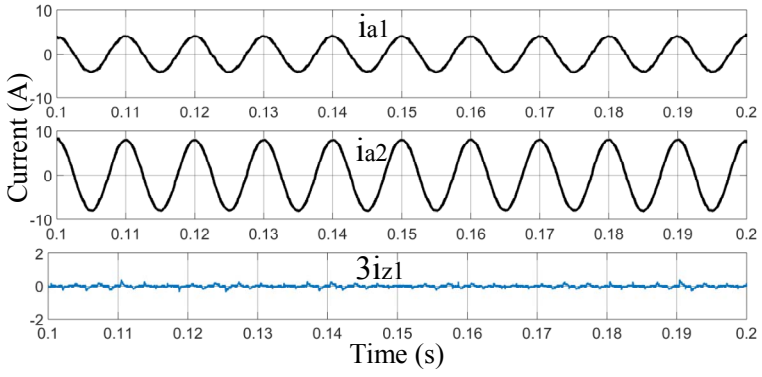
	THD of inverter 1 or inverter 2 current	THD of total output current
NTSV	2.5%	1.5%
CMR	5.2%	2%
Proposed mod.	3.5%	2.1%

To further verify the ZSCC control capability of proposed modulation, comparison is conducted with CMR modulation and with proposed modulation assuming unequal current reference. From Fig. 3-12, it can be observed that the ZSCC can be effectively controlled with proposed modulation.

To verify the analysis on neutral point voltage balancing capability of the proposed method, the simulation is conducted which the neutral point is floating. The initial voltages of the two capacitor are set to be different values. Fig .3-13 shows the results with the proposed modulation and control strategy. The voltages of the two capacitors can be well regulated and balanced.



(a)



(b)

Fig. 3-12. Phase output currents and ZSCC with unequal current reference, $I_{1\_ref} = 4\ A$, $I_{2\_ref} = 8\ A$, (a) with CMR modulation, (b) with the proposed modulation.

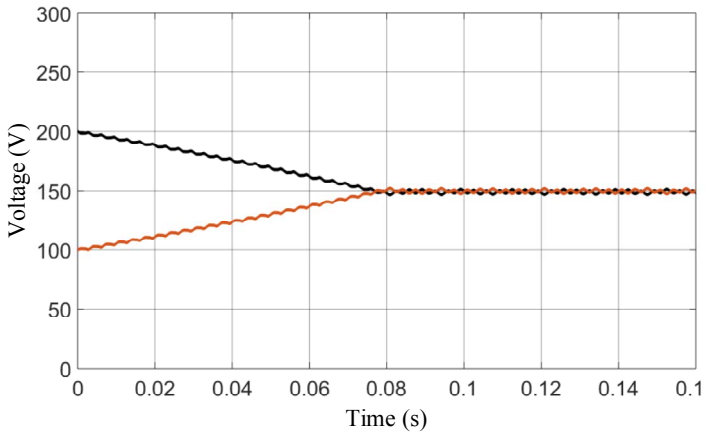


Fig. 3-13. Voltages of the two dc-link capacitors.

3.3.2 Experimental Results

Two paralleled three-level NPC inverters are constructed for experiment. Fig. 3-14 shows three phases output voltages and CMV when the conventional NTSV modulation is applied. Fig. 3-15 shows three phases output voltages and CMV when the proposed modulation is applied with k=0.

Comparing Fig. 3-14 and Fig. 3-15, the CMV amplitude with proposed modulation reduces to half of the CMV amplitude with conventional NTSV method. The output phase voltage of proposed modulation will be clamped to P or O or N in certain subsectors, which is a characteristic of discontinuous PWM. Hence, switching loss is also reduced.

Similar to simulation, the experiment is conducted at the case that the two inverters has different dead-time delay (167 ns difference). Dead-time difference among paralleled inverters generates low frequency harmonics, distorts the current and increases ZSCC. Fig. 3-16 (a) and Fig. 3-16(b) shows the phase output currents and ZSCC without control and with proposed modulation and control, respectively. From Fig. 3-16 (b), current distortion and ZSCC are well suppressed with the proposed method.

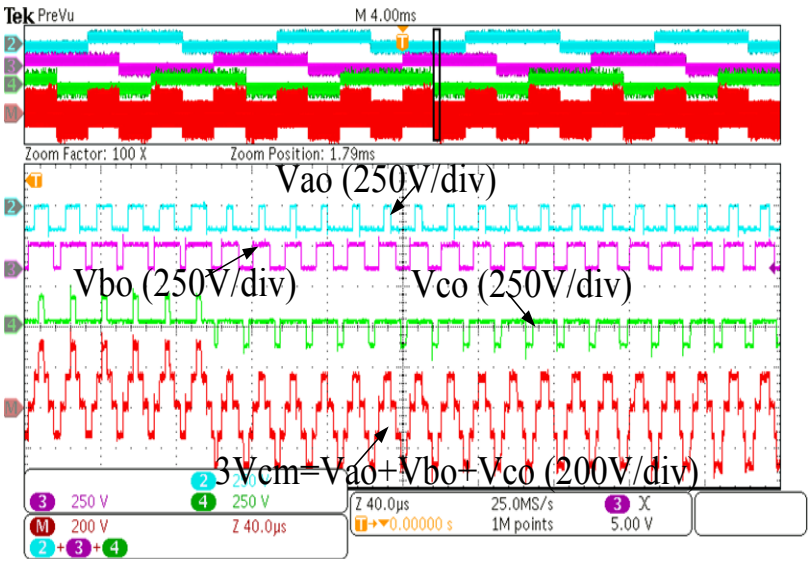


Fig. 3-14. Three phases output voltage and CMV.

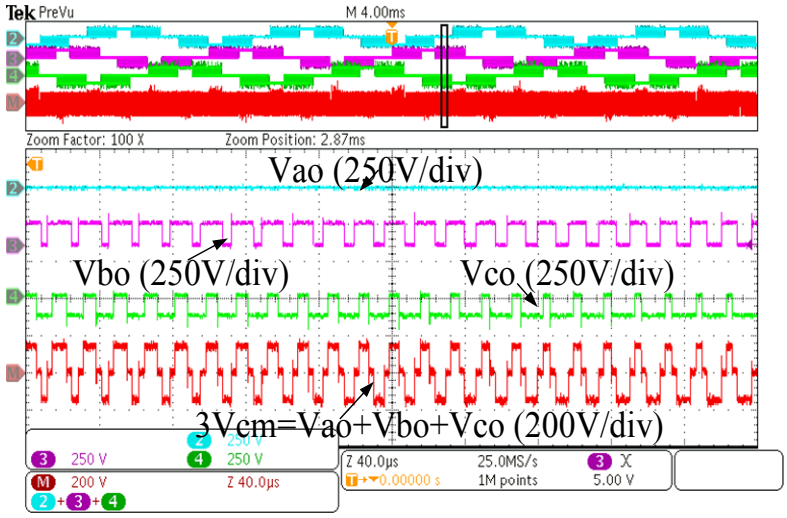
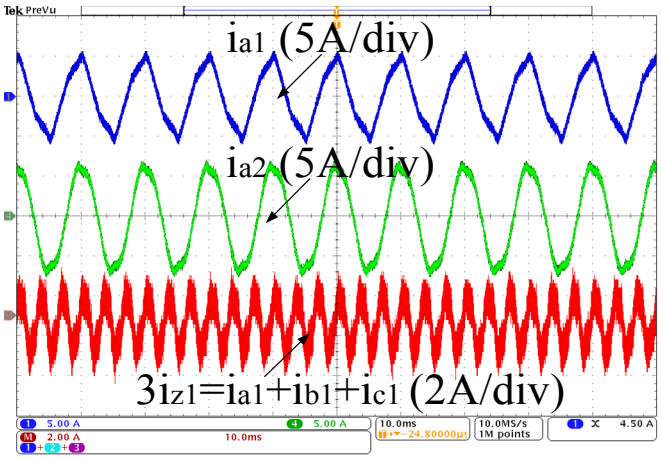
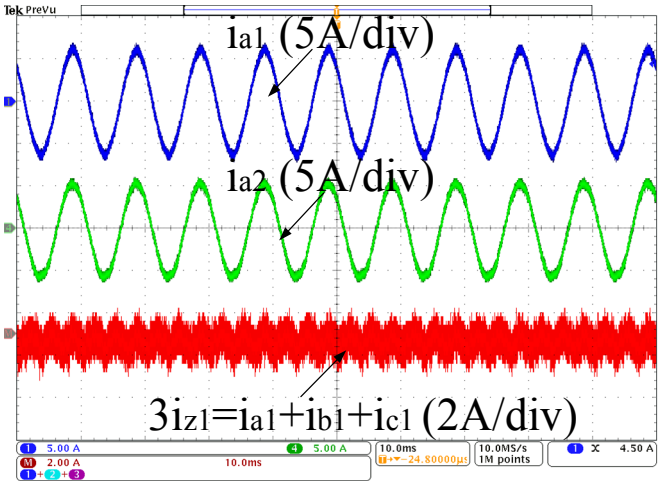


Fig. 3-15. Three phases output voltage and CMV.



(a)



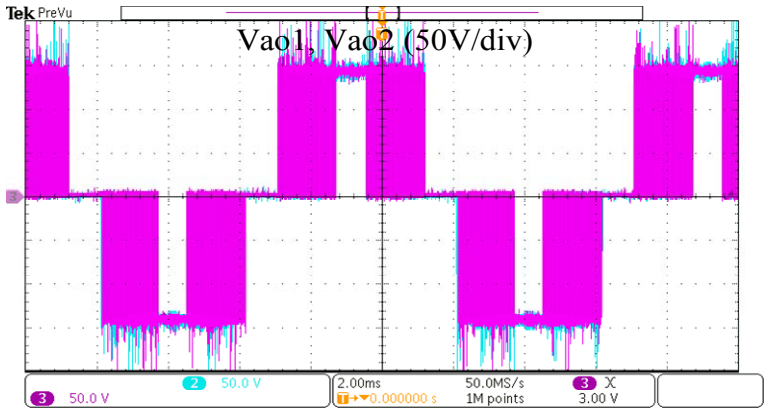
(b)

Fig. 3-16. Experiment waveforms when PWM mismatch exists among two paralleled inverters, (a) without control, (b) with proposed modulation and control strategy.

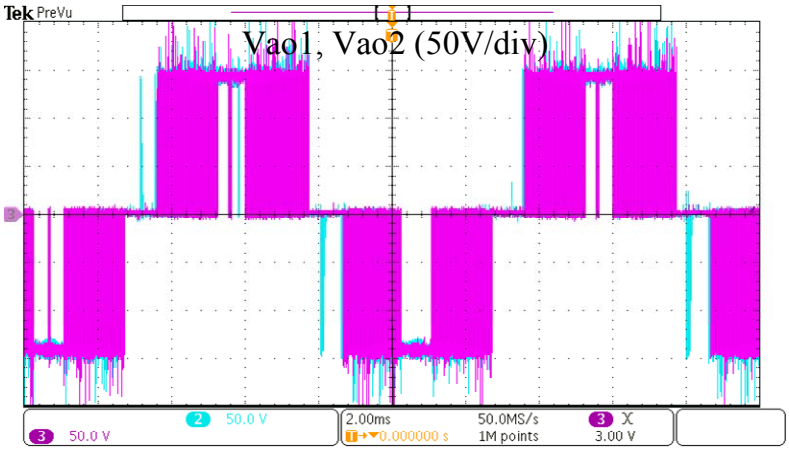
As discussed, when ZSCC is very small and within the limit, variable *k* will be zero to reduce switching loss. When ZSCC may exceed the limit value, ZSCC controller output is set to variable *k* to suppress ZSCC. Fig. 3-17 shows the phase output voltage comparison in the two cases. There is extra pulses in Fig. 3-17(b) at the position which is clamped to P or O or N in Fig. 3-17(a), which

indicating that the ZSCC controller is working to reduce the ZSCC. From Fig. 3-17(b), there is only one inverter have extra pulses at one time constant while another inverter is still clamped. These matches previous analysis. In the worst case, there is ten switching actions in one switching cycle for two paralleled inverters. Switching loss is still reduced compared to conventional NTSV method which have twelve switching actions in one switching cycle for two inverters.

To further demonstrate the ZSCC control ability of proposed modulation, comparison experiments are conducted with the proposed modulation and with CMR modulation. Fig. 3-18 shows the phase output currents and ZSCC when the two paralleled inverters have unequal current reference ($I_{1\_ref} = 4\ A$ and $I_{2\_ref} = 8\ A$). Fig. 3-19 shows the phase output currents and ZSCC when the two paralleled inverters have unequal output inductances ($L_{c1} = 450\ uH$ and $L_{c2} = 250\ uH$). For both cases, large ZSCC occurs and distorts the current when CMR modulation is applied as CMR modulation does not have ZSCC control ability. When the proposed modulation applied, the ZSCC are well suppressed and current distortion are significantly reduced.

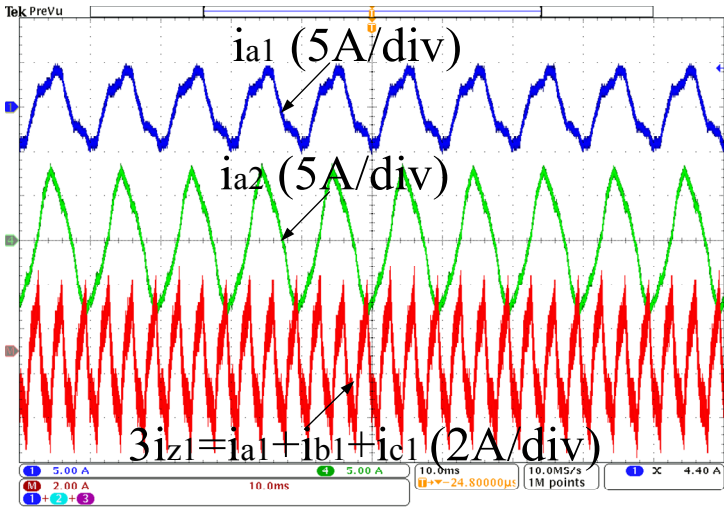


(a)

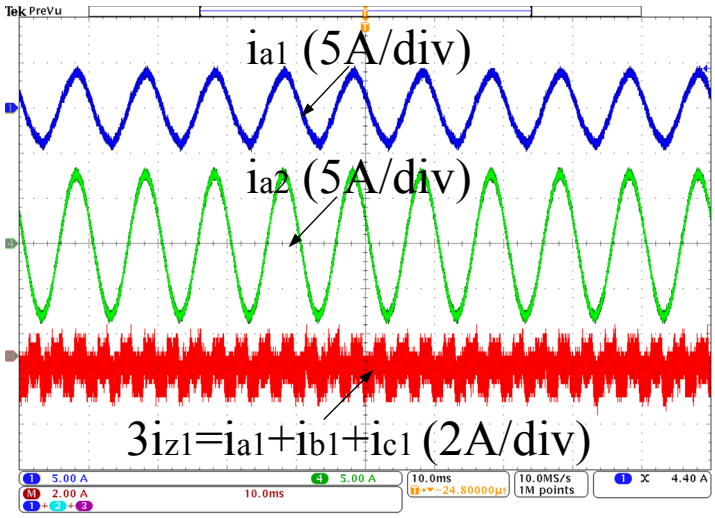


(b)

Fig. 3-17. Experiment waveforms of the phase output voltage, (a) ZSCC is small and within the limit, (b) ZSCC may exceed the limit.

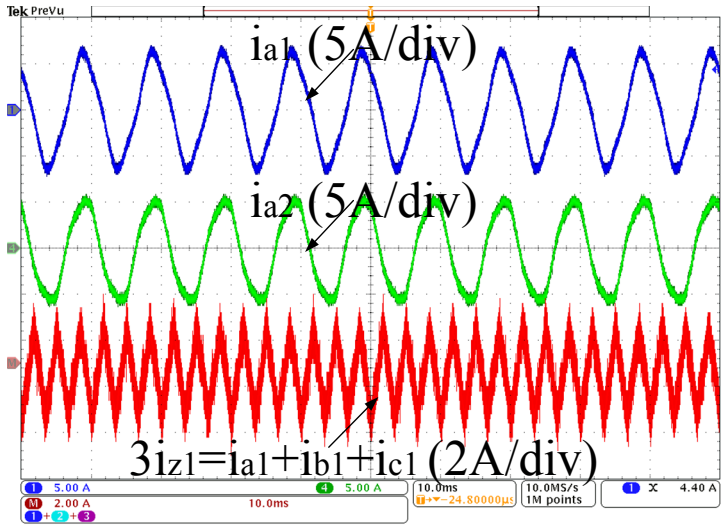


(a)

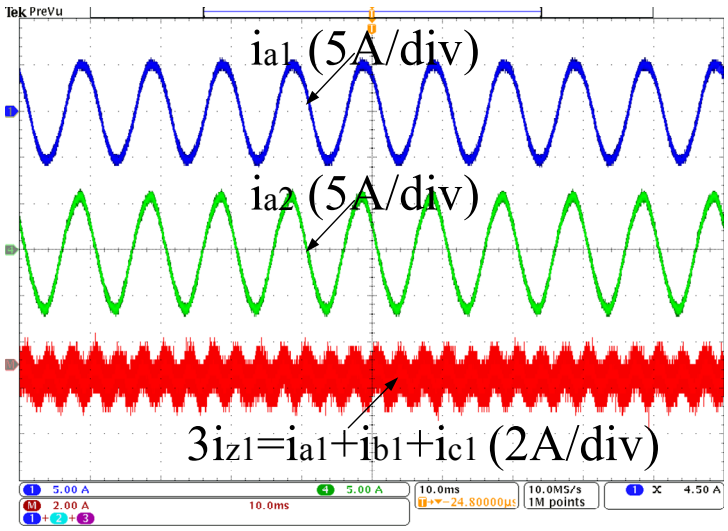


(b)

Fig. 3-18. Experiment waveforms when two paralleled inverters have unequal current reference, $I_{1\_ref} = 4\ A$, $I_{2\_ref} = 8\ A$, $L_{c1} = L_{c2} = 250\ uH$, (a) with CMR modulation, (b) with the proposed modulation.



(a)



(b)

Fig. 3-19. Experiment waveforms when two paralleled inverters have unequal output inductance, $I_{1\_ref} = I_{2\_ref} = 6\,A$, $L_{c1} = 450\,uH$, $L_{c2} = 250\,uH$ (a) with CMR modulation, (b) with the proposed modulation.

3.4 Conclusion

This chapter proposes a space vector modulation for paralleled three-level inverters which reduces the ZSCC, the CMV and switching loss simultaneously. The proposed modulation has adjustable AZSV in every switching cycle and thus ZSCC control can be achieved. The proposed modulation only uses vectors with a CMV magnitude equal to or smaller than $V_{dc}/6$. Hence, the CMV is reduced to half of conventional modulations. When ZSCC is small and within defined limit, the proposed modulation is the same as CMR modulation, and switching action is eight times for two paralleled inverters. When ZSCC exceeds the limit, even for the worst case that the fourth vector regulates in every switching cycle, the switching action is ten times for two inverters. Therefore, switching loss is reduced compared to the conventional modulations which have twelve switching actions for two inverters. Simulations and experiment results are demonstrated and verify the feasibility and validity of the proposed modulation method.

4. Coupled Inductor Flux Minimization for Parallel Interleaved Three-Level Inverters

Coupled inductor (which is also termed intercell transformer in some literature) is usually used as circulating current filter to suppress high frequency circulating current in parallel interleaved inverters. Due to strong magnetic coupling effect, the low frequency flux linkage components generated by the line currents of two parallel interleaved inverters in the coupled inductor are cancelled. Hence, only high frequency flux linkage components exist. The size and weight of coupled inductor can be reduced by reducing either the maximum flux linkage or the core loss. In high power applications, because the switching frequency is relatively low, the coupled inductor design is usually limited by the saturation of magnetic cores, which is determined by the maximum flux linkage in the coupled inductor. The PWM method for coupled inductor flux linkage reduction in parallel interleaved three-level inverters as shown in Fig. 4-1 is investigated in this chapter. A modulation method is proposed which could achieve lowest maximum flux linkage for the coupled inductor in parallel interleaved three-level inverters for all modulation indexes.

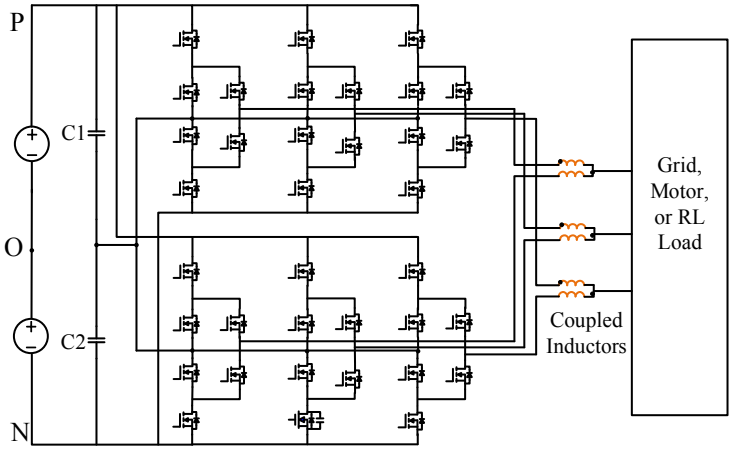


Fig. 4-1. Parallel interleaved three-level active NPC inverters.

4.1 Modulation for Coupled Inductor Flux Linkage Reduction

4.1.1 Flux Linkage of Coupled Inductor

The circulating current between two inverters is defined as

$$I_{X,c} = \frac{I_{X1} - I_{X2}}{2} \tag{4-1}$$

where X = {A, B, C}, I_{X1} and I_{X2} are the resultant phase currents of two parallel interleaved inverters, and $I_{X,c}$ denotes the circulating current.

The flux linkage is expressed as

$$\lambda_X(t) = L_C I_{X,c} = \int (V_{X1o} - V_{X2o})dt \tag{4-2}$$

where V_{X1o} and V_{X2o} are the phase-neutral voltages of the two inverters, L_c is the inductance offered to the circulating current, and λ_X is the flux linkage in the coupled inductor.

From (4-2), the differential voltage across coupled inductor ($V_{X1o} - V_{X2o}$) generates the flux linkage. To reduce the flux linkage maximum value, the time integral of this differential voltage should be reduced. It is evident that the PWM sequence determine the flux linkage pattern. The coupled inductor flux linkage maximum value is strongly impacted by the PWM method applied.

The space vector based PWM is functionally equivalent to the carrier based PWM. And for all the carrier based PWM methods, the modulation reference can be considered as a pure sinusoidal plus a zero sequence offset. Therefore, the optimal modulation can be found by finding the zero sequence offset which resulting in the lowest maximum flux linkage for the coupled inductor.

First, consider a general case, the phase-neutral voltages of two parallel interleaved inverters and the circulating current patterns are shown in Fig. 4-2. The duty cycle of the inverter phase-

neutral voltage is represented by D.

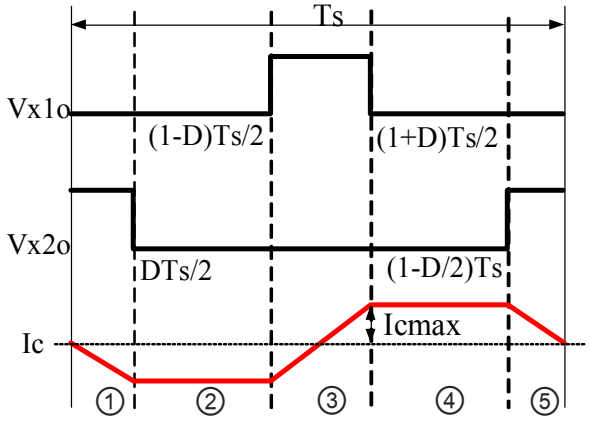
For the case that $D < 1/2$, the maximum flux linkage λ_{max} in the coupled inductor is

$$\lambda_{max} = L_c I_{cmax} = \frac{E}{2} D T_s \qquad (4-3)$$

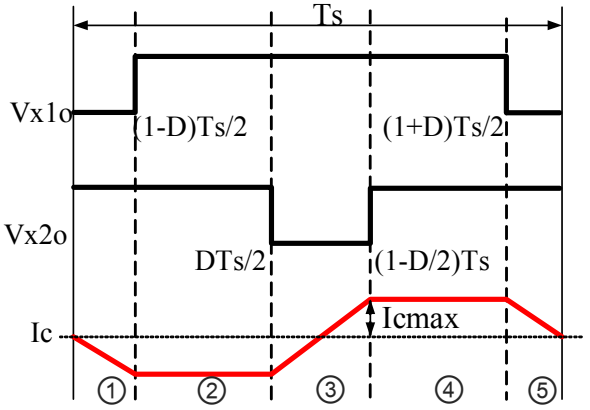
For the case that $D \geq 1/2$, the maximum flux linkage λ_{max} in the coupled inductor is

$$\lambda_{max} = L_c I_{cmax} = \frac{E}{2}(1-D) T_s \qquad (4-4)$$

where E is the dc voltage, and T_s is the switching period.



(a)



(b)

Fig. 4-2. Phase-neutral voltage and circulating current patterns, (a) $D < 1/2$, (b) $D \geq 1/2$.

Then, consider a three-level inverter, the carrier based implementation of the popular phase disposition pulse width modulation (PDPWM) is shown in Fig. 4-3. The modulation reference is depicted as V_X^* and compared with two triangle carriers. The reference can be considered as a constant in one switching cycle, and is made up by a pure sinusoidal plus a zero sequence offset as follow

$$V_X^* = V_X + V_0 \tag{4-5}$$

where V_X represents the pure sinusoidal and V_o represents the zero sequence offset.

As shown in Fig. 4-3, the distance between V_X^* and the line $x = 1/2$ (when $V_X^* \geq 0$) or the distance between V_X^* and the line $x = -1/2$ (when $V_X^* < 0$) is denoted as H.

When $D < 1/2$,

$$D = \frac{1}{2} - H \tag{4-6}$$

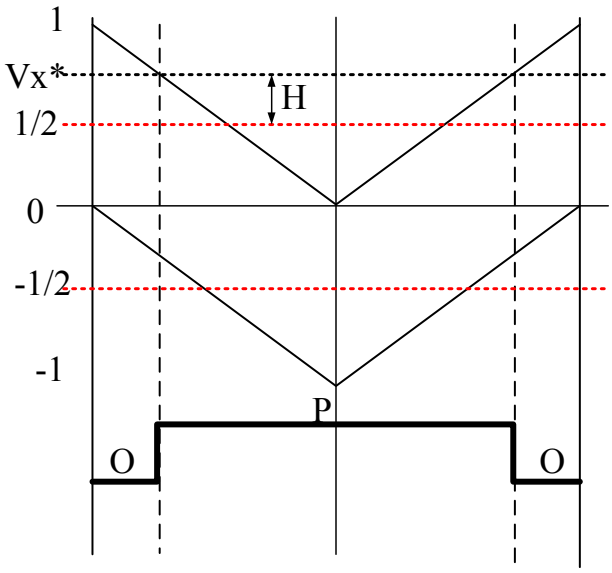
When $D \geq 1/2$,

$$D = \frac{1}{2} + H \tag{4-7}$$

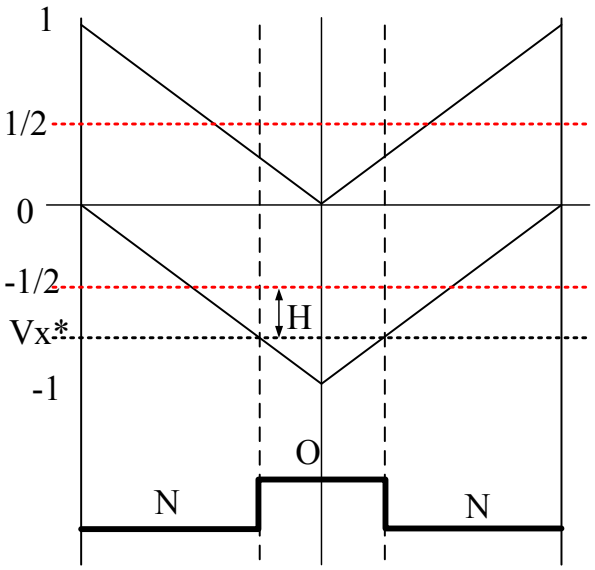
Combine (4-3) and (4-6), and (4-4) and (4-7), the maximum value of flux linkage λ_{max} in the coupled inductor is derived as

$$\lambda_{max} = L_c I_{cmax} = \frac{1}{2}\frac{E}{2}T_s\left(\frac{1}{2} - H\right) \tag{4-8}$$

From (4-8), λ_{max} has the minimum value when H is maximum.



(a)



(b)

Fig. 4-3. Carrier based PDPWM implementation for a three-level inverter, (a) reference $V_X^* > 0$, (b) reference $V_X^* < 0$.

4.1.2 Optimal Zero Sequence Offset

As discussed, to achieve minimum value for the maximum flux linkage λ_{max}, the zero sequence offset V_0 should make H to be maximum. As V_0 is added to all three phases, the objective is to find V_0 that makes the minimum H in three phases to have maximum value. The minimum H in three phases is represented as $\overline{H}$ and calculated as

$$\overline{H} = \min\left(\left||V_A + V_0| - \frac{1}{2}\right|, \left||V_B + V_0| - \frac{1}{2}\right|, \left||V_C + V_0| - \frac{1}{2}\right| \right) \quad (4-9)$$

Here V_X (X = {A, B, C}) is defined as

$$\begin{aligned} V_A &= M\cos\theta \\ V_B &= M\cos\left(\theta + \frac{2}{3}\pi\right) \\ V_C &= M\cos\left(\theta + \frac{4}{3}\pi\right) \end{aligned} \quad (4-10)$$

where M represents the modulation index and θ indicates the phase angle.

Then, the optimal zero sequence offset V_{opt} should let $\overline{H}$ to be maximum. V_{opt} can be found by sweeping V_0 from its minimum value (-1) to its maximum value (+1) for all possible references. However, this requires too much calculation time and is not practical for online implementation. The analytical solution is developed as follows.

For better illustration, define the pure sinusoidal voltages as

$$\begin{aligned} V_{max} &= \max(V_A, V_B, V_C) \\ V_{mid} &= \text{mid}(V_A, V_B, V_C) \\ V_{min} &= min(V_A, V_B, V_C) \end{aligned} \quad (4-11)$$

Then, the references are represented as

$$\begin{aligned} V_{max}^* &= V_{max} + V_0 \\ V_{mid}^* &= V_{mid} + V_0 \\ V_{min}^* &= V_{min} + V_0 \end{aligned} \quad (4-12)$$

First, when the zero sequence offset $V_0 > 0$, the three phase references will shift up. $\bar{H}$ will be impacted when V_0 varies. However, $\bar{H}$ will achieve maximum value only at several extreme points of the references. Considering the modulation index range, there are five possible cases.

Case 1: the distance between V_{max}^* and the line $x = 1/2$ is equal to the distance between V_{min}^* and the line $x = -1/2$, which means,

$$\left|\frac{1}{2} - (V_{max} + V_0)\right| = \left|(V_{min} + V_0) - \left(-\frac{1}{2}\right)\right| \quad (4-13)$$

In this case the zero sequence offset is derived as

$$V_{0(1+)} = \frac{V_{mid}}{2} \quad (4-14)$$

Note that $V_{0(1+)} > 0$ should be met. The maximum $\bar{H}$ is

$$\bar{H}_{(1+)} = \min\left(\left|V_{max} + \frac{1}{2}V_{mid} - \frac{1}{2}\right|, \left|\frac{3}{2}V_{mid} - \frac{1}{2}\right|\right) \quad (4-15)$$

Case 2: V_{max}^* and V_{mid}^* are at two sides of the line $x = 1/2$ and their distances to the line $x = 1/2$ are equal, which means,

$$(V_{max} + V_0) - \frac{1}{2} = \frac{1}{2} - (V_{mid} + V_0) \quad (4-16)$$

In this case the zero sequence offset is derived as

$$V_{0(2+)} = \frac{1 + V_{min}}{2} \quad (4-17)$$

The maximum $\bar{H}$ is

$$\bar{H}_{(2+)} = \min\left(\left|V_{max} + \frac{1}{2}V_{min}\right|, \left|\frac{3}{2}V_{mid} + 1\right|\right) \quad (4-18)$$

Case 3: the distance between V_{mid}^* and the line $x = 1/2$ is equal to the distance between V_{min}^* and the line $x = -1/2$, which means,

$$\left|\frac{1}{2} - (V_{mid} + V_0)\right| = \left|(V_{min} + V_0) - (-\frac{1}{2})\right| \quad (4-19)$$

In this case the zero sequence offset is derived as

$$V_{0(3+)} = \frac{V_{max}}{2} \quad (4-20)$$

The maximum $\bar{H}$ is

$$\bar{H}_{(3+)} = \min\left(\left|\frac{1}{2}V_{max} + V_{mid} - \frac{1}{2}\right|, \left|\frac{3}{2}V_{max} - \frac{1}{2}\right|\right) \quad (4-21)$$

Case 4: V_{mid}^* and V_{min}^* are at the two sides of the line $x = 1/2$ and their distances to the line $x = 1/2$ are equal, which means,

$$(V_{mid} + V_0) - \frac{1}{2} = \frac{1}{2} - (V_{min} + V_0) \quad (4-22)$$

In this case the zero sequence offset is derived as

$$V_{0(4+)} = \frac{(1 + V_{max})}{2} \quad (4-23)$$

The maximum $\bar{H}$ is

$$\bar{H}_{(4+)} = \frac{1}{2}V_{max} + V_{mid} \quad (4-24)$$

Case 5: V_{max}^* is equal to the line $x = 1$, which means,

$$V_{0(5+)} = 1 - V_{max} \quad (4-25)$$

The maximum $\overline{H}$ is

$$\overline{H}_{(5+)} = \min\left(\left||V_{mid} + 1 - V_{max}| - \frac{1}{2}\right|, \left||V_{min} + 1 - V_{max}| - \frac{1}{2}\right|\right) \quad (4-26)$$

Second, when the zero sequence offset $V_0 < 0$, the three phase references will shift down. Similarly, $\overline{H}$ will achieve maximum value only at several extreme points of the references. There are also five possible cases which are similar as the previous discussion and which not be repeated here. In addition, the case $V_0 = 0$ could also be an extreme point.

In summary, all the possible optimal zero sequence offset candidates and the corresponding $\overline{H}$ are analytically derived and summarized in Table 4-1. Then, the optimal zero sequence offset V_{opt} can be obtained by calculating the maximum $\overline{H}$ among all the candidates identified in Table 4-1. Fig. 4-4 illustrates the flowchart to determine V_{opt}.

Table 4-1. The Optimal Zero Sequence Offset Candidates V_0 and the Corresponding $\overline{H}$

when $V_0 > 0$
$V_{0(1+)} = \frac{V_{mid}}{2}, V_{0(1+)} > 0$ $\overline{H}_{(1+)} = \min\left(\left\|V_{max} + \frac{1}{2}V_{mid} - \frac{1}{2}\right\|, \left\|\frac{3}{2}V_{mid} - \frac{1}{2}\right\|\right)$
$V_{0(2+)} = \frac{1 + V_{min}}{2}$ $\overline{H}_{(2+)} = \min\left(\left\|V_{max} + \frac{1}{2}V_{min}\right\|, \left\|\frac{3}{2}V_{mid} + 1\right\|\right)$
$V_{0(3+)} = \frac{V_{max}}{2}$ $\overline{H}_{(3+)} = \min\left(\left\|\frac{1}{2}V_{max} + V_{mid} - \frac{1}{2}\right\|, \left\|\frac{3}{2}V_{max} - \frac{1}{2}\right\|\right)$

Table 4-1 Continued

$V_{0(4+)} = \frac{1 + V_{max}}{2}$ $\bar{H}_{(4+)} = \frac{1}{2}V_{max} + V_{mid}$
$V_{0(5+)} = 1 - V_{max}$ $\bar{H}_{(5+)} = \min\left(\left\|\lvert V_{mid} + 1 - V_{max}\rvert - \frac{1}{2}\right\|, \left\|\lvert V_{min} + 1 - V_{max}\rvert - \frac{1}{2}\right\|\right)$
when $V_0 < 0$
$V_{0(1-)} = \frac{V_{mid}}{2}, V_{0(1-)} > 0$ $\bar{H}_{(1-)} = \min\left(\left\|V_{max} + \frac{1}{2}V_{mid} - \frac{1}{2}\right\|, \left\|-\frac{3}{2}V_{mid} - \frac{1}{2}\right\|\right)$
$V_{0(2-)} = \frac{-1 + V_{max}}{2}$ $\bar{H}_{(2-)} = \min\left(\left\|-V_{min} - \frac{1}{2}V_{max}\right\|, \left\|-\frac{3}{2}V_{max} + 1\right\|\right)$
$V_{0(3-)} = \frac{V_{min}}{2}$ $\bar{H}_{(3-)} = \min\left(\left\|V_{max} + \frac{1}{2}V_{min} - \frac{1}{2}\right\|, \left\|-\frac{3}{2}V_{min} - \frac{1}{2}\right\|\right)$
$V_{0(4-)} = \frac{-1 + V_{min}}{2}$ $\bar{H}_{(4-)} = V_{max} + \frac{1}{2}V_{min}$
$V_{0(5-)} = -1 - V_{min}$ $\bar{H}_{(5-)} = \min\left(\left\|\lvert V_{mid} - 1 - V_{min}\rvert - \frac{1}{2}\right\|, \left\|\lvert V_{max} - 1 - V_{min}\rvert - \frac{1}{2}\right\|\right)$
when $V_0 = 0$
$V_{0(0)} = 0$ $\bar{H}_{(0)} = \min\left(\left\|V_{max} - \frac{1}{2}\right\|, \left\|V_{mid} - \frac{1}{2}\right\|, \left\|V_{min} - \frac{1}{2}\right\|\right)$

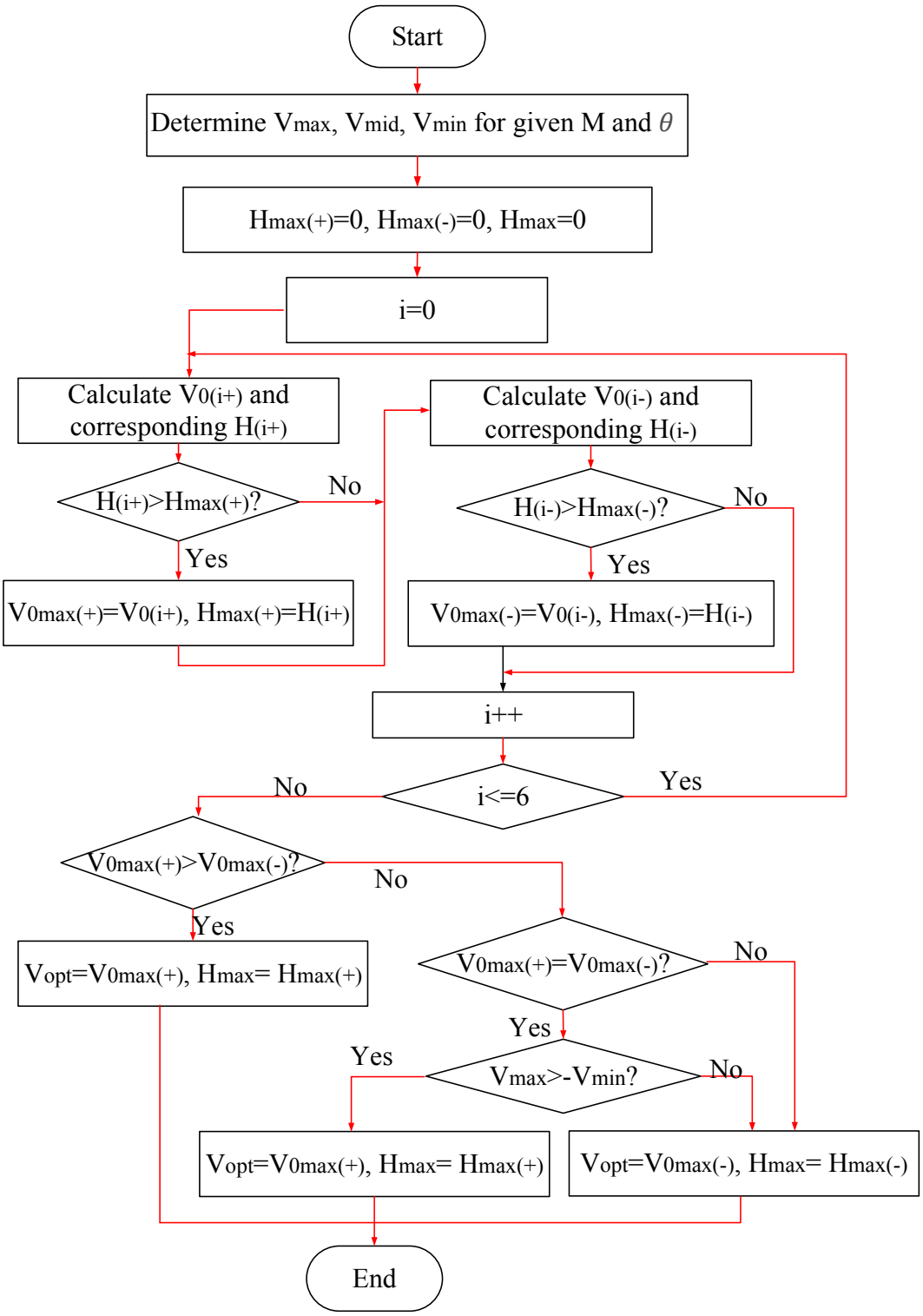
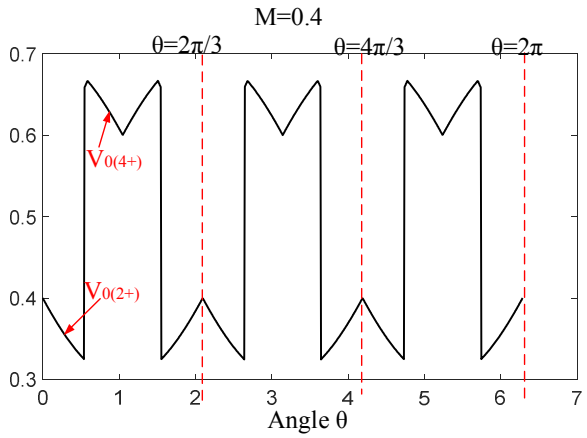
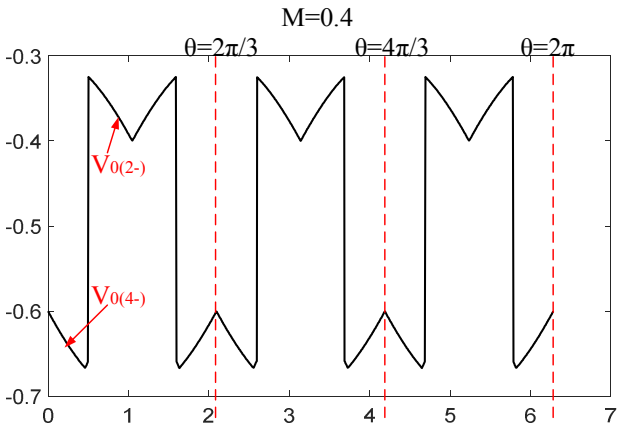


Fig. 4-4. Flow chart to determine the optimal zero sequence offset V_{opt}.

The optimal zero sequence offset V_{opt} is actually made up by several segments of the candidates calculated in Table I and is a function of the modulation index. For example, Fig. 4-5 shows the optimal zero sequence offset V_{opt} when modulation index M=0.4. Due to symmetry, only one sixth of the fundamental cycle needs to be calculated. From Fig. 4-5(c), V_{opt} is made up by candidates $V_{0(2+)}$ and $V_{0(2-)}$. Fig. 4-6 shows the optimal zero sequence offset at typical modulation indexes.

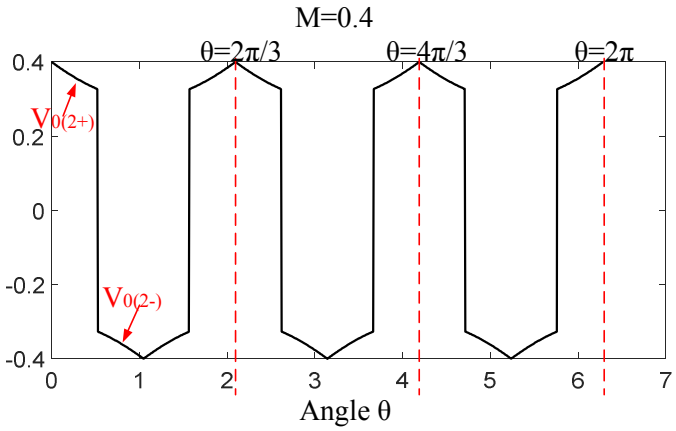


(a)



(b)

Fig. 4-5. The optimal zero sequence offset V_{opt} when modulation index M=0.4, (a) $V_0 > 0$, (b) $V_0 < 0$, (c) V_0 has no limit.



(c)

Fig. 4-5. Continued.

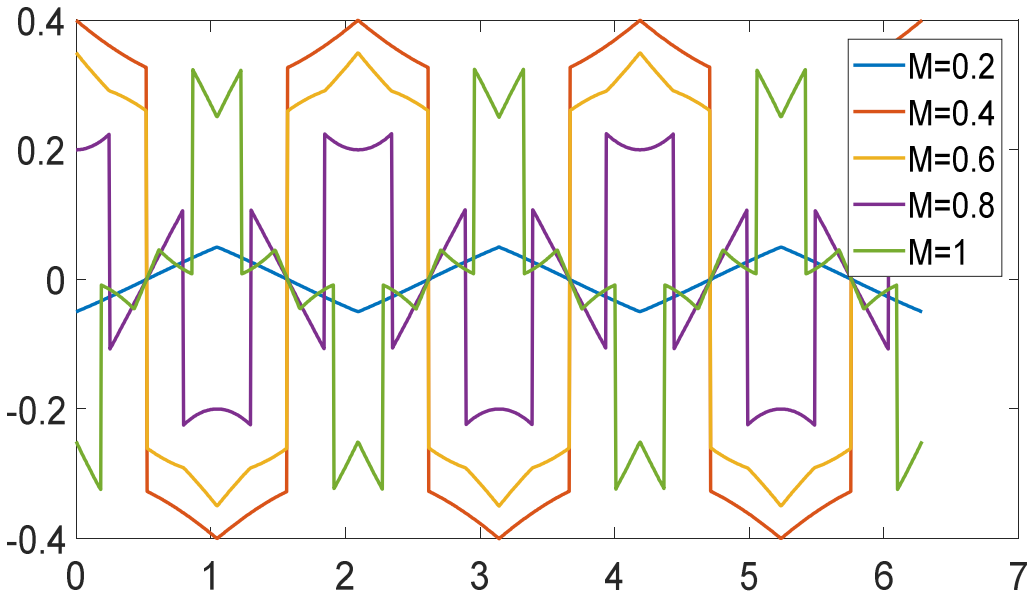


Fig. 4-6. The optimal zero sequence offset V_{opt} at different modulation indexes.

4.1.3 Discuss on Neutral Point Voltage Balance

For a three-level NPC inverter, the two dc-link capacitors are connected in series and the two capacitor voltages need to be balanced. The neutral point (NP) voltage balance strategy with the proposed modulation method is discussed.

The NP voltage will be influenced when the output current is connected to the NP point. As shown in Fig. 4-7, point O is the neutral point. If the averaged NP current $\overline{i_{np}}$ in a switching cycle is larger than zero, the lower capacitor is discharged and V_{C2} decreases. If $\overline{i_{np}}$ is smaller than zero, the lower capacitor is charged and V_{C2} increases.

Define I_{max}, I_{mid}, and I_{min} as the phase output currents of the corresponding maximum, medium, and minimum reference voltages, respectively. To simplify the analysis, the case that the output voltage and current has the same polarity is analyzed. When the load power factor is not unity there is a chance that the output voltage and current have different polarity. However, the analysis method is the same.

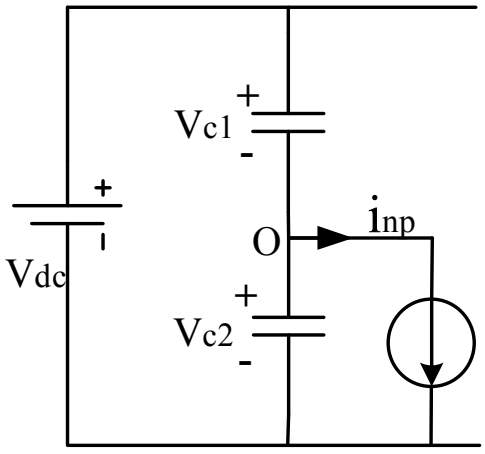


Fig. 4-7. NP in the three-level NPC inverter.

For unity power factor case, $I_{max} > 0$ and $I_{min} < 0$ is always met while I_{mid} can be either larger or smaller than zero.

When $I_{mid} \geq 0$, the average NP current is formed as

$$\overline{i_{np}} = (1 - D^*_{max})I_{max} + (1 - D^*_{mid})I_{mid} + D^*_{min}I_{min} \qquad (4-27)$$

When $I_{mid} < 0$, the average NP current is formed as

$$\overline{i_{np}} = (1 - D^*_{max})I_{max} + D^*_{mid}I_{mid} + D^*_{min}I_{min} \qquad (4-28)$$

where $D^*_{max} = V_{max} + V_0$, $D^*_{min} = 1 + V_{min} + V_0$, $D^*_{mid} = V_{mid} + V_0$ when $V_{mid} \geq 0$ and $D^*_{mid} = 1 + V_{mid} + V_0$ when $V_{mid} < 0$.

From (4-27) and (4-28), compared to no zero sequence offset case, the average NP current $\overline{i_{np}}$ will decrease when $V_0 > 0$ and will increase when $V_0 < 0$. Therefore, the NP voltage can be regulated by the polarity of the zero sequence offset. When $\Delta V = V_{c1} - V_{c2} > 0$, to balance NP voltage, the zero sequence offset should be confined to $V_0 \geq 0$ when calculating the optimal zero sequence offset V_{opt}. When $\Delta V < 0$, to balance NP voltage, the zero sequence offset should be confined to $V_0 \leq 0$ when calculating V_{opt}. A PI controller can be applied to regulate the low frequency NP voltage ripples slowly. Fig. 4-8 shows the flowchart for NP voltage balance control with the proposed modulation. This strategy can also be used to suppress the low frequency circulating current especially the dc offset in the parallel inverters.

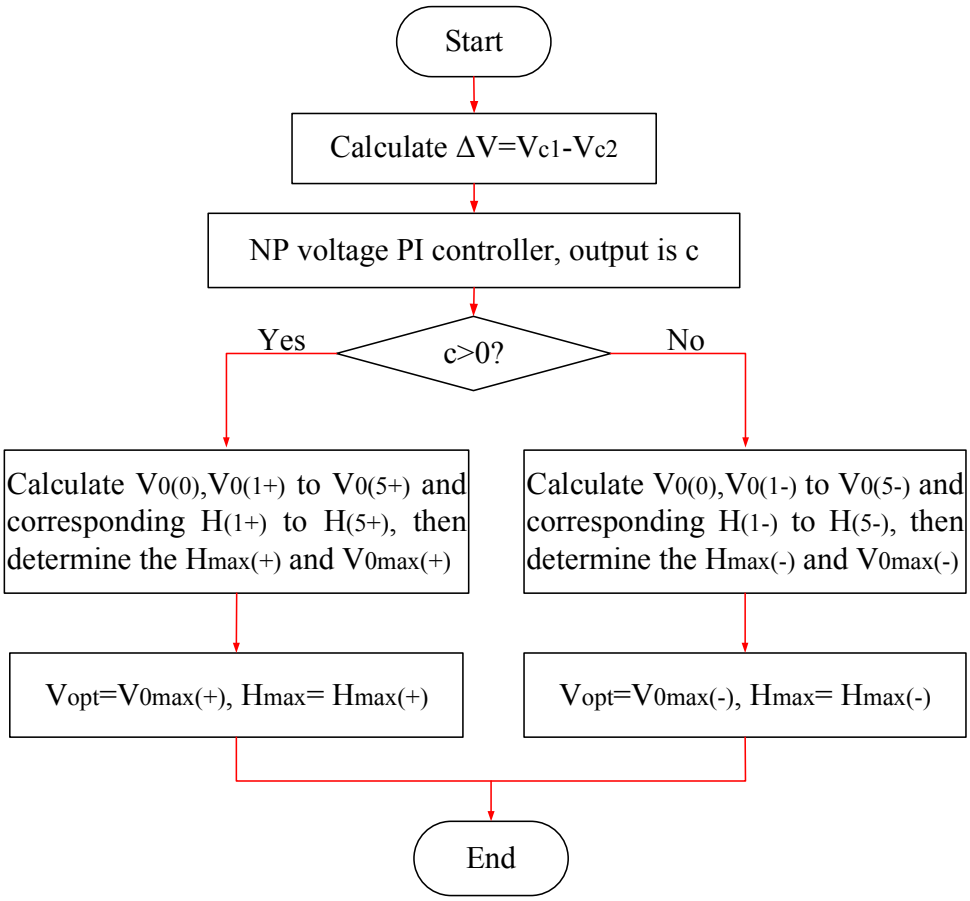


Fig. 4-8. Flowchart for NP voltage balance control with the proposed modulation.

4.2 Modulation Methods Comparison

4.2.1 General Method for Circulating Current Prediction

To calculate the circulating currents of different modulation methods, a general method for circulating current prediction is developed. Although various PWM methods can be applied, the general circulating current pattern for parallel interleaved inverter is the same as shown in Fig. 4-2. The circulating current is composed of five segments. For each segment, the slope and duration time are calculated. Thus, the circulating current can be predicted.

Table 4-2. Duration Time and Slope of Each Segment of the Circulating Current

Segment	$D < \frac{1}{2}$		$D \geq \frac{1}{2}$	
	duration	slope	duration	slope
①	$\frac{D}{2}T_s$	$-\frac{ET_s}{2L_c}$	$\frac{(1-D)}{2}T_s$	$-\frac{ET_s}{2L_c}$
②	$(\frac{1}{2}-D)T_s$	0	$(D-\frac{1}{2})T_s$	0
③	DT_s	$\frac{ET_s}{2L_c}$	$(1-D)T_s$	$\frac{ET_s}{2L_c}$
④	$(\frac{1}{2}-D)T_s$	0	$(D-\frac{1}{2})T_s$	0
⑤	$\frac{D}{2}T_s$	$-\frac{ET_s}{2L_c}$	$\frac{(1-D)}{2}T_s$	$-\frac{ET_s}{2L_c}$

Table 4-2 summarizes the duration time and slope of each segment of the circulating current of two parallel interleaved three-level inverters. For different modulation method, the equivalent zero sequence offset is different, and the duty cycle *D* will be different. When *D* is determined, the circulating current and the flux linkage of the coupled inductor can be predicted.

4.2.2 Modulation Comparison

Five modulation methods including the carrier based SPWM, the carrier based discontinuous PWM, the nearest three space vector (NTSV) modulation, the common-mode reduction (CMR) modulation, and the proposed modulation are compared.

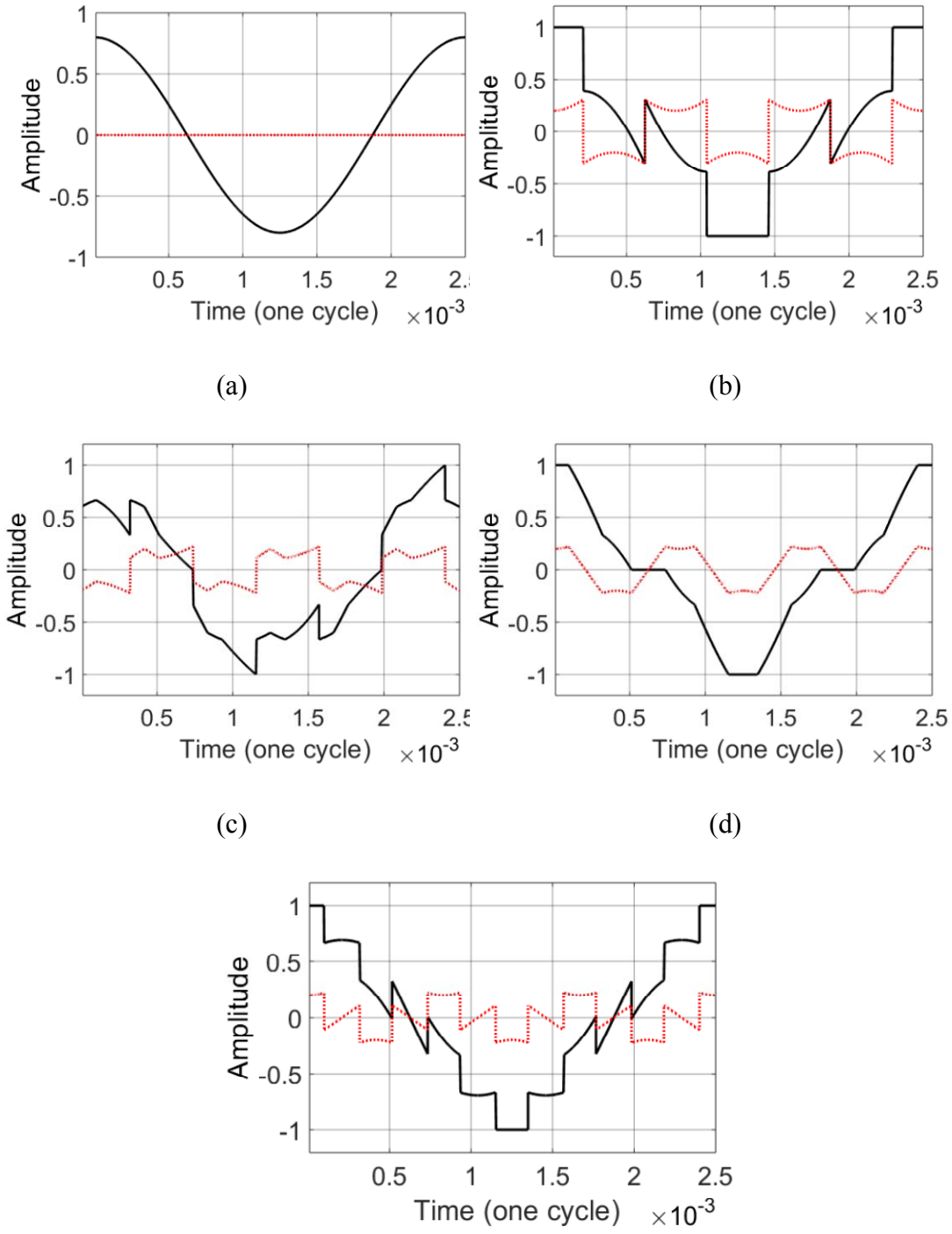
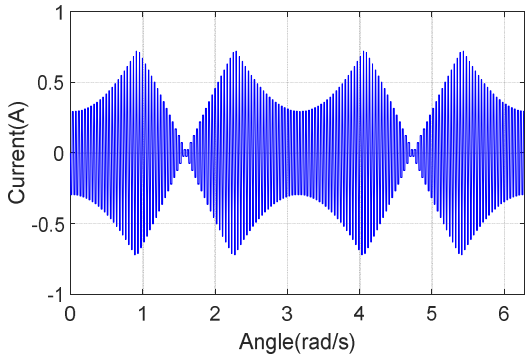
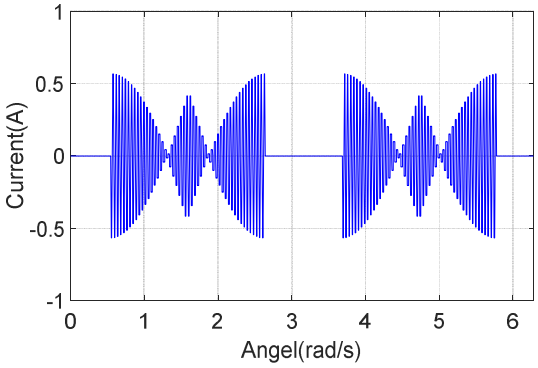


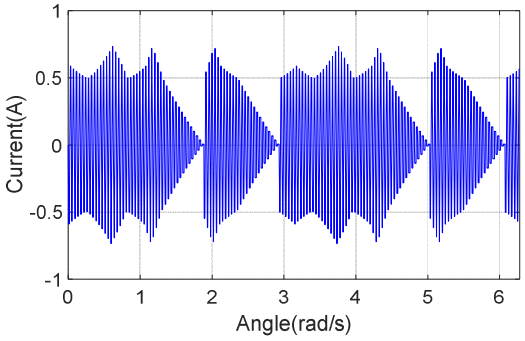
Fig. 4-9. The reference (black solid line) and zero sequence offset (red dash line) of different PWM methods at modulation index M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation.



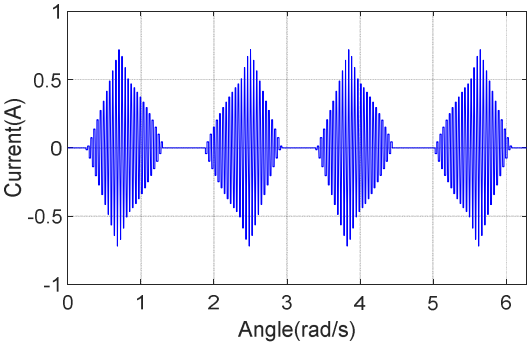
(a)



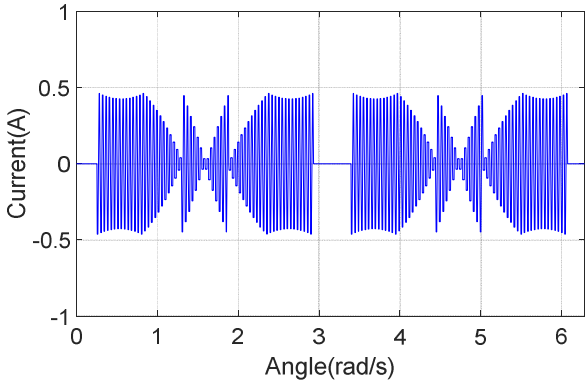
(b)



(c)



(d)



(e)

Fig. 4-10. Calculated circulating currents with different PWM methods at modulation index M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation.

The modulation references and zero sequence offsets of the carrier based SPWM and DPWM methods in one switching cycle are shown in Fig. 4-9(a) and Fig. 4-9(b), respectively. For space vector based PWM, the equivalent reference and zero sequence offset can be calculated. Fig. 4-9(c) and Fig. 4-9(d) shows the equivalent reference and zero sequence of the NTSV and CMR modulation methods, respectively. The reference and zero sequence offset of the proposed modulation method is shown in Fig. 4-9(e). Then, the duty cycle of each modulation method is calculated and the circulating current pattern in one fundamental cycle are predicted as shown in Fig. 4-10.

With (4-8), the normalized flux linkage for the five modulation methods are calculated and summarized as Fig. 11. Note that the curve of NTSV is almost overlapped with the curve of CMR. From Fig. 4-11, the proposed optimal modulation has the lowest maximum coupled inductor flux linkage in all modulation indexes. When modulation index is low, the flux linkage of proposed modulation is reduced to around 50% of that of DPWM, NTSV and CMR methods, and to around 80% of that of SPWM. When modulation index is high, the maximum flux linkage of the proposed modulation is reduced to around 60% of the flux linkage of SPWM, NTSV and CMR methods.

Then, to further evaluate the performance of the proposed modulation method, power device loss and coupled inductor loss and output current THD with different modulation methods are compared using MATLAB/Simulink simulation. A case study is conducted. The parameters for simulation are the same as Table 4-3 in next section. The power devices loss are calculated using simulation results and datasheet from device manufacture. Nanocrystalline cut core is selected for coupled inductor. The MSE method is used for magnetic loss calculation and Steinmetz equations coefficients obtained is used. Fig. 4-12 summarizes the power devices loss and coupled inductors loss and current THD of different modulation methods at different modulation indexes.

From Fig. 4-12, the loss and THD characteristics of the proposed modulation are similar to other continuous PWM methods (SPWM and NTSV) as the proposed modulation has continuous PWM patterns at most modulation indexes. An exception occurs when modulation index M is around 0.8. As illustrated, the optimal zero sequence offset is made up of several candidates in Table I. When M is around 0.8, the candidates $V_{05(+)}$ and $V_{05(-)}$ will be parts of the optimal zero sequence offset V_{opt}. The reference will be clamped to (+1) or (-1) in several segments of one fundamental cycle and shows discontinuous PWM pattern. As can be observed in Fig. 4-12(b), the switching loss of the proposed modulation is smaller than nearby when M is around 0.8.

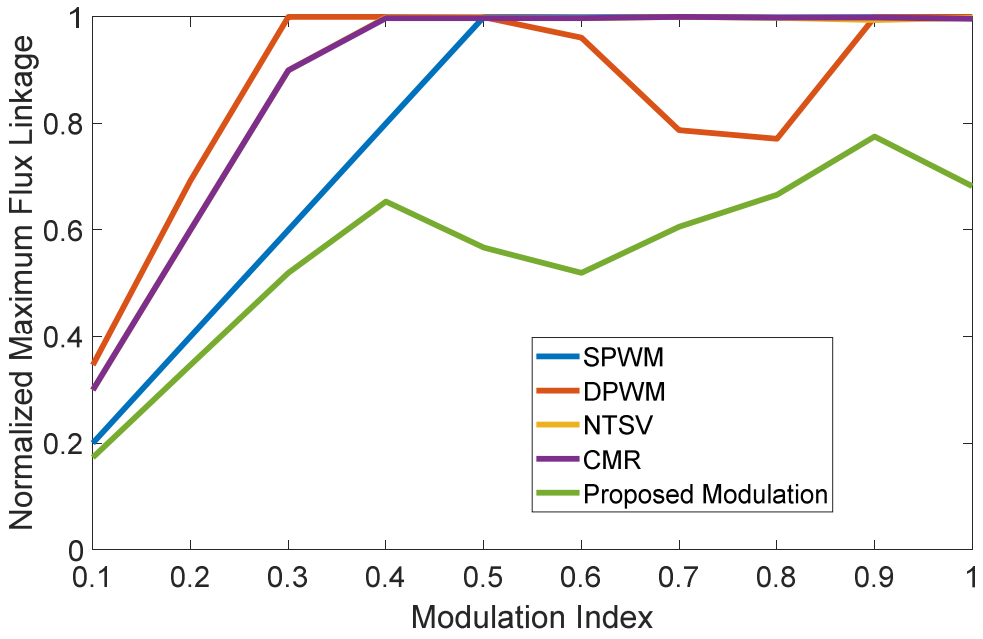
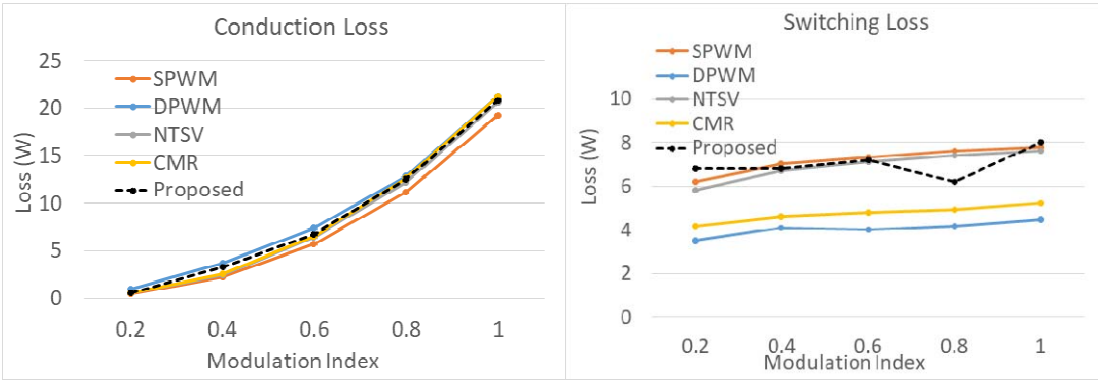
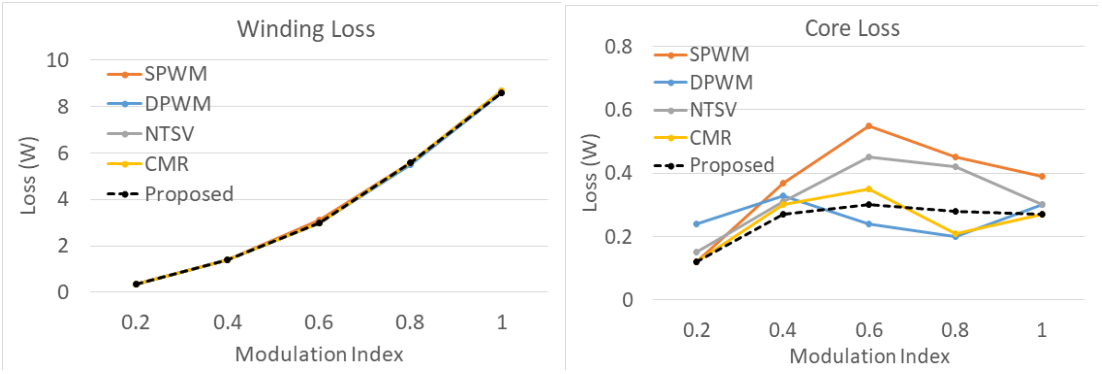


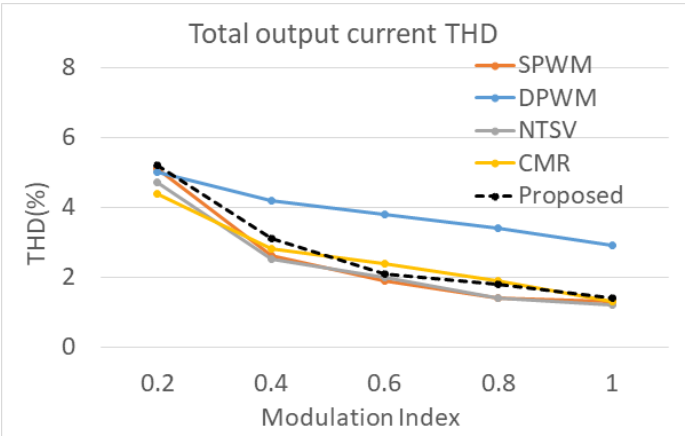
Fig. 4-11. Maximum flux linkage comparison with different modulation methods.



(a) (b)



(c) (d)



(e)

Fig. 4-12. Loss and THD comparison of different modulation methods at different modulation indexes, (a) devices conduction loss, (b) devices switching loss, (c) inductor winding loss, (d) inductor core loss, (e) current THD.

4.3 Simulation and Experimental Results

Table 4-3. Parameters for Simulation and Experiments

DC input voltage	300 V
Carrier frequency	60 kHz
Fundamental frequency	400 Hz
MOSFETs	Wolfspeed C3M0065100K
Coupled inductor	VAC nanocrystalline cut core T60102-L2083-W156, turns N=16, inductance Lc=860 uH
RL load	L=320 uH, R=10 Ω each phase

Simulation and experiments are conducted on two parallel interleaved three-level active NPC inverters as shown in Fig. 4-1. The main parameters for the simulation and experiment are listed in Table 4-3.

4.3.1 Simulation Results

The simulation is conducted using MATLAB/Simulink. Fig. 4-13 shows the voltage and current waveforms with the proposed modulation at modulation index M=0.8. To verify the NP balancing control capability of the proposed modulation, the initial voltages of the two dc-link capacitors are set to different values. Fig. 4-14 shows the results with the proposed modulation and control strategy illustrated in Fig. 4-8. The voltages of the two dc-link capacitors can be well regulated and balanced. Fig. 4-15 shows the simulation results of circulating currents with different modulation methods at modulation index M=0.8. The pattern of the circulating currents match with the theoretical calculation results in Fig. 4-10. Simulations are also conducted with the five modulation methods at different modulation indexes to get the loss and THD.

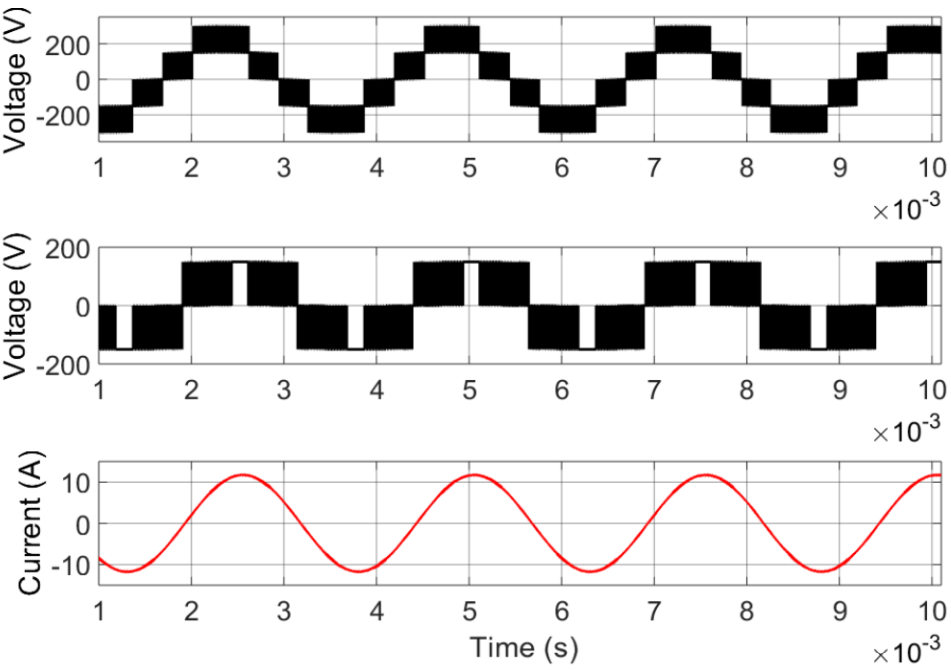


Fig. 4-13. Waveforms with the proposed modulation. From top to bottom: line voltage and phase voltage of one inverter, total output current.

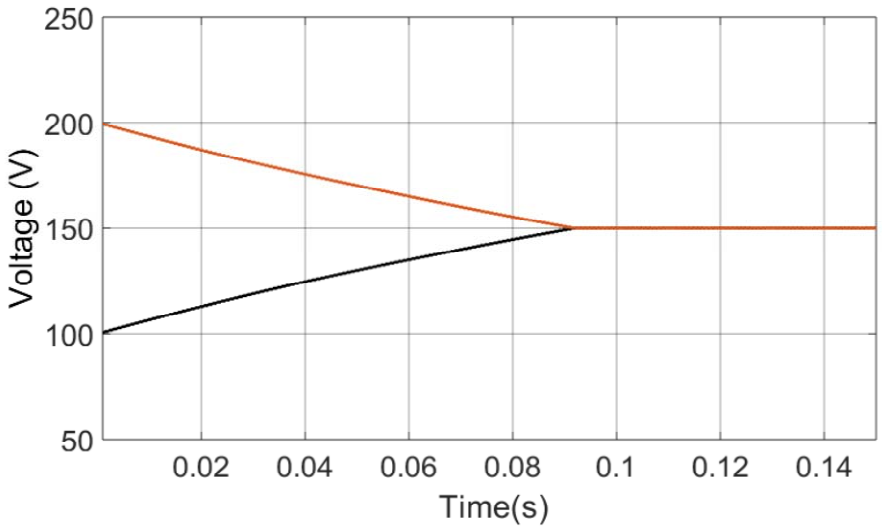


Fig. 4-14. Voltages of the two dc-link capacitors.

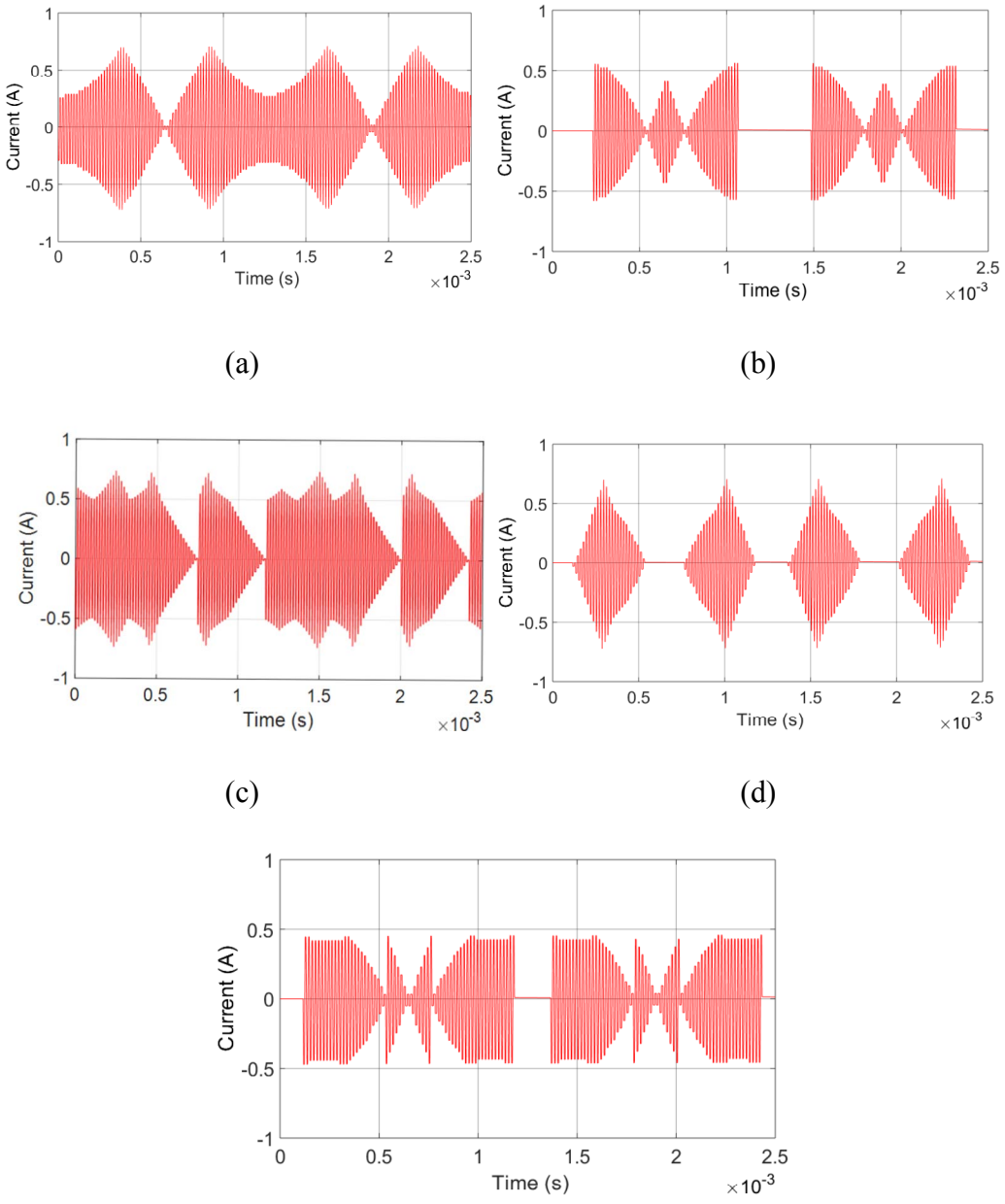


Fig. 4-15. Simulation results of circulating currents with different PWM methods at modulation index M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation.

4.3.2 Experimental Results

Fig. 4-16 shows the tested line voltage and phase voltage of one inverter, and total output current waveforms with the proposed modulation at modulation index M=0.8. Fig. 4-17 shows the voltages of two dc-link capacitors when the NP point is floating.

The output currents of the two parallel interleaved inverters and the circulating current are measured at different modulation index. Fig. 4-18 and Fig. 4-19 shows the waveforms at M=0.8 and M=0.4, respectively. The circulating current pattern and value match with theoretical analysis.

Other four modulation methods mentioned above are also implemented in experiments. Fig. 20 shows the circulating current comparison with these different modulation methods, all at the condition modulation index M=0.8. Comparing Fig. 4-20 with Fig. 4-10 and Fig. 4-13, the circulating currents match well with theoretical calculation and simulation results.

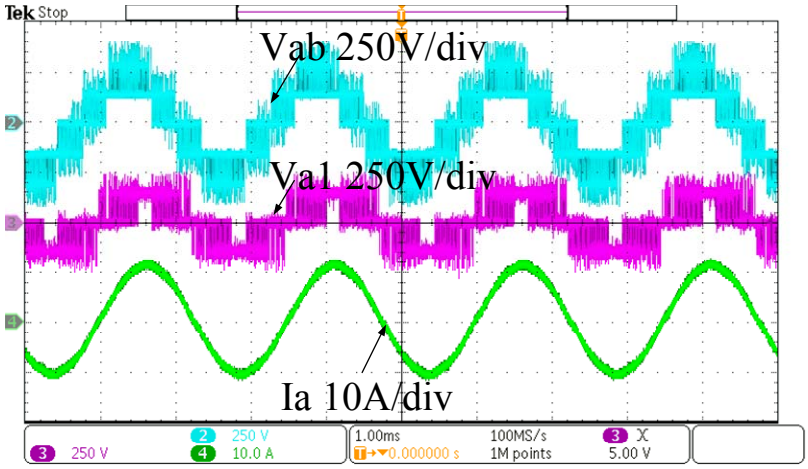


Fig. 4-16. Waveforms with the proposed modulation. From top to bottom: line voltage, phase voltage of inverter 1, total output current.

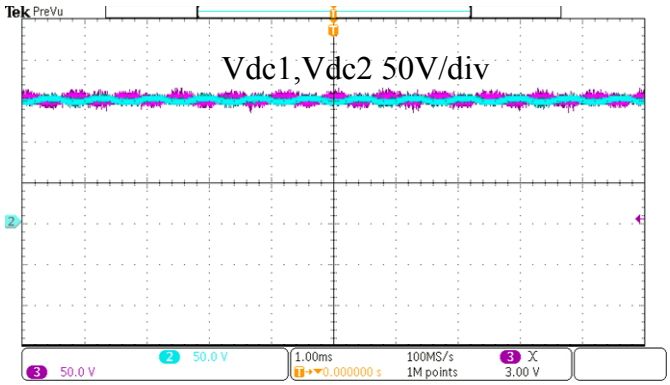
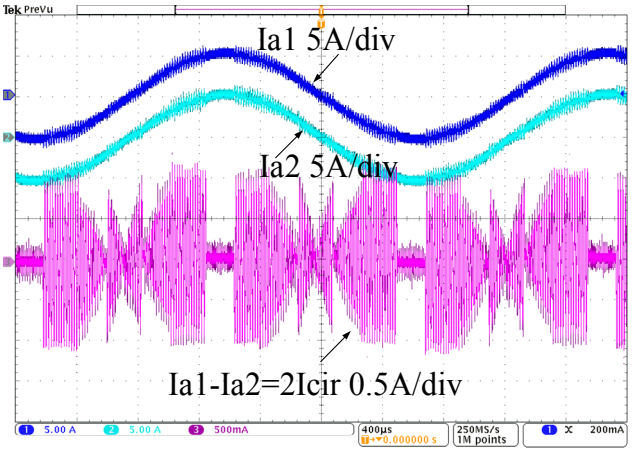
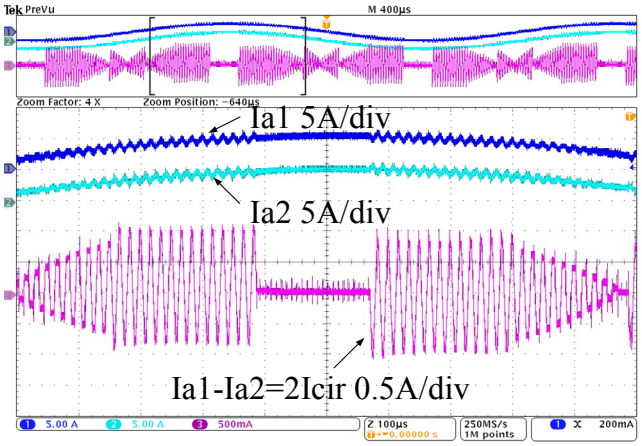


Fig. 4-17. Voltages of the two dc-link capacitors.

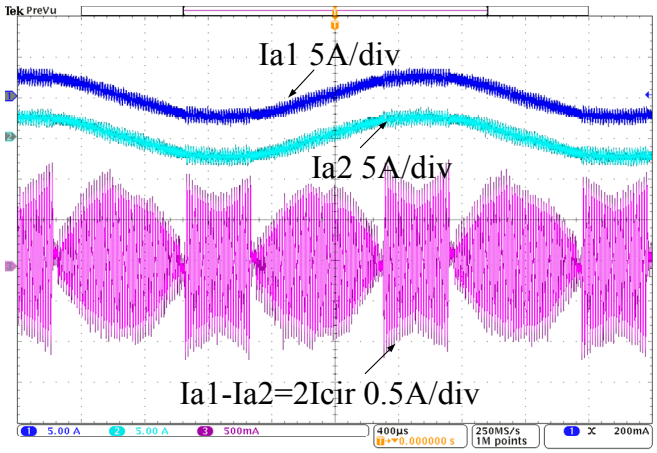


(a)

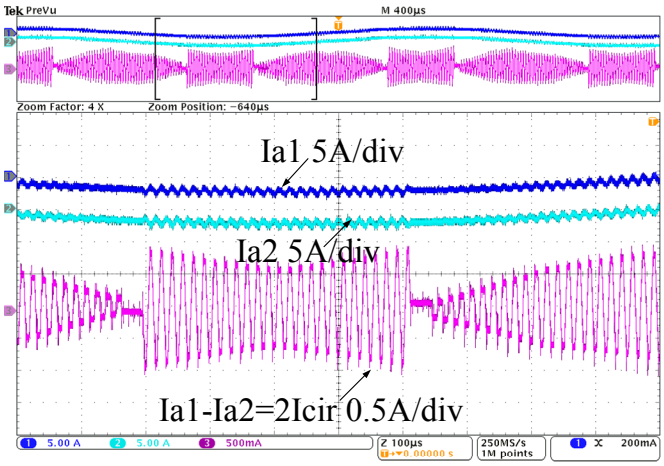


(b)

Fig. 4-18. (a) Output currents (Ia1 and Ia2) of two interleaved inverters and circulating current (Icir) at M=0.8, (b) Zoom in waveforms.



(a)

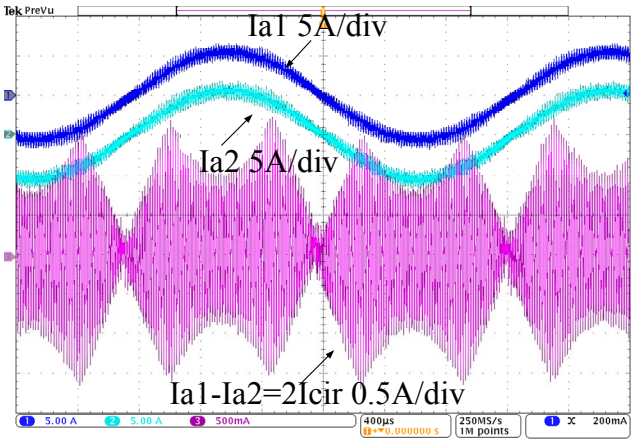


(b)

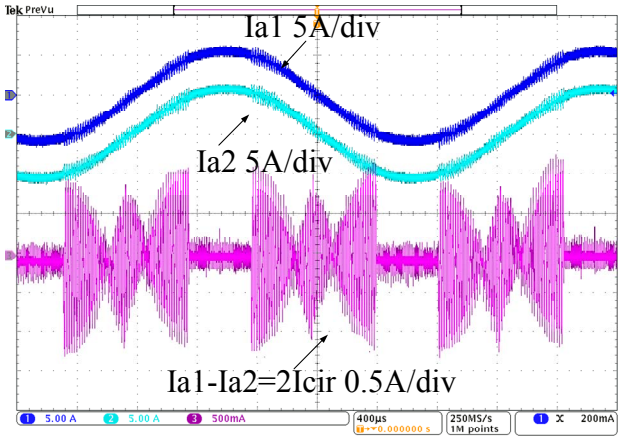
Fig. 4-19. (a) Output currents (Ia1 and Ia2) of two interleaved inverters and circulating current (Icir) at M=0.4, (b) Zoom in waveforms.

From (4-8), the maximum flux linkage is proportional to the maximum circulating current. The maximum circulating current value with the five modulation methods at different modulation indexes are measured and summarized as shown in Fig. 4-21. The results match the trends illustrated in Fig. 4-11. The proposed modulation method has the lowest maximum flux linkage in all the modulation methods. The maximum flux linkage reduced to around 60% of that of other

modulation methods in high modulation index range. The output current THD with the five modulation methods are also measured and summarized in Fig, 4-22. The proposed modulation method has similar THD behavior as other continuous PWM methods.

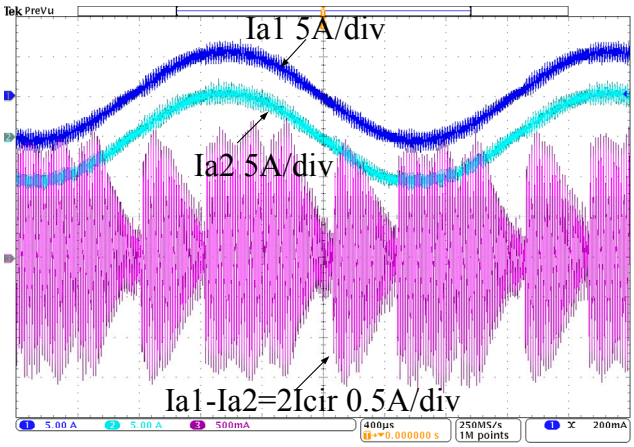


(a)

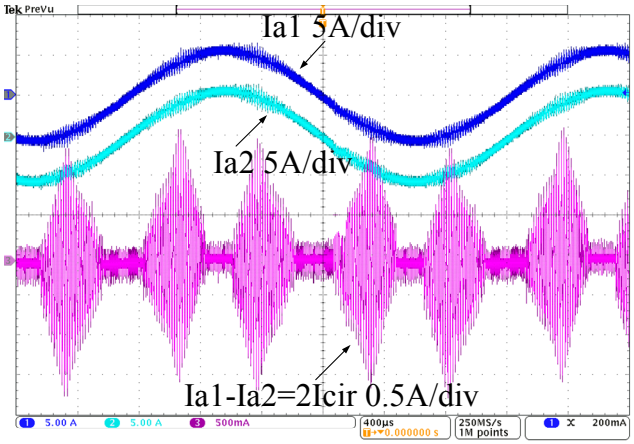


(b)

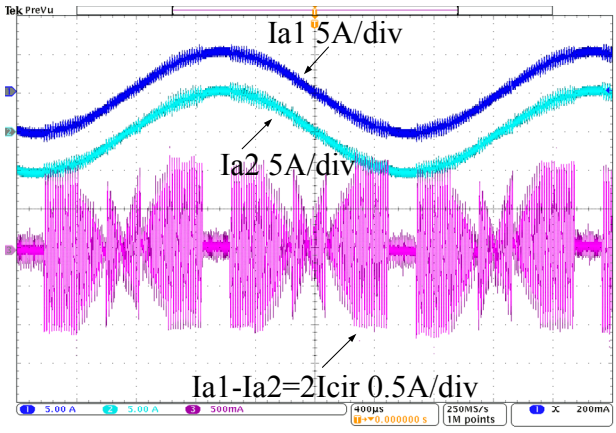
Fig. 4-20. Circulating currents with different PWM methods at M=0.8, (a) SPWM, (b) DPWM, (c) NTSV, (d) CMR, (e) the proposed modulation.



(c)



(d)



(e)

Fig. 4-20. Continued.

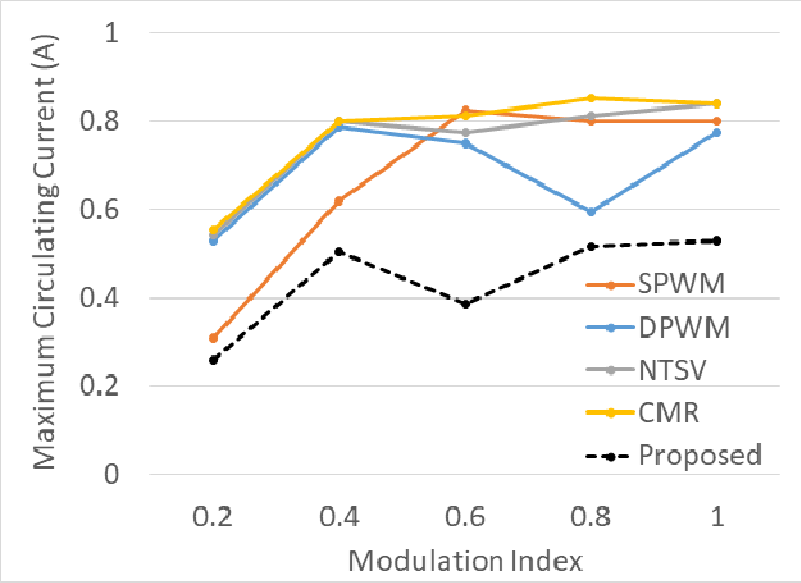


Fig. 4-21. Maximum circulating currents with different modulation methods.

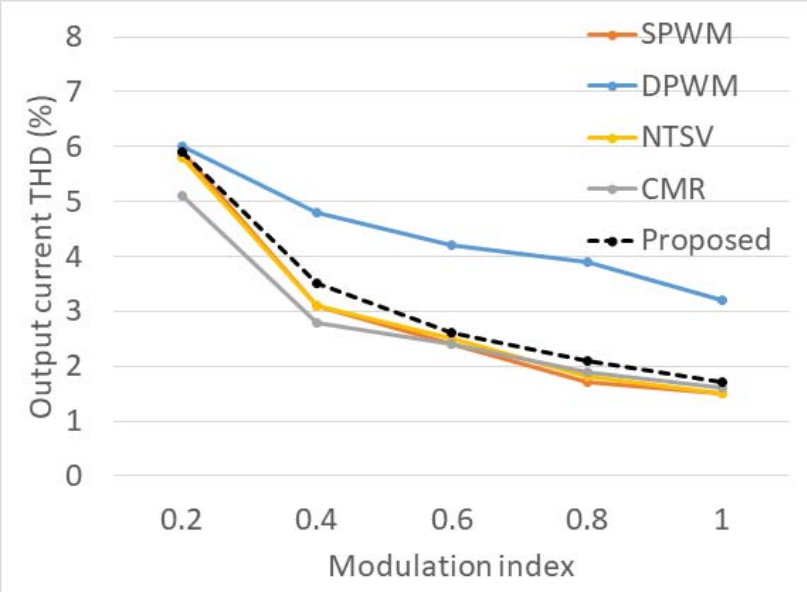


Fig. 4-22. Output current THD with different modulation methods.

4.4 Conclusion

This chapter aims to minimize the flux linkage in the coupled inductor for parallel interleaved three-level inverters. A carrier based PWM method is proposed which could achieve the lowest maximum flux linkage in the coupled inductor. This modulation method is realized by injecting an optimal zero sequence offset to the sinusoidal modulation. The optimal zero sequence offset is made up by several zero sequence candidates and is a function of modulation index. The proposed modulation method has the capability to balance the neutral point voltage for three-level NPC inverter.

The proposed modulation method is compared with other popular carrier based and space vector based PWM methods for three-level inverter. When modulation index is low, the flux linkage of proposed modulation is reduced to around 50% of that of DPWM, NTSV and CMR methods, and to around 80% of that of SPWM. When modulation index is high, the maximum flux linkage of the proposed modulation is reduced to around 60% of the flux linkage of other modulation methods. The proposed modulation method has similar loss and THD characteristics as other continuous PWM methods.

The effectiveness of the proposed modulation method is verified by simulation and experimental results on two parallel interleaved three-level active NPC inverters. The proposed modulation method is suitable for coupled inductor in the applications where the switching frequency is relatively low and the coupled inductor design is governed by saturation of the magnetic core.

5. Inverter and Filter Topology to Reduce CM Noise for Three-Level Inverter

EMI filter is required in inverter system to suppress EMI noise and pass EMI standards. Bulk EMI filter is one of the main barrier for achieving high power density. One effective approach to reduce the required EMI filters is to reduce EMI noise. This chapter investigates inverter and filter topology to reduce CM noise for three-level inverter. The three-level fourth-leg inverter topology is developed for CM noise reduction. An impedance balance filter topology is proposed to reduce CM noise for aircraft motor drive application where both dc and ac sides need to pass EMI standards.

5.1 Three-Level Fourth-leg Topology

The fourth-leg topology was first used by Julian et al. to reduce CMV and CM noise. A fourth-leg and a fourth phase LC filter are inserted into the two-level inverter. The zero vector is not used in the modulation to achieve zero CMV. This section investigates the fourth-leg for CM noise reduction in three-level inverters. Unlike the case in two-level inverters, the nearest three vectors can be maintained to synthesize the reference while achieving zero CMV in three-level inverters with the fourth-leg.

5.1.1 Topology and Modulation

The three-level active NPC inverter with the fourth-leg topology is shown in Fig. 5-1 [219]. Similar to the two-level inverter, the fourth-leg is connected to the three main phases through a fourth phase LC filter. To achieve zero CMV, the summation of the four phase-legs voltages

should be zero as (5-1), and the fourth phase LC filter parameters should be identical to the three phase LC filter as (5-2).

$$V_a + V_b + V_c + V_f = 0 \qquad (5-1)$$

$$L_f = L, C_f = C \qquad (5-2)$$

In a two-level inverter, when the zero vector - PPP and NNN as shown in Fig. 5-2 - are applied, a two-level fourth-leg output voltage, which only has two states P or N, cannot compensate the voltage summation of three phases and meet (5-1).

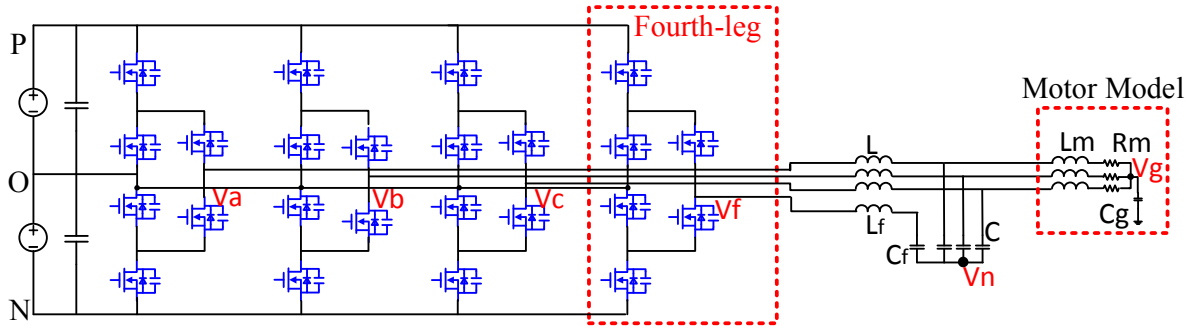


Fig. 5-1. Three-level active NPC inverter with the fourth-leg.

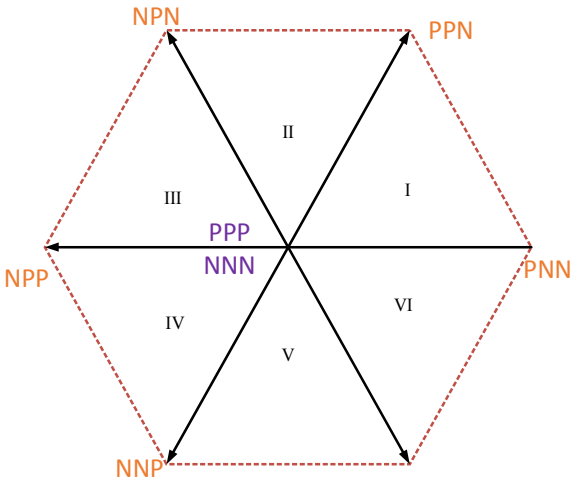
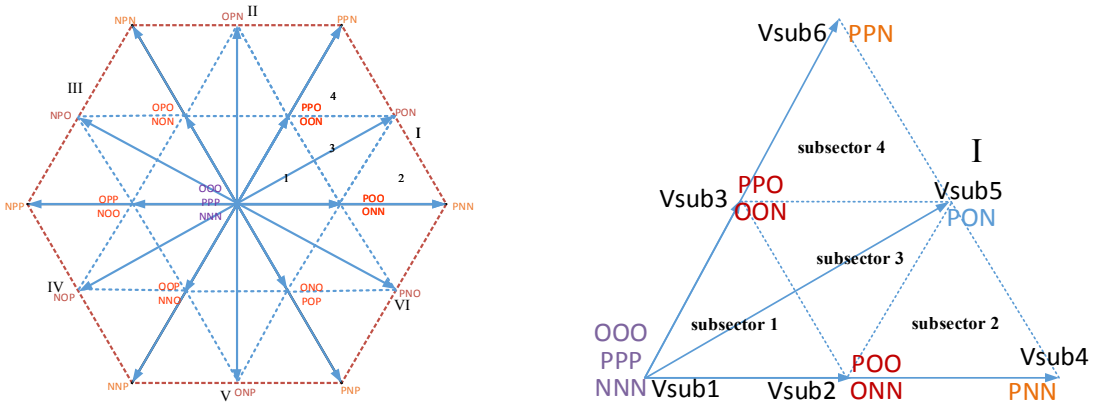


Fig. 5-2. Space vectors for a two-level inverter.

However, the situation in the three-level inverter is different. Fig. 5-3(a) shows the space vectors for three-level SVM. The small and zero vectors have redundant switching states. By appropriately selecting the redundant switching states, (5-1) can be met in all the sectors. Fig. 5-3(b) shows the vector details of sector I. The space vector arrangement of large sector 1 for the three main phases and the fourth-leg are illustrated as shown in Fig. 5-4. The space vector arrangement of sector II to sector VI are similar and will not be repeated here. In order to meet (5-5), the redundant switching state with lower CMV will always be selected (for example, POO is selected instead of ONN). Therefore, the modulation scheme of the three main phases is actually the same as the CMR scheme. Three nearest space vectors are used to synthesis the reference, and the max modulation index is the same as conventional SVM. One phase has no switching action in every switching circle, so the switching loss will be reduced compared to the conventional SVM. For the fourth-leg, it has four switching actions in every switching circle. The dwell time of vectors for the fourth-leg follows the three main phases. No extra calculation is need in the digital controller for the gating control of the fourth-leg.



(a) (b)

Fig. 5-3. (a) Space vectors a for three-level inverter, (b) vectors of sector I.

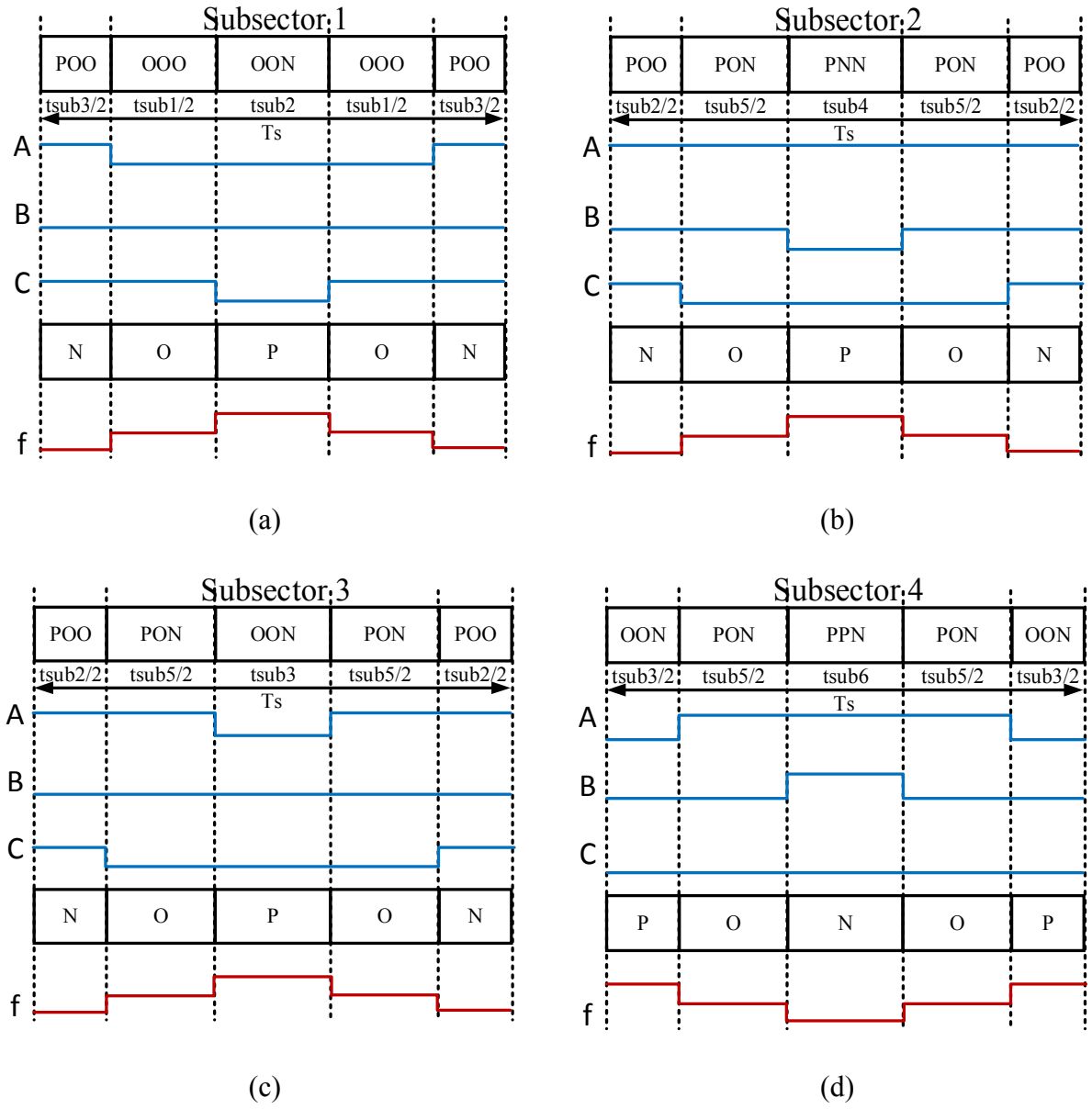


Fig. 5-4. Space vector arrangement for three main phase legs and the fourth-leg in sector I, (a) subsector 1, (b) subsector 2, (c) subsector 3, (d) subsector 4.

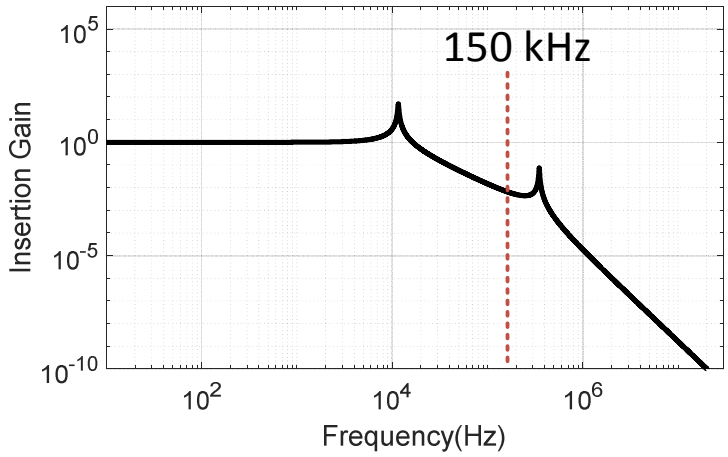


Fig. 5-5. Insertion gain amplitude versus frequency.

The CM noise attenuation performance of the four-leg topology is investigated. With the fourth-leg added, based on the basic circuit theory, the transfer function from the motor neutral point voltage V_g to the fourth-leg output voltage V_f can be derived as (5-3).

$$G1 = \frac{V_g}{V_f} = \frac{-4}{C_g} \frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1}$$

$$b_4 = 4LCL_m + 3CL^2, b_3 = 4R_m LC + 4RCL_m + 6RCL,$$

$$b_2 = \frac{12LC}{C_g} + 4RCR_m + 4(L + L_m) + 3CR^2, b_1 = \frac{12RC}{C_g} + 4(R + L_m), b_0 = \frac{12}{C_g} \quad (5-3)$$

Without the fourth-leg,

$$V_g = \frac{V_a + V_b + V_c}{3} = -\frac{V_f}{3}$$

$$G2 = \frac{V_g}{V_f} = -\frac{1}{3} \quad (5-4)$$

Hence, the insertion gain IG can be defined as

$$IG = \left|\frac{G1}{G2}\right| = \frac{12}{C_g}\frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} \qquad (5-5)$$

The insertion gain amplitude is plotted as shown in Fig. 5-15. In the EMI frequency range (150 kHz to 30 MHz), the amplitude of the insertion gain is significantly reduced, which means V_g and CM noise current will be significantly reduced when the fourth-leg is applied.

5.1.2 Experimental Results

A SiC-based three-level ANPC inverter is constructed for experimental verification as shown in Fig. 5-6. The main parameters of the inverter are summarized in Table 5-1.

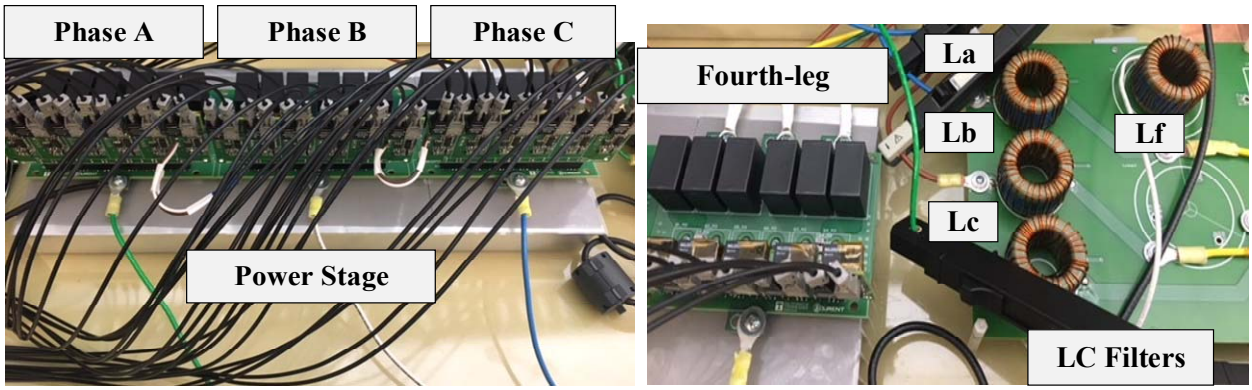


Fig. 5-6. The three-level active NPC inverter.

Table 5-1. Main Parameters of the Inverter

DC input voltage	200V
Fundamental frequency	400 Hz
Carrier frequency	60 kHz
SiC MOSFETs	C3M0065100K
LC filters	L=390 uH, C=0.47 uF

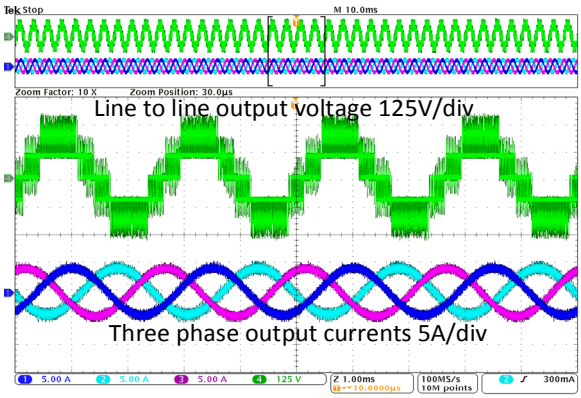
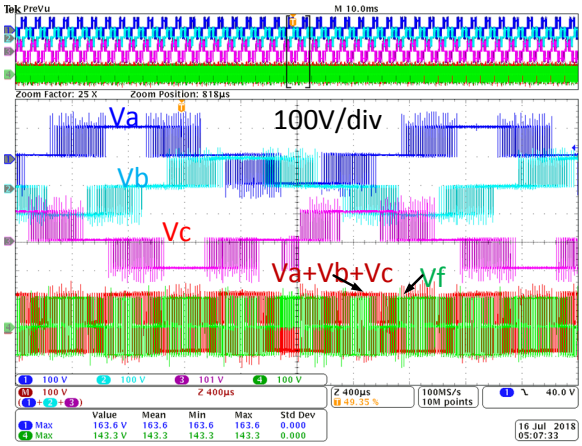
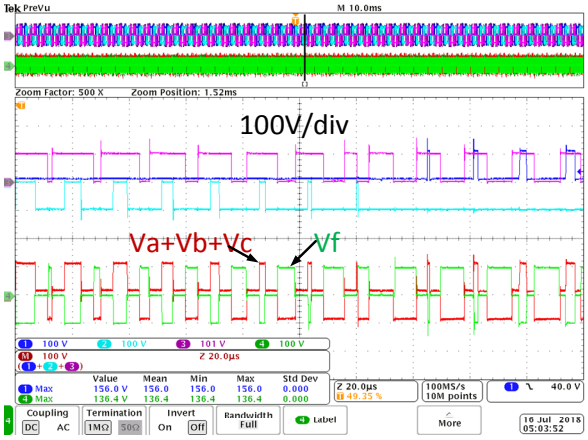


Fig. 5-7. Inverter output line to line voltage and three phase currents.



(a)



(b)

Fig. 5-8. (a) Three phase output voltage, their summation, and the fourth-leg output voltage, (b) zoom in waveforms.

Fig. 5-7 shows the three-level ANPC inverter output line voltage and three phase currents, which is the operating point for EMI noise test. Fig. 5-8(a) shows the three phase output voltages V_a, V_b, V_c, their summation $V_a + V_b + V_c$, and the fourth-leg output voltage V_f. Fig. 5-8 (b) is the zoom in waveforms. From Fig. 5-8(b), the voltage of the fourth-leg cancels out with the three phase voltages summation, so (5-1) is met.

The comparison between the measured CM EMI noise without the fourth-leg and with the fourth-leg are shown in Fig. 5-9. It can be observed that the CM noise is significantly reduced with the fourth-leg applied. Specifically, at the first noise peak (3rd carrier harmonic, 180 kHz) in the EMI frequency range, the CM noise has been reduced by ~25 dB. In the ideal case, the CM noise current will be eliminated. However, as can be observed in Fig. 5-8(b), the rising/falling edge of the fourth-leg does not exactly overlap with the falling/rising edge of the three phase voltage summation. More accurate gate signal tuning method can be considered to improve the CM noise attenuation performance.

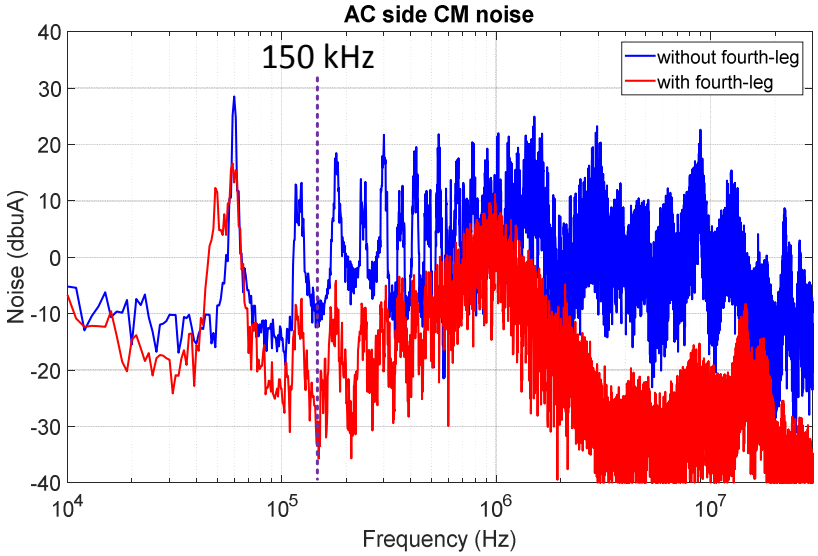


Fig. 5-9. Tested CM noise comparison w/ and w/o the fourth-leg.

5.1.3 Discuss on Alternative Fourth-leg Filter Structure

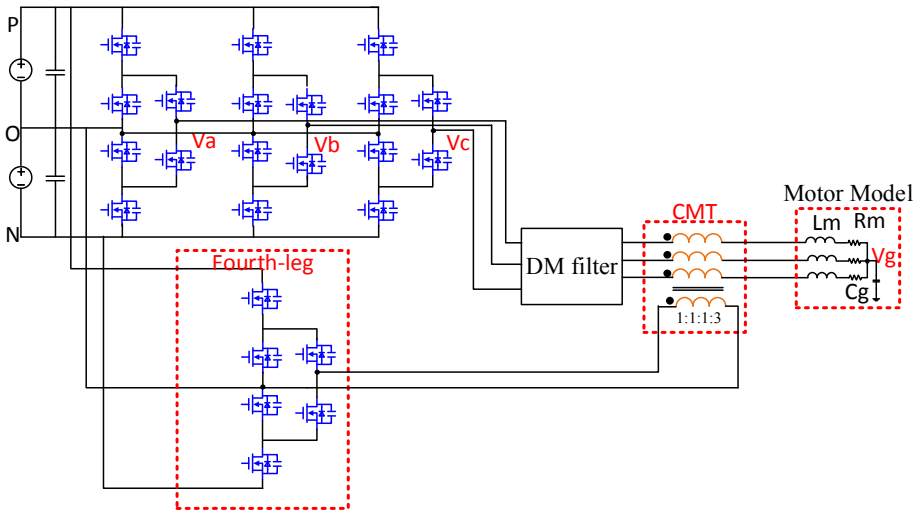
As discussed above, the fourth-leg of three-level NPC inverter can compensate the CMV generated by the three main phase legs. The voltage generated by the fourth-leg needs to be injected to the main circuit through a certain filter network.

The first fourth-leg filter structure considered is LC type DM filter. As shown in Fig. 5-1, both the three main phase legs and the fourth-leg need a single stage LC filter to be connected together. The benefit of this filter structure is that it can make use of the DM filters existing in the main circuit when DM filters are necessary. For example, for motor drive in aircraft application, the inverter ac output is connected to the motor through long cables and needs to meet DO-160 EMI standards. DM LC filters are required to suppress the DM EMI noise. Hence, the main circuit LC filters are not dedicated filters for the implementation of the fourth-leg circuitry.

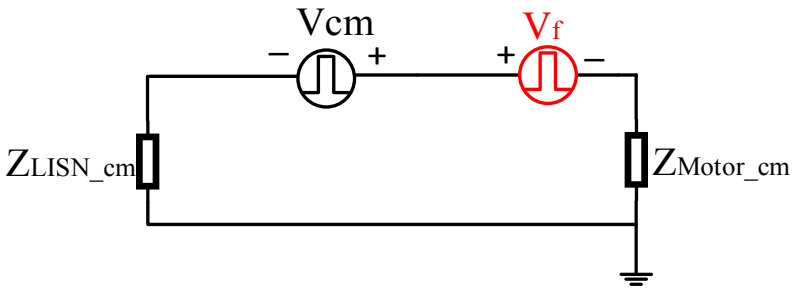
However, two limitations exist with the DM filter structure. The first limitation is the limited DM filter type can be employed. For example, an LCL filter may be optimal for the three phase inverter DM noise reduction. But the fourth-leg is not able to be connected to the three main phase through a LCL filter. If the three main phases still use the LCL filters and the fourth-leg uses a LC filter, the CM noise reduction performance will be significantly reduced. The second limitation is that the fourth-leg is coupled with the main circuit power level. The fourth-leg filter parameters are exactly the same as the three main phase legs DM filters, which means that the current ripple of the fourth-leg is at the same level as the current ripple of the three main phases. For high power applications, the losses in the fourth-leg devices are high, and the size of the fourth-leg LC filter is large.

The second fourth-leg filter structure considered is a common-mode transformer (CMT). As shown in Fig. 5-10(a), the fourth-leg is connected to the main circuit through a CMT. Fig. 5-10(b)

shows the simplified CM equivalent circuit. Compared to the first filter structure, this filter structure is independent of the main circuit DM filter structure. However, as the CMT is cascade in the main circuit, the fourth-leg is still coupled with the main circuit power level. Also, the CMT is complicated. For high power applications, the losses in the fourth-leg devices are high, and the size of the CMT is large.



(a)



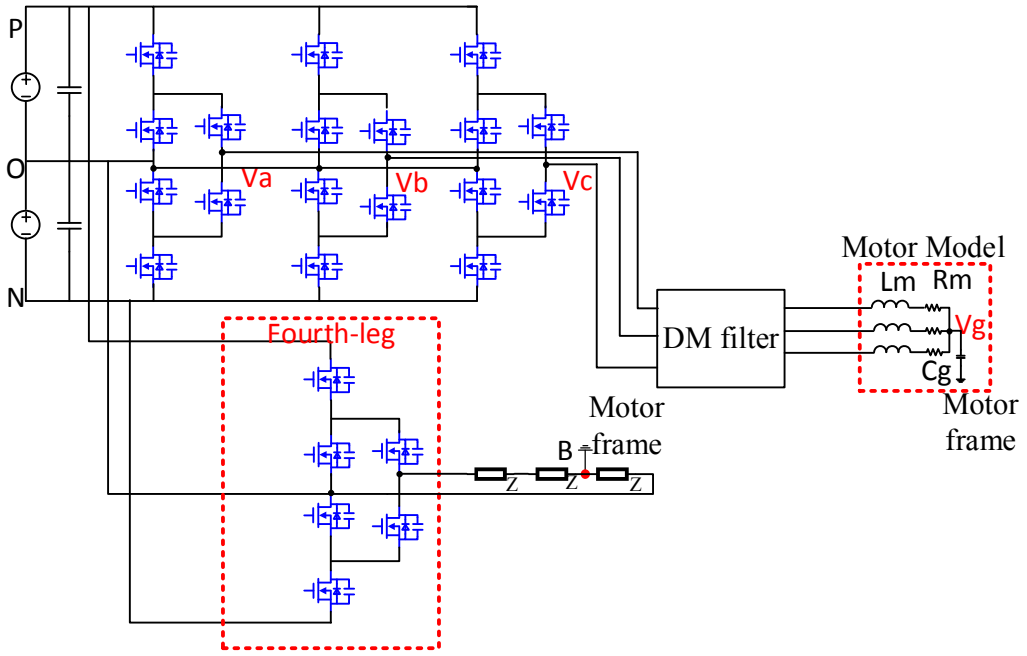
(b)

Fig. 5-10. (a) Fourth-leg connected to three main phases through a CMT, (b) simplified CM equivalent circuit.

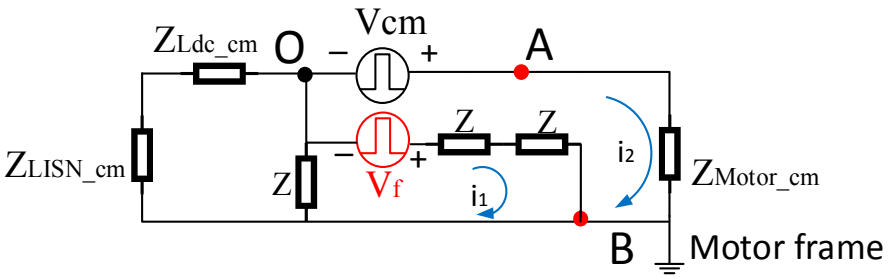
To decouple the fourth-leg from the main circuit power level, a filter structure is proposed as shown in Fig. 5-11. In Fig. 5-11(a), the voltage generated by the fourth-leg is connected to an impedance (R or RC, indicated by Z in Fig. 5-21) network. Point B is connected to the motor frame, which is usually grounded. Fig. 5-11(b) shows the CM equivalent circuit. When i_1 is much large than i_2, which can usually be satisfied as the CM current flowing through the motor is very small, voltage V_{BO} is almost one third of the voltage V_f generated by the fourth-leg. Then, the potential of point A and B is the same, no CM voltage is applied to the motor.

The fourth-leg with the impedance network is not directly connected to the main circuit, and the current of the fourth-leg is determined only by the impedance network. Hence, the proposed filter structure is independent of main circuit DM filter, and it decouples the fourth-leg from the main circuit power level. As the potential of point A and B is same as the ground and considered as zero, point O becomes a pulsating point, and a CM filter is needed in the dc side.

In conclusion, the first fourth-leg filter structure is suitable for a main circuit that DM filter exists and DM filter type can be implemented on the fourth-leg. The second fourth-leg filter structure can be employed to the main circuit where DM filter is not needed or DM filter type cannot be implemented on the fourth-leg. The proposed fourth-leg filter structure is independent of the main circuit DM filter and decouples the fourth-leg from the main circuit power level. Hence, it is suitable for high power applications. However, a CM filter in the dc side is required.



(a)



(b)

Fig. 5-11. (a) Proposed fourth-leg connected filter, (b) simplified CM equivalent circuit.

5.2 Impedance Balancing Filter Topology

5.2.1 Existing Impedance Balancing Circuit for DC side CM Noise Reduction

The impedance balancing circuit for dc side CM noise attenuation is suitable for motor drive applications where only the dc side needs to pass EMI standards. Fig. 5-12 shows such a motor drive system with the dc side impedance balancing circuit. L_1 and C_1 are the dc side conventional

CM filters. An additional inductor L_2 is connected between the dc and ac side to establish the impedance balancing bridge. The simplified CM equivalent circuit is shown in Fig. 5-13. The inverter CM noise source is modeled as V_{cm}, the motor and cable CM impedance is modeled as a capacitor C_{mg}, and C_{bg} denotes the dc side CM capacitance including CM capacitor and power stage parasitic capacitance. These components form an impedance bridge, and the dc side line impedance stabilization networks (LISNs) CM impedance is in the middle of the bridge.

The CM current flowing through the LISNs will theoretically be zero if the bridge impedance meets

$$\frac{L_2}{L_1} = \frac{C_{bg}}{C_{mg}} \qquad (5-6)$$

Since the motor and cable CM impedance is one of the branches which establish the dc side impedance balancing bridge, its impedance characteristic will influence the CM noise reduction performance of the impedance balancing circuit. The impedance bridge can be well balanced only when the motor and cable CM impedance can be modeled as a constant value capacitor. An improvement can be made as shown in Fig. 5-14. A three phase CM capacitor C_{CM} is paralleled with the motor and cable.

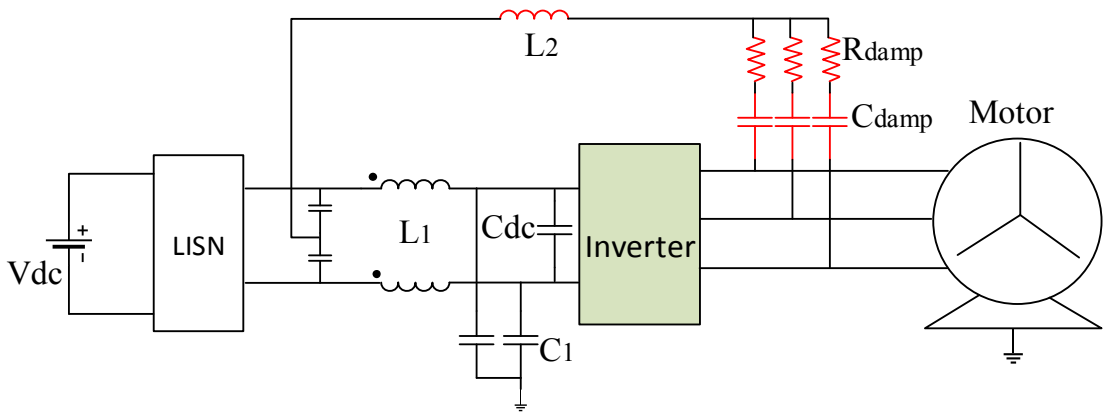


Fig. 5-12. Dc side impedance balancing circuit.

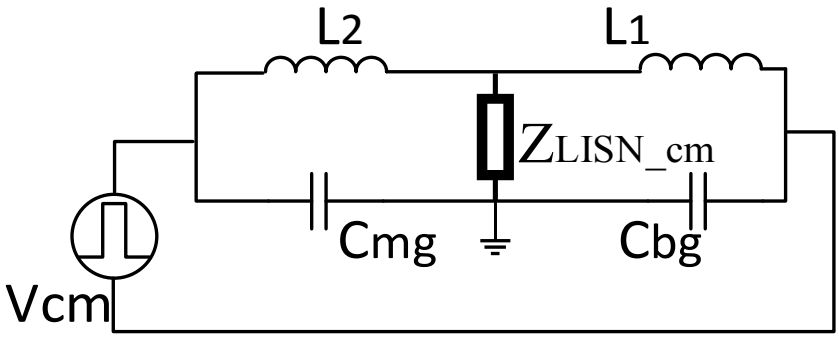


Fig. 5-13. Simplified equivalent CM circuit.

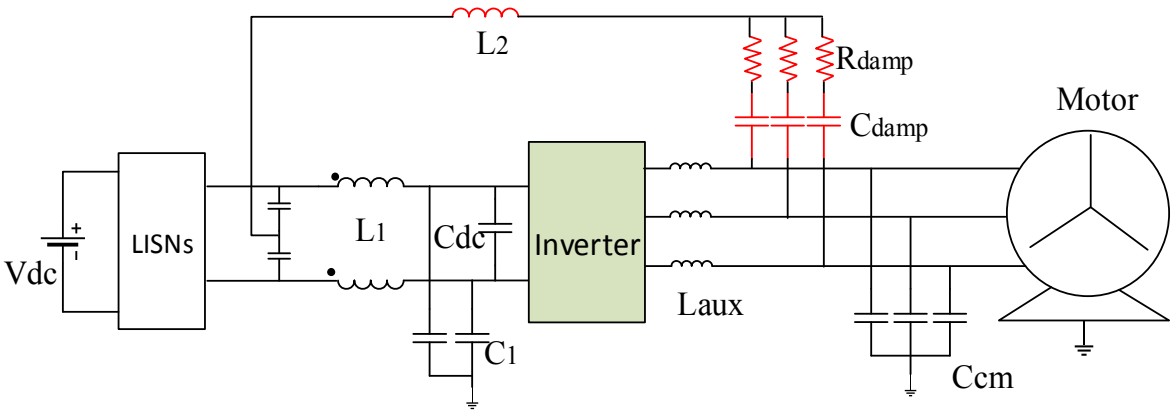


Fig. 5-14. Improvement of the dc side impedance balancing circuit.

If the impedance meets the relationship

$$Z_{Ccm} \ll Z_{motor_{CM}} \tag{5-7}$$

Then, the impedance behavior of this branch largely depends on capacitor C_{CM} instead of the motor and cable impedance. Hence, (5-6) can be met in a wider EMI frequency range, and the effectiveness and noise reduction performance of the dc side impedance balancing circuit will be better. A small auxiliary inductor L_{aux} can be inserted into the ac side to eliminate the influence of the additional ac side CM capacitor on switching speed. A small air core auxiliary inductor can effectively help to achieve faster switching and reduce switching loss without much loss penalty. Also, the auxiliary inductor is capable of mitigating motor side terminal overvoltage, leakage current, and so on.

5.2.2 Analysis of Motor Drive with Input and Output CM Filters

Fig. 5-15 shows the dc-fed three phase motor drive system with both input and output EMI filters. CM noise conducts in the same direction of each phase and flows to the ground through motor parasitic capacitance and the ac side EMI filter, and then flows back to the noise source through the line impedance stabilization networks (LISNs) and the dc side EMI filter. As shown in Fig. 5-15, CM noise current is measured at both the input and output of the inverter system. The dc side CM noise current is defined as $i_{cm\_dc} = (i_p + i_n)/2$ and the ac output motor side CM noise current is defined as $i_{cm\_ac} = (i_a + i_b + i_c)/3$. Both the dc and ac sides EMI noise current need to meet EMI standards.

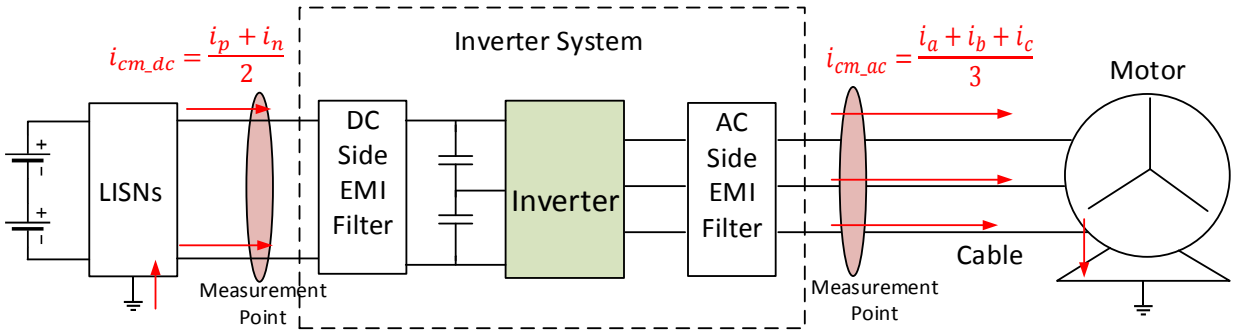


Fig. 5-15. Dc-fed motor drive system with input and output EMI filters.

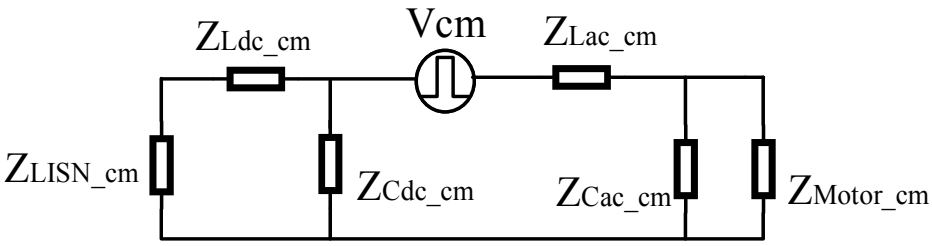


Fig. 5-16. CM equivalent circuit with one stage LC filter at both the dc and ac sides.

The dc and ac side CM noise current share the same propagation path and are coupled with each other, which makes the CM noise reduction more complex. Fig. 5-16 shows the CM equivalent circuit for a single stage LC filter applied to both the dc and ac sides. The CM impedance of the LISNs is represented as Z_{LISN_cm}. Motor and cable CM impedance is represented as Z_{motor_cm}. CM noise current flowing through the ac side motor and dc side LISNs can be reduced by increasing the conventional CM filter inductance or capacitance. However, increasing CM capacitance on one side will decrease CM noise current on this side but increase CM noise current on the other side. For example, when the ac side CM capacitance increases, CM noise flowing to the motor decreases. But the entire loop CM impedance decreases, and CM current flowing to the dc side LISNs increases. Also, the total capacitance that can be applied to the system is limited by system leakage current requirement. On the other hand, increasing CM inductance increases the

entire loop CM impedance and thus reduces both the dc and ac sides CM noise. However, unlike capacitors which only conduct high frequency harmonics, the inductors are in the main current conduction path and are usually bulky since a large core and winding should be used to deal with the main current produced leakage flux density and power loss. Increasing the inductance may significantly degrade system efficiency and power density, especially in high power converter systems. Therefore, it is desired to develop new EMI techniques which can reduce both the dc and ac sides CM noise in a power converter system where both sides need to pass EMI standards, and in the meantime, reduce the required inductance of the conventional CM inductors.

5.2.3 Proposed Impedance Balancing Circuit

The proposed impedance balancing circuit for CM noise reduction is shown in Fig. 5-17 [220]. Unlike the impedance balancing circuit for the dc side CM noise reduction, two auxiliary branches are added: one branch consists of an inductor L_r connecting ac side and the ground (C_r is used to block the fundamental and low frequency components and R_r is used to damp the resonance); another branch is a capacitor C_{return} connecting the ac and dc sides through the ac side DM capacitors Y connection point and dc-link cap midpoint. The components L_{cmdc} , C_{cmdc} , $L_{cmac}$and C_{dmac} are conventional filters of the dc and ac sides.

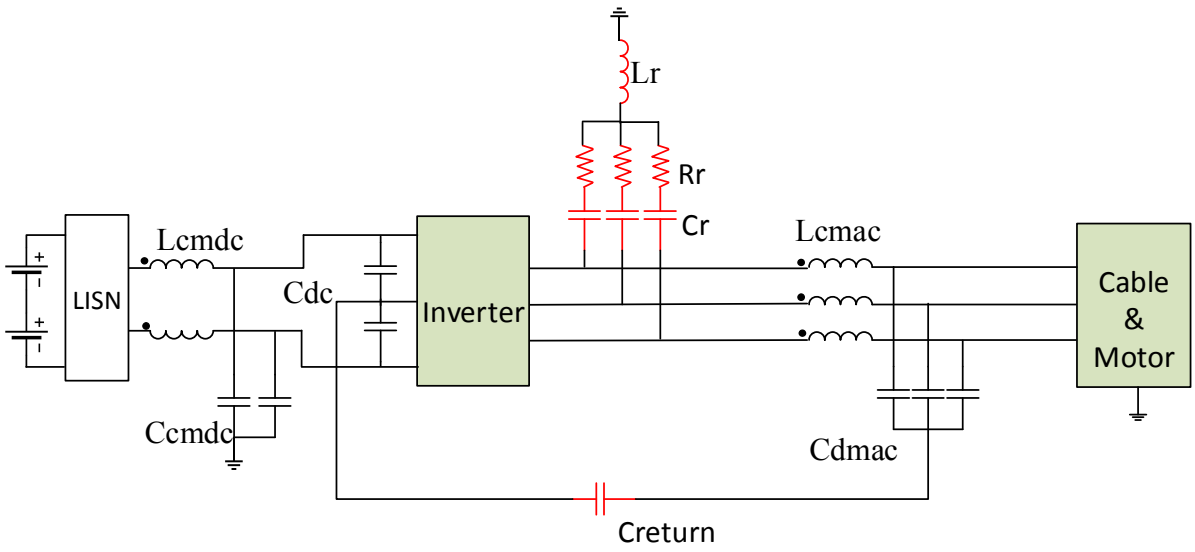
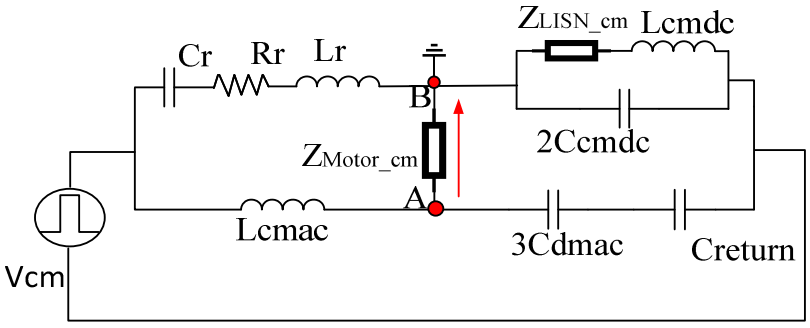
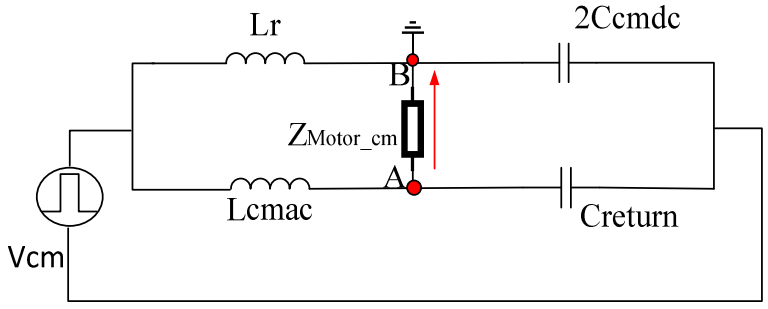


Fig. 5-17. Proposed impedance balancing circuit.



(a)



(b)

Fig. 5-18. (a) CM equivalent circuit. (b) Simplified CM equivalent circuit.

First, the influence of the proposed impedance balancing circuit on the ac motor side CM noise current is investigated. Fig. 5-18(a) shows the CM equivalent circuit of the inverter system. In the EMI frequency range (150 kHz ~ 30 MHz), the impedance relationship satisfies

$$Z_{Lr} \gg Z_{Cr} + R_r$$

$$Z_{2Ccmdc} \ll Z_{Lcmdc} + Z_{LISN\_cm}$$

$$Z_{Creturn} \gg Z_{3Cdmac} \qquad (5-8)$$

Hence, the CM equivalent circuit can be simplified to the circuit shown in Fig. 5-18(b). The four components L_r , L_{cmac}, $2C_{cmdc}$, and C_{return} establish an impedance bridge. If the impedance bridge meets the relationship

$$\frac{Z_{Lr}}{Z_{Lcmac}} = \frac{Z_{2Ccmdc}}{Z_{Creturn}} \qquad (5-9)$$

The potentials of points A and B are the same (i.e., $V_{AB} = 0$). Thus, CM current flowing through the ac side motor can theoretically be zero. (5-9) can be simplified, as,

$$\frac{L_r}{L_{cmac}} = \frac{C_{return}}{2C_{cmdc}} \qquad (5-10)$$

Therefore, for ac side CM noise reduction, the impedance balancing circuit parameters should meet (5-10) to maximize the ac side CM noise reduction performance. Note that the motor CM impedance is not involved, as shown in (5-10). The noise reduction performance of the impedance balancing circuit is only determined by L_r , L_{cmac}, C_{cmdc}, and C_{return}. Hence, the CM noise reduction performance is not dependent on motor and cable models. It is not necessary that the motor CM model must behave like a constant value capacitor in a wide EMI frequency range.

Next, the influence of the proposed impedance balancing circuit on the dc LISN side CM noise is analyzed. Without the impedance balancing circuit (the added two auxiliary branches), the CM

current path flowing through the LISN is shown in Fig. 5-19(a). With the impedance balancing circuit, in the ideal case, the impedance bridge is perfectly balanced and no current will flow through the motor CM impedance. The motor CM impedance branch can be considered as open circuit. The CM current path flowing through the LISN is shown in Fig. 5-19(b). To reduce CM current flowing to the LISNs, the propagation path impedance with impedance balancing circuit should be larger than that without the impedance balancing circuit,

$$Z_{Lr} > Z_{Lcmac} + Z_{Motor_{cm}} \qquad (5-11)$$

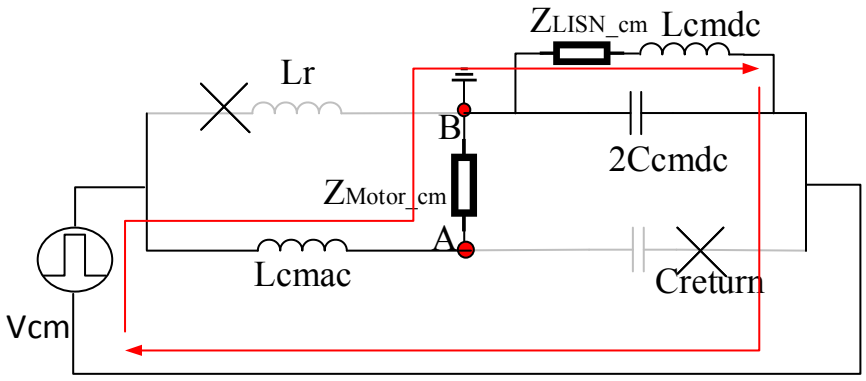
Define the impedance balancing circuit ratio *n* as

$$n = \frac{L_r}{L_{cmac}} = \frac{C_{return}}{2C_{cmdc}} \qquad (5-12)$$

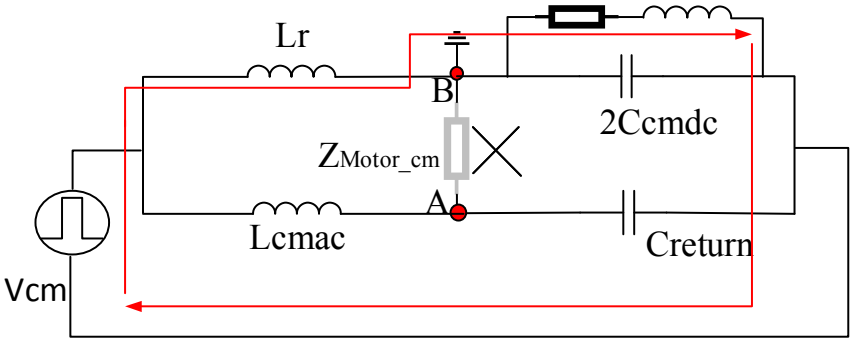
To meet (5-15), the ratio *n* should at least satisfy

$$n > 1 \qquad (5-13)$$

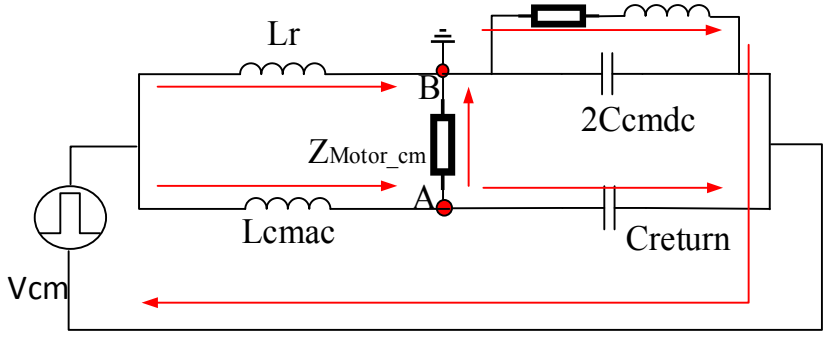
With larger *n*, CM current flowing through the LISNs will be smaller. Considering that the impedance bridge may not be perfectly balanced over all the frequency range, there is CM current flowing through the LISNs. Then, the CM current path flowing through the LISNs is shown in Fig. 5-19(c). The auxiliary capacitor C_{return} will help to bypass CM noise current. With larger *n*, C_{return} is larger, more CM current will be bypassed. Therefore, with larger impedance balancing circuit ratio *n,* L_r and C_{return}, which both help to reduce CM noise current flowing through the LISNs, will be larger, and as a result, better dc side CM noise reduction performance is achieved.



(a)



(b)



(c)

Fig. 5-19. (a) LISN CM current conduction path w/o impedance balancing circuit; (b) LISN CM current conduction path w/ impedance balancing circuit; (c) LISN CM current conduction path considering the impedance bridge is not perfectly balanced.

Therefore, for dc side CM noise reduction, the impedance balancing circuit parameters should meet (5-13), and better dc side CM noise reduction performance can be obtained with larger impedance balancing circuit ratio *n*.

In conclusion, the proposed impedance balancing circuit can reduce both the ac motor side and the dc LISN side CM noise if the design criteria are met. The ac side motor CM impedance is in the middle of the impedance bridge, and no CM current flows to the motor since the CM current of the impedance bridge branches cancel with each other if the bridge is well balanced. The impedance bridge also changes the propagation path impedance of the CM noise current flowing to the LISNs, and thus reduce the dc side CM noise.

5.2.4 Noise Attenuation Performance Modeling and Analysis

The CM noise attenuation performance of the proposed impedance balancing circuit is analyzed. The impedance bridge analysis above does not consider the power stage capacitive coupling to the ground. Considering this parasitic capacitance, the CM equivalent circuit is now modified as the circuit in Fig. 5-20.

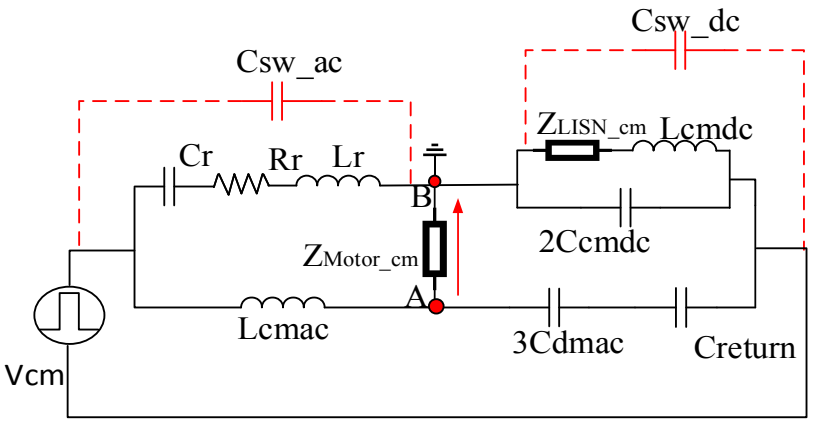


Fig. 5-20. CM equivalent circuit considering power stage parasitic capacitance.

The ac side power stage parasitic capacitance and the dc side power stage parasitic capacitance are presented as C_{sw_ac} and C_{sw_dc}, respectively. The ac side power stage parasitic capacitance is in parallel with the auxiliary inductor L_r and dc side power stage parasitic capacitance is in parallel with the dc side CM capacitor C_{cmdc}.

The impedance relationship in (5-9) is modified to

$$\frac{Z'_{Lr}}{Z_{Lcmac}} = \frac{Z'_{2Ccmdc}}{Z_{Creturn}} \qquad (5-14)$$

where the impedance $Z'_{Lr} \approx Z_{Lr} \,||\, Z_{Csw\_ac}$ and $Z'_{2Ccmdc} \approx Z_{2Ccmdc} \,||\, Z_{Csw\_dc}$.

Usually the dc and ac sides power stage parasitic capacitance are in the tens or hundreds of pico-farad range, and the dc side CM capacitors are in several nanofarads range. The dc side CM capacitor is much larger than dc side power stage parasitic capacitance, so Z'_{2Ccmdc} is nearly the same as Z_{2Ccmdc}. Hence, the dc side power stage parasitic capacitance will not influence the CM noise attenuation performance of the impedance balancing circuit. However, at the ac side, in the interested EMI frequency (150 kHz ~ 2 MHz) range, when L_r is not very large, $Z_{Lr} \ll Z_{Csw\_ac}$, Z'_{Lr} mainly depends on Z_{Lr}. But if the impedance balancing ratio *n* is very large, Z_{Lr} is very large and comparable to Z_{Csw_ac}, then Z'_{Lr} is limited by Z_{Csw_ac} and will not increase as much as Z_{Lr}. The relationship in (5-14) cannot be met and the impedance bridge will not be well balanced.

Theoretically, the ac side CM noise is zero if (5-14) is satisfied over all the EMI frequency range. In fact, due to the physical implementation of EMI filters and the parasitics of both power stage and CM filters, the left side and right side of (5-14) cannot be identical in the interested EMI frequency range, and some difference always exists.

To quantify the impact of imperfectly balanced impedance bridge on the ac side CM noise

attenuation performance, an analytical model is provided. Defining the insertion gain IG as

$$IG = \left|\frac{I_{cm2}}{I_{cm1}}\right| \qquad (5-15)$$

where I_{cm1} and I_{cm2} are the CM current flowing to the motor without and with the impedance balancing circuit, respectively. The CM equivalent circuit in Fig. 9 can be simplified to the circuit shown in Fig. 5-21. The impedances $Z_1 = (Z_{Lr} + R_r + Z_{cr}) \,||Z_{Csw\_ac}$, $Z_2 = L_{cmac}$, $Z_3 = \left(Z_{LISN_{cm}} + Z_{Lcmdc}\right)||Z_{2Ccmdc}||Z_{Csw\_dc}$, $Z_4 = Z_{3Cdmac} + Z_{Creturn}$, and $Z_m = Z_{Motor\_cm}$.

Without the impedance balancing circuit, the motor CM current I_{cm1} is

$$I_{cm1} = \frac{1}{Z_2 + Z_m + Z_3} V_{cm} \qquad (5-16)$$

With the impedance balancing circuit, the motor CM current I_{cm2} can be expressed as

$$I_{cm2} = \frac{Z_1 Z_4 - Z_2 Z_3}{Z_1 Z_2 Z_3 + Z_1 Z_2 Z_4 + Z_1 Z_3 Z_4 + Z_2 Z_3 Z_4 + Z_1 Z_2 Z_m + Z_1 Z_4 Z_m + Z_2 Z_3 Z_m + Z_3 Z_4 Z_m} V_{cm} \qquad (5-17)$$

Hence, the insertion gain can be expressed as an equation of the five impedances

$$\mathrm{IG} = \frac{(Z_1 Z_4 - Z_2 Z_3)(Z_2 + Z_3 + Z_m)}{Z_1 Z_2 Z_3 + Z_1 Z_2 Z_4 + Z_1 Z_3 Z_4 + Z_2 Z_3 Z_4 + Z_1 Z_2 Z_m + Z_1 Z_4 Z_m + Z_2 Z_3 Z_m + Z_3 Z_4 Z_m} \qquad (5-18)$$

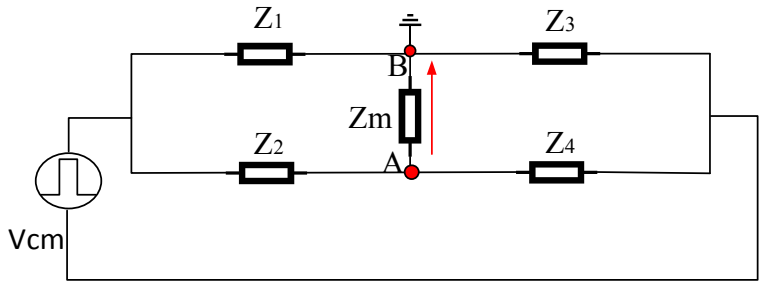


Fig. 5-21. Simplified CM equivalent circuit.

All five impedances can be measured or calculated. With (5-18), the noise attenuation performance of the ac side CM impedance balancing circuit can be quantified. Also, the influence of the different components of the impedance bridge (such as the power stage parasitic capacitance) on the CM noise attenuation performance can be evaluated. The modeling use the same parameters in the experiment. For simplification, only the CM inductor L_{cmac} and the auxiliary inductor L_r use measured impedance curve data since these Nanocrystalline core inductors have frequency-dependent and non-linear characteristics in the interested EMI frequency range. Impedance of other components shown in Fig. 5-21 are regarded to be ideal inductors or capacitors. The power stage capacitive coupling to ground are considered. The measured ac side parasitic capacitance is around 76 pF. Fig. 5-22 shows the calculated insertion gain curve. At the switching frequency point (280 kHz), the predicted ac CM noise attenuation with the impedance balancing circuit is 19 dB. From the insertion gain curve, above 1 MHz, the CM noise attenuation performance is limited, which also matches previous experiment results.

Then, to demonstrate the influence of power stage parasitic capacitance on CM noise attenuation, insertion gain curves with different ac side power stage parasitic capacitance and dc side power stage parasitic capacitance are calculated and plotted as shown in Fig. 5-23(a) and Fig. 5-23(b), respectively. From Fig. 5-23(a), the ac side CM noise attenuation performance of the impedance balancing circuit decreases when the ac side power stage parasitic capacitance increases. Specifically, at the 280 kHz switching frequency point, the CM noise attenuation is 21.3 dB, 18.5dB, and 16.2 dB when the ac side power stage parasitic capacitance is 50 pF, 100 pF and 150 pF, respectively. From Fig. 5-23(b), the ac side CM noise attenuation nearly does not change when the dc side power stage parasitic capacitance changes. The three insertion gain curves overlap with each other. All the results match the analysis presented above.

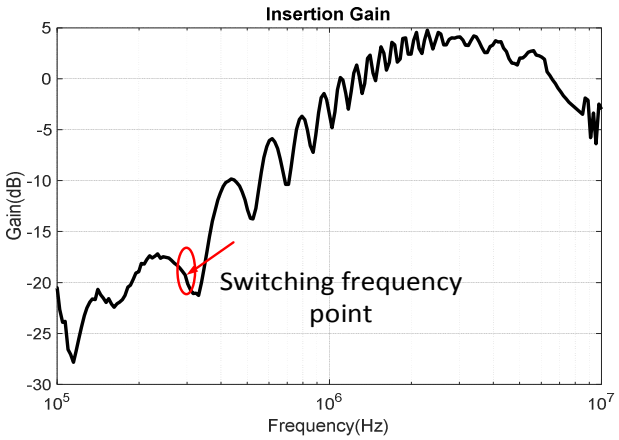
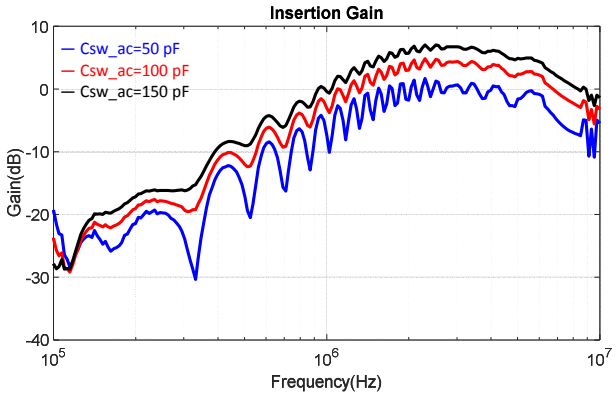
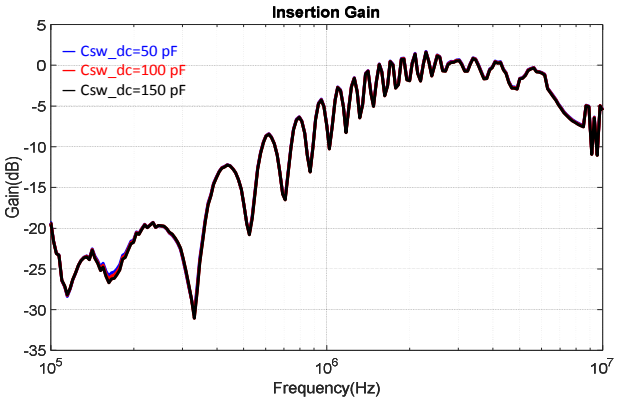


Fig. 5-22. Insertion gain curve.



(a)



(b)

Fig. 5-23. (a) Insertion gain curves at different ac side power stage parasitic capacitances. (b) Insertion gain curves at different dc side power stage parasitic capacitances.

5.3 Experimental Results and Analysis

A silicon carbide MOSFET based active NPC inverter is constructed for experimental verification of proposed method. In this case study, 3 kHz fundamental frequency and 280 kHz switching frequency are selected. The proposed impedance balancing circuit shown in Fig. 5-17 is applied. The inverter system conventional CM filter parameters are L_{cmac}=500 uH, L_{cmdc}=2.1 mH and C_{cmdc}=2 nF. Fig. 5-24 shows the inverter hardware platform and the inverter output voltage and current waveform.

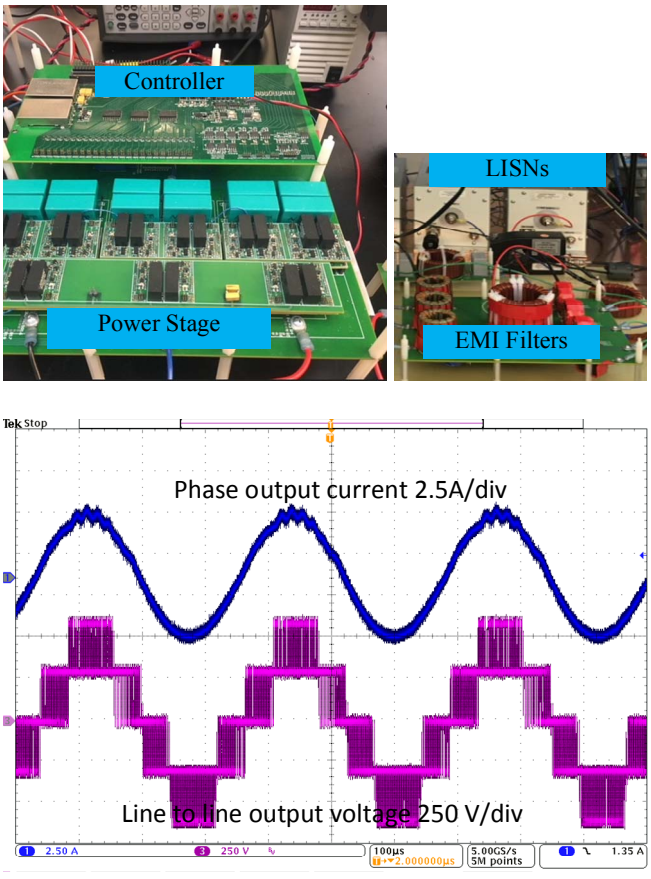
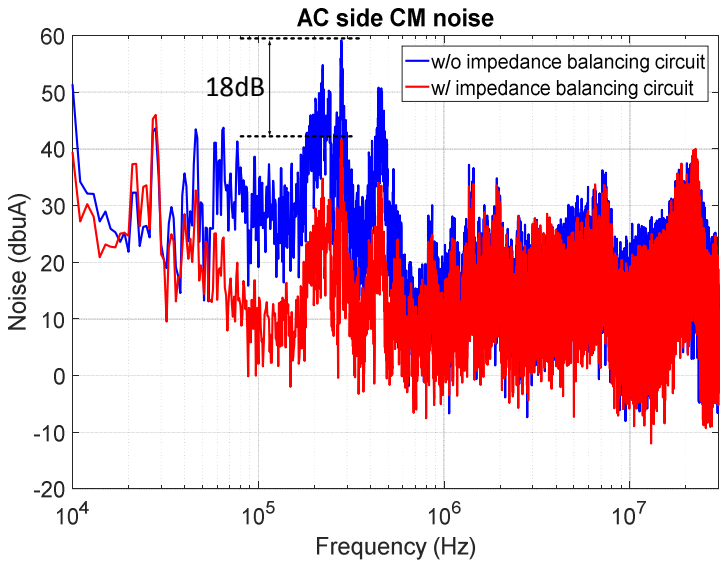


Fig. 5-24. Inverter platform and voltage/current waveforms.

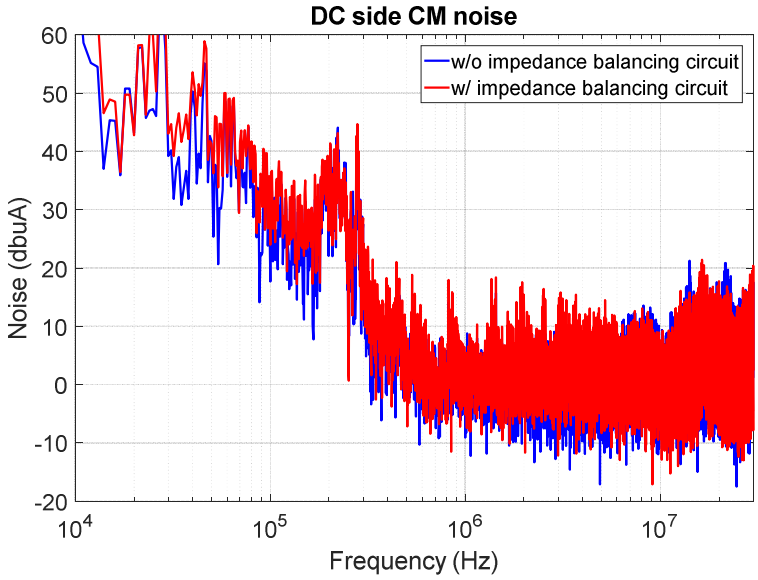
5.3.1 Impedance Balancing Circuit Design to Reduce Only AC side CM Noise

According to the analysis, (5-10) should be met for the ac motor side CM noise reduction. The impedance balancing circuit ratio is first selected as n=1 for the sake of principle verification. Then, the impedance balancing circuit parameters are determined as L_r=500 uH and C_{return}=4 nF (with the damping network parameters R_r=200 Ohm and C_r=4 nF). In this case, the ac side CM noise attenuation can be expected, and the dc side CM noise will not be decreased. The comparison experiments are conducted without the impedance balancing circuit (having only the conventional CM filterL_{cmac}, $L_{cmdc}$and C_{cmdc} as shown in Fig. 5-17) and with the impedance balancing circuit (having the conventional CM filter L_{cmac}, L_{cmdc}, C_{cmdc} and the added two impedance balancing circuit branches L_r and C_{return} as shown in Fig. 5-17).

The CM noise current test results are shown in Fig. 5-25. From Fig. 5-25(a), when the impedance balancing circuit is applied, 10 ~ 20 dB ac side CM noise attenuation has been achieved in the 150 kHz to 1 MHz frequency range, and around 18 dB attenuation is obtained at the switching frequency noise peak. In the lower frequency range from 10 kHz to 150 kHz, the impedance balancing circuit also helps to reduce CM noise. From Fig. 5-25(b), no CM noise attenuation can be observed in the dc side. These results match the theoretical analysis.



(a)



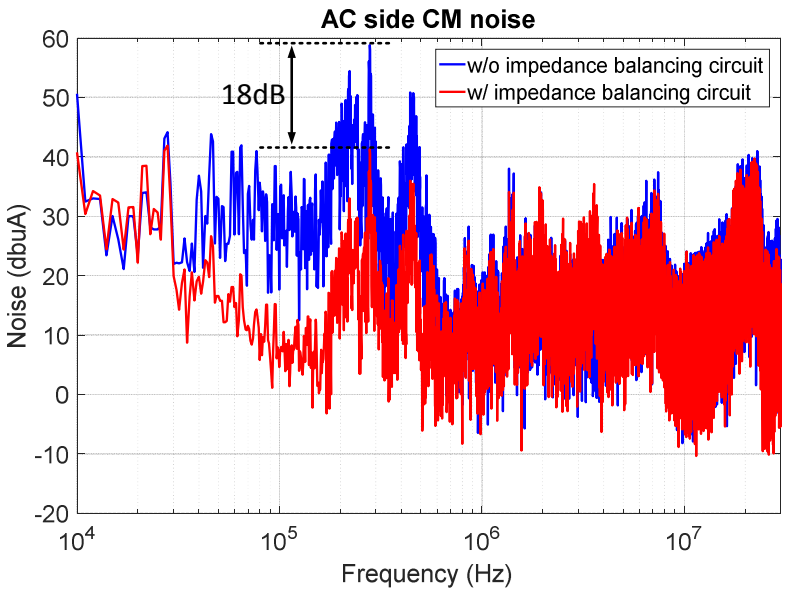
(b)

Fig. 5-25. CM EMI noise with and without the impedance balancing circuit at *n*=1, (a) ac side, (b) dc side.

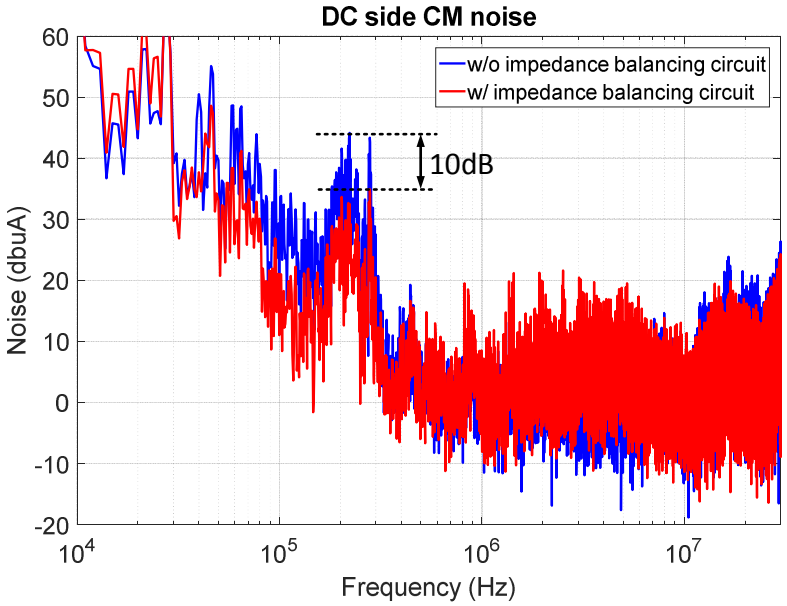
5.3.2 Impedance Balancing Circuit Design to Reduce both AC and DC Sides CM Noise

Both (5-10) and (5-13) should be met to reduce both the ac and dc sides CM noise. Therefore, the impedance balancing circuit is selected with n=4. Then, the impedance balancing circuit parameters are determined as L_r=2 mH and C_{return}=16 nF. The comparison experiments are conducted. Fig. 5-26(a) shows the ac side CM noise current spectrum. Similarly, as previous case where n=1, 10~20 dB noise attenuation has been achieved in the 150 kHz to 1 MHz frequency range, and around 18 dB attenuation is obtained at the switching frequency noise peak when the impedance balancing circuit is applied. Fig. 5-26(b) shows the dc side CM noise current spectrum. With the impedance balancing circuit, 5~15 dB noise attenuation has been achieved in the 150 kHz to 1 MHz frequency range, and around 10 dB attenuation is obtained at the switching frequency noise peak. These results match the theoretical analysis.

The impedance balancing circuit ratio n is further increased to be n=8 to demonstrate the influence of an increased ratio. Then, the impedance balancing circuit parameters are determined as L_r= 4 mH and C_{return}=32 nF. Fig. 5-27(a) shows that, at the switching frequency noise peak (280 kHz), 15 dB noise attenuation is obtained for ac side CM noise when the impedance balancing circuit is applied. Compared to the case where n=1 and n=4 (the ac side CM noise attenuation at the switching frequency peak is 18 dB for the two cases), the CM noise attenuation decreases slightly. This is because the ac side power stage parasitics begin to influence the performance of the impedance bridge when the impedance balancing circuit ratio n=8. However, the degradation is still very small at n=8. More performance degradation can be expected if the ratio n is further increased. Fig. 5-27(b) shows the dc side CM noise current spectrum, at the switching frequency noise peak, 14 dB attenuation has been achieved when the impedance balancing circuit is applied, which is larger than the case when n=4 (10 dB in this case). These results also match the analysis.

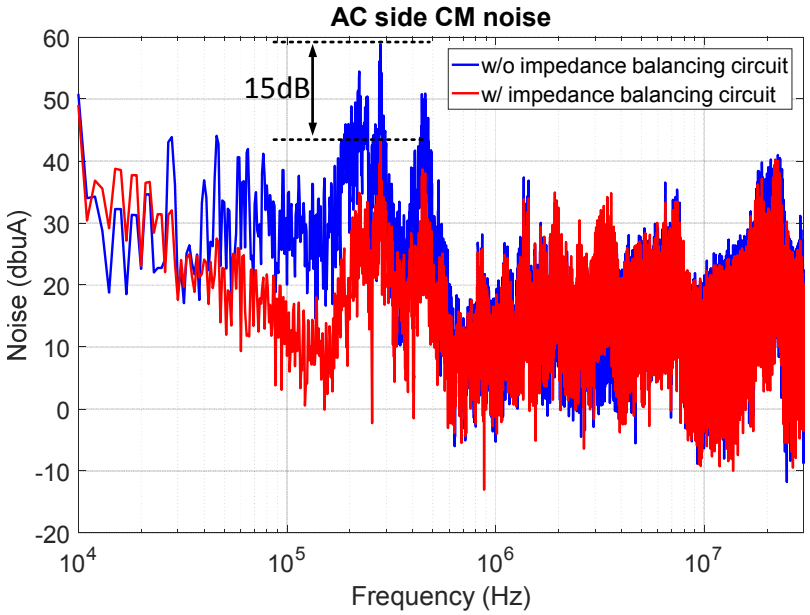


(a)

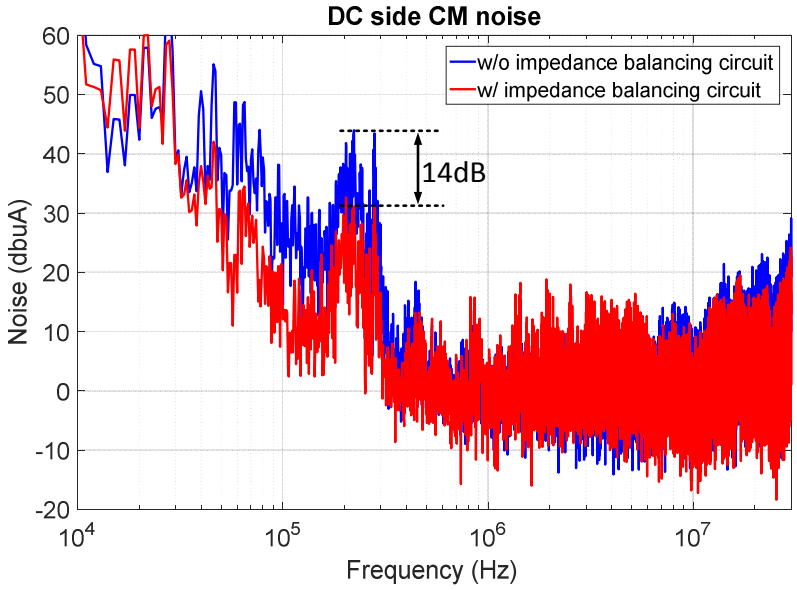


(b)

Fig. 5-26. CM EMI noise with and without the impedance balancing circuit at n=4, (a) ac side, (b) dc side.



(a)



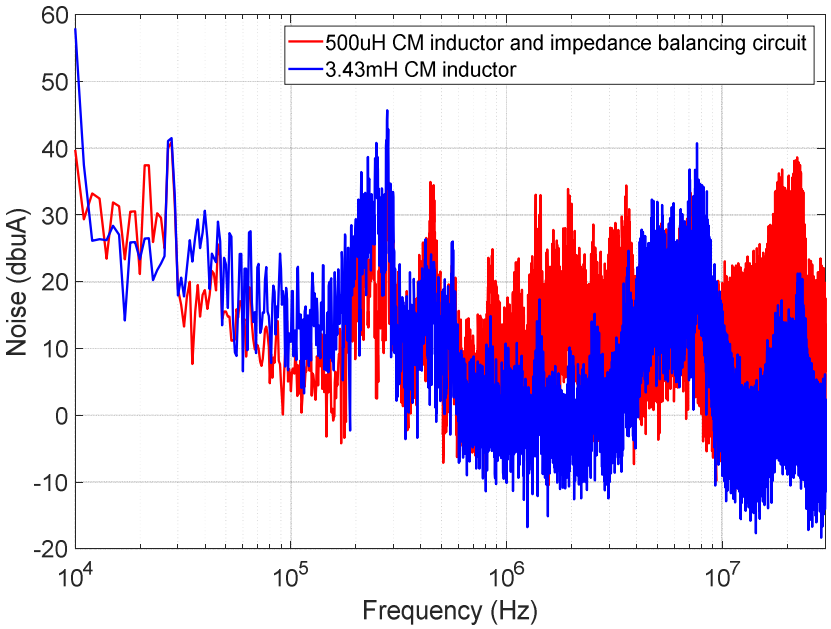
(b)

Fig. 5-27. CM EMI noise with and without the impedance balancing circuit at n=4, (a) ac side, (b) dc side.

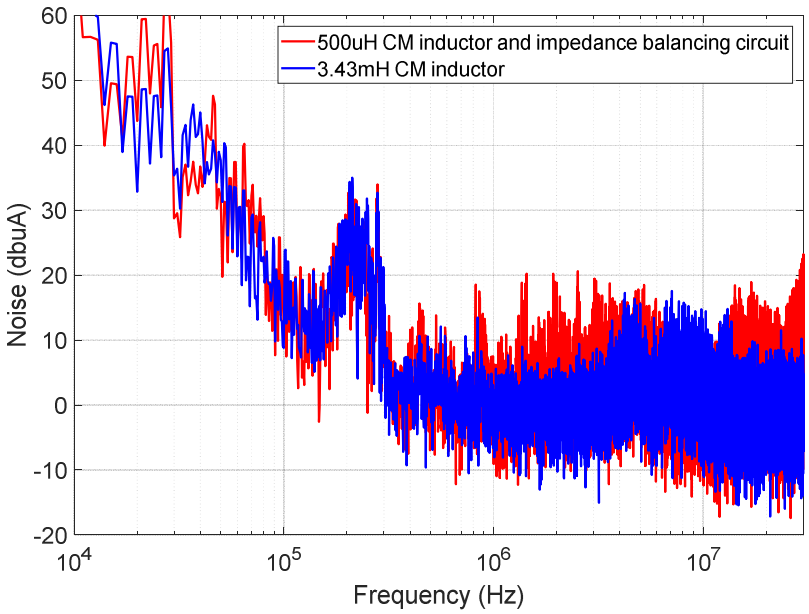
From Fig. 5-25, Fig. 5-26 and Fig. 5-27, it can be found that the ac side impedance balancing circuit only slightly alters the EMI noise level above 1 MHz. This is because in the MHz frequency range, the adverse effect of the power stage parasitic capacitances begins to influence balancing performance of the impedance bridge. Also, the parasitics of EMI filters in the impedance bridge, such as the equivalent parallel parasitic capacitance (EPC) of the CM inductor, cannot be neglected in the high frequency range. The impedance bridge is not balanced well and (5-10) is not met in the high frequency range. To improve the high frequency performance of the impedance balancing circuit, from physical design point of view, the power stage parasitic capacitance and passive filter parasitics need to be well controlled and reduced.

5.3.3 Comparison to the Conventional CM Filter

Experiment results show that the proposed impedance balancing circuit can effectively reduce both the dc and ac sides CM noise. This indicates that the required inductance of the conventional CM inductor can be reduced to get the same CM noise level. Compared to the design case n=4, to get the same ac and dc sides CM noise at the switching frequency noise peak without the impedance balancing circuit, the ac side CM inductance need to be increased to L_{cmac}=3.43 mH. Experiments are conducted to verify this.



(a)



(b)

Fig. 5-28. CM EMI noise comparison: with 500 uH inductor and impedance balancing circuit, and with the increased 3.43 mH CM inductor, (a) ac side. (b) dc side.

Fig. 5-28(a) shows the ac side CM noise comparison with the 500 uH inductor and the impedance balancing circuit, and with the increased 3.43 mH CM inductor. Specifically, at the 280 kHz switching frequency point, the noise level with the 500 uH CM inductor and the impedance balancing circuit is 41 dB, and the noise level with the 3.43 mH CM inductor is around 45 dB. Fig. 5-28(b) shows the dc side CM noise comparison. At switching frequency point, the CM noise current of the case with 500 uH CM inductor and the impedance balancing circuit is almost the same as the CM noise current of the case with 3.43 mH CM inductor. In conclusion, to achieve the same CM noise level, the ac side CM inductance can be reduced by approximately a factor of 7 with the proposed impedance balancing circuit.

The inductor loss of the two cases are estimated and summarized in Fig. 5-29. As the impedance balancing circuits are not in the power current conduction path and conduct only the CM noise current, their losses are very small compared to the conventional CM filters. The power loss of the impedance balancing circuit auxiliary inductor is 7.8% of the 500 *uH* ac side CM inductor. Also, the power loss of the 500 uH inductor plus the auxiliary inductor is 62.5% of the loss of the 3.43 mH inductor. Note that in this case study, the power current is relatively small, and the core loss takes a large portion of the total CM inductor loss. If the converter power current increases, the copper loss and total loss of the ac side CM inductor increases, but the loss of the auxiliary inductor will not change much as it only conducts CM noise current. Then, the loss ratio between the auxiliary inductor and the conventional CM inductor will be even smaller. Hence, the impedance balancing circuit is more effective and promising for high power applications.

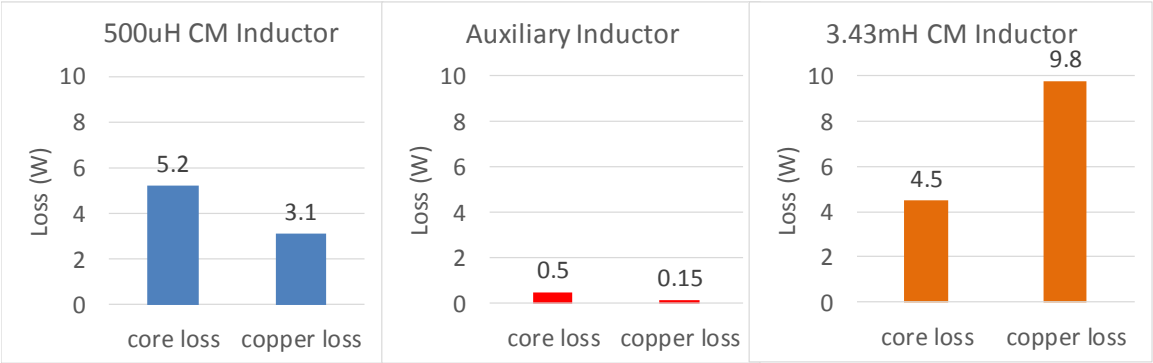


Fig. 5-29. Loss of the 500 uH CM inductor, auxiliary inductor and the 3.43 mH inductor.

5.4 Conclusion

This chapter investigates inverter and filter topology to reduce CM noise for three-level inverter.

First, the fourth-leg strategy is applied to the three-level inverter fed motor drive for CM noise reduction. Unlike the case in two-level inverters, the nearest three vectors can be maintained to synthesize the reference while zero CMV can be achieved at the same time. Alternative fourth-leg filter structures are investigated. Experiments conducted on a three-level NPC inverter show that with the fourth-leg and presented modulation scheme applied, the CM noise has been significantly reduced, and ~25 dB attenuation can be observed at the first noise peak in the EMI frequency range.

Second, an impedance balancing circuit is proposed for dc-fed motor drive where both the dc source side and ac motor side need to meet EMI standards and require EMI filters. The CM noise reduction performance of the proposed method does not depend on motor and cable models. The topology, design criteria, and performance evaluation model are developed and illustrated. Experiment results shows that both the ac and dc side can achieve 10~20 dB CM noise attenuation in the 150 kHz to 1 MHz frequency range. Specifically, at the switching frequency noise peak

point, 18 dB ac side attenuation and 10 dB dc side attenuation have been achieved when impedance balancing circuit ratio is selected as n=4, and 16 dB ac side attenuation and 14 dB dc side attenuation have been achieved when n=8 is selected. The required CM inductance of the conventional ac side CM inductor significantly reduced from 3.43 mH to 500 uH in the experiment.

6. CM Inductor Modeling, Analysis, and Design Optimization for Three-Level Inverter

To reduce the required EMI filter, one approach is to reduce the EMI noise in the power inverter system as discussed in last chapter, another approach is EMI filter design optimization. CM inductor is one of the dominant weight contributors of EMI filter. Core saturation is usually the main limitation for inductor size and weight reduction in high power low switching frequency applications. Overdesign of the inductor core is a safe way to prevent saturation, but it also decrease the inverter system power density. This chapter will focus on the CM flux density modeling, analysis and CM inductor design optimization.

6.1 Spectrum Concept for CM Inductor Design Optimization

6.1.1 Spectrum Concept Analysis

For a CM inductor, when the inductance is fixed, the CM volt-second or CM current determines CM flux density. Instead of time domain CM current, frequency domain spectrum concept is introduced to CM current analysis to provide an insightful view. A typical CM inductor CM current spectrum is shown in Fig. 6-1 [226]. The components in the current spectrum can be classified into three categories: 1) switching frequency related components; 2) impedance resonance frequency related components; and 3) modulation frequency related components. To reduce the CM flux density and optimize CM inductor design, each component in the inductor CM current spectrum needs to be reduced.

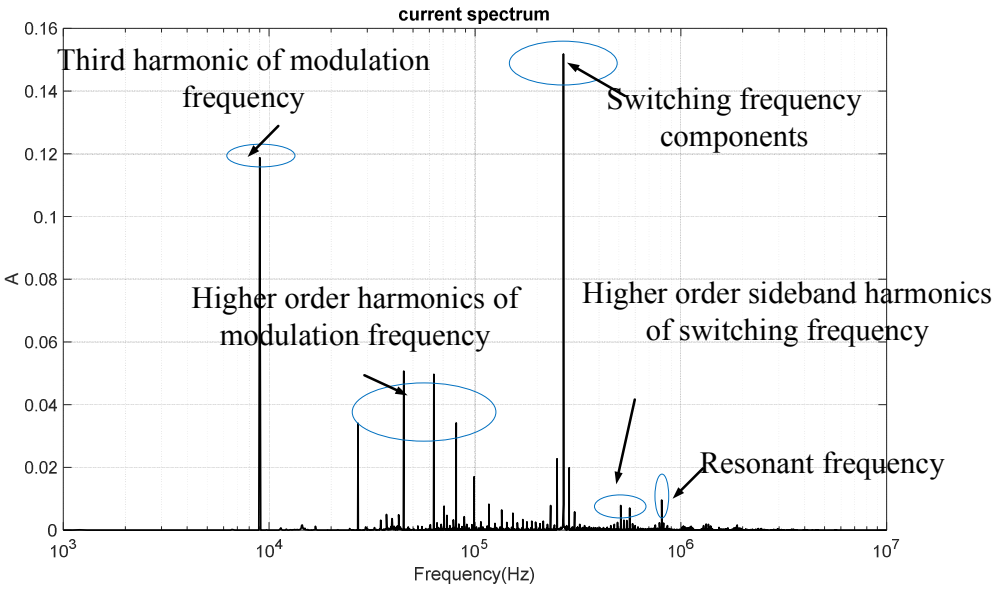


Fig. 6-1. CM inductor CM current spectrum.

The switching frequency related current components refer to switching frequency component and its sideband harmonics. The magnitudes of these components are determined by switching frequency related CM voltage and CM noise propagation path impedance. The CM noise propagation path impedance will be discussed later. To reduce switching frequency related CM voltage, PWM schemes which reduce CM voltage amplitude can be applied such as the active zero state PWM (AZSPWM) and near state PWM (NSPWM) for two-level inverter, and common-mode reduction (CMR) scheme for three-level inverter. Another method is to use variable switching frequency, which spreads the centralized noise peak around the switching frequency and its multiples to a wider frequency range and thus reduces the CM voltage peak.

The impedance resonance frequency related current components are introduced by LC filter resonance, LC filter parasitic resonance, and load resonance. If the impedance resonance frequencies are close to the peak points of the CM voltage spectrum, the CM current will be

amplified due to the relatively low impedance at these frequency points. LC filter corner frequency is determined by the required EMI noise attenuation obtained from the comparison of bare noise and EMI standards. If the designed LC filter corner frequency f_c is higher than switching frequency f_{sw}, which usually occurs when f_{sw} multiples is below the EMI frequency range and the switching frequency determines the LC filter corner frequency, then it is possible that the current will be amplified at certain multiples of f_{sw}. For example, as shown in Fig. 6-2, the LC filter corner frequency f_c is determined by the noise peak at switching frequency multiple $n2 \cdot f_{sw}$, but another switching frequency multiple $n1 \cdot f_{sw}$ is very close to the resonance point. Then CM current can be amplified and even cause core saturation. Hence, LC filter damping is necessary to avoid overdesign of the inductor. Load resonance can also cause large CM current and flux density. This excess CM current can be reflected in the EMI current bare noise spectrum. In this case, the LC filter corner frequency may be determined by the noise peak at resonance frequency instead of switching frequency or its multiples. This is not desired for an optimal design. It is better to first damp this load resonance and then measure EMI bare noise and then determine the LC filter corner frequency. LC filter parasitic resonance involves filter parasitic or the coupling effect between multi-stage filters. In this case, it is suggested to check the EMI noise spectrum peak points after the EMI filter is added. If certain noise peaks are identified to be caused by impedance resonance, then damping networks can be considered. A Rd-Cd damping network can be employed for impedance resonance.

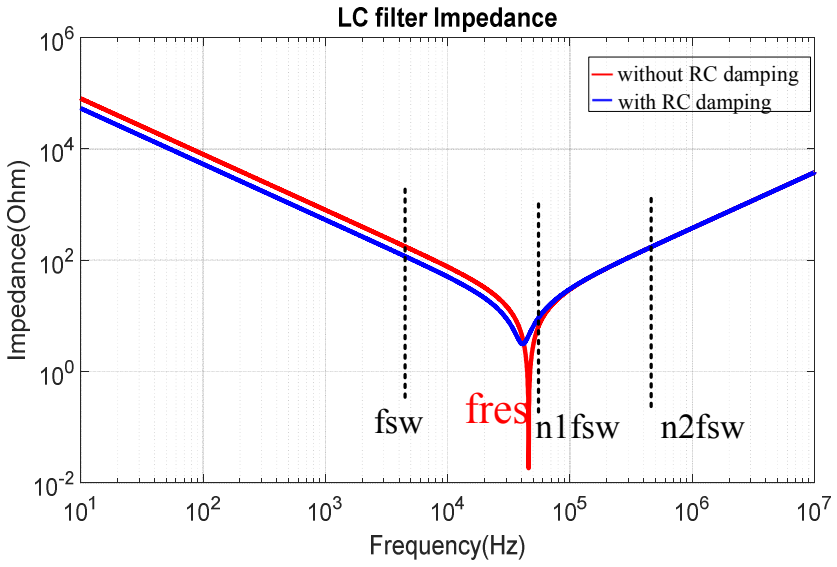
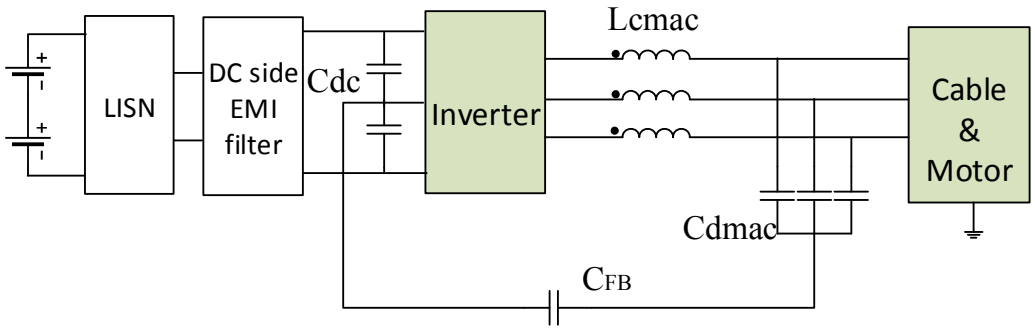


Fig. 6-2. LC filter corner frequency position and damping.

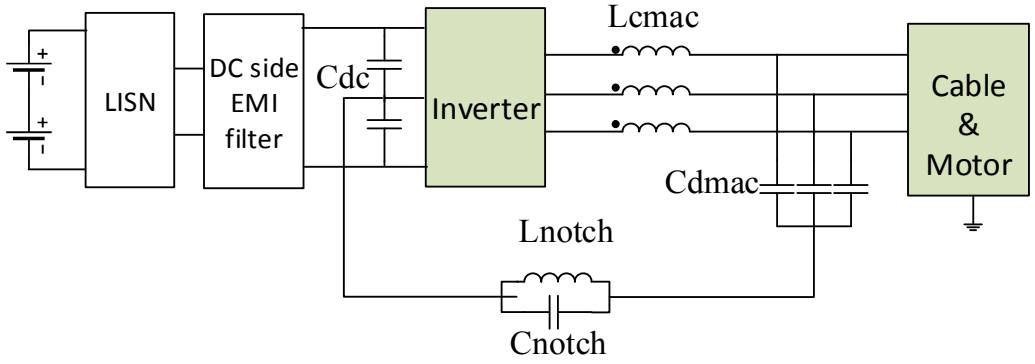
The modulation frequency related components refer to the third or higher order harmonics of the fundamental component. SVM method introduces low frequency modulation frequency related CM voltage and can generate large CM flux density and even cause core saturation. As shown in Fig. 6-1, the 3rd and higher order of fundamental frequency harmonics exist in the CM current spectrum when the central aligned continuous space vector modulation is used.

The connecting ac and dc side midpoint EMI filter topology is popular in three phase converters such as rectifiers and inverters. Fig. 6-3(a) shows a connecting ac and dc midpoint with a capacitor structure in dc-fed motor drives. The capacitor C_{FB} provides a low impedance for high frequency CM noise and limits the CM noise within the converter, thus suppressing both ac and dc side CM noise. However, C_{FB} also provides a path for modulation frequency related components. A large capacitor C_{FB} will lead to large modulation frequency related CM current, which may cause CM inductor core saturation. To keep the EMI noise reduction performance of capacitor C_{FB} and suppress the modulation frequency related third harmonic, a notch filter structure is proposed as

shown in Fig. 6-3(b). The resonance frequency of the notch filter is designed at the third harmonic of the modulation frequency. Since the notch filter only provides a high impedance around its resonance point, high frequency EMI noise bypassed by C_{notch} will not be influenced. Also, the notch inductor L_{notch} is not in the main current conduction path and mainly conducts the third harmonic components. It is significantly lighter than conventional EMI inductors, especially in high power conversion systems.



(a)



(b)

Fig. 6-3. (a) Connecting ac and dc midpoint CM filter structure in dc-fed motor drives. (b) Proposed notch filter structure.

Considering this analysis, for CM filter design, first the EMI bare noise should be investigated. The noise peaks which can probably determine CM filter corner frequency need to be analyzed and categorized. If the switching frequency related noise peak is very large, then a modulation method which reduces CM voltage magnitude can be considered. If system impedance resonance frequency related noise peak is dominant, then a damping network can be employed. Then, the CM filter is designed based on the updated noise attenuation requirement. After the CM filter is employed, system EMI noise and CM inductor current spectrum should be checked again to see if the CM filter introduces new resonances and if impedance resonance components and modulation frequency related components cause large CM flux density in the inductor core. If these components are large, then further damping and the proposed notch filter structure can be considered.

6.1.2 Experimental Verification

A SiC device based three-phase three-level active neutral point clamped inverter is developed to verify the proposed concept and method. The switching frequency is 280 kHz and inverter ac output fundamental frequency is 3 kHz.

To reduce the switching frequency related CM voltage, CMR modulation scheme is employed. Fig. 6-4 shows the CM voltage spectrum comparison. Compared to conventional SVPWM, the CM voltage peak at switching frequency point reduced by a factor of 2 using CMR scheme, thus switching frequency related CM flux density will be reduced.

To reduce impedance resonance frequency related CM flux density components, the filter design concept and Rd-Cd damping networks discussed above are employed. Fig. 6-5 shows the CM noise current spectrum versus DO-160 EMI standard limit in aircraft application. All LC filters

and load impedance resonance points are identified and well damped as shown in Fig. 6-5. The detailed filter and damping network parameters are not presented here for simplification. With this design, CM noise current and impedance resonance related CM flux density are not amplified and are quite small. The main LC filter parameters are designed based on the switching frequency noise peak attenuation requirement instead of the resonance peak to optimize inductor design.

To reduce modulation frequency related components, the proposed notch filter structure in Fig. 6-3(b) is employed. SVM scheme is used to improve dc voltage utilization, the main modulation frequency related component is the third harmonic, which is 9 kHz in the experiment.

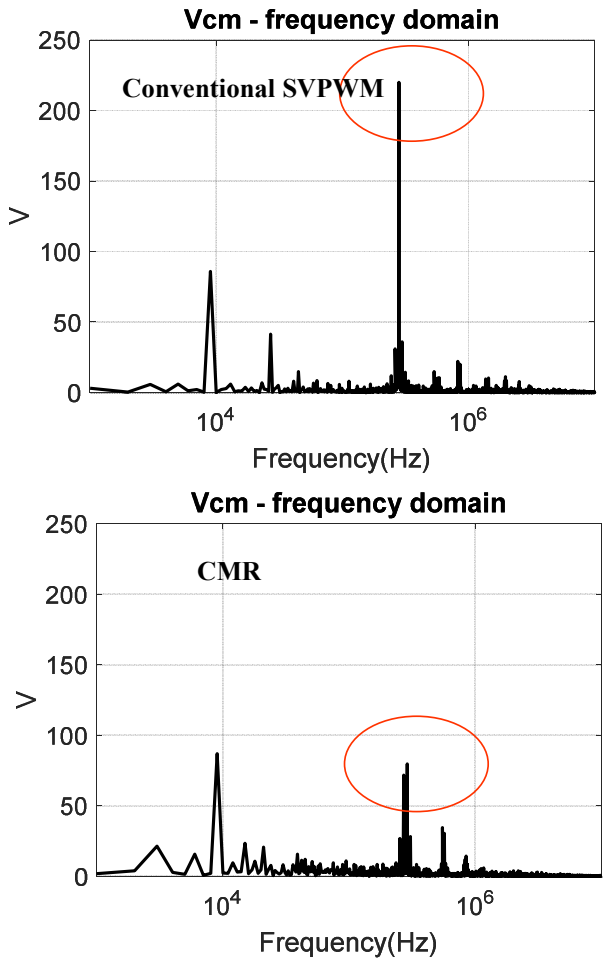


Fig. 6-4. CM voltage spectrum comparison: conventional SVPWM scheme versus CMR scheme.

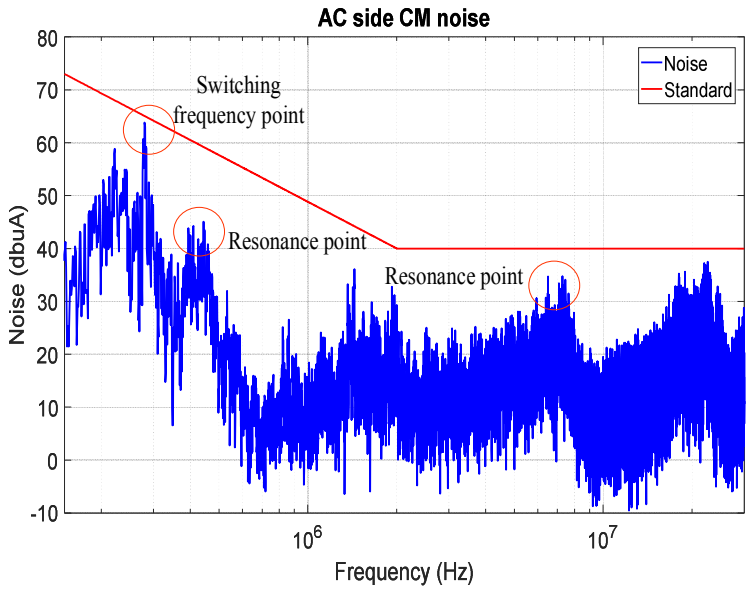


Fig. 6-5. EMI CM noise spectrum with impedance resonances well damped.

Fig. 6-6 shows the comparison experiment results with only capacitor C_{FB} and with a notch filter (L_{notch} and C_{notch}). The capacitor values of the two cases are set to be 100 nF. To suppress the third harmonic, a notch inductor is determined as L_{notch}=3.3 mH. Fig. 6-6 shows the time domain waveform and related CM current spectrum using only C_{FB} . Large CM current distortion can be observed and the current spike exceeds 2.6 A when only C_{FB} is used. This is because CM inductor is locally saturated due to large CM current while the third harmonic is the dominant component causing core saturation according to the current spectrum in Fig. 6-6. The time domain waveform and related CM current spectrum using a notch filter is shown in Fig. 6-7. CM current is significantly reduced and no current spike is observed. CM inductor will not be saturated. From the CM current spectrum, the 9 kHz third harmonic current is reduced by 3.75 times compared to the case using a capacitor.

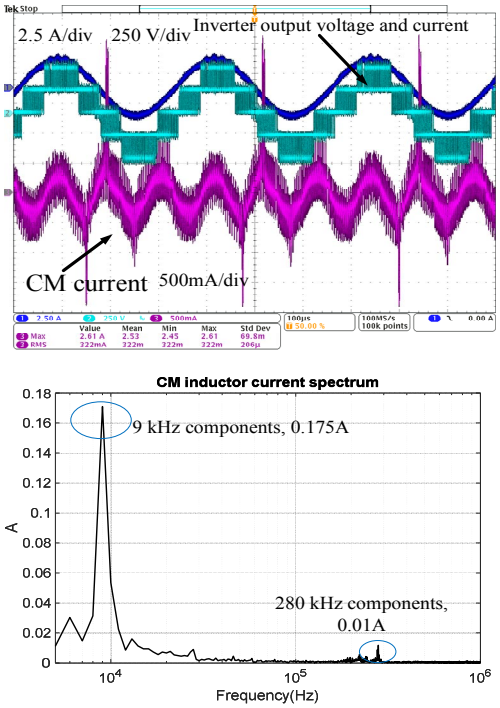


Fig. 6-6. Time domain waveform and related CM inductor CM current spectrum with C_{FB}.

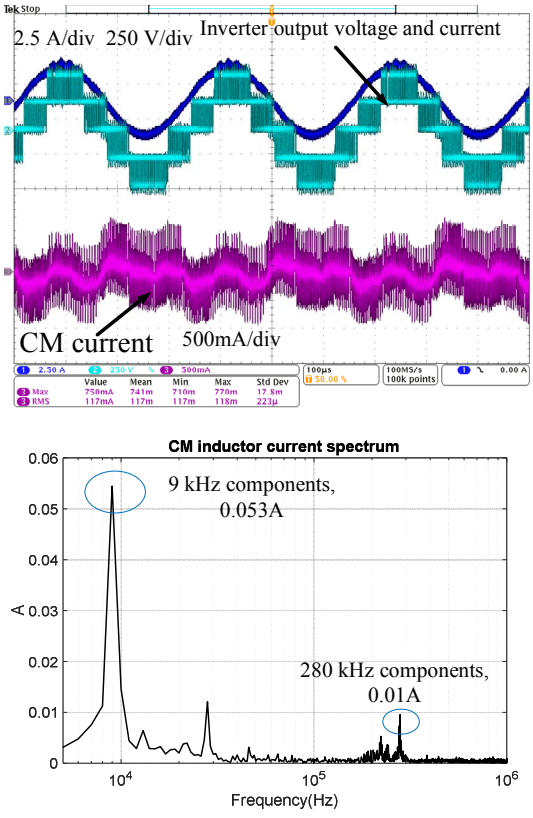


Fig. 6-7. Time domain waveform and related CM inductor CM current spectrum with notch filter.

6.2 CM Inductor Flux Density Modeling and Analysis

A typical three-level inverter with dc side one stage LC CM filter system is shown in Fig. 6-8. The comprehensive CM inductor flux density modeling and analysis is conducted in this section.

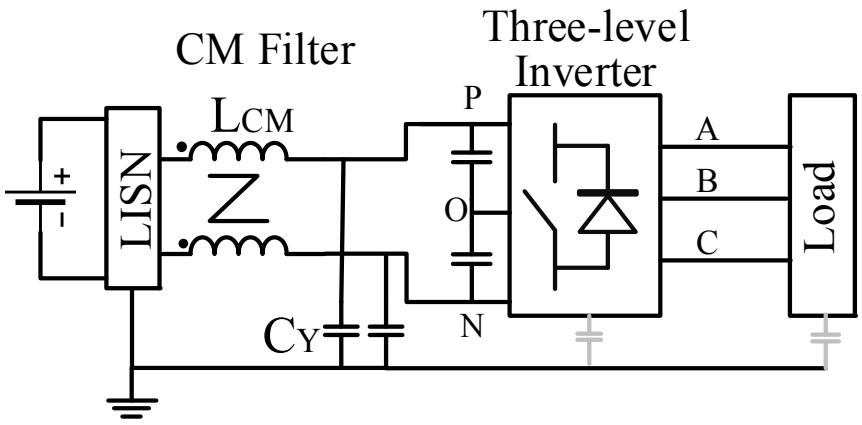


Fig. 6-8. Three-level inverter with dc side EMI filter system.

6.2.1 Basic Model

DM current generates magnetic flux in the CM inductor core. Most of this DM current generated flux of different phases cancel with each other in a balanced system. However, part of the DM flux of different phases which are not coupled will not be cancelled which is known as the leakage flux. The CM voltage of a converter generates CM current through the impedance loop formed by CM filter and system parasitic capacitance to ground. This CM current also generates flux in the CM inductor magnetic core. Hence, the flux density in a CM inductor core can be considered as two parts as shown in Fig. 6-9.

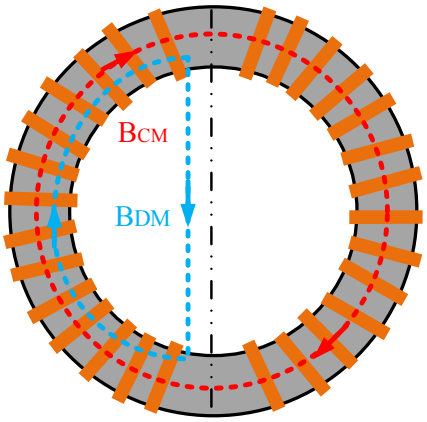


Fig. 6-9. Flux density in a CM inductor.

The total flux density is

$$B = B_{DM} + B_{CM} \tag{6-1}$$

where B_{DM} is the DM current generated flux density and termed as DM flux density, B_{CM} is the CM current generated flux density and termed as CM flux density. The DM flux density can be calculated as

$$B_{DM} = \frac{\mu_0 \mu_{DM} N I_{DM}}{L_{eff}} \tag{6-2}$$

where μ_o is the free space permeability, N is the number of turns, μ_{DM} is the equivalent leakage flux path relative permeability and L_{eff} is the equivalent leakage flux mean path length, respectively. Both μ_{DM} and L_{eff} are the function of the core geometry. When the core is selected, μ_{DM} and L_{eff} can be determined. DM current is represented as I_{DM}.

For dc side CM inductor, the DM current mainly contains dc component which is the power current delivered to load. Although switching frequency ripple current may exists, the contribution of ripple current to the DM flux density is very small and can be neglected if THD is small. The DM current can be denoted as

$$I_{DM} = \frac{P}{\eta V_{dc}} \tag{6-3}$$

where P represents load power and η denotes inverter system efficiency. Therefore, all parameters in (6-2) can be determined, and the DM flux density is modeled analytically.

The CM flux density can be calculated as

$$B_{CM} = \frac{\mu_0 \mu_r N I_{cm}}{L_e} \tag{6-4}$$

where μ_r is the relative permeability, N is the number of turns, and L_e is the mean path length. CM current is represented as I_{CM}.

For dc side CM inductor, the CM current mainly contains switching frequency related harmonics. To calculate CM current, both the CM voltage and CM noise propagation path impedance need to be modeled. The CM voltage is a variable duty cycle PWM voltage and its harmonics can be analyzed in frequency domain using double Fourier integral analysis. The CM noise propagation path impedance including CM inductor has frequency-dependent characteristic and need to be modeled in frequency domain. The frequency domain CM voltage and CM impedance are expressed as $V_{CM}(f)$ and $Z_{CM}(f)$, and the frequency domain CM current is calculated as

$$I_{CM}(f) = \frac{V_{CM}(f)}{Z_{CM}(f)} \tag{6-5}$$

Then, the time domain CM current can be derived using inverse FFT as

$$I_{CM}(t) = iFFT\big(I_{CM}(f)\big) \tag{6-6}$$

For the three-level inverter system shown in Fig. 6-8, the CM equivalent circuit is illustrated as Fig. 6-10.

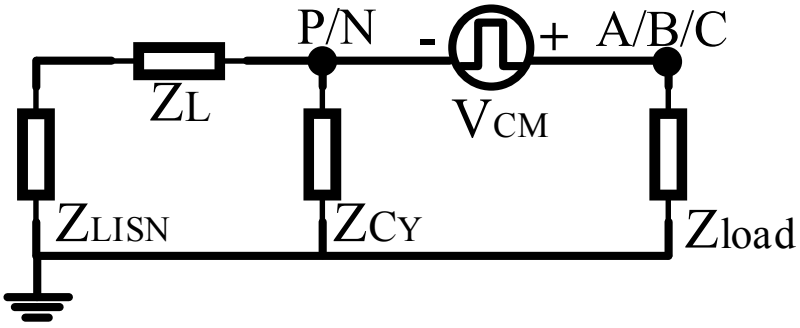


Fig. 6-10. Simplified CM equivalent circuit.

The CM voltage is

$$V_{CM} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \tag{6-7}$$

where V_{AO}, V_{BO}, V_{CO} are three phase voltages.

The spectrum of pulse width modulated phase leg voltage can be expressed as (6-8), and the harmonic coefficient is calculated as (6-9).

$$f(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(ny) + B_{0n}\sin(ny)] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} [A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)] \tag{6-8}$$

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{y_s}^{y_e}\int_{x_r}^{x_f} f(x,y)e^{j(mx+ny)}dxdy\,, x = \omega_c t, y = \omega_0 t \tag{6-9}$$

where $f(x,y)$ is the output voltage. *m* and *n* are carrier and baseband integer indices, respectively. Carrier and fundamental angular frequency are represented by ω_c and ω_0, respectively.

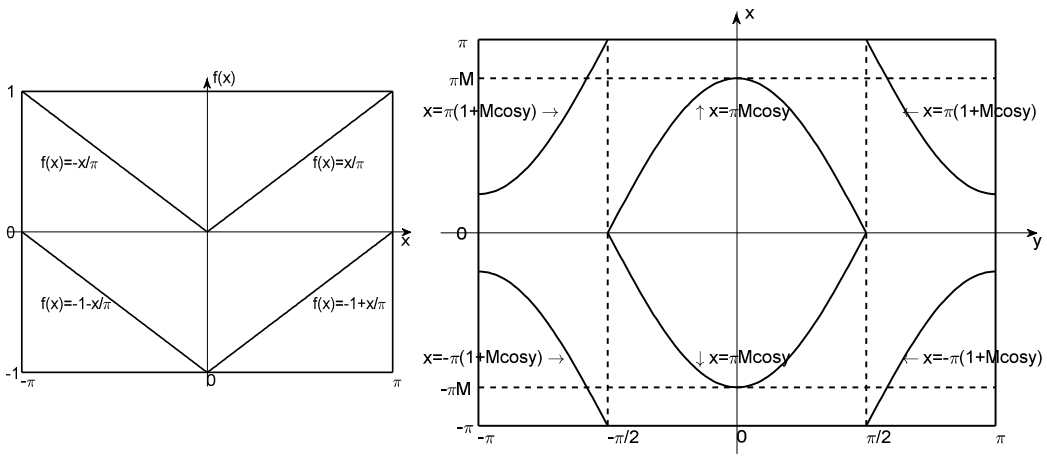
The phase voltage is impacted by the modulation method. In this study, the basic three-level phase disposition PWM (PDPWM) method is used as example to conduct the modeling and

analysis.

Fig. 6-11(a) shows the three-level PDPWM carrier waveform, and the unit cell contour plot is shown in Fig. 6-11(b) when the sinusoidal reference is $f(y) = Mcosy$. Then the double Fourier integral limits for calculating the harmonic coefficient of (6-8) is summarized in Table 6-1.

As the phase voltage harmonic is calculated, the CM voltage can be derived as

$$V_{CM} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} = \frac{1}{3}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} C_{mn}\cos(mx + ny)\left(1 + 2\cos\left(n\frac{2\pi}{3}\right)\right) \qquad (6-10)$$



(a) (b)

Fig. 6-11. (a) Three-level PDPWM carrier waveform, (b) the unit cell contour plot.

Table 6-1. Double Fourier Integral Limits of Basic PDPWM

y_s	y_e	x_r	x_f	$f(x,y)$
$-\frac{\pi}{2}$	$\frac{\pi}{2}$	$-\pi Mcosy$	$\pi Mcosy$	$\frac{V_{dc}}{2}$
$-\pi$	$-\frac{\pi}{2}$	$-\pi$	$-\pi(1+Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+Mcosy)$	π	
$\frac{\pi}{2}$	π	$-\pi$	$-\pi(1+Mcosy)$	$-\frac{V_{dc}}{2}$
		π	$\pi(1+Mcosy)$	

In Fig. 6-10, Z_{LISN} represents the LISN CM impedance defined in EMI standards. Z_L and Z_{CY} are the CM inductor and CM capacitor impedance, respectively. Z_{load} denotes the load CM impedance. RL load is used. A capacitor connecting three phase load neutral point and ground is added which represents the parasitic capacitance in motor drive system. The power device stray capacitance is ignored here as the stray capacitance is usually in the picofarad range and only impact the very high frequency EMI noise.

Thus, the CM loop impedance is calculated as

$$Z_{loop} = Z_{load} + Z_{CY}||(Z_{LISN} + Z_L) \quad (6-11)$$

The CM impedance seen by the CM inductor is the transfer function from CM voltage to CM current flowing through the CM inductor, which can be calculated as

$$Z_{CM} = Z_{loop}(1 + \frac{Z_{LISN} + Z_L}{Z_{CY}}) \quad (6-12)$$

As CM voltage V_{CM} and CM impedance Z_{CM} are derived in frequency domain, with (6-5) and (6-6), CM current can be calculated. Thus, all parameters in (6-4) can be determined, and the CM flux density is modeled analytically. The total flux density can then be modeled.

With the developed flux density calculation model, the impact of modulation index, dead time, NP voltage variation and loop impedance on the CM inductor maximum flux density are comprehensively investigated in next sections. The modulation index, dead time, and NP voltage variation impact the CM voltage and thus impact CM flux density. The CM inductor inductance impact the loop impedance and thus impact CM flux density. Case studies are conducted with the inverter system main parameters listed in Table 6-2.

Table 6-2. Inverter System Main Parameters

DC voltage	600 V
Fundamental frequency	400 Hz
Carrier frequency	60 kHz
Load	L=320 uH and R=10 Ohm for each phase, parasitic capacitance Cg=10 nF
CM inductor	nanocrystalline core (T60006-L2040-W424) and number of turns N= 9 for each phase
CM capacitor	4.7 nF for each phase

6.2.2 Impact of Modulation Index

With developed model, the maximum CM flux density, DM flux density and total flux density of the CM inductor at different modulation indexes are calculated and summarized in Fig. 6-12. From Fig. 6-12, for three-level inverter, the maximum flux density shows a non-monotonous relationship with modulation index. This is because the maximum CM flux density has a non-monotonous relationship with modulation index and CM flux density dominates the total flux density characteristic. The maximum flux density does not occur at full load (modulation index is 1) but at a certain operation point where the modulation index is around 0.7.

The calculation is based on PDPWM but the conclusion is also true if other modulations are used. Fig. 6-13 shows the results when continuous nearest three space vector (NTSV) modulation – for which the reference can be considered as a sinusoidal plus third order harmonics - is applied. Similar trend can be observed. The maximum CM flux density occurs at a certain operation point where modulation index is around 0.6 and the value is nearly twice the value of full load point.

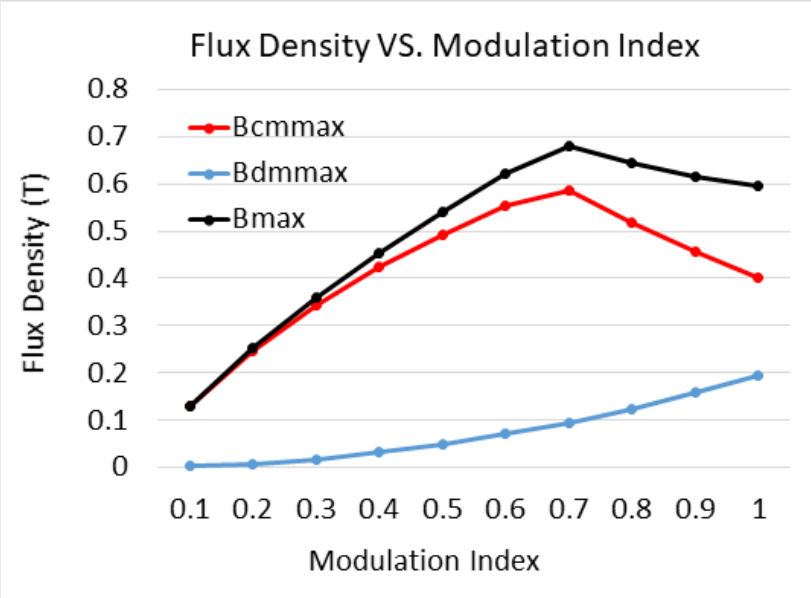


Fig. 6-12. CM inductor flux density versus modulation index.

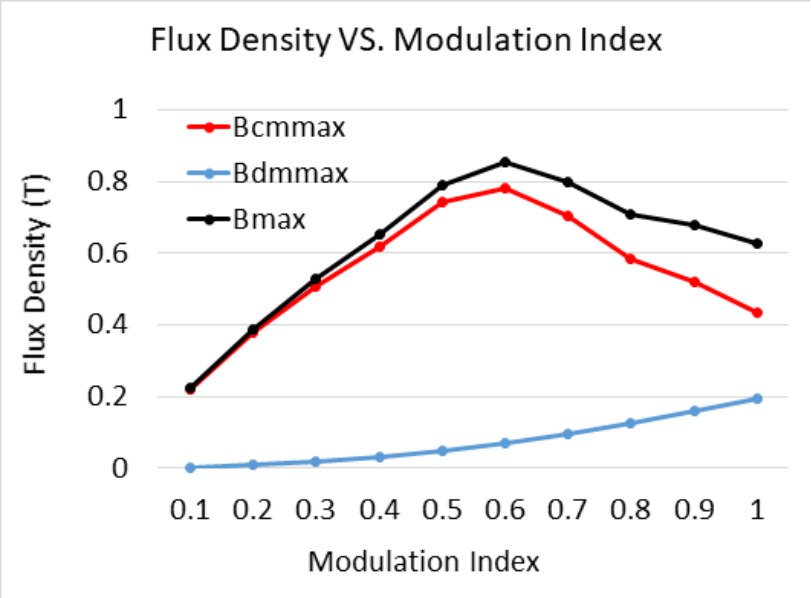


Fig. 6-13. CM inductor flux density with NTSV modulation.

For three-level inverter in motor drive application, the fundamental frequency is variable. Consider the motor with fun load, the torque varies with speed squared and the power varies with speed cubed. Assuming v/f control is applied, and the fundamental frequency varies from 100 Hz to 1 kHz when the modulation index varies from 0.1 to 1. Let the output current to be the same as the RL load case for full load operation point. The flux density at different modulation index is calculated and summarized as Fig. 6-14. Compared to the RL load case with fixed fundamental frequency case, the fundamental frequency variation in motor drive application impacts the switching frequency sideband harmonics of CM voltage and thus impacts the CM inductor flux density. However, similar trend can be observed in Fig. 6-15. The maximum occurs at a certain operation point instead of full load.

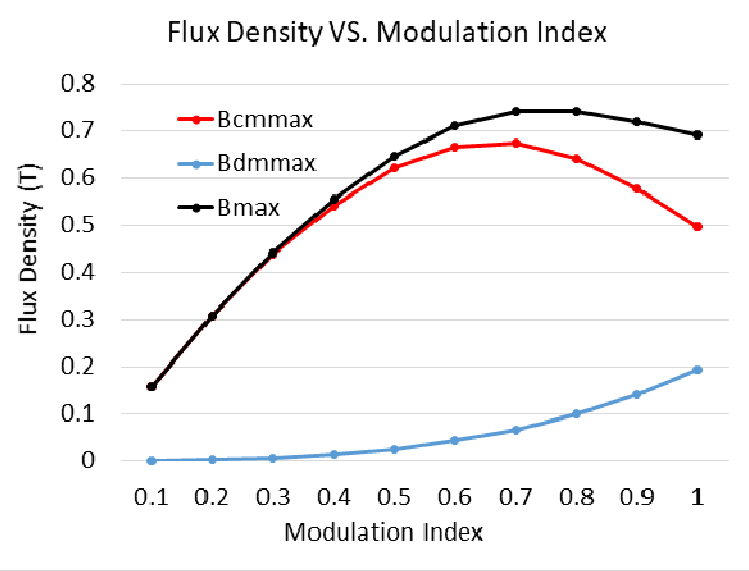


Fig. 6-14. CM inductor flux density versus modulation index for motor with fun load.

6.2.3 Impact of Dead Time

Dead time is implemented in a phase leg to avoid shoot-through failure in real applications. During dead time period, the output voltage is determined by the output current direction of the corresponding phase leg. Thus, the output voltage, the CM voltage, and the CM flux density of the CM inductor will all be impacted by dead time.

For a classical edge delay based dead time generation, the rising edge of each PWM signal is delayed for a certain time t_d. For a three-level inverter, considering the possible voltage and current polarities, the phase output voltage with dead time are illustrated as Fig. 6-15. Thus, a term $2\pi\frac{t_d}{T_s}$ needs to be added to the inner integral limits of rising or falling edge based on voltage and current polarities when calculating phase voltage harmonics.

For unit power factor case, the double Fourier integral limits for calculating phase voltage harmonic coefficient is listed in Table 6-3. Then, the CM voltage and CM flux density can be calculated. The maximum CM flux density for several typical dead time (2%, 5%, and 10% of the switching period) are calculated and summarized in Fig. 6-16.

From Fig. 6-16, the impact of dead time on maximum CM flux density highly depends on modulation index. When modulation index is high, larger dead time results in higher maximum flux density. When modulation index is low, larger dead time leads to lower maximum flux density. This can be understood by investigating the dead time impact on CM voltage.

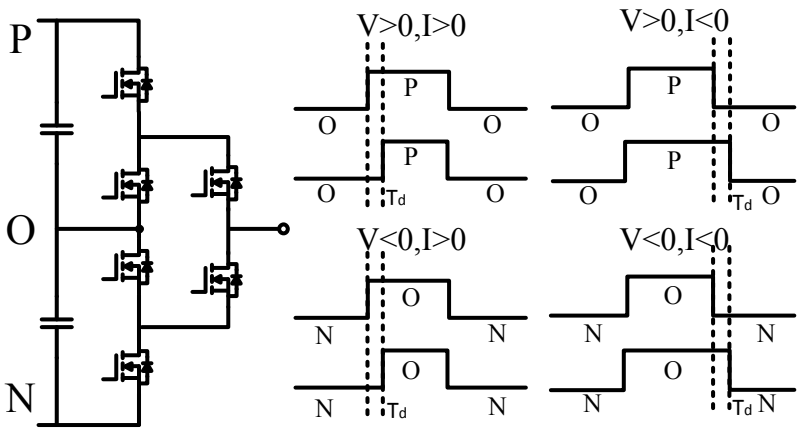


Fig. 6-15. Phase output voltage of a three-level inverter considering dead time.

Table 6-3. Double Fourier Integral Limits of Basic PDPWM Considering Dead Time

y_s	y_e	x_r	x_f	$f(x,y)$
$-\frac{\pi}{2}$	$\frac{\pi}{2}$	$-\pi Mcosy + 2\pi\frac{t_d}{T_s}$	$\pi Mcosy$	$\frac{V_{dc}}{2}$
$-\pi$	$-\frac{\pi}{2}$	$-\pi$	$-\pi(1+Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+Mcosy)+2\pi\frac{t_d}{T_s}$	π	
$\frac{\pi}{2}$	π	$-\pi$	$-\pi(1+Mcosy)$	$-\frac{V_{dc}}{2}$
		$\pi(1+Mcosy)+2\pi\frac{t_d}{T_s}$	π	

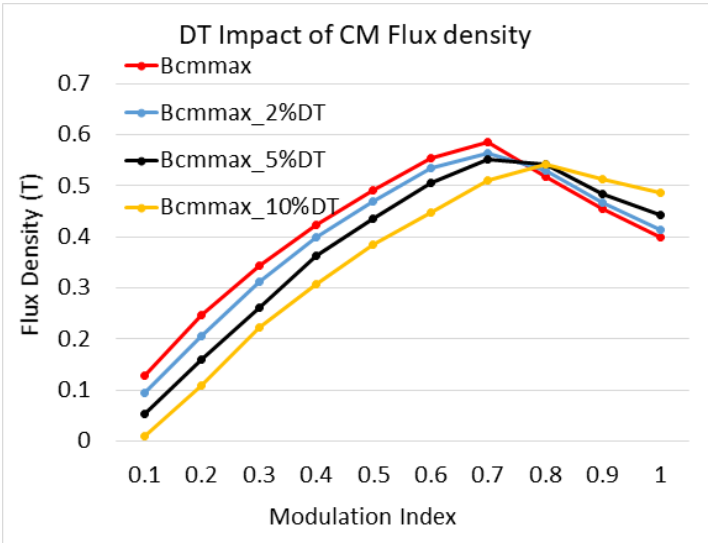


Fig. 6-16. Impact of dead time on CM inductor maximum flux density.

Table 6-4. Phase Voltage and CM Voltage Main Components at M=1

	f_0	$3f_0$	f_c	$2f_c \pm f_0$
V_a without DT	300	0	99	20.3
V_a with DT	281	6.4	107.8	25.9
	f_0	$3f_0$	f_c	$2f_c \pm 3f_0$
V_{cm} without DT	0	0	99	2.9
V_{cm} with DT	0	6.4	107.8	14.2

Table 6-5. Phase Voltage and CM Voltage Main Components at M=0.4

	f_0	$3f_0$	f_c	$2f_c \pm f_0$
V_a without DT	120	0	127.6	47.2
V_a with DT	101	6.4	106	51.7
	f_0	$3f_0$	f_c	$2f_c \pm 3f_0$
V_{cm} without DT	0	0	127.6	20.9
V_{cm} with DT	0	6.4	106	11.4

Table 6-4 and Table 6-5 show the calculated phase voltage and CM voltage main components at modulation index M=1 and M=0.4, respectively. Dead time impacts both fundamental frequency and switching frequency related components. The dead time impact on fundamental frequency related components does not change with modulation index. Dead time will decrease the fundamental frequency component and increase the third harmonic by a fixed value if dead time is fixed. The dead time impact on switching frequency harmonic and sidebands is high dependent on modulation index and shows complicated trend. When modulation index is high, if dead time

increases, both the third harmonic and the dominant switching frequency harmonic of the CM voltage will increase. As a result, the maximum CM flux density and total flux density will increase if dead time increases. When modulation index is low, if dead time increases, the dominant switching frequency harmonic will decrease although the third harmonic will increase. As a result, the maximum CM flux density and total flux density will decrease if dead time increases.

6.2.4 Impact of Neutral Point Voltage Variation

As discussed in literature, the dc-link capacitor NP voltage variation exists in a three-level inverter. With PDPWM, how the NP voltage variation impacts CM voltage and CM flux density is analyzed as follows.

Considering NP voltage variation, the CM equivalent circuit shown in Fig. 6-10 is modified as Fig. 6-17. The CM voltage is divided to two parts represented by V_{CM_ac} and V_{CM_dc}.

The dc side CM voltage

$$V_{CM_{dc}}(t) = \frac{V_{OP}(t) + V_{ON}(t)}{2} = \frac{(\frac{V_{dc}}{2} - \Delta V(t)) - (\frac{V_{dc}}{2} + \Delta V(t)}{2} = -\Delta V(t) \qquad (6-13)$$

$\Delta V(t)$ indicates NP voltage variation, which is determined by the current flowing through the dc-link capacitors. The low frequency current flowing through NP is denoted as

$$\overline{i_{neu}} = d_a i_a + d_b i_b + d_c i_c \qquad (6-14)$$

where i_a, i_b, i_c are three phase ac currents, and d_a, d_b, d_c are duty cycles of three phases.

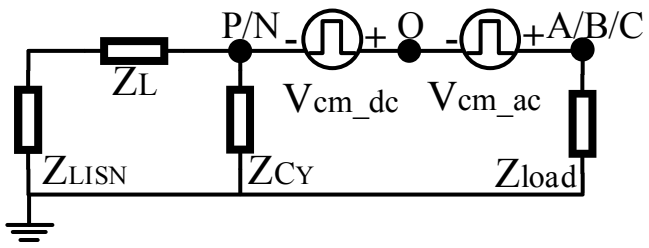


Fig. 6-17. Simplified CM equivalent circuit considering NP voltage variation.

The three phase ac currents are expressed as

$$i_a = I_o \cos(\omega_0 t - \varphi), i_b = I_o \cos\left(\omega_0 t - \frac{2}{3}\pi - \varphi\right), i_c = I_o \cos\left(\omega_0 t - \frac{4}{3}\pi - \varphi\right) \quad (6-15)$$

where I_o represents ac current amplitude, ω_0 is the angular fundamental frequency, φ is the phase angle.

A fundamental cycle can be divided to six regions based on the voltage polarities. In region I ($-\frac{\pi}{6} < \omega_0 t < \frac{\pi}{6}$), the three phase duty cycles with PDPWM are expressed as

$$d_a = m\cos(\omega_0 t), d_b = -m\cos\left(\omega_0 t - \frac{2}{3}\pi\right), d_c = -m\cos\left(\omega_0 t - \frac{4}{3}\pi\right) \quad (6-16)$$

Thus, the switching cycle averaged neutral point current is calculated as

$$\overline{i_{neu}} = d_a i_a + d_b i_b + d_c i_c = \frac{mI_o}{2}(2\cos(2\omega_0 t - \varphi) - cos\varphi) \quad (6-17)$$

In other regions, the expression for $\overline{i_{neu}}$ can be calculated similarly. Table 6-6 summarized the averaged neutral point current in a fundamental cycle.

Table 6-6. Averaged Neutral Point Current in a Fundamental Cycle

region	$\overline{i_{neu}}$
I ($-\frac{\pi}{6} < \omega_0 t < \frac{\pi}{6}$)	$\frac{mI_o}{2}(2\cos(2\omega_0 t - \varphi) - cos\varphi)$
II ($\frac{\pi}{6} < \omega_0 t < \frac{\pi}{2}$)	$\frac{mI_o}{2}(2\cos\left(2\omega_0 t - \varphi + \frac{\pi}{3}\right) + cos\varphi)$
III ($\frac{\pi}{2} < \omega_0 t < \frac{5\pi}{6}$)	$\frac{mI_o}{2}(2\cos\left(2\omega_0 t - \varphi + \frac{2\pi}{3}\right) - cos\varphi)$
IV ($\frac{5\pi}{6} < \omega_0 t < \frac{7\pi}{6}$)	$\frac{mI_o}{2}(-2\cos(2\omega_0 t - \varphi) + cos\varphi)$
V ($\frac{7\pi}{6} < \omega_0 t < \frac{3\pi}{2}$)	$\frac{mI_o}{2}(2\cos\left(2\omega_0 t - \varphi - \frac{2\pi}{3}\right) - cos\varphi)$
VI ($\frac{3\pi}{2} < \omega_0 t < \frac{11\pi}{6}$)	$\frac{mI_o}{2}(2\cos\left(2\omega_0 t - \varphi - \frac{\pi}{3}\right) + cos\varphi)$

The averaged neutral point current $\overline{i_{neu}}$ mainly contains the third order harmonic and it has six current zero-crossing point for a fundamental cycle. The phase angle of zero-crossing point in region I is calculated as

$$\theta_I = \frac{1}{2}\left(-\arccos\left(\frac{1}{2}cos\varphi\right) + \varphi\right) \qquad (6-18)$$

The NP voltage variation

$$\Delta V(t) = \frac{1}{2}\left(V_{PO}(t) - V_{ON}(t)\right) = \frac{1}{2C}\int\left(i_{c1}(t) - i_{c2}(t)\right)dt = \frac{1}{2C}\int i_{neu}(t)dt \qquad (6-19)$$

The high frequency current components contributed NP voltage variation can be neglected due to the large dc-link capacitance, thus the NP voltage variation is

$$\Delta V(t) \approx \frac{1}{2C}\int \overline{i_{neu}(t)}dt \qquad (6-20)$$

The NP voltage variation $\Delta V(t)$ is a piecewise function of $\omega_0 t$. As the NP voltage variation is mainly third order harmonic, it can be further simplified as

$$\Delta V(t) \approx V_e \cos\big(3(\omega_0 t + \varphi_e)\big) \tag{6-21}$$

where V_e and φ_e are the equivalent voltage amplitude and initial phase angle, respectively. By investigating the relationship between $\Delta V(t)$ and $\overline{i_{neu}(t)}$, V_e and φ_e are calculated as

$$\varphi_e = \frac{\pi}{3} - \theta_I \tag{6-22}$$

$$V_e = \frac{mI_o}{4\omega_0 C}\left(-2\sin(2\theta_I - \varphi) + (2\theta_I)cos\varphi + \sin\left(\frac{\pi}{3} - \varphi\right) - \sin\left(\frac{\pi}{3} + \varphi\right)\right) \tag{6-23}$$

Therefore, the NP voltage variation impact on dc side CM voltage can be quantified. NP voltage variation will also impact the ac side CM voltage.

In ideal case, the phase output voltage can be expressed as

$$V_{AO}(t) = \frac{V_{dc}}{2} \cdot s(t) \tag{6-24}$$

where $s(t)$ is the phase switching function.

Considering NP voltage variation, the phase voltage is expressed as

$$V_{AO}(t) = \left(\frac{V_{dc}}{2} + \Delta V(t)\right) \cdot s_1(t) + \left(\frac{V_{dc}}{2} - \Delta V(t)\right) \cdot s_2(t) = \frac{V_{dc}}{2} \cdot s(t) + \Delta V(t) \cdot s_{12}(t) \tag{6-25}$$

where $s_1(t)$ and $s_2(t)$ represents the switching function of upper most and bottom most devices, respectively, and $s_{12}(t)$ is defined as $s_{12}(t) = s_1(t) - s_2(t)$.

The Fourier transform

$$V_{AO}(\omega) = \frac{V_{dc}}{2} s(\omega) + s_{12}(\omega) \otimes \Delta V(\omega) \tag{6-26}$$

Define the NP voltage variation's contribution to the phase voltage spectrum $\Delta V_{AO}(\omega)$

$$\Delta V_{AO}(\omega) = s_{12}(\omega) \otimes \Delta V(\omega) \tag{6-27}$$

It can be derived that

$$\Delta V_{AO}(\omega) = \frac{V_e}{2}\left(e^{j(3\varphi_e)} s_{12}(\omega - 3\omega_0) + e^{j(-3\varphi_e)} s_{12}(\omega + 3\omega_0)\right) \tag{6-28}$$

It shows that the spectral content of the NP voltage variation's contribution to the ac voltage is the superposition of switching function spectrum $s_{12}(\omega)$ with frequency shifts of $\pm 3\omega_0$. The harmonic coefficients of Fourier series of $s_{12}(t)$ can be calculated with double Fourier integral. Assuming the harmonic coefficients of $s_{12}(t)$ is $\overline{C_{mn}} = \overline{A_{mn}} + j\overline{B_{mn}}$, the harmonic coefficients of $\Delta V_{AO}(t)$ is $\widehat{C_{mn}} = \widehat{A_{mn}} + j\widehat{B_{mn}}$, which can be calculated as

$$\widehat{A_{00}} = \frac{V_e}{2}\left(\overline{A_{03}} cos\varphi_e + \overline{B_{03}} cos\varphi_e\right)$$

$$\widehat{A_{mn}} = \frac{V_e}{2}\left((\overline{A_{m,n-3}} + \overline{A_{m,n+3}}) cos\varphi_e + (\overline{B_{m,n-3}} - \overline{B_{m,n+3}}) sin\varphi_e\right)$$

$$\widehat{B_{mn}} = \frac{V_e}{2}\left((\overline{B_{m,n-3}} + \overline{B_{m,n+3}}) cos\varphi_e - (\overline{A_{m,n-3}} - \overline{A_{m,n+3}}) sin\varphi_e\right) \tag{6-29}$$

Thus, the phase voltage spectrum considering NP voltage variation can be calculated. The CM voltage source and CM inductor flux density can be calculated accordingly. Table 6-7 lists the main components of phase voltage and CM voltage without NP voltage variation. Table 6-8 calculates the main components of phase voltage and CM voltage with NP voltage variation at different power factors. The dc-link voltage variation is in the 2%~5% range of half dc voltage which is typical.

Comparing Table 6-7 and Table 6-8, the NP voltage variation introduces extra third order fundamental frequency harmonics and slightly changes the switching frequency component and

sidebands. In a motor drive system with tens of kilowatts power rating, the parasitic capacitance is typically a couple of nanofarads. In the studied system, a 10 nF parasitic capacitance is assumed, and the CM loop shows a large impedance at the third harmonic of fundamental frequency point. As a result, the third harmonic of CM current is very small and can be neglect. The impact of NP voltage variation on switching frequency components of CM current can also be neglected.

Table 6-7. Main Components of Phase Voltage and CM Voltage without NP Voltage Variation (M=1, Vdc=300 V, Io=20 A)

	f_0	$3f_0$	f_c	$2f_c \pm f_0$
V_a	300	0	98.9	20.3
	f_0	$3f_0$	f_c	$2f_c \pm 3f_0$
V_{cm}	0	0	98.9	2.8

Table 6-8. Main Components of Phase Voltage and CM Voltage with NP Voltage Variation (M=1, Vdc=300 V, Io=20 A)

	PF=1				PF=0			
	f_0	$3f_0$	f_c	$2f_c \pm f_0$	f_0	$3f_0$	f_c	$2f_c \pm f_0$
V_a	300	8.4	98.9	20.3	300	12.5	96.8	20.2
	f_0	$3f_0$	f_c	$2f_c \pm 3f_0$	f_0	$3f_0$	f_c	$2f_c \pm 3f_0$
V_{cm_ac}	0	8.4	98.9	2.8	0	12.5	96.8	2.9
V_{cm_dc}	0	13.6	0	0	0	9.9	0	0
V_{cm}	0	5.2	98.9	2.8	0	11.2	96.8	2.9

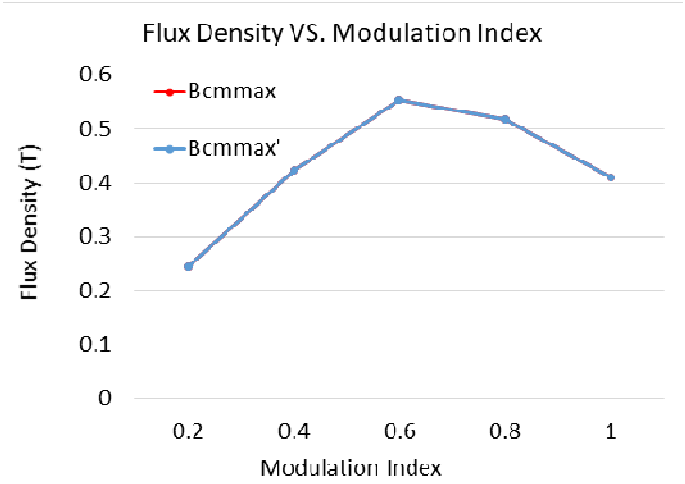


Fig. 6-18. Impact of NP voltage variation on CM inductor maximum flux density.

Fig. 6-18 shows the calculated maximum CM flux density without and with NP voltage variation at different modulation indexes. The two curves almost overlap with each other. In conclusion, the impact of NP voltage variation on CM current and CM flux density of the CM inductor can be neglected due to the low parasitic capacitance in motor drive system and the little impact of NP voltage variation on switching frequency related components of CM voltage.

6.2.5 Impact of CM Inductance

Selecting the CM inductor value is critical for CM filter design. Following the classical EMI filter design procedure, the LC filter corner frequency can be determined by the required CM noise attenuation. Usually the CM capacitor value is limited by system safety and leakage current requirements and is set to maximum. Thus, CM inductor value can be determined. However, this value may not be optimal considering inductor physical design. In some cases increasing the CM inductor value can actually help to reduce CM inductor size and weight in addition to further enhance the filter attenuation. The CM inductor inductance selection impacts the CM impedance

and thus impacts the CM flux density. With the developed model, the impact of CM inductor value on the CM flux density is studied.

The relative position of switching frequency f_{sw} and CM impedance resonant frequency f_{res} determines the trend how CM inductor value impact the CM flux density of CM inductor. Note that here the CM impedance resonant frequency refers to the frequency that CM impedance achieves minimum value instead of resonant frequency of LC filter.

Fig. 6-19 shows the typical CM impedance of the studied system based on calculation of (6-12). When resonance frequency is lower than switching frequency as shown in Fig. 6-20(a), increasing the CM inductor value decreases resonant frequency and increases CM impedance at switching frequency point. Thus, the dominated switching frequency component of CM current decreases. When resonance frequency is higher than switching frequency as shown in Fig. 6-20(b), increasing the CM inductor value decreases resonant frequency and decreases CM impedance. Thus, the dominated switching frequency component of CM current increases. Only when the CM inductance increased to a certain value that the new resonance frequency is lower than switching frequency, the trend will be reversed.

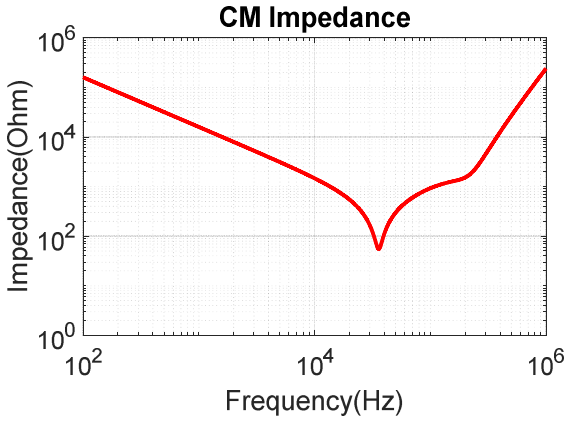
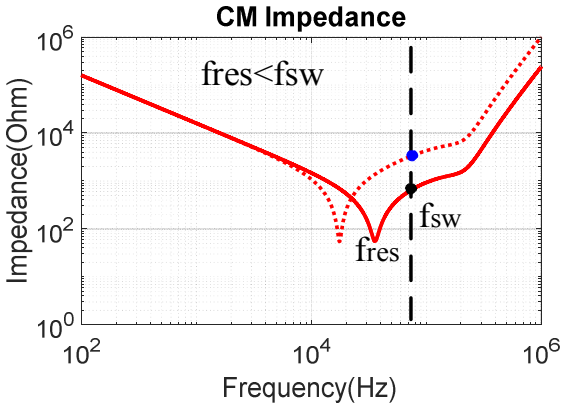
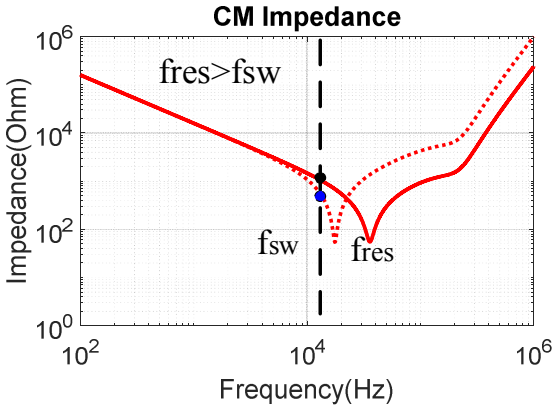


Fig. 6-19. A typical CM impedance of the studied three-level inverter system.



(a)



(b)

Fig. 6-20. Relative position of the CM impedance resonance frequency and switching frequency, (a) $f_{res} > f_{sw}$, (b) $f_{res} < f_{sw}$.

With the developed model, when the CM inductance varies from 320 uH to 4.1 mH (corresponding number of turns varies from 5 to 18), the calculated maximum DM flux density, maximum CM flux density, and maximum flux density of the CM inductor at modulation index M=1 is summarized as Fig. 6-21. From Fig. 6-21, when CM inductor value increases, the maximum DM flux density increases and the maximum CM flux density decreases. The minimum total flux density is achieved when the CM inductor value is 2.5 mH (corresponding number of

turns is 14) in the studied case. If the needed CM inductor value from the CM noise attenuation requirement is smaller than 2.5 mH, by further increasing the CM inductor value, the maximum flux density will be decreased. In another word, a smaller core can be used.

As discussed above, the relative position of resonance frequency and switching frequency determines the trend how CM inductor value impact the maximum CM flux density. If the switching frequency is 20 kHz, the calculated maximum DM flux density, maximum CM flux density, and maximum flux density of the CM inductor when the CM inductance varies from 320 uH to 4.1 mH is summarized as Fig. 6-22. The trend is different from previous case. When the CM inductor value increases, the maximum flux density will also increases. Only when the CM inductor value increased to 3.2 mH (corresponding number of turns is 16), the maxim flux density began to decrease.

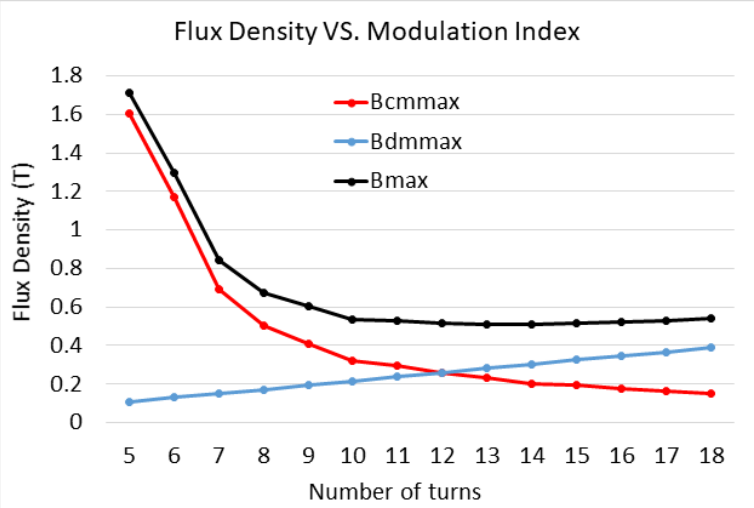


Fig. 6-21. Impact of CM inductance on CM inductor maximum flux density.

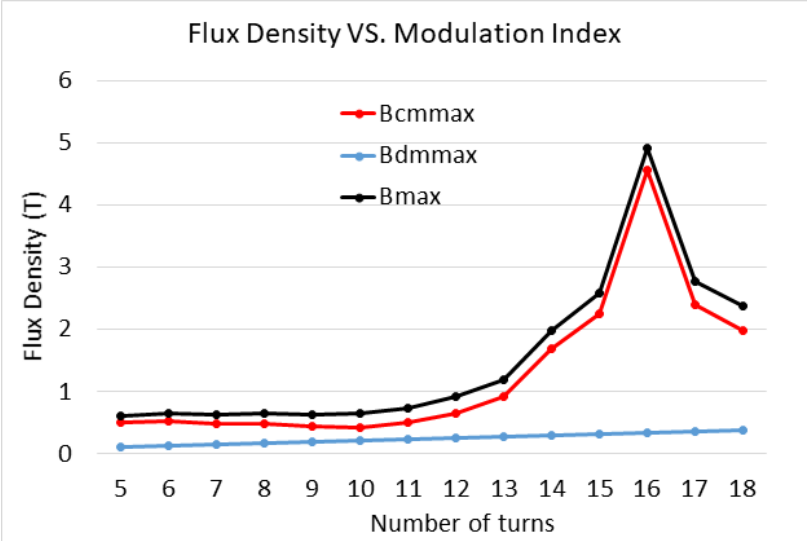


Fig. 6-22. Impact of CM inductance on CM inductor maximum flux density when switching frequency is 20 kHz.

6.3 Improved CM Filter Design Procedure

Based on the analysis presented in last section, the modulation index and CM inductance have large impact on CM inductor maximum flux density and need to be addressed for CM filter design.

Two conclusions can be made. First, the maximum CM flux density has a non-monotonous relationship with modulation index. Thus, the worst operation condition for CM inductor flux density need to be identified and used as the saturation constraint in CM inductor design to avoid under design. Only consider the full load or minimum load operation when design the CM inductor may result in core saturation. Second, the minimum CM inductor value obtained from the CM noise attenuation requirement is not necessary the best value for CM inductor size reduction. Increasing the CM inductor value may lead to reduced maximum flux density and thus reduced CM inductor size. The CM inductor value optimization need to be conducted to avoid overdesign.

An improved CM filter design procedure is proposed with these considerations. First, following the conventional EMI filter design procedure, the CM inductor value L_{min} is determined based on CM noise attenuation requirement. Based on L_{min}, the CM inductor physical design is conducted following conventional method. Inductor geometrical parameters are determined and the number of turns is determined as N_0. The CM inductor maximum flux density is calculated as B_0 and the CM impedance resonance frequency is calculated as f_{res0}. The wire diameter d is determined by full load current assuming a certain current density. Usually the CM inductor adopts single layer structure to reduce the parasitic capacitance. For a given core, the maximum number of turns N_{max} is determined by the single layer constraint.

Then, CM inductor value can be increased by increasing the number of turns. If the resonance frequency f_{res0} is lower than switching frequency, increases the number of turns by one turn, the new CM inductor value is L_1 and maximum flux density is B_1. If $B_1 < B_0$, increases the number of turns by one more turn. Repeat this process until that the number of turns have been increased by (x+1) turns and the calculated flux density satisfy $B_{x+1} > B_x$ or the number of turns have reached N_{max}. If the resonance frequency f_{res0} is higher than switching frequency, first increases the number of turns by y turns which makes $f_{res0} > f_{sw}$. Then follow the same procedure of previous case. With this procedure, the CM inductor value is determined as L_x.

Second, the maximum CM inductor flux density is calculated for the given modulation index range, and the operation point which leads to maxim flux density is identified. Then, the CM inductor physical design is re-conducted with L_x at the worst operation point. Fig. 6-23 illustrates the improved CM filter design procedure.

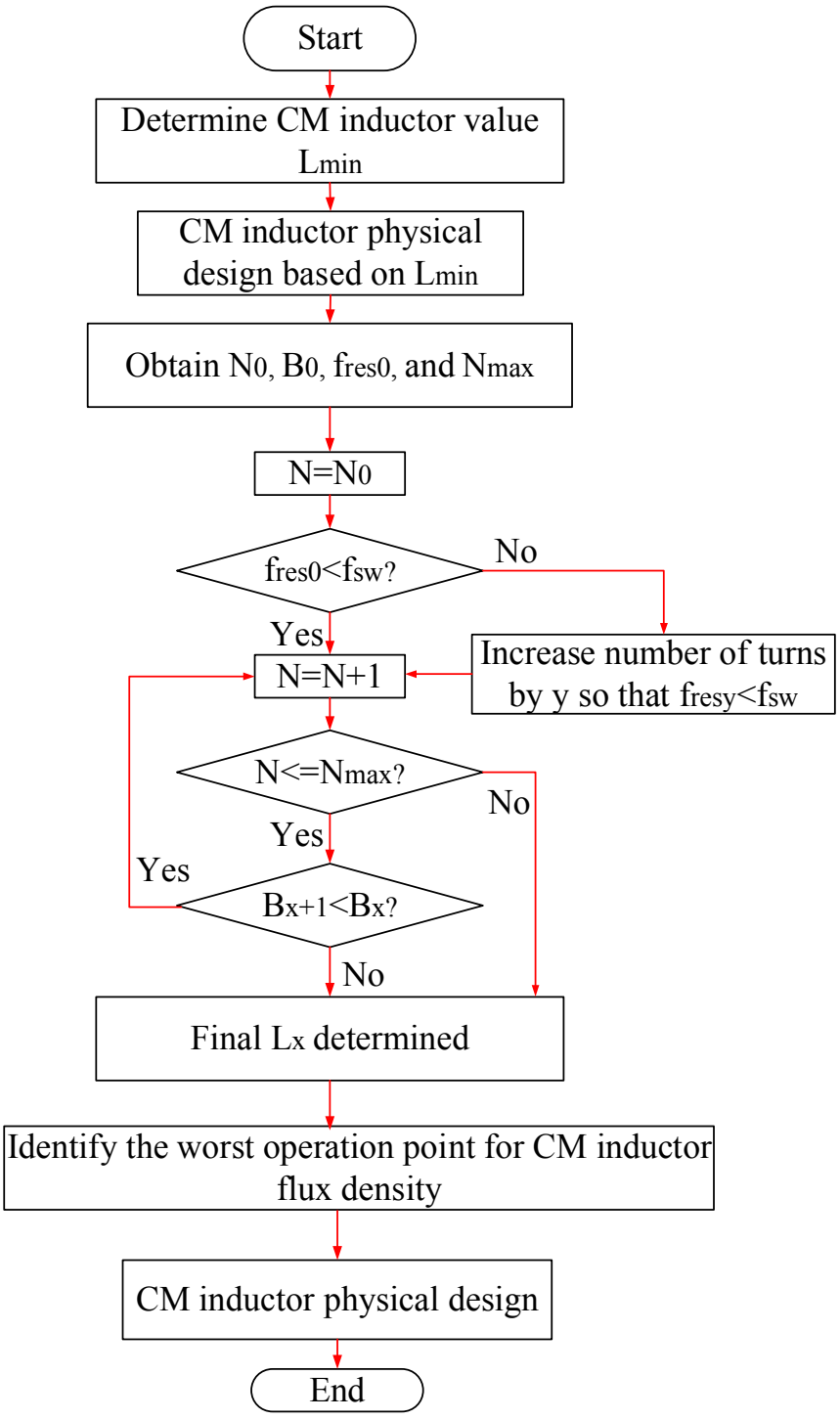


Fig. 6-23. Improved CM filter design procedure.

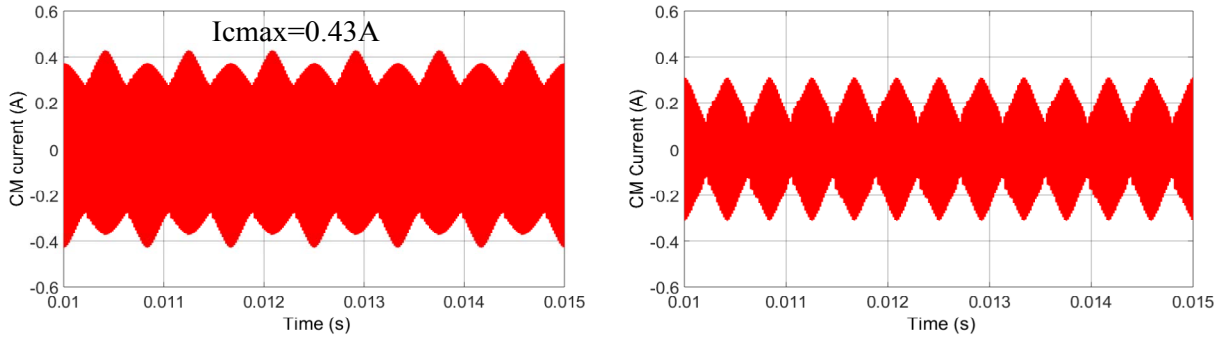
6.4 Verification

To verify the impact of modulation index, dead time, NP voltage variation, and CM inductance on the CM inductor maximum flux density, comparison verification are conducted.

Fig. 6-24(a) and Fig. 6-24(b) show the measure CM current of the CM inductor when modulation index is 0.7 and 1, respectively. The maximum CM current in the two cases are 0.43 A and 0.31 A. The trend matches theoretical analysis that maximum CM flux density has a non-monotonous relationship with modulation index and maximum flux density does not occur at full load.

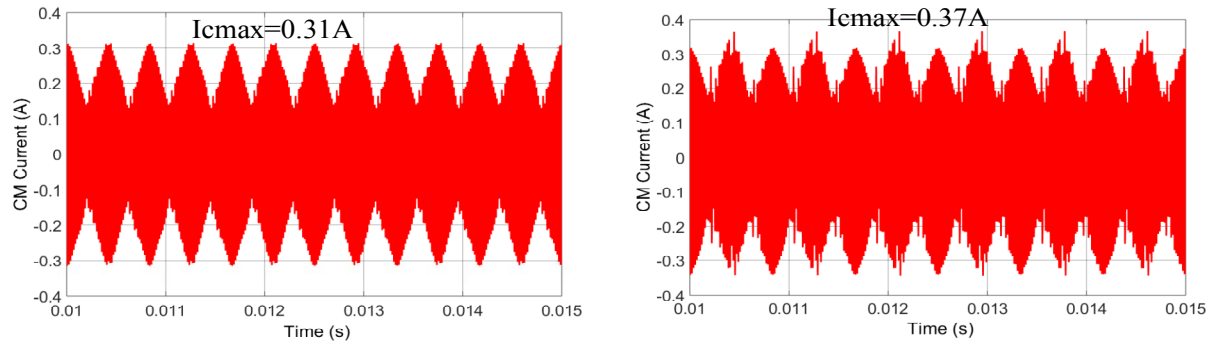
Fig. 6-25(a) and Fig. 6-25(b) show the measure CM current of the CM inductor when the dead time is 2% of switching period and 10% of switching period, respectively. Both at the modulation index M=1. The maximum CM current in the two cases are 0.31 A and 0.37 A. The trend matches theoretical analysis that larger dead time result in higher maximum CM flux density when modulation index is high.

Fig. 6-26(a) and Fig. 6-26(b) show the measure CM current of the CM inductor when the dead time is 2% of switching period and 10% of switching period, respectively. Both at the modulation index M=0.4. The maximum CM current in the two cases are 0.3 A and 0.22 A. The trend matches theoretical analysis that larger dead time result in lower maximum CM flux density when modulation index is low.



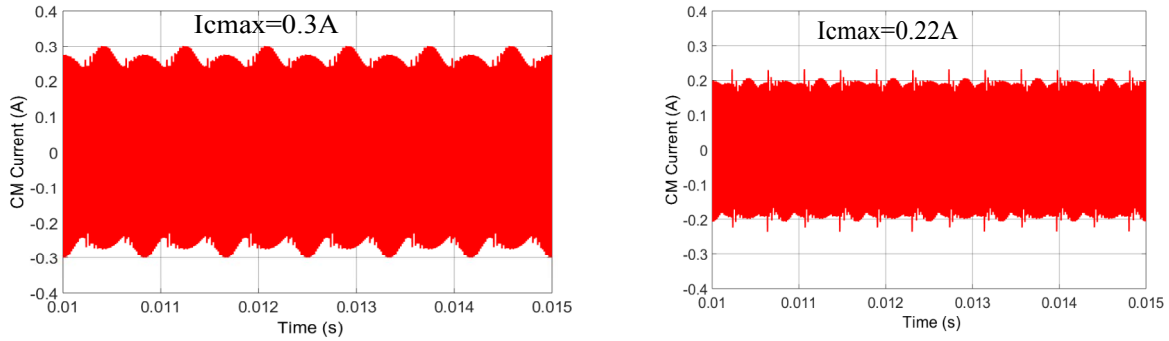
(a) (b)

Fig. 6-24. CM current of the CM inductor at different modulation index, (a) M=0.7, (b) M=1.



(a) (b)

Fig. 6-25. CM current of the CM inductor with different dead time at M=1, (a) dead time is 2% of switching period, (b) dead time is 10% of switching period.



(a) (b)

Fig. 6-26. CM current of the CM inductor with different dead time at M=0.4, (a) dead time is 2% of switching period, (b) dead time is 10% of switching period.

Fig. 6-27 shows the voltages of the two dc-link capacitors when M=1. The NP voltage variation mainly contains the third harmonic. The CM current is measure at this condition and shown as Fig. 6-28. Comparing Fig. 6-28 and Fig. 6-24(b), the CM current is almost the same. It verifies the analysis that the impact of NP voltage variation on the CM inductor flux density can be neglected.

Fig. 6-29(a) and Fig. 6-29(b) show the measure CM current of the CM inductor when the CM inductor value is selected as 600 uH and 2.5 mH, respectively. Both at the condition that switching frequency is 60 kHz and M=1. The maximum CM current in the two cases are 0.68 A and 0.1 A. Fig. 6-30(a) and Fig. 6-30(b) show the measure CM current of the CM inductor when the CM inductor value is selected as 600 uH and 2.5 mH, respectively. Both at the condition that switching frequency is 20 kHz and M=1. The maximum CM current in the two cases are 0.46 A and 0.82 A.

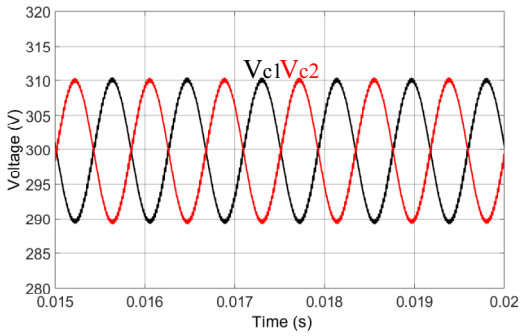


Fig. 6-27. Voltages of the two dc-link capacitors.

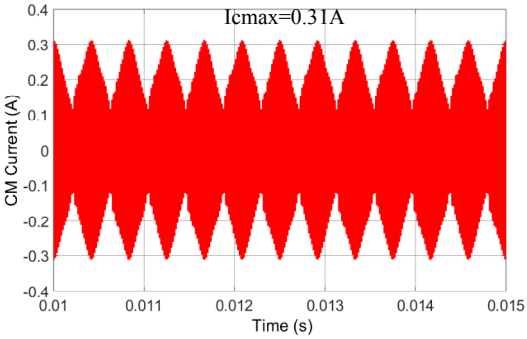
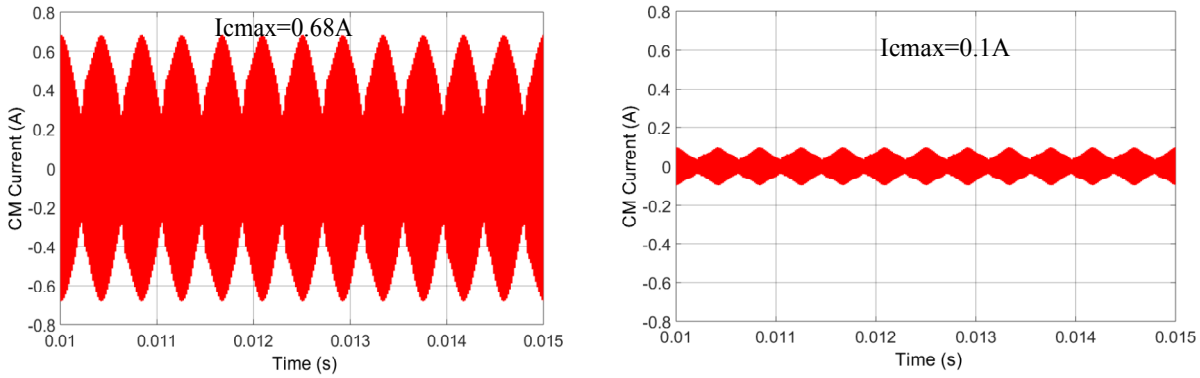
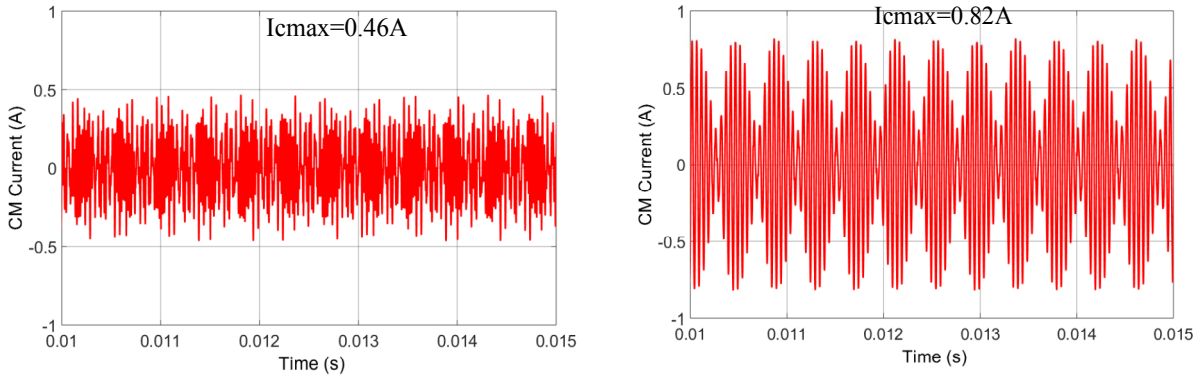


Fig. 6-28. CM current of the CM inductor with NP voltage variation.



(a) (b)

Fig. 6-29. CM current of the CM inductor with different CM inductor value when switching frequency is 60 kHz. (a) CM inductor value is 600 uH, (b) CM inductor value is 2.5 mH.



(a) (b)

Fig. 6-30. CM current of the CM inductor with different CM inductor value when switching frequency is 20 kHz. (a) CM inductor value is 600 uH, (b) CM inductor value is 2.5 mH.

With the improved CM filter design procedure, the CM inductor design results are summarized in Table 6-9. Table 6-10 summarizes the CM inductor design results following conventional CM filter design procedure. Fig, 6-31 shows the simulation results of dc side CM noises with the two designs. With the improved CM filter design procedure, the CM inductor size and weight are significantly reduced in addition to further reduced EMI noise level.

Table 6-9. CM Inductor Design Results with Improved CM Filter Design Procedure

Design description	Volume	Weight
Core: nanocrystalline Vitroperm 500F T60006-L2040-W424 (OD=40 mm, ID=25 mm, H=15 mm) Winding: wire AWG 15, number of turns N=13 Inductance: 2.07 mH	1150 cm3	90 g

Table 6-10. CM Inductor Design Results with Conventional CM Filter Design Procedure

Design description	Volume	Weight
Core: nanocrystalline Vitroperm 500F T60006-L2063-W517 (OD=63 mm, ID=50 mm, H=25 mm) Winding: wire AWG 15, number of turns N=8 Inductance: 660 uH	2890 cm3	183 g

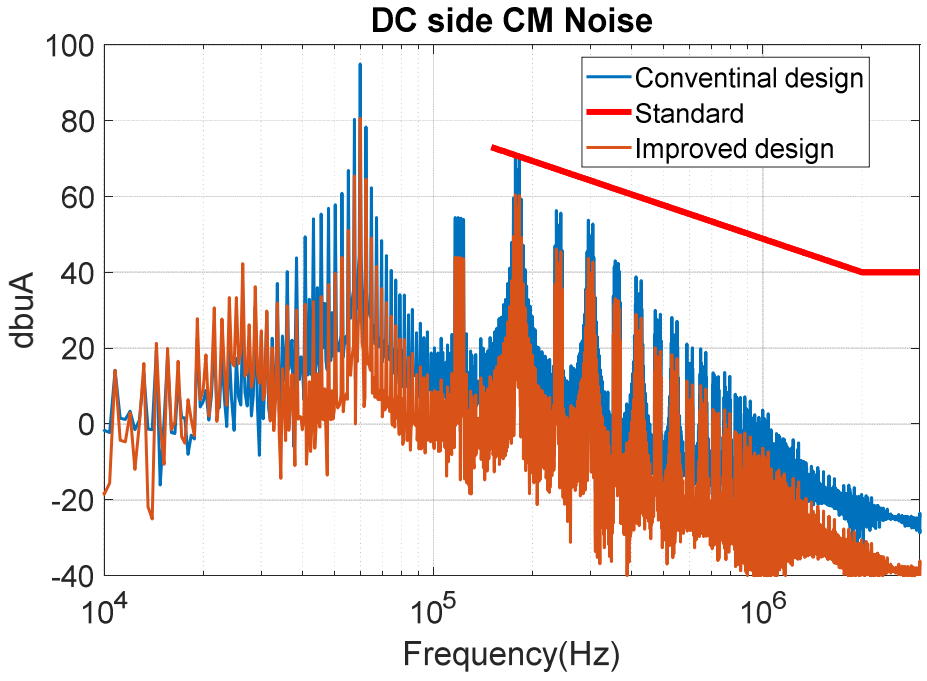


Fig. 6-31. Simulation results of the dc side CM noises of the two design cases.

6.5 Conclusion

This chapter presents the CM inductor flux density modeling, analysis and design optimization for three-level inverter.

First, the spectrum concept is introduced for CM inductor core saturation analysis and design optimization. Three components in the CM inductor which may cause large CM flux density and core saturation are summarized: (1) switching frequency related components, (2) impedance resonance frequency related components, and (3) modulation frequency related components. Each component is investigated for CM flux density reduction and filter design optimization. A connecting ac and dc side midpoint with notch filter structure is proposed to reduce modulation frequency related components. Experiment results shows that, with the optimized design, switching frequency related CM voltage components and impedance resonance components are significantly reduced, and the notch filter structure reduced the modulation frequency related components by 3.75 times and avoided the CM inductor core saturation.

Second, the CM inductor in a three-level inverter system with dc side CM filter is studied. The CM flux density calculation model has been developed. The impact of modulation index, dead time, NP voltage variation, and CM inductor value on the maximum CM inductor flux density are comprehensively analyzed. The conclusion are made as follows. (1) The maximum CM flux density has a non-monotonous relationship with modulation index and the worst case does not occur at full load or minimum load condition. (2) The impact of dead time on maximum CM flux density is highly dependent on modulation index. When modulation index is high, larger dead time results in higher maximum flux density. When modulation index is low, larger dead time leads to lower maximum flux density. (3) The impact of NP voltage variation on CM current and CM flux density of the CM inductor can be neglected due to the low parasitic capacitance in motor drive

system and the little impact of NP voltage variation on switching frequency related components of CM voltage. (4) The CM inductor value largely impact the maximum flux density. In some cases increasing the CM inductor value could reduce the dominated switching harmonic of the CM current. The CM inductor size and weight can be reduced in addition to further enhance the filter attenuation. Based on the CM inductor flux density analysis, an improved CM filter design procedure is proposed to avoid over-design or under-design of the CM inductor.

7. Design and Demonstration of a MW Three-Level Inverter with Cryogenic Cooling

The components for power generation, distribution, and transformation are not currently available in the high power range with necessary efficiency and power density required for transport-class aircraft. Accordingly, the development of high efficiency, high specific power high power electronics intended for eventual use in aircraft electric propulsion drives are critical.

The cryogenic power electronics can be beneficial thanks to the following features: (1) it is reported that several power devices, such as silicon and gallium nitride based, offers decreased specific on-state resistance and increased switching speed at low temperature. Thus, power stage efficiency can be improved. Furthering more, with the given loss budget, switching frequency can be increased, enabling less requirement of filters in the system. (2) Resistivity of conductors, such as copper and aluminum, significantly reduced as temperature decreases. Hence, less usage of the bus bars, and inductor windings is required considering the same thermal management. (3) At the system level in aircraft applications, superconducting technologies such as motors/generators along with their supportive power systems will grow in importance. Integrating the associated power electronics into the superconductive motor/generator system can avoid extra thermal insulation and temperature regulation system, and thus reduce system complexity and power density.

This chapter presents the design and demonstration of a MW three-level inverter with cryogenic cooling for aircraft applications.

7.1 Power Devices and Magnetics Characterization at Cryogenic Temperature

7.1.1 Power Devices Characterization

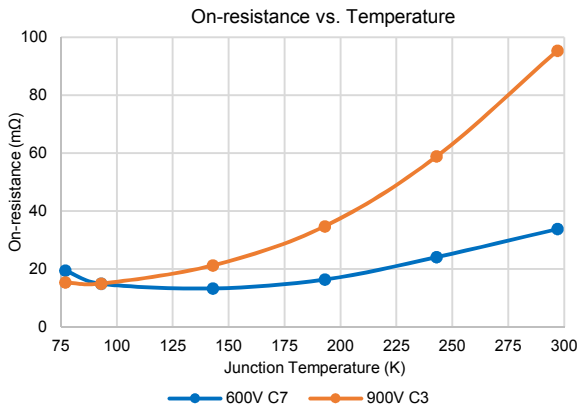
The methodology for static and dynamic characterization of power devices at cryogenic temperature has been illustrated in previous literature and will not be repeated here [221]. The state-of-the-art Si, SiC, and GaN MOSFETS in the 600 V~1.2 kV and tens of Amps range are selected as candidates and are comprehensively characterized.

Si MOSFETs in general show improved characteristics at cryogenic temperature. Performance of two Si MOSFETs from Infineon are characterized including 600 V/ 50 A IPZ60R040 C7 CoolMos and 900 V/ 35 A IPW90R120 C3 CoolMos.

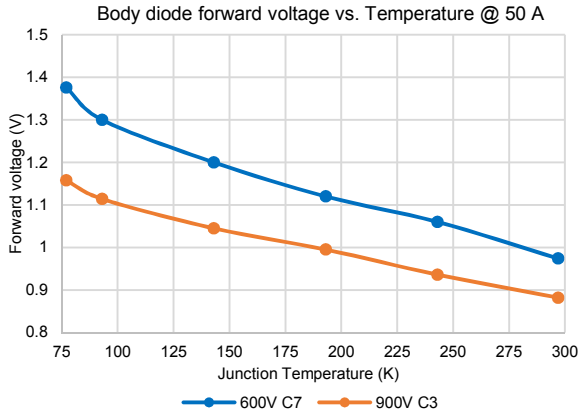
Fig. 7-1 summarizes their performance with respect to the on-resistance, body diode forward voltage, breakdown voltage, threshold voltage, transconductance, and switching losses. From Fig. 7-1, both the on-state resistance and switching loss decreases at cryogenic temperature while the breakdown voltage also decreases.

SiC devices, however, show increased on-state resistance as indicated in the literature. Three state-of–the-art 1.2 kV SiC MOSFETs from different manufacturers are characterized including Wolfspeed 1200 V /30 A C3M0075120K, Rohm 1200 V /72 A SCT3030KL, and ST 1200 V /65 A SCT50N120 [221].

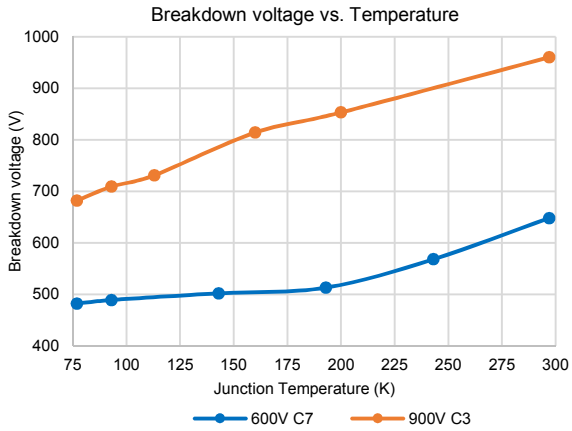
Fig. 7-2 summarizes their performance with respect to the on-resistance, body diode forward voltage, breakdown voltage, threshold voltage, transconductance, and switching losses. From Fig. 7-2, as temperature decreases, the on-state resistance increases while the breakdown voltage keeps constant. For devices from different manufacturers, the switching loss show various trends.



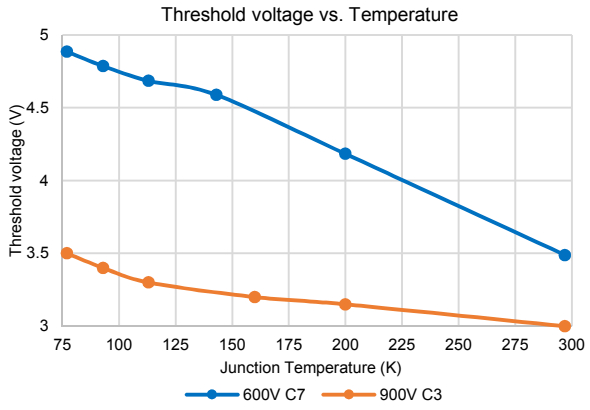
(a) On-resistance vs. temperature



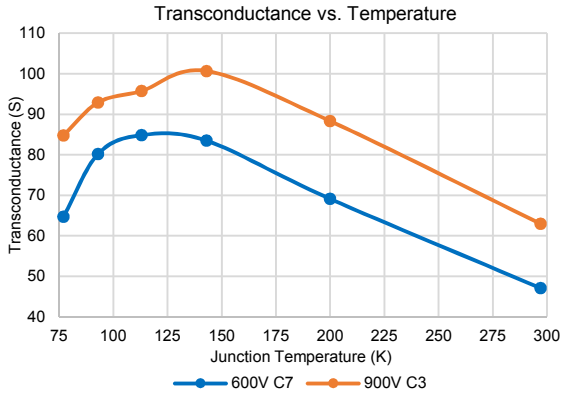
(b) Diode forward voltage vs. temperature



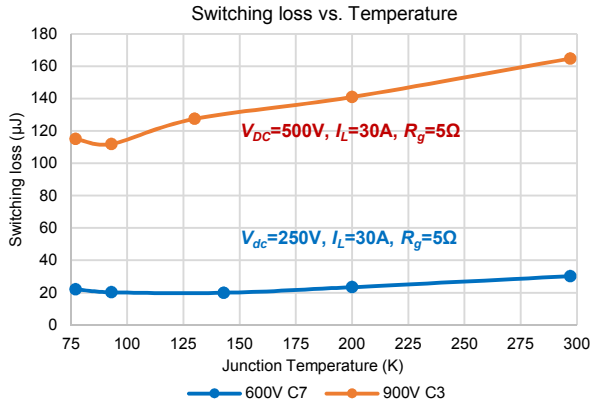
(c) Breakdown voltage vs. temperature



(d) Threshold voltage vs. temperature

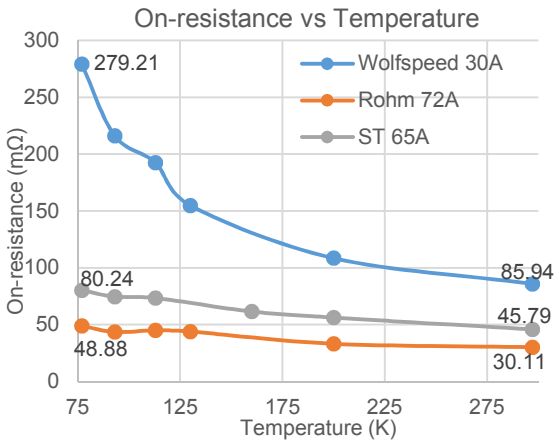


(e) Transconductance vs. temperature

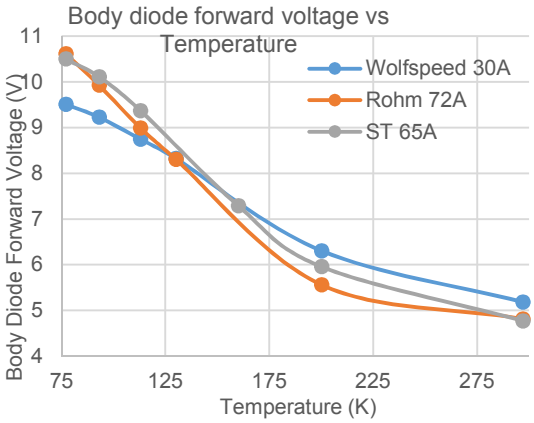


(f) Switching loss vs. temperature

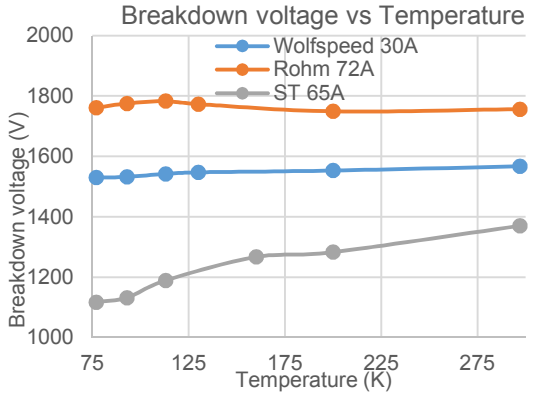
Fig. 7-1. Performance of two Si MOSFET candidates at cryogenic temperature.



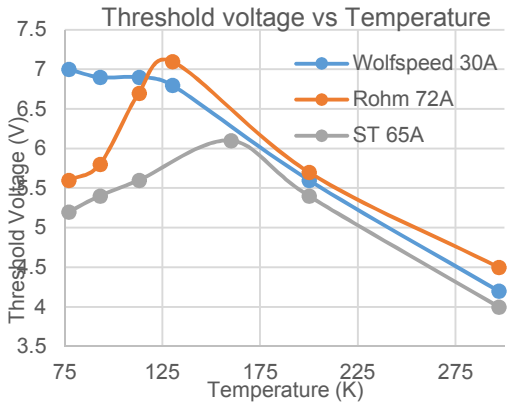
(a) On-resistance vs. temperature



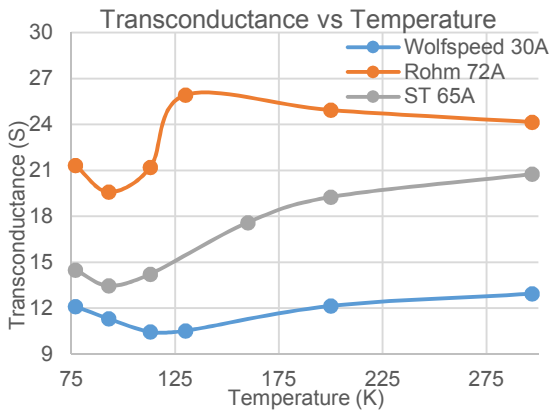
(b) Diode forward voltage vs. temperature



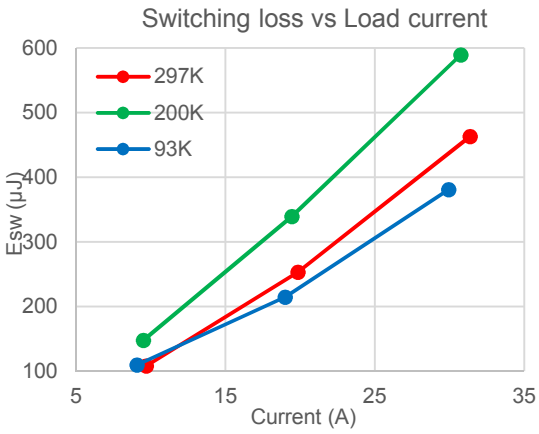
(c) Breakdown voltage vs. temperature



(d) Threshold voltage vs. temperature

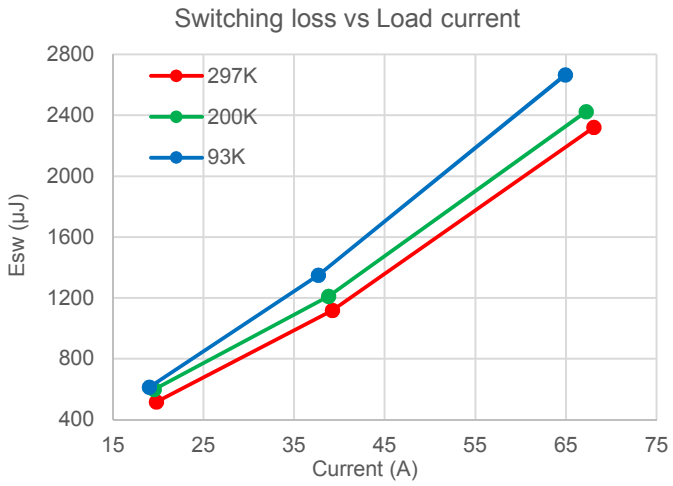


(e) Transconductance vs. temperature



(f) Switching loss vs. load (Wolfspeed device, 500V, 1 Ω gate resistance)

Fig. 7-2. Performance of three SiC MOSFET candidates at cryogenic temperature.

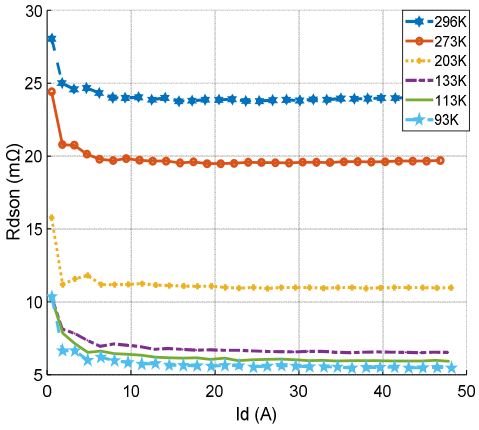


(g) Switching loss vs. load (Rohm device, 500V, 1 Ω gate resistance)

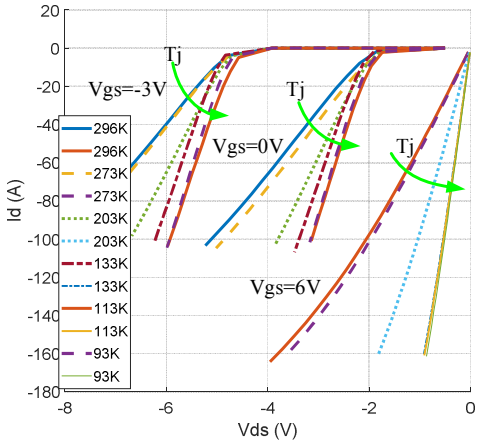
Fig. 7-2. Continued.

GaN MOSFETs in general also show improved characteristics at cryogenic temperature. Performance of a 650 V GaN HEMT GS66516T from GaN System is characterized [222].

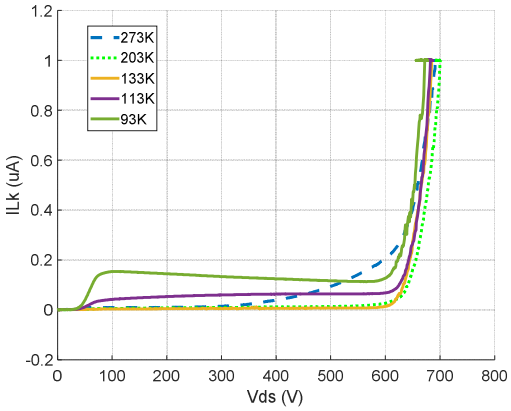
Fig. 7-3 summarizes their performance with respect to the on-resistance, reverse conduction characteristics, breakdown voltage, threshold voltage, transconductance, and switching losses. From Fig. 7-3, both the on-state resistance and switching loss can be reduced by around 30% at cryogenic temperature while the breakdown voltage keeps constant. Thus, the 650V enhancement GaN HEMT is a promising candidate for cryogenic power electronics system. Due to the extreme fast switching speed at cryogenic temperature, the high dv/dt induced self-turn-on and high di/dt induced gate voltage over-shoot of the device should be took care of.



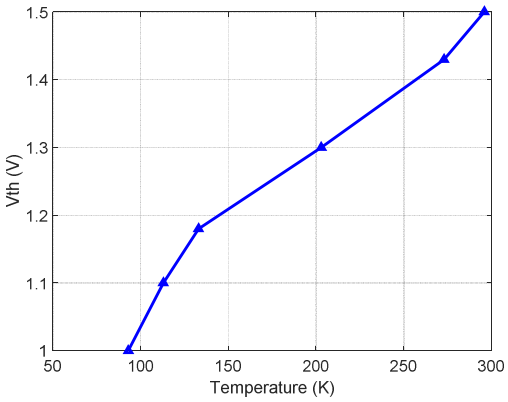
(a) On-resistance vs. temperature



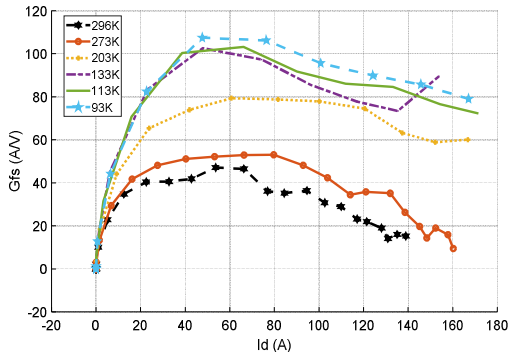
(b) Reverse conduction characteristics vs. temperature



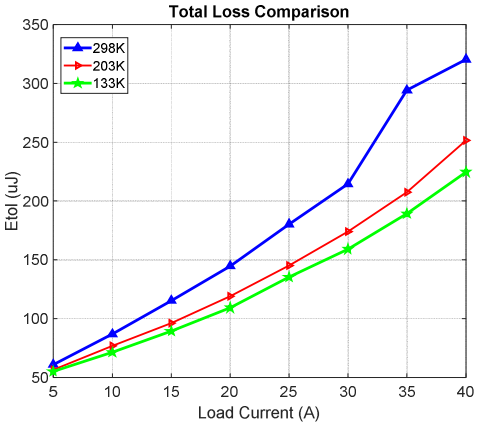
(c) Breakdown voltage vs. temperature



(d) Threshold voltage vs. temperature



(e) Transconductance vs. temperature



(f) Switching loss vs. load (400 V, gate resistance turn on 20Ω, turn off 2Ω)

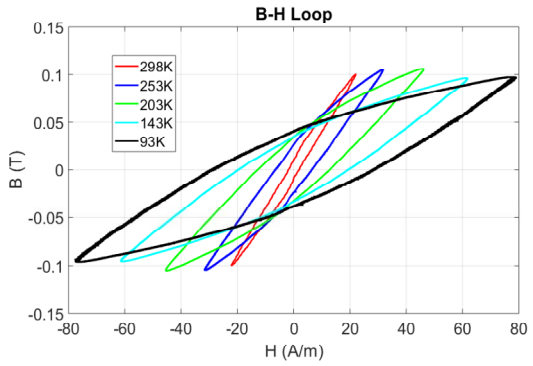
Fig. 7-3. Performance of 65V GaN HEMT at cryogenic temperature.

7.1.2 Magnetics Characterization

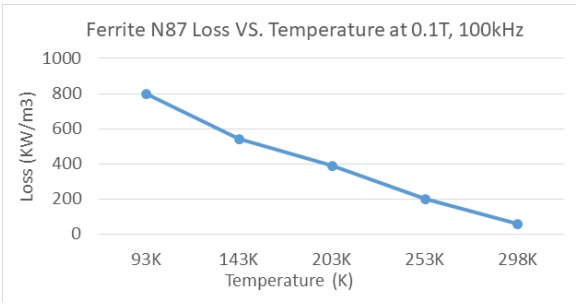
Two commonly used magnetic materials, ferrite N87 and nanocrystalline core Vitroperm 500F, are selected for the following case study to demonstrate the performance of magnetic core at cryogenic temperature. Since B-H curve is a function of temperature, frequency and flux density, two materials are tested in the range from room temperature to cryogenic temperature. Under each temperature point, the B-H curve test is conducted with varying sinusoidal exciting frequencies from 3 kHz to 500 kHz, and different levels of flux density until the core is saturated. In the end, the influence of low temperature on magnetic core characteristics is summarized [224].

Fig. 7-4(a) shows the Ferrite N87 B-H curves dependence on temperatures under the operating point of 0.1 T and 100 kHz. The corresponding core loss as a function of temperature is presented in Fig. 7-4(b). It can be found that the core loss increases by a factor of 13 as temperature decreases from 298 K to 93 K. The core loss dependence on temperature under more operating frequencies and flux density levels are tested and summarized in Fig. 7-5. A similar trend can be found that the core loss increases more than 10 times when temperature decreases from room temperature to cryogenic temperature.

Similarly, for the nanocrystalline Vitroperm 500F material, B-H curves at different temperatures at the operating point 0.5 T and 20 kHz are given in Fig. 7-6(a). The corresponding core loss as a function of temperature is summarized in Fig. 7-6(b). The core loss doubles as temperature decreases from 298 K to 93 K. The core loss as a function of temperature and flux density at frequencies of 20 kHz, 70 kHz, 100 kHz and 200 kHz are presented in Fig. 7-7. A similar trend can be observed that core loss increases 1.5~2.5 times at the cryogenic temperature as compared to that at the room temperature.

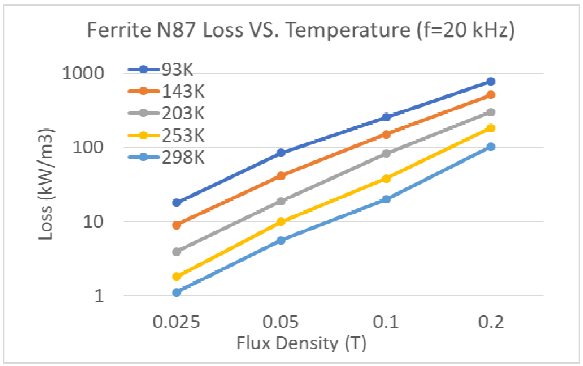


(a) B-H curves vs. temperature

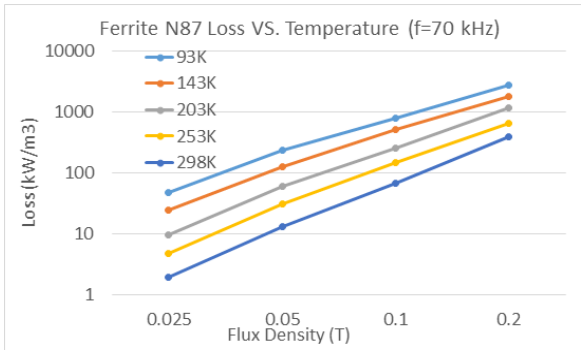


(b) Core loss vs. temperature

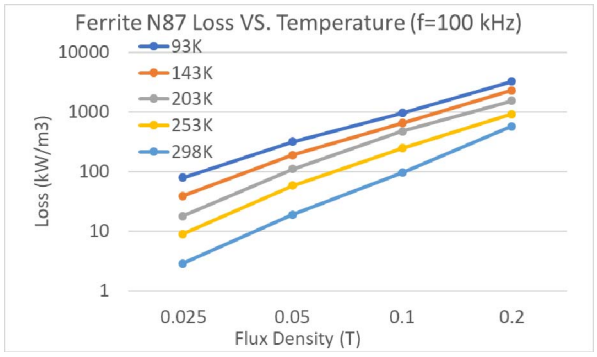
Fig. 7-4. Ferrite N87 characteristics under operating point 0.1 T and 100 kHz.



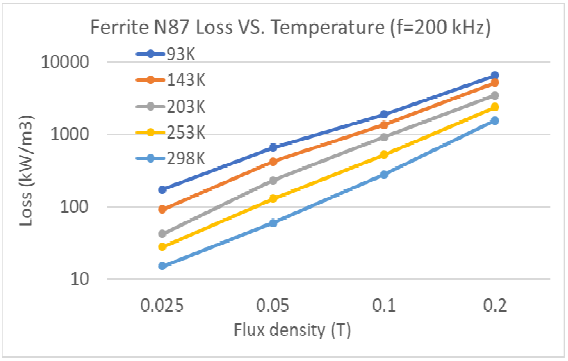
(a)



(b)

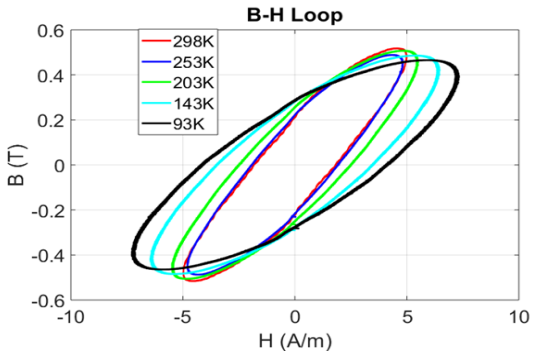


(c)

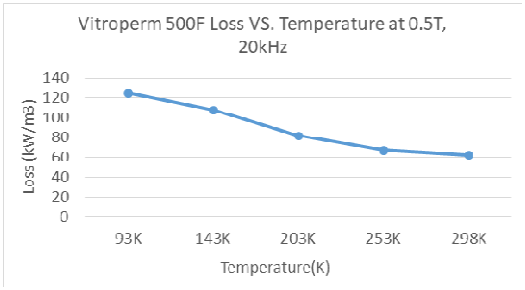


(d)

Fig. 7-5. Ferrite N87 temperature dependent characteristics under different frequencies, (a) 20 kHz, (b) 70 kHz, (c) 100 KHz, (d) 200 kHz.

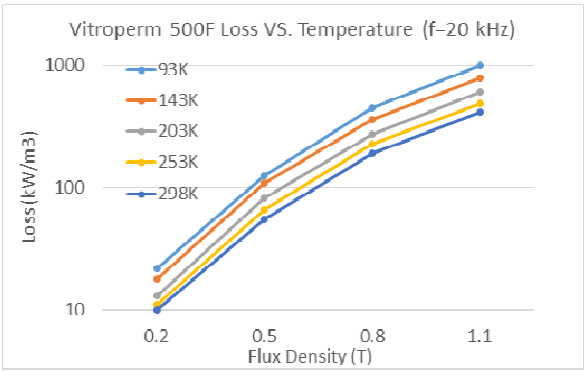


(a) B-H curves vs. temperature

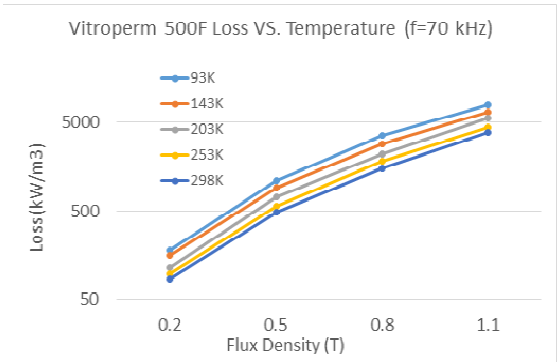


(b) Core loss vs. temperature

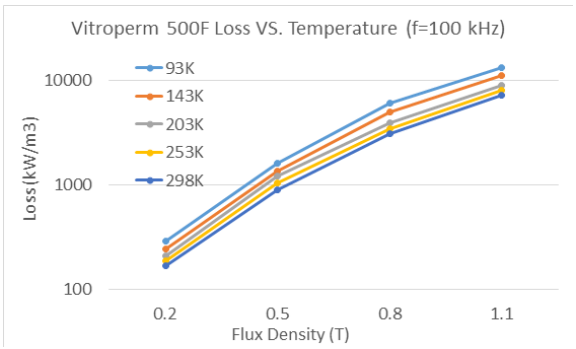
Fig. 7-6. Vitroperm 500F characteristics under operating point 0.5 T and 20 kHz.



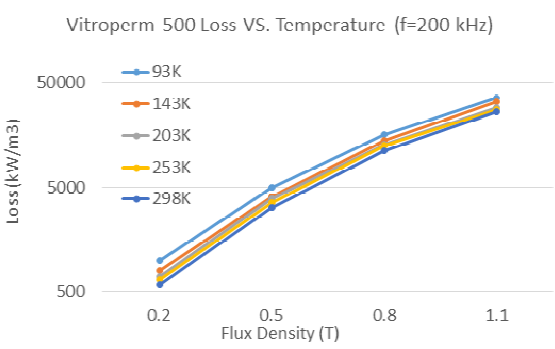
(a)



(b)



(c)



(d)

Fig. 7-7. Vitroperm 500F temperature dependent characteristics under different frequencies, (a) 20 kHz, (b) 70 kHz, (c) 100 KHz, (d) 200 kHz.

The saturation flux density B_s is identified based on B-H curve where the flux density does not increase when the exciting H field increases to a certain value. Fig. 7-8 shows the B-H curve of ferrite N87 at 20 kHz with a large exciting source applied at different low temperatures. Although the core is not fully saturated in the tested curve due to the limitation of the testing equipment, it can be predicted that the saturation flux density will slight increase when the temperature decreases from 298 K to 93 K, with a value around 0.4 T. Fig. 7-9 shows the B-H curves of the nanocrystalline Vitroperm 500F at 20 kHz under different temperatures. It is observed that the saturation flux density slightly increases in the range of 1.2 T~1.3 T when the temperature decreases from 298 K to 93 K.

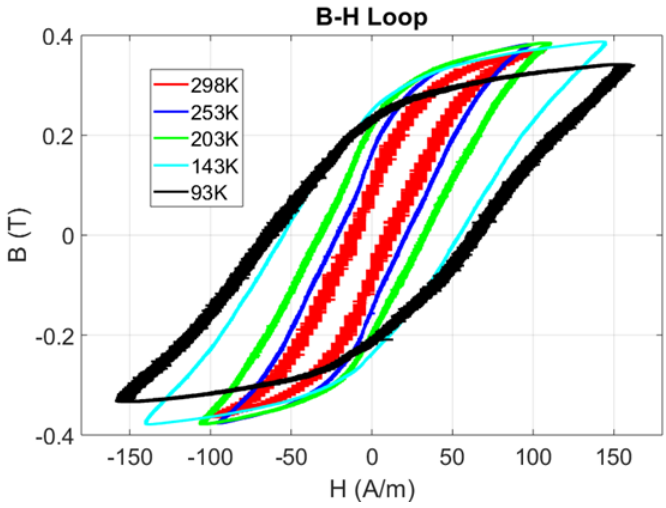


Fig. 7-8. Ferrite N87 saturation flux density dependence on temperature.

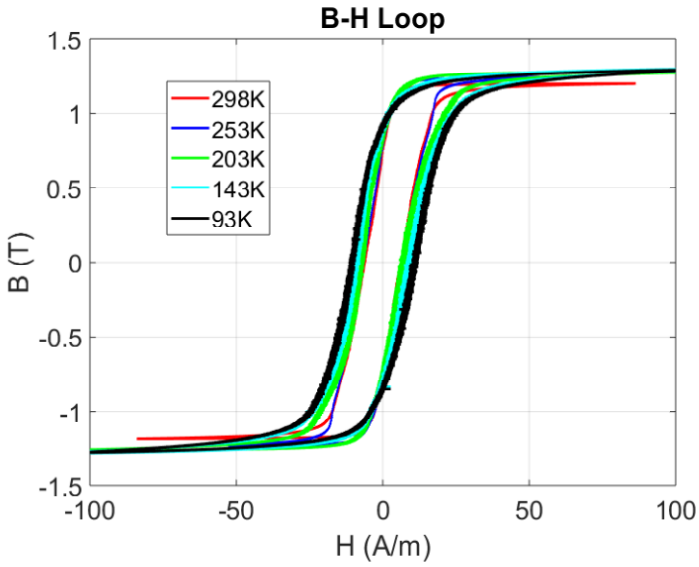
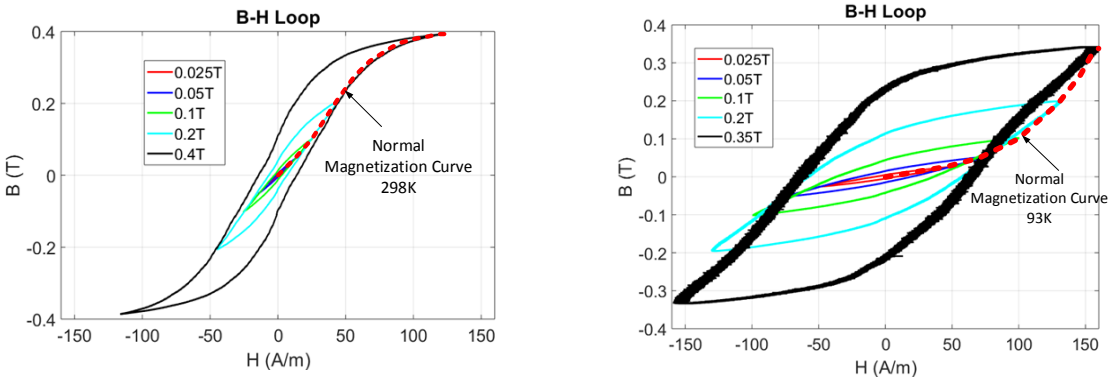


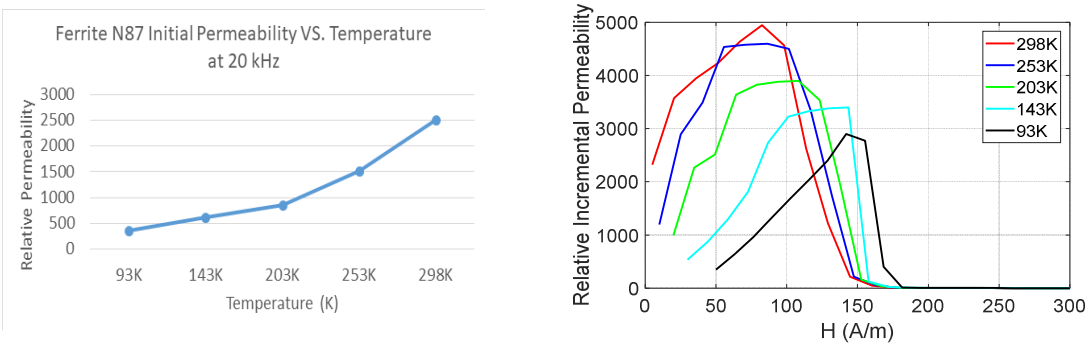
Fig. 7-9. Vitroperm 500F saturation flux density dependence on temperature.

Permeability can be assessed based on the B-H curve. As shown in Fig. 7-10, (Ferrite N87 B-H curve at 20 kHz), the dashed red curve (normal magnetization curve) consisting of all tips of the B-H curves clearly shows the magnetization scopes: first initial magnetization associated with low flux density below 0.025 T, then magnetization with a higher incremental permeability, and finally rotation magnetization before saturation. The initial permeability and incremental permeability can be calculated based on this curve. Fig. 7-11 summarizes the permeability of Ferrite N87 (both initial permeability and incremental permeability) dependence on temperatures. At room temperature (298K), the initial relative permeability is 2510, which matches the datasheet value 2200±25%. At cryogenic temperature (93 K), the initial permeability is 350, decreased by a factor of 7.2. Similarly, the incremental permeability also decreases as temperature decreases.



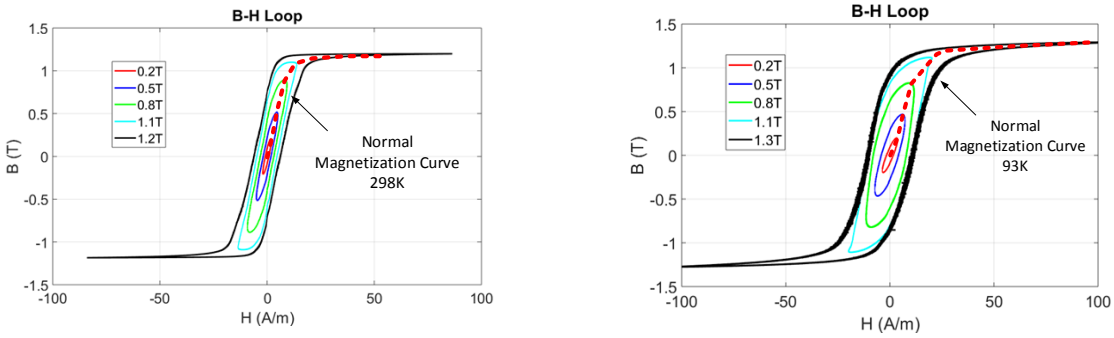
(a) Room temperature (b) 93 K

Fig. 7-10. Ferrite N87 B-H curve dependence on temp. with magnetization curve highlighted.



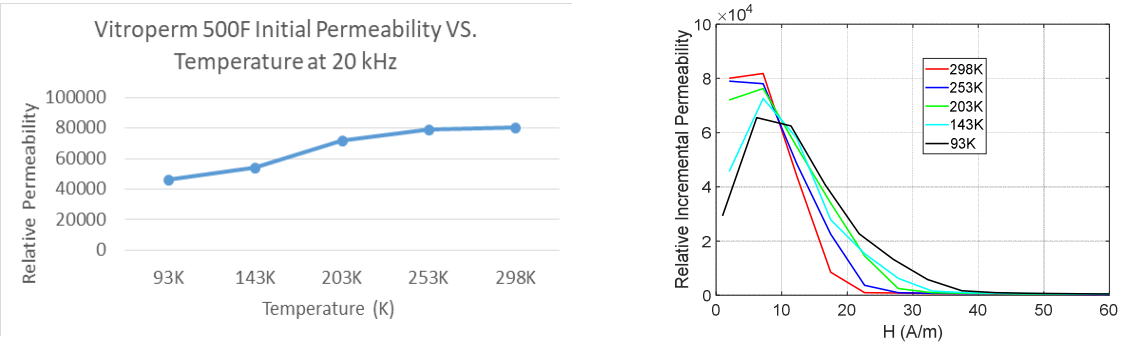
(a) Initial permeability (b) Incremental permeability curve

Fig. 7-11. Ferrite N87 permeability dependence on temperature at 20 kHz.



(a) Room temperature (b) 93 K

Fig. 7-12. Vitroperm 500F B-H curve dependence on temp. with magnetization curve highlighted.



(a) Initial permeability (b) Incremental permeability curve

Fig. 7-13. Vitroperm 500F permeability dependence on temperature at 20 kHz.

Similarly, for the nanocrystalline Vitroperm 500F material, the B-H curves with the magnetization curve under different temperatures are summarized in Fig. 7-12. Fig. 7-13 displays the permeability dependence on temperature for Vitroperm 500F. The initial permeability at 93 K decreases by 42% as compared to the value at room temperature. Also, the incremental permeability as a function of magnetic field strength H shows a similar trend to initial permeability when temperature decreases.

7.2 MW Three-Level Inverter System Design

7.2.1 Power Module Selection and Paralleling Strategy

Based on power device characterization results at cryogenic temperature, Si and GaN MOSFETs are the preferred candidates. However, no commercial available high current Si or GaN MOSFET modules exist in the market. Considering a MW-level inverter with 1 kV voltage and 1 kA current rating, tens of devices or converters need to be paralleled to deliver 1 MW power if using the discrete Si or GaN MOSFETs with tens of amps current capability, which makes this

approach not practical in real applications. Hence, high current SiC power module is selected for the 1 MW three-level inverter.

The latest Wolfspeed 900 V/ 800 A SiC power module is selected. Fig. 7-14 shows the module sample picture. The module static and dynamic characterization is conducted. Fig. 7-15 shows the on-state resistance versus temperature. The lowest on-state resistance is achieved at around 0°C. Fig. 7-16 shows the breakdown voltage trend versus the temperature. The breakdown voltage slightly increases as temperature decreases and keeps above 1 kV. Fig. 7-17 illustrates the switching transient waveforms at 500 V bus voltage and 760 A load condition with 1.3 Ω gate resistance. The maximum voltage of the upper MOSFET during turn on is 938 V while the maximum voltage of the lower MOSFET during turn off is 862 V. Fig. 7-18 summarizes the switching loss at different load conditions and comparison with datasheet.

To achieve 1 MW power, two converters need to be paralleled based on the selected module. Interleaving angle optimization discussed in the previous chapter is utilized for the two paralleled 500 kW inverters to reduce EMI noise.



Fig. 7-14. Wolfspeed 900 V/ 800 A high current power module.

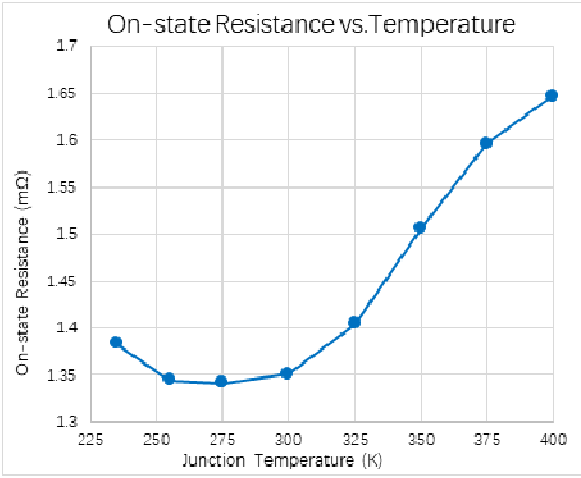


Fig. 7-15. On-state resistance versus temperature.

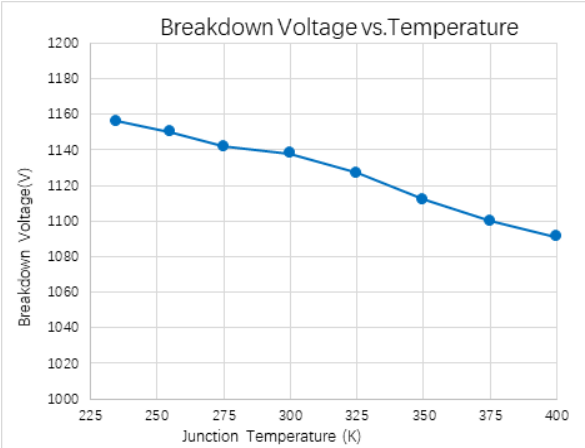


Fig. 7-16. Breakdown voltage versus temperature.

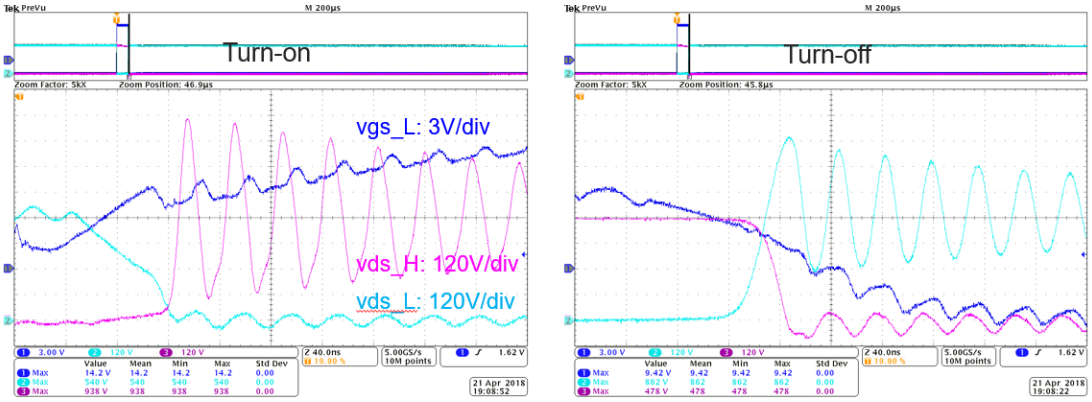


Fig. 7-17. Switching transient waveforms.

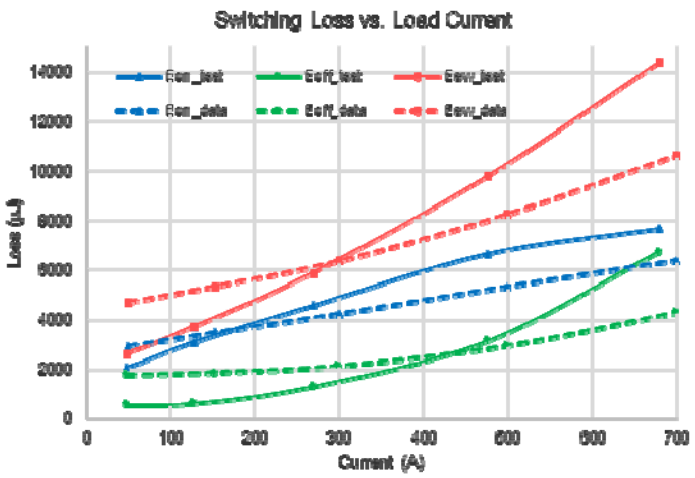


Fig. 7-18. Switching loss versus load.

7.2.2 Switching Loop Analysis and Busbar Design

The equivalent circuit of a single phase of the three-level ANPC inverter is illustrated as Fig. 7-19. Different busbars, parasitic inductances, and commutation loops are highlighted. Fig. 7-20 shows the operation scheme. There are two commutation loops for a three-level ANPC inverter. One commutation loop involves S_{1L} and S_{3L}, which is similar to a conventional loop in the two-level phase legs. The parasitic inductance resonates with the output capacitance of S_{1L} or S_{3L} depending on which one is the synchronous switch. The other commutation loop involves S_{3H}, S_{2H}, S_{2L}, and S_{1L}. Since S_{2L} and S_{3H} are in on state, S_{2H} is equivalently paralleled with S_{3L}. Hence, when S_{3L} is commutating with S_{1L}, the drain-source voltage of S_{2H} follows the drain-source voltage of S_{3L} although S_{2H} is a non-active switch during the half line cycle. The parasitic inductance resonates with the output capacitance of S_{2H}.

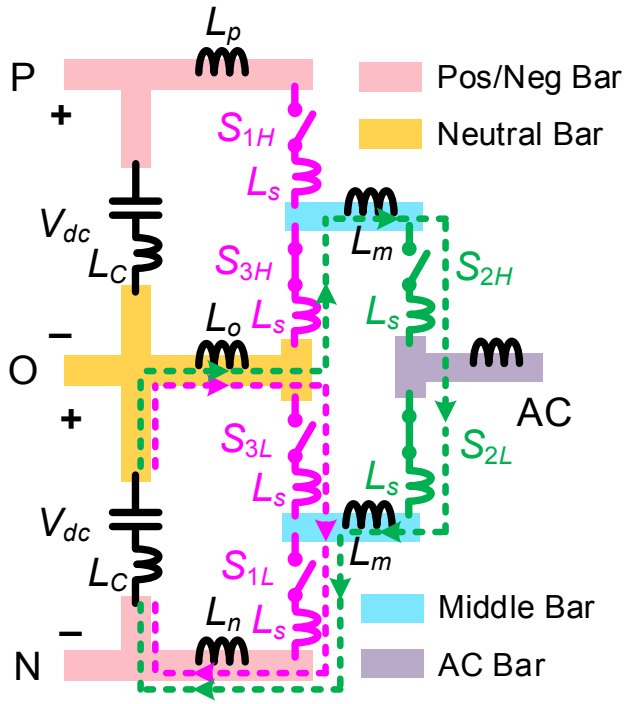


Fig. 7-19. A single phase of the three-level ANPC inverter with parasitic inductance.

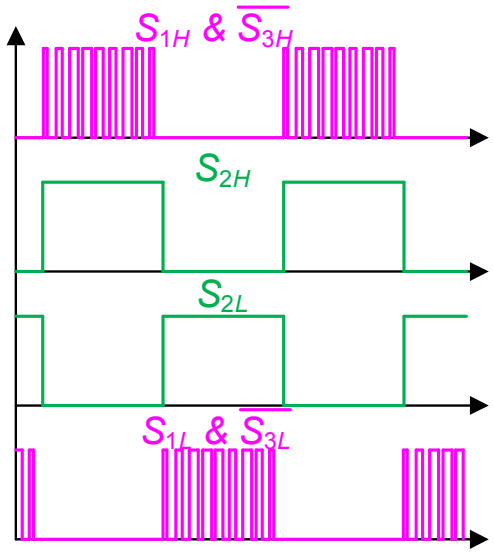


Fig. 7-20. Operation principle of the three-level ANPC inverter.

Busbar is the main source of the inductance in a commutation loop. To reduce the loop parasitic inductance, the magnetic cancelling principle must be followed and laminated busbar structure is used. The small commutation loop only involves the neutral busbar and the negative or positive busbar. The two parts should be laminated and put in two layers. The larger commutation loop consist of four busbar parts including the neutral busbar, negative busbar and two middle busbars. Considering the overall layout including the placement of power modules and capacitors, Fig. 7-21 shows the finalized busbar design for a single phase. The neutral busbar is a whole plate and serve as the return path of the commutation loop, and other busbars are in another layer. The busbar parts are coupled and the magnetic field can be canceled with the opposite current flowing direction, resulting in lower loop inductance. Fig. 7-22 shows the measured small and large loop impedance with the fabricated busbar prototype. The small and large loop inductance without the power module are 2.5 nH and 10 nH, respectively.

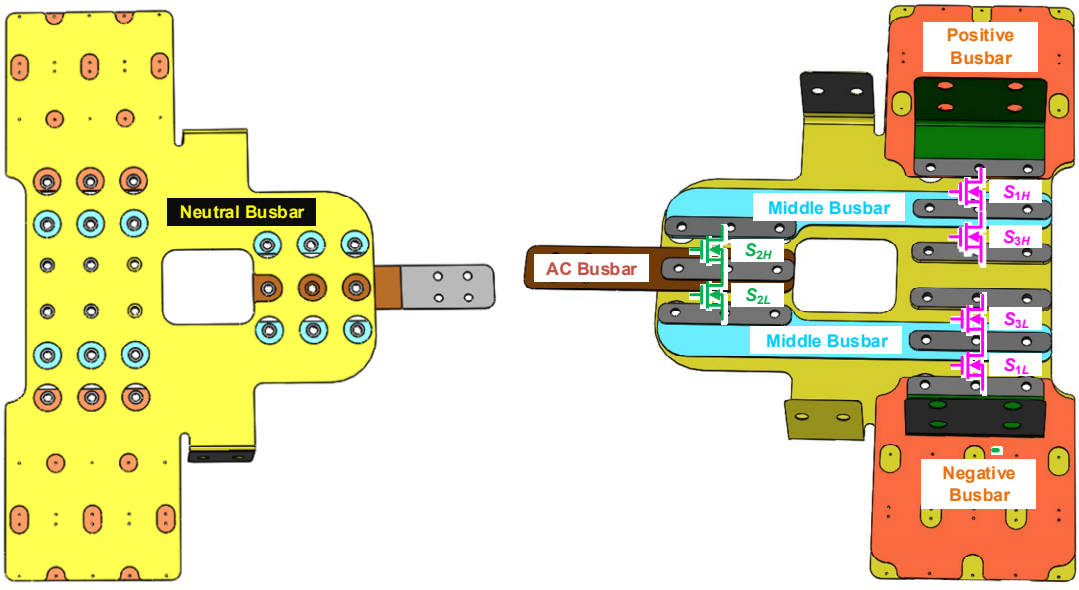


Fig. 7-21. Laminated busbar design for a single phase of three-level ANPC inverter.

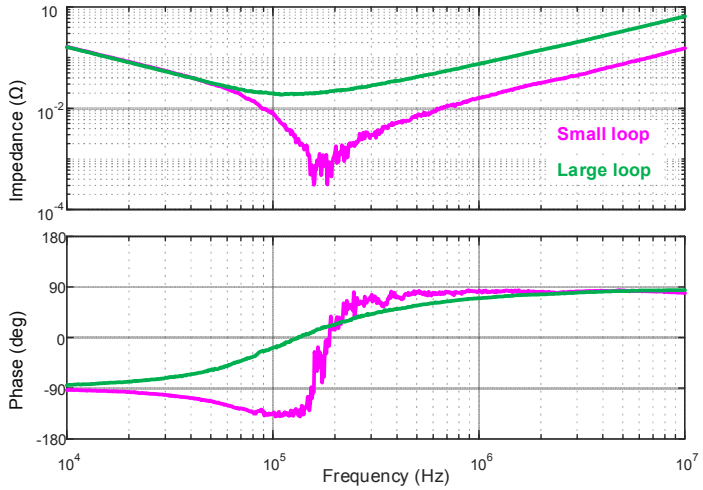


Fig. 7-22. Measure impedance of the busbar.

7.2.3 Controller Design

Controller which can support four paralleled inverter is designed. 1 DSP (TMS320C6748) +1 FPGA (Spartan-6) based control structure is selected. The control algorithm splits into calculation and modulation. DSP handles most of the computation while FPGA performs as a PWM generator. The function diagrams are shown in Fig. 7-23 and Fig. 7-24.

7.2.4 Filter Design

Filters in the MW inverter system consists of coupled inductors, CM filters and DM filters. To improve the inverter system power density, the switching frequency and interleaving angle are optimized, modulation strategy to reduce circulating current and CM voltage and switching loss is implemented, coupled inductor and CM inductor modeling and design optimization are also conducted. The details are illustrated in previous chapters and are not repeated here.

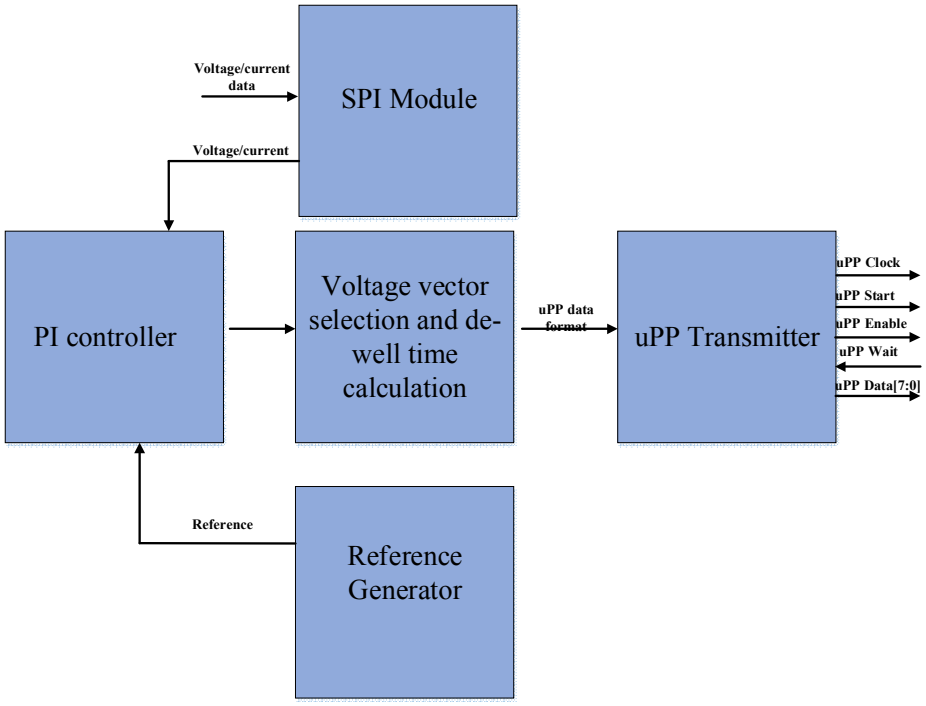


Fig. 7-23. Function diagram of DSP.

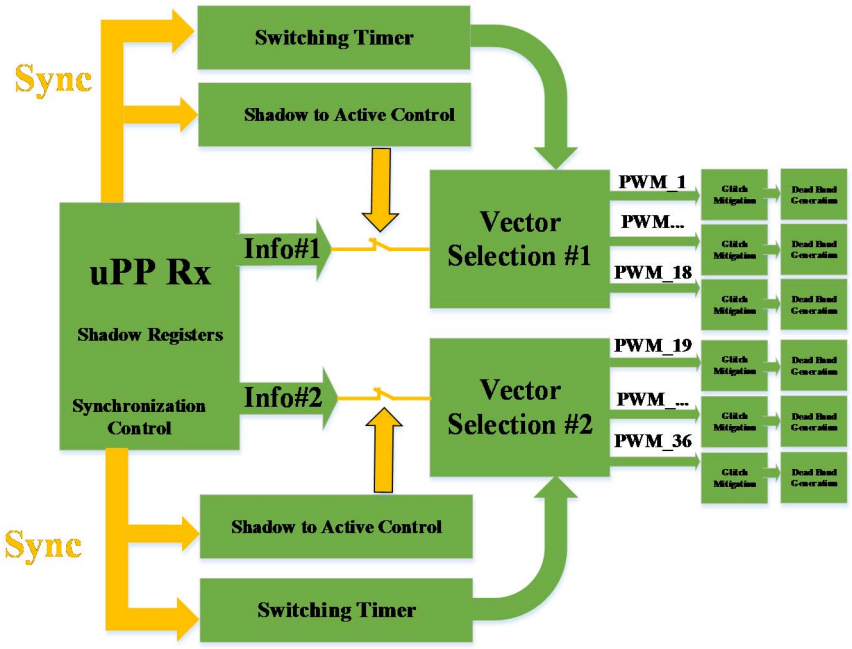


Fig. 7-24. Function diagram of FPGA.

Although magnetic cores show degraded performance in very low temperature, cryogenic cooling benefits the inductors windings due to a significant reduction in copper resistivity, allowing a decrease in weight and increase in efficiency. Based on their magnetic characterization results in low temperature, nanocrystalline material is selected for the coupled inductors and CM chokes in the system. The DM inductors use air core structure due to the relatively low inductance required and to maximize the benefit of cryogenic cooling. A unique feature of the inductors is the use of 3-D printed thermoplastic housing that accommodates liquid nitrogen cooling for the large inductors and reduce housing weight. The cooling of the inductor is tailored so that the windings are kept cold, while the core is at highest possible temperature of the inductor. Fig. 7-25 and Fig. 7-26 shows the housing structure of the coupled inductor and CM inductor, respectively.

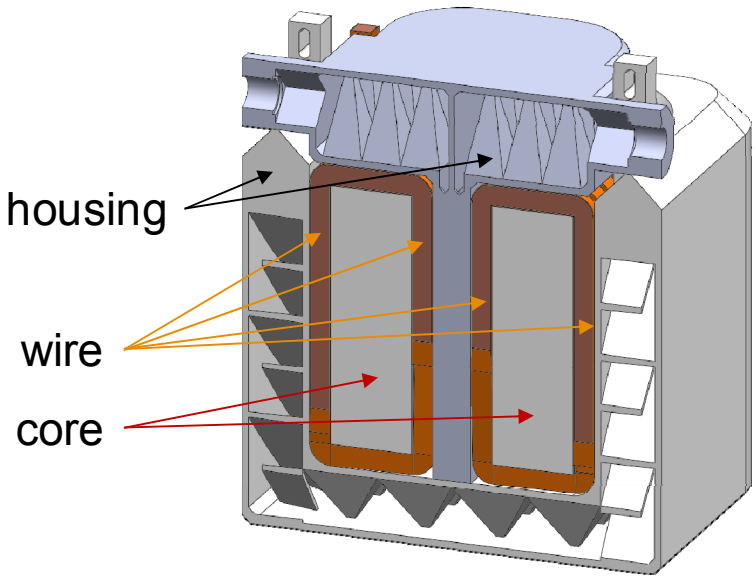


Fig. 7-25. Housing design of the coupled inductor.

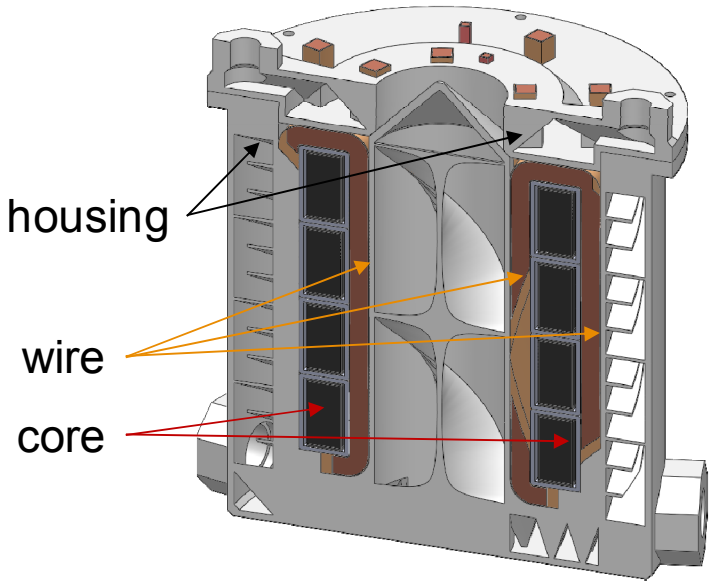


Fig. 7-26. Housing design of the CM inductor.

7.2.5 Cooling System Integration

As the SiC power module does not perform well at very low temperature, the power stage is cooled with cold gas nitrogen. The coldplate is especially design to fit the gas cooling and a temperature around 0°C is expected for half power operation point. The filters are cooled with liquid nitrogen. 3D printing based housing are designed for all the inductors. The housing is specially designed to accommodate liquid nitrogen and inductor heat dissipation requirement. Thermal insulation are also implemented. Fig. 7-27 shows the cooling for the inverter system. Fig. 7-28 shows the inverter system integration including the power stage, EMI filters, controller, cooling, connection bars, and enclosure [225].

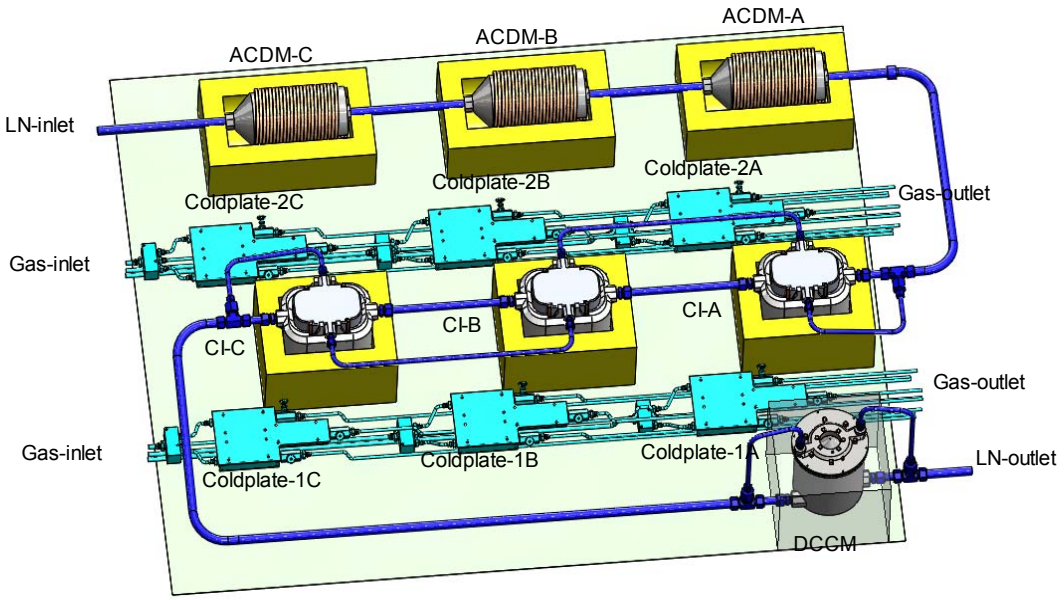


Fig. 7-27. Cooling of the inverter system.

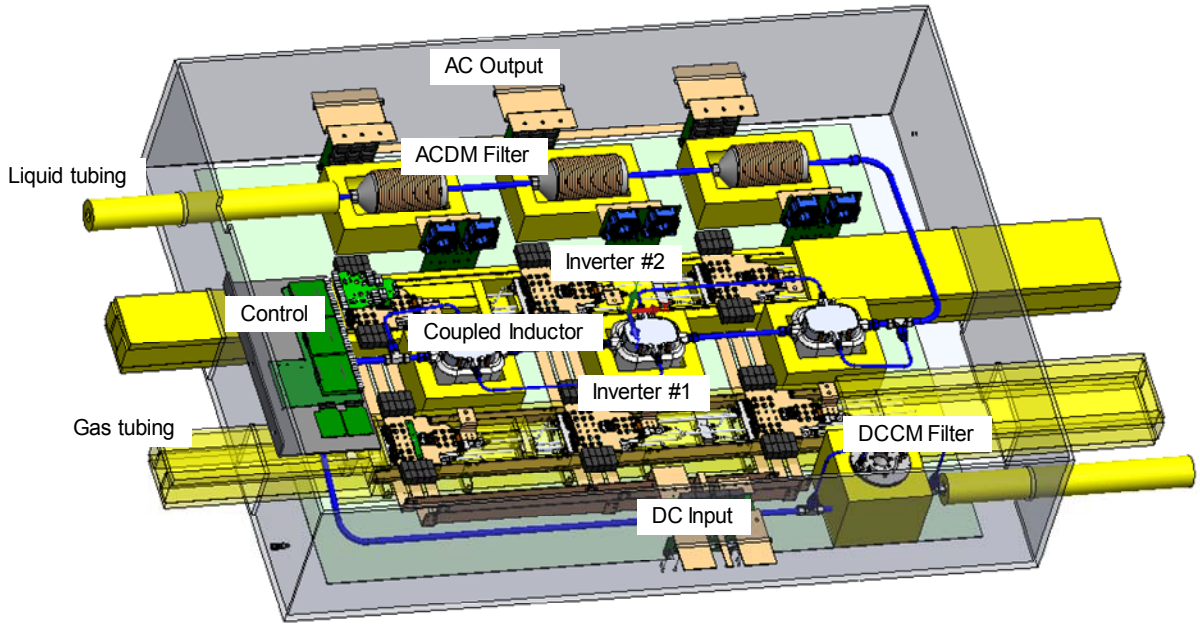


Fig. 7-28. Inverter system integration.

7.3 MW Three-Level Inverter System Testing

7.3.1 Hardware

The 1 MW inverter system was fabricated. Fig. 7-29 shows one single phase of the inverter prototype including the power modules, busbars, dc-link capacitors, gate drive circuits, and isolated power supply. Fig. 7-30 shows the controller hardware including a DSP-FPGA core board, communication units, voltage/current sampling circuits and ADC, and fiber optic boards. Fig. 7-31 and Fig. 7-32 shows the coupled inductor and CM inductor prototypes with 3D printing housing, respectively. Fig. 7-33 shows the fabricated inverter prototype inside the enclosure.

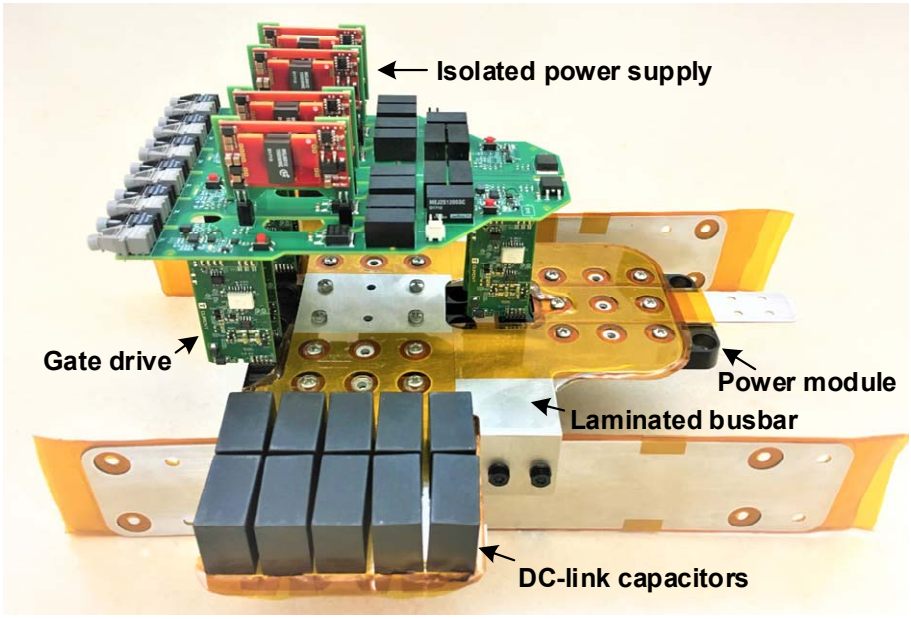


Fig. 7-29. A single phase of the three-level ANPC inverter prototype.

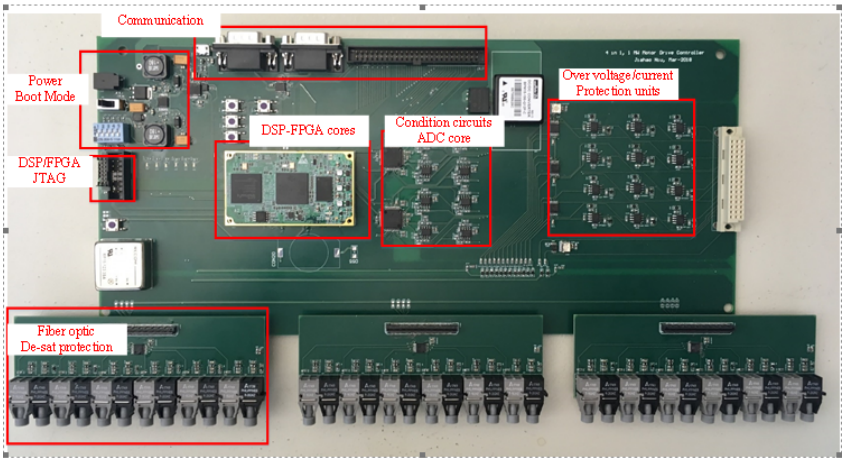


Fig. 7-30. Controller hardware.

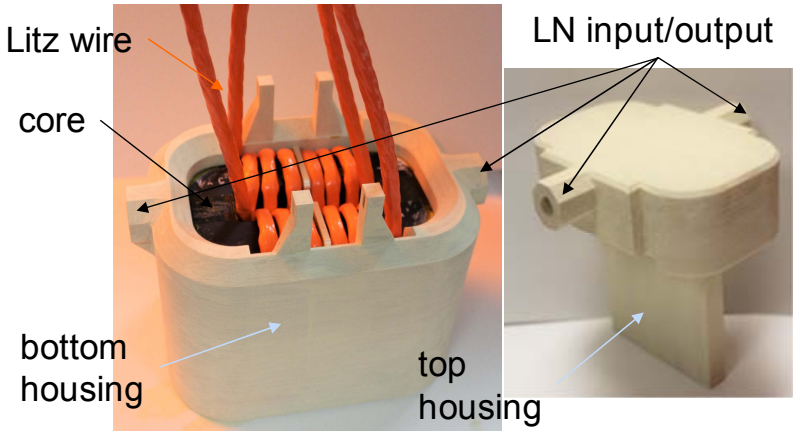


Fig. 7-31. Coupled inductor with 3D printing housing.

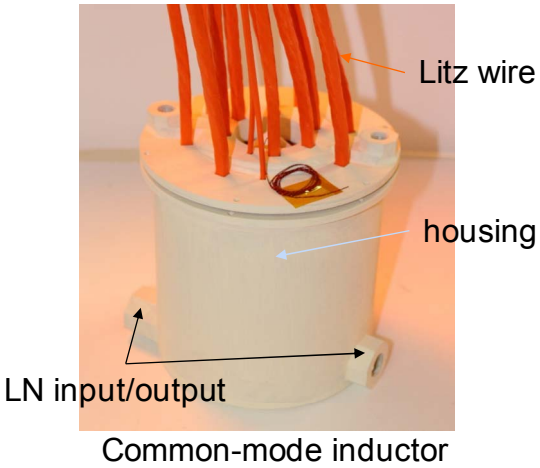


Fig. 7-32. CM inductor with 3D printing housing.

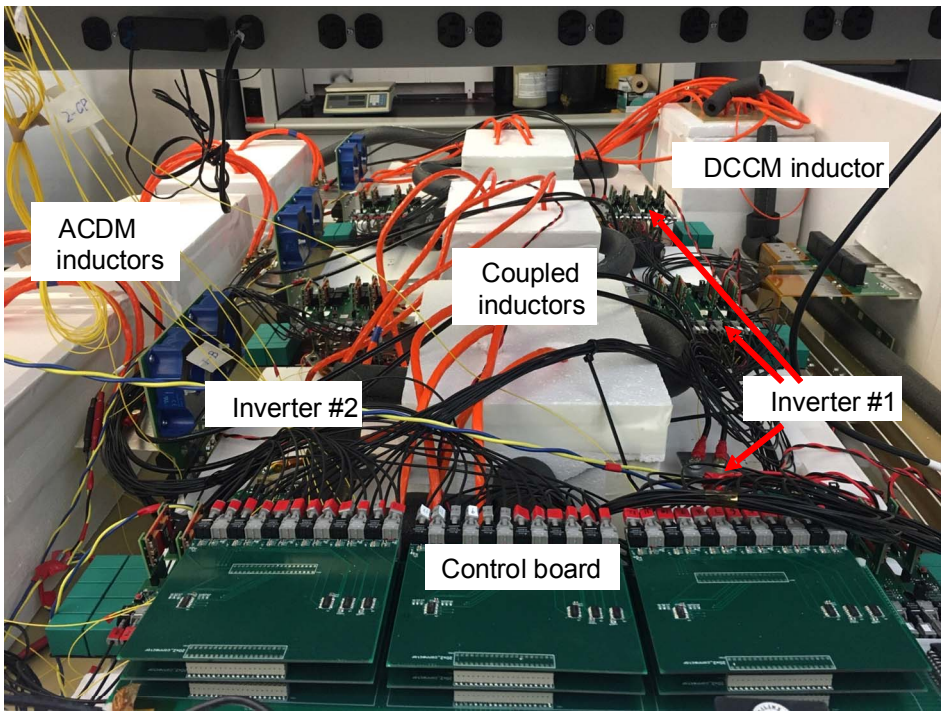


Fig. 7-33. The inverter system.

7.3.2 Function Verification

Fig. 7-34 and Fig. 7-35 shows the pulse test results of one inverter at rated voltage and current level. Fig. 7-36 shows the continuous power test waveforms at room temperature.

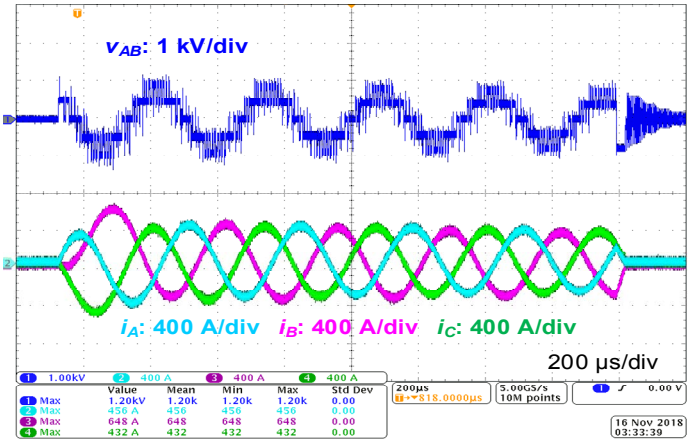


Fig. 7-34. Pulse test – output voltage and current waveforms.

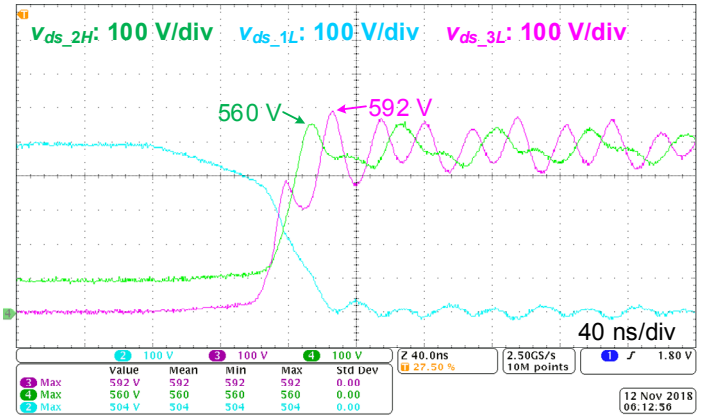


Fig. 7-35. Pulse test – switching transient waveforms.

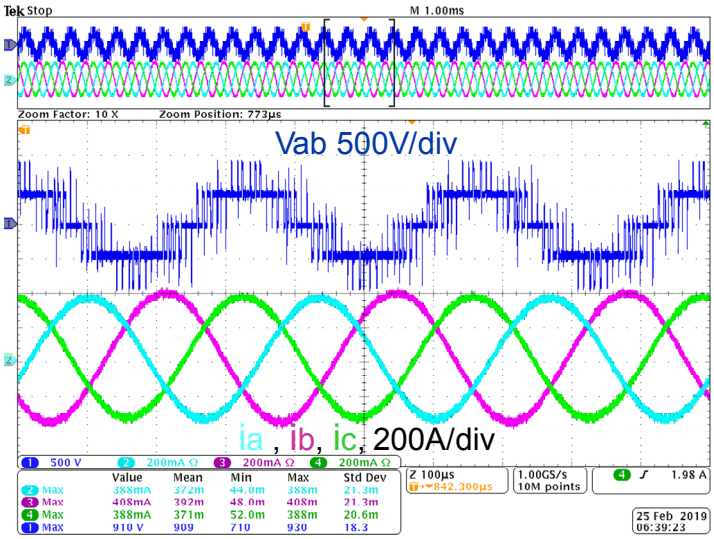


Fig. 7-36. Continuous power test – output voltage and current waveforms.

Fig. 7-37 show the phase voltages of the two parallel interleaved inverters with 60° interleaving angles. Fig. 7-38 shows the CM EMI noise current comparison with 0° and 60° interleaving angle. The 60° interleaving angle results in significantly reduced 3rd and 4th order switching harmonics when compared to a 0° interleaving angle. Fig. 7-39 shows the three phase currents of one inverter and one phase current of the second inverter. From Fig. 7-39, the Ia1 and Ia2 current waveforms overlap with each other, which indicate a good load sharing between the two inverters.

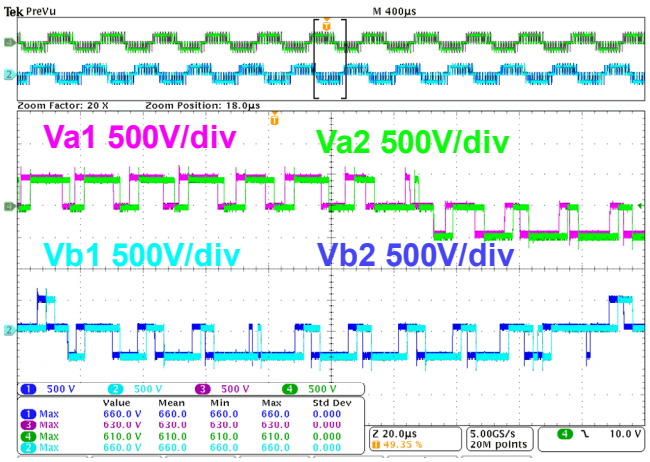


Fig. 7-37. Phase voltages of two 60° interleaved inverters.

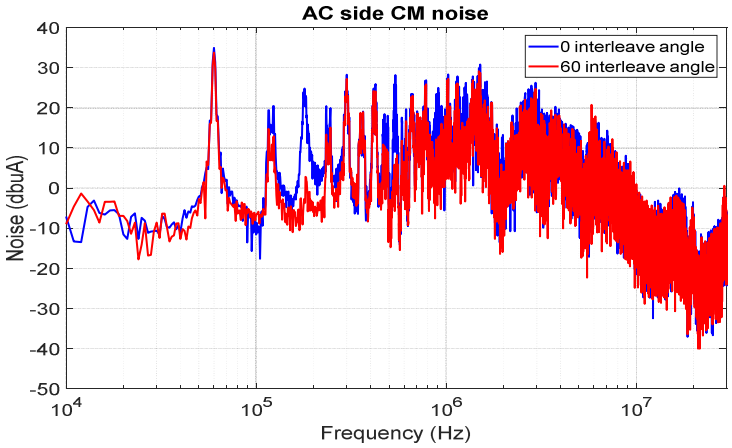


Fig. 7-38. CM EMI noise comparison with 0° and 60° interleaving angles.

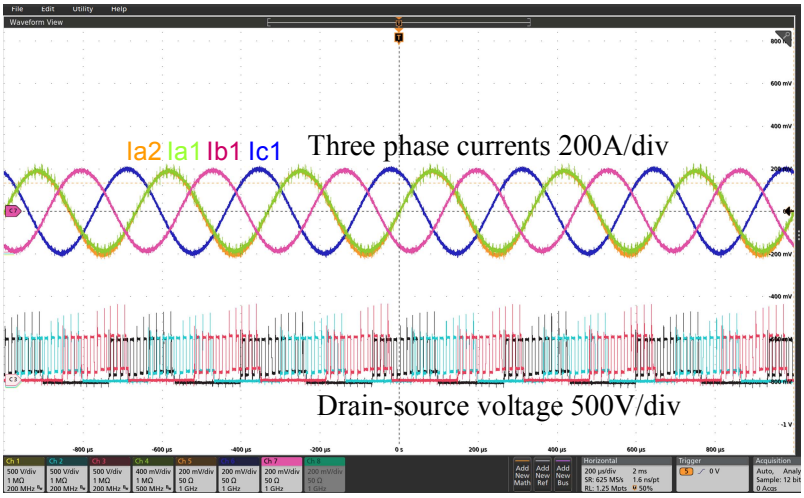


Fig. 7-39. Output currents of two paralleled inverters.

7.3.3 Cryogenic Temperature Testing

As discussed, the EMI filter is cooled with liquid nitrogen, and the cooling channels are presented in Fig. 7-27. The implementation is straightforward. The power stage is cooled with cold gas nitrogen. Fig. 7-40 shows the cooling concept. The room temperature gas nitrogen will go through coils which are submerged into a liquid nitrogen bucket. By adjusting the height of the jack, the number of turns of the coils that are submerged into liquid nitrogen can be adjusted. The cooling performance of the gas nitrogen system can be controlled by adjusting the flow rate of the gas through a regulator combined with adjusting the number of coils turns submerged into the liquid nitrogen. Fig. 7-41 shows the cooling system setup.

The inverter system is tested with cryogenic cooling. Fig. 7-42 shows the voltage and current waveforms of one inverter. The three phase currents are measured with Rogowski coils and the peak current is 520 A. The measured temperature of power modules in three phases and the cold plate are 52°C, 49°C, 45°C, and 34°C, respectively. By increasing the gas nitrogen flow rate, the power module temperature can be further reduced for efficiency optimization.

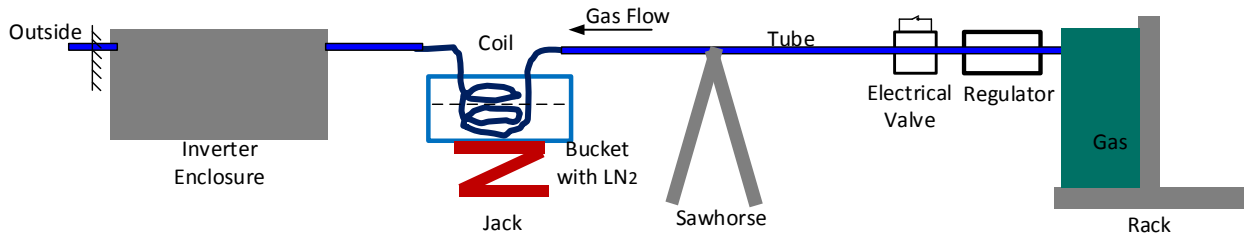


Fig. 7-40. Power stage cooling concept.

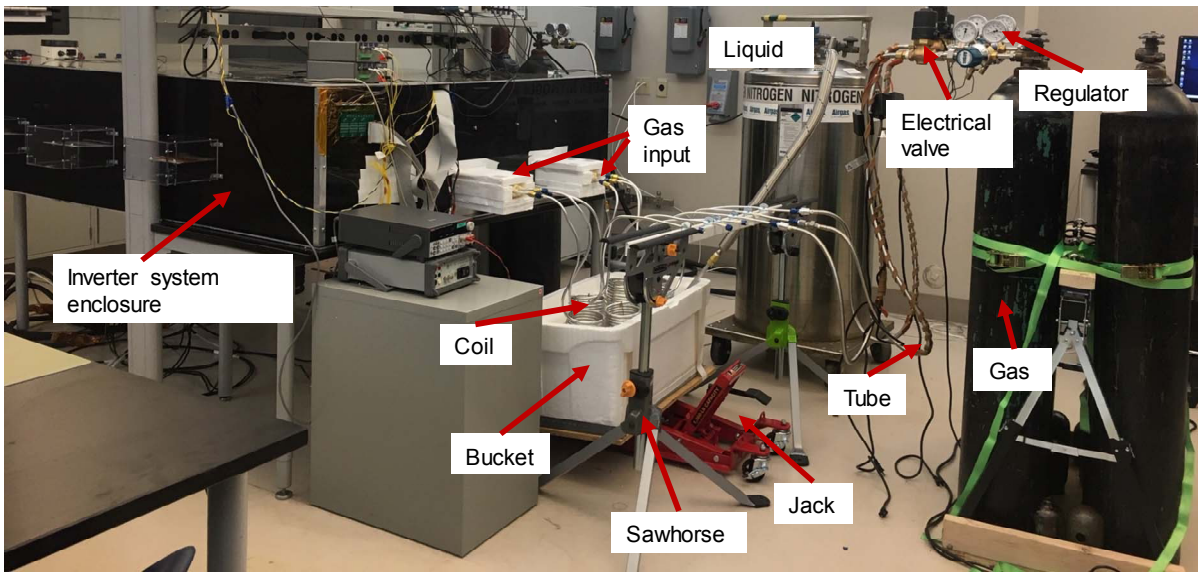


Fig. 7-41. Cooling system setup.

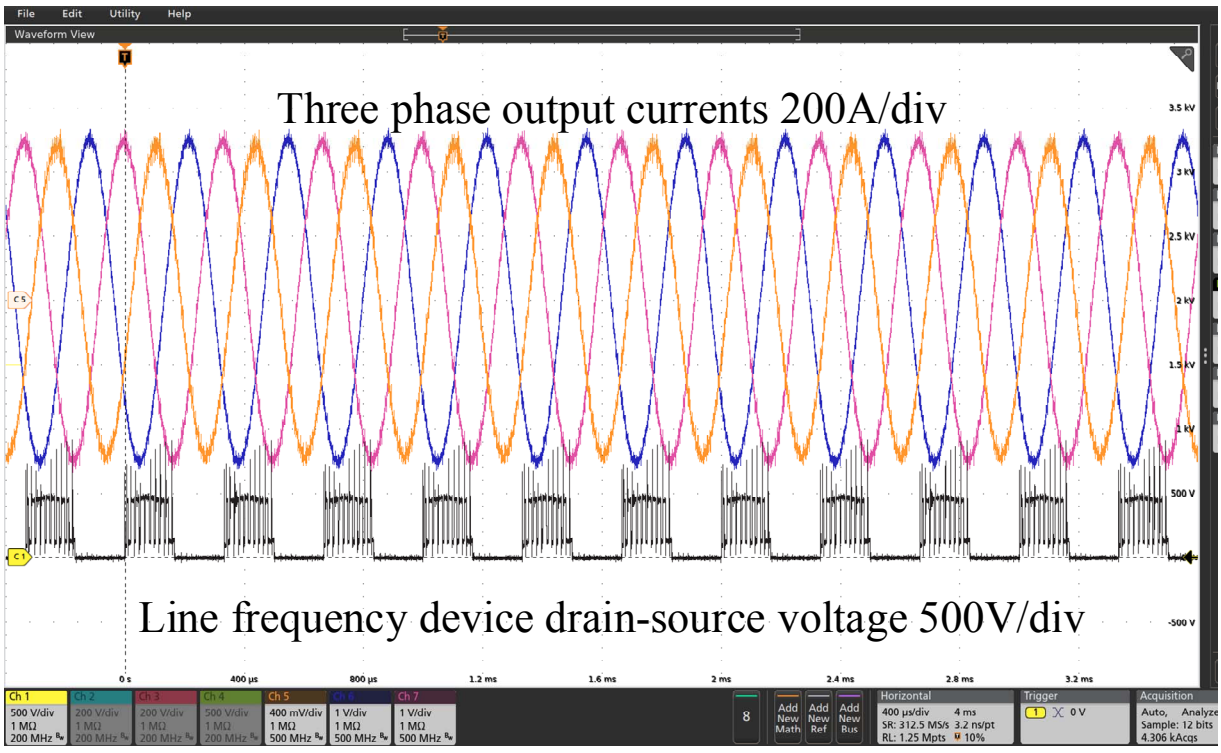


Fig. 7-42. Voltage and current waveforms.

7.4 Conclusion

This chapter presents the design and demonstration of a 1 MW three-level inverter with cryogenic cooling. First, the state-of-the-art power devices and magnetics are comprehensively characterized at cryogenic temperature. In general, the silicon and GaN MOSFETs have improved performance (lower on-stage resistance and faster switching speed) at low temperature and are the promising candidates for cryogenic applications while SiC MOSFETs have degraded performance (increased on-state resistance and switching loss) at very low temperature. Both ferrite and nanocrystalline magnetic materials have degraded performance (increased core loss and decreased permeability) at very low temperature while the conductors (for winding and busbar) have significantly reduced resistivity at low temperature. Second, due to the lack of silicon or GaN based high current modules in the market, SiC power module is selected for the 1 MW inverter design. Two 500 kW three-level ANPC inverters are paralleled to achieve 1 MW power delivery. The inverter design including the power stage, controller, filters and cooling integration to fit cryogenic cooling and achieve high power density are illustrated. Third, a MW three-level inverter prototype with the cryogenic cooling system has been built. Experimental results are demonstrated and verify the functionality of the inverter.

8. Conclusion and Future Work

8.1 Conclusion

This dissertation studies the three-level inverter for aircraft application. The research focuses on design of high power density three-level inverter emphasizing on passive reduction through novel modulation and control, paralleling and interleaving strategy, filter modeling and design optimization. The conclusions can be drawn as follows.

- Analytical models for harmonic calculation of three-level NPC inverter with SVM are developed, and the unique dc current harmonics characteristic of the NPC inverter are identified. Accuracy of the models are experimentally verified. The optimal interleaving angle to reduce dc-link capacitor high frequency current ripple is derived and experimentally verified, which is highly dependent on power factor and modulation index and different from the two-level inverter case. For example, at high modulation index, optimal interleaving angle range is around 180° and around 90° for high power factor and low power factor, respectively. The optimal interleaving angle ranges for CM and DM filter corner frequency are also derived and experimentally verified, which is highly dependent on switching frequency. For example, with 60 kHz switching frequency and impedance resonance well damped, around 180° and 30°~90° interleaving angle ranges are preferred for CM filter, and 30°~60° and 120°~180° interleaving angle ranges are preferred for DM filter.
- To improve inverter system power density, a space vector modulation is proposed for paralleled three-level inverters to reduce common-mode voltage and switching loss in addition to suppress the low frequency circulating current. The proposed modulation has adjustable AZSV in every switching cycle, and thus ZSCC control can be achieved. The proposed

modulation only uses vectors with a CMV magnitude equal to or smaller than $V_{dc}/6$. Hence, the CMV is reduced to half of conventional modulations. When ZSCC is small and within the defined limit, the proposed modulation is the same as CMR modulation, and switching action is eight times for two paralleled inverters. When ZSCC exceeds the limit, even for the worst case that the fourth vector regulates in every switching cycle, the switching action is ten times for two inverters. Therefore, switching loss is reduced compared to conventional modulations which have twelve switching actions for two inverters.

- To reduce the coupled inductor size and weight, a carrier based PWM method to achieve minimum flux linkage for the coupled inverter in interleaved three-level inverters is proposed. This modulation method is realized by injecting an optimal zero sequence offset to the sinusoidal modulation. The optimal zero sequence offset is made up by several zero sequence candidates and is a function of modulation index. The proposed modulation method has the capability to balance the neutral point voltage for a three-level NPC inverter. The proposed modulation method is compared with other popular carrier based and space vector based PWM methods for three-level inverters. When the modulation index is low, the flux linkage of the proposed modulation is reduced to around 50% of that of DPWM, NTSV and CMR methods, and to around 80% of that of SPWM. When modulation index is high, the maximum flux linkage of the proposed modulation is reduced to around 60% of the flux linkage of other modulation methods. The proposed modulation method has similar loss and THD characteristics as other continuous PWM methods.
- To reduce EMI noise and thus reduce the required EMI filter, the inverter and filter topology for common-mode noise reduction in a three-level inverter is investigated. First, the fourth-leg strategy is applied to the three-level inverter fed motor drive for CM noise reduction.

Unlike the case in two-level inverters, the nearest three vectors can be maintained to synthesize the reference while zero CMV can be achieved at the same time. Experiments conducted on a three-level NPC inverter show that with the fourth-leg and presented modulation scheme applied, the CM noise has been significantly reduced, and ~25 dB attenuation can be observed at the first noise peak in the EMI frequency range. Second, an impedance balancing circuit is proposed for motor drive where both the dc source side and ac motor side need to meet EMI standards and require EMI filters. The CM noise reduction performance of the proposed method does not depend on motor and cable models. Experiment results shows that both the ac and dc side can achieve 10~20 dB CM noise attenuation in the 150 kHz to 1 MHz frequency range. The required CM inductance of the conventional ac side CM inductor is significantly reduced from 3.43 mH to 500 uH in the experiment.

- To reduce the required filters, CM inductor flux density modeling, analysis, and filter design optimization is conducted for three-level inverter. First, the spectrum concept is introduced for CM inductor core saturation analysis and design optimization. Three components in the CM inductor which may cause large CM flux density and core saturation are summarized: switching frequency related components, impedance resonance frequency related components, and modulation frequency related components. Each component is investigated for CM flux density reduction and filter design optimization. Second, the CM flux density calculation model has been developed. The impact of modulation index, dead time, NP voltage variation, and CM inductor value on the maximum CM inductor flux density are comprehensively analyzed. The maximum CM flux density has a non-monotonous relationship with modulation index, and the worst case does not occur at full load or minimum load condition. The impact of dead time on maximum CM flux density is highly dependent on modulation index. When

modulation index is high, larger dead time results in higher maximum flux density. When modulation index is low, larger dead time leads to lower maximum flux density. The impact of NP voltage variation on CM current and CM flux density of the CM inductor can be neglected due to the low parasitic capacitance in motor drive systems and the negligible impact of NP voltage variation on switching frequency related components of CM voltage. The CM inductor value largely impacts the maximum flux density. In some cases, increasing the CM inductor value could reduce the dominant switching harmonic of the CM current. Based on the CM inductor flux density analysis, an improved CM filter design procedure is proposed to avoid over-design or under-design of the CM inductor.

- The design and demonstration of a MW three-level inverter with cryogenic cooling is presented, which provides guidance for high power three-level inverter design and cryogenic power converter. In general, the Si and GaN MOSFETs have improved performance (lower on-stage resistance and faster switching speed) at low temperature and are promising candidates for cryogenic applications while SiC MOSFETs have degraded performance (increased on-state resistance and switching loss) at very low temperature. Both ferrite and nanocrystalline magnetic materials have degraded performance (increased core loss and decreased permeability) at very low temperature while the conductors (for winding and busbar) have significantly reduced resistivity at low temperature. The inverter design including the power stage, controller, filters, and cooling integration to fit cryogenic cooling and achieve high power density is illustrated and experimentally verified.

8.2 Publication List

- R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and

B. B. Choi, "Modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level neutral point clamped inverters with space vector modulation," *IEEE Trans. Power Electron.*, 2019, early access.

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8.3 Future Work

The recommended future work is drawn as follows.

- Comprehensive filter modeling and design optimization

Although EMI filters have been well adopted in most power electronic system, the design is usually based on ideal filter components and the design result is usually inaccurate or not optimized. The non-ideality in filter components such as frequency dependent permeability of nanocrystalline magnetic for CM inductors, current dependent permeability of powder core for DM inductors, coupling and parasitic effect between filter components, core saturation impact on inductance and noise attenuation performance needs to be further modeled and should be integrated to the filter design procedure.

- Multi-interleaved multilevel inverter topology

Increasing switching frequency is an effective way to reduce passives in an inverter system. Although the emerging of wide bandgap semiconductor devices significantly increases the switching frequency of power electronic converters, the switching frequency of inverter which has a power rating of hundreds of kilowatts or megawatts can only operate at tens of kilohertz with state of the art technologies.

To further increase the equivalent switching frequency at the input and output terminals of an inverter, Multi-interleaved multilevel inverter topology is a promising candidate. Both multilevel topology and interleaving topology result in increased equivalent switching frequency. Moreover, with multilevel topology, the required voltage rating of individual device is reduced, which enables more freedom in device selection. With the same current rating, usually the device with lower breakdown voltage has lower on-state resistance and faster switching speed, which helps to further increase switching frequency. With multi-paralleling topology, the current rating of the individual

inverter is also reduced, due to reduced di/dt, the switching frequency of individual inverter can also be further increased.

- Power inverter design to maximize the benefit of cryogenic cooling

Based on power semiconductor device characterization results presented in this dissertation, GaN MOSFETs have significantly reduced on-state resistance and switching loss at cryogenic temperatures. Thus, GaN based inverter with cryogenic cooling is a promising candidate to enable high switching frequency and achieve high power density.

Current source inverter has the inherent advantage of easier to be paralleled. With cryogenic cooling, superconducting coils can be applied and significantly reduce the size and weight of the bulky dc side inductors that required for current source inverter. Thus, multi-interleaving current source inverters with cryogenic cooling is also a promising candidate to achieve high power density.

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