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UWB Precise Indoor Localization System Performance, Limitations and its Integration

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UWB Precise Indoor Localization System Performance, Limitations and its Integration

A Dissertation Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

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Abstract

An indoor localization system that was built at University of Tennessee is extensively studied and improved. The goal of the system is to achieve mm down to sub-mm accuracy/precision.

Sub-sampling is used to alleviate the high sampling rate required for UWB signals. Current commercial direct sampling systems are still too slow or prohibitively expensive for UWB applications. We developed two different sub-sampling techniques, but the two systems suffer numerous shortcomings: low throughput, non-robustness, non-linearity. A third system is introduced that achieve both high accuracy and high through-put. Changes in the detection algorithm and the frame synchronization are developed to accommodate the new scheme.

We present our efforts to replace hybrid components by recently developed MMIC chips, and an integrated digital module developed by ULM University and UT respectively. Similar localization performance was achieved but rather with significantly reduced power consumption, much smaller footprints, and higher throughput.

Step Recovery Diode (SRD) based UWB pulse generators suffer from jitter caused by AM-to-PM conversion, SRD shot noise and clock jitter. A mathematical model for simulation of the jitter and amplitude variation effect in the equivalent time sampling technique has been developed and used in SystemVue simulations. A criterion as an estimate of system accuracy is defined as Signal to Distortion Ratio (SDR) and used. Similarly, a model for AM and PM noise analysis for an SRD based UWB pulse generator is developed that was validated experimentally.

We estimate the achievable system localization error. A mathematical model and simulation platform are developed to describe its behavior. Limits on the location accuracy as a function of the parameters of the UWB system are described. A discussion of the dominant reasons for errors that include picoseconds pulsar jitter, sampling clock jitter, sampling rate, and system additive white Gaussian noise (AWGN) is presented. We show a simple method to calculate the total system jitter, and describe error biasing phenomenon as the tag moves approaching one base-station and distancing another. Design curves are provided to determine the specifications of system components to achieve a certain positioning accuracy.

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Nomenclature

AWG	Additive White Gaussian
CMOS	Complementary Metal Oxide Semi-conductor field effect transistor
FFT	Fast Fourier Transform
FMCW	Frequency Modulation Continuous Wave
GCPW	Grounded Co-Planar Waveguide
GPS	Global Positioning System
HBT	Hetrojunction Bipolar Transistor
OCXO	Oven Compensated Crystal Oscillator
PRF	Pulse Repetition Frequency
RFID	Radio Frequency Identification
RMS	Root Mean Square
Si-Ge	Silicon Germanium
TCXO	Temperature Compensated Crystal Oscillator
TDoA	Time Difference of Arrival
TW-ToF	Two Way - Time of Flight
UWB	Ultra Wide Band

Chapter 1

Introduction

Localization and Tracking systems have added greatly to the prosperity and advancement of humans. Outdoor localization system i.e. GPS is used in our daily life and for copious of application ranging from maritime navigation to missile guidance. GPS satellites triangulate position by measuring time delays via precise time atomic clocks.

Indoor localizations systems are developed to complement the GPS-like systems where satellites signal is not present. It finds applications in businesses, hospitals, and manufacturing facilities. Store navigation, targeted advertisement, airport maps, and assets tracking are examples of current and potential utilization of indoor localization. Definitely, RFID market is developing fast for more accurate, reliable, and real-time localization systems to track people and assets.

Indoor precise localization systems, i.e. sub-mm to mm, as well are indispensable for high demanding operations e.g. robotics surgery, positron emission tomography, precise machining, etc...

1.1 Overview of Indoor Localization Technologies

The world demand for accurate, real-time, robust, and reliable indoor system augment year after year. A survey of indoor commercial and research-oriented positioning

systems are introduced in [1]. The author shows different localization technologies i.e. Infra-Red, ultra-sound, RFID, WLAN, Blue-tooth, UWB, and magnetic technology. He also discusses techniques to locate objects i.e. triangulation, fingerprinting, proximity, and vision analysis. Triangulation can be performed in three methods i.e. received signal strength, angle of arrival, and time of arrival. Moreover, he addresses the criteria used to assess indoor localization systems i.e. security and privacy, cost, performance, robustness, complexity, user preferences, commercial availability, and limitations.

The most common triangulation methods are ToA, RSS, and AoA. ToA is the most accurate, it can filter out multi-path received signals, however, it is more complex to implement. ToA and RSS require three reference elements while AoA requires only two. AoA though may contain large errors for far object positioning.

1.2 UWB Positioning Systems at University of Tennessee

At UT we have a system that uses TDoA of a UWB pulse received by at least four synchronized base-stations for 3D localization to locate a wireless non-synchronized tag. In TDoA we use the difference in arrival time at one reference base-station and all the remaining base-stations to triangulate the tag position to avoid the need to synchronize the wireless tag. The tag generates a 300 ps pulse that modulates a 8 GHz carrier.

The major strength of UWB pulse-based signal is that it requires less power since it operates in a small fraction of time, the ability to exist side-by-side with the narrow band signals, and the immunity to multi-path interference because of its short temporal existence.

UWB system accuracy is less than IR-based systems. At UT we were able to reach 2-5 mm 3D accuracy. The system is explained in more details in Chapter 7.

Table 1.1: Comparison of Different Technology Products [1]

System Name	Technology	Security	Cost	Performance	Robustness	Complexity	Limitations
Firefly[7]	Infrared	No	controller+32 tags \$27,500	Error <3.0mm; high throughput	influence from light source	Low	Scope within 7m
OPTOTRAK[8]	Infrared	No	Expensive	Accuracy of 0.1 to 0.5 mm 95%	Line of sight req.	Low	Limited coverage area
Criquet[9]	Ultrasound	Yes	Cheap	Accuracy of 10 cm	Good	Low	tag battery
Sonitor[10]	Ultrasound	No	Inexpensive	Room level accuracy	Non line of sight	Numerous detectors	No absolute position measurements
WhereNet[11]	RFID	No	Not Cheap	Error 2 to 3m; Rate 5s to 1h	-	Complex	Accuracy not good enough
COMPASS[12]	WLAN	No	Inexpensive	Accuracy 1.65 m	Considers human body effects	Reuses WLAN infrastructure	No real-time tracking
Topaz[13]	Bluetooth	No	HIGH	2 to 3 m	-	Many APs	calculate position 10 s
Ubisense[2]	UWB	No	4 sensors+ 5 tags \$18,354	Accuracy 1 cm	Good	Low; 4 sensors cover 400m ²	Price is high
MotionStar[14]	Magnetic	No	Expensive	Accuracy 1 cm	Influenced by metal elements	Small coverage area	not scalable; Short rang
Easy Living[15]	Vision based	No	Inexpensive stereo cameras	Accuracy cannot be gauranteed	not reliable in dynamic environment	Low; 2 cameras cover a room	req. substantial processing power
Beep[16]	Audible sound	Yes	Inexpensive	Accuracy 0.4 cm 90%	Influenced by sound sources	Low	-

1.3 Objectives

The purpose of our work is to build a mm down to sub-mm accuracy localization pulse based UWB indoor system. There are different factors contributing to the inaccuracy of the localization system we built at UT. This dissertation addresses some of the problems to get more closer to sub-mm accuracy. The current system suffers from problems that prevent achieving sub-mm accuracy. A list is given below:

1. Phase center problem adds error to 2D and 3D tracking. The error is caused by different time delays encountered by the received signal at different reception angles of the receiving antenna and as a result there will be an error as we move away off the antenna bore-sight.
2. Sampling clock imperfection is also a problem. Clock jitter translates into noise that limits the RMS error achievable. Clock slow drift where the period of sampling clock varies slowly over time which restrains the repeatability of the system and requires numerous calibration. It also causes time scaling effects.
3. AWG noise increases the RMS error. The SNR changes as we move the tag closer and further to the receiving antennas and that has complications to mm accuracy.
4. Indoor multi-path UWB received signals that changes the pulse shape and affect even the leading edge if the reflection body is too close. This change adds uncertainty to the detected time delay.
5. Sampling rate at the receiver caps the minimum resolution distance that we can achieve, consequently we need to utilize high sampling rate.
6. The strict requirement of low phase noise of the local oscillators at the receiver and transmitter in the non-coherent architecture used now.

7. The receiver chain based on IQ demodulation. A single channel I or Q is alternative. The RF chain is either complex in the case of IQ or introduce intolerable error in the case of single I or Q demodulator.
8. Slow sampling process where we acquire one sample per pulse is another problem. Dynamical performance of the system depends on the throughput of the system i.e. faster system response requires faster pulse processing. Also averaging methods that improve the system accuracy depend on such throughput.

Some of the aforementioned problems are addressed by [17] and [18]. In [17] Zhang has addressed the problem of the necessary high sampling rate by using an analog sub-sampler, he also has made antenna phase center characterization and proposed a Vivaldi rod antenna to dilute the phase center problem. In [18], Kuhn has developed an adaptive leading edge detection algorithm, that detect the pulse arrival based on its leading edge that alleviates the multi-path error problem, he also studied non-line of sight and weak received signal accuracy behavior. My work will address the clock and pulse generation noise and how they affect final accuracy.

1.4 Organization

Chapter 2 is a literature review of both commercial and research localization systems. Chapter 3 summarize the first generation problems that compromise its accuracy/precision. Chapter 4 demonstrates two hardware improvements to the system: self multiplication mixer, and sub-sampling methods. Chapter 5 is a study of the sub-sampling methods, developed in Chapter 4, shortcomings. Chapter 6 discusses the integration of the system RF front-end into single MMIC chip, and the integration of the digital back-end. Chapter 7 depicts the SRD pulse generator noise and jitter conversion mechanisms. Chapter 8 is an accuracy assessment and a system

level modeling of the whole system. Chapter 9 poses a general look and suggests future improvements to the system. Chapter 10 is the conclusion.

1.5 Contributions

My contributions are:

- System level simulation/mathematical model development.
- SRD Jitter generation/conversion mechanisms, simulation, modeling, and measurements.
- Sub-sampling methods study and comparison. Developing the direct sub-sampling with frequency synthesizer.
- Self-multiplication demodulator design/implementation.
- Writing of firmware of the integrated DBE to accommodate total system operation.
- Integrating MMIC whole receiver/transmitter in the system, and studying its performance compared to discrete system.

Chapter 2

Literature Review

The chapter discusses commercial and research localization systems. The focus is on the localization accuracy, precision, localization dimensions, modulation, and range.

2.1 Commercial Localization UWB Systems

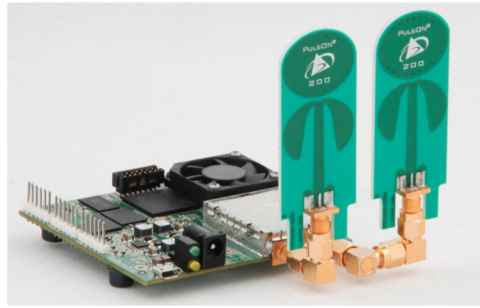
In this section, I will cover the state of the art of the commercial systems, table 2.1 compares their specifications.

2.1.1 PulsON 410 by Time Domain

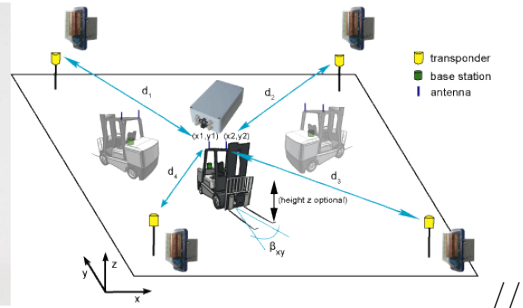
PulsON 410 module is built by Time Domain [19], the tag and receiver has the same hardware. It uses TW-ToF to find the distance between two modules. A single module can work also as a mono-static radar, Fig 2.1a. Modules in the system can exchange data as well.

2.1.2 DART by Zebra Technologies

DART by Zebra [21], Fig 2.1c has accuracy of less than 30 cm. The battery would work for 7 years at 1 Hz update rate. The update rate is programmable from 0.02



(a) PulsON 410 Module in Mono-static Radar Mode[19].



(b) lpr-2d system by Symeo [20]. //



(c) Dart system components [21].

Figure 2.1: Commercial UWB indoor positioning system

Hz to 200 Hz. The positioning rang is 50 m and the presence detection is 200. The system support 3500 update.tag/sec.

2.1.3 Ubisense



Figure 2.2: A tag of a commercial UWB indoor localization system i.e. Ubisense [2].

UWB technology offers some advantage over other systems. No need for line of sight and it has high penetration capabilities. It has higher accuracy than WLAN systems but lower than that of IR. Coverage volume is much larger than IR systems though. An Example is Ubisense funded by AT&T Cambridge [2], Fig 2.2. It works in the frequency range of 5.8 to 7.2 GHz. the tag size is $3.9 \times 1.65 \text{ cm}^2$. The system has a capacity of 1000 tag working concurrently. The update rate is 20 Hz and the accuracy is 15 cm.

2.1.4 LPR-2D

LPR-2D by Symeo is a 2D localization system [20], Fig 2.1b. It is an example of FMCW systems. The tag weight is 1.4 kg because it is designed for vehicle tracking. The system accuracy is 10 cm. The transponder, tag, update rate is 25 Hz. system rang is 400 m.



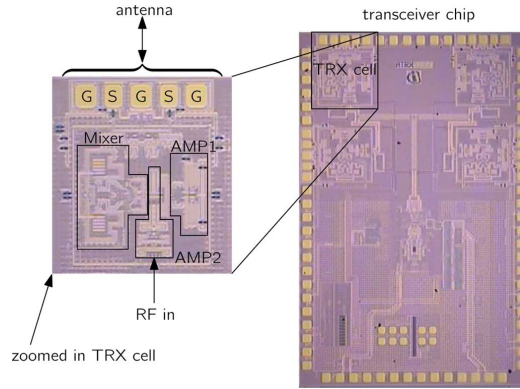
Figure 2.3: Evaluation board of DW1000 Scensor.

2.1.5 decaWave

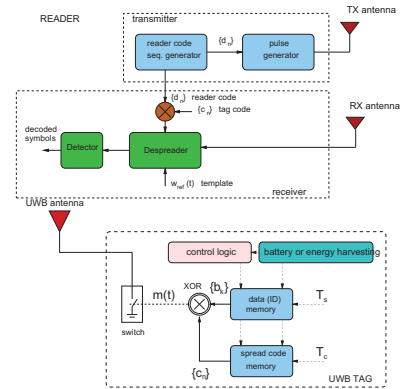
decaWave have developed DW1000 ScenSor [22], it is a single chip UWB transceiver compliant with IEEE802.15.4 standards. It allows real-time indoor localization of a precision 10 cm indoors. The rang is up to 300 m and the tag density of up to 11,000 tags in a 20 m radius. Fig. 2.3 shows the evaluation kit based on DW1000 ScenSor.

Table 2.1: Commercial UWB Positioning Systems Summary

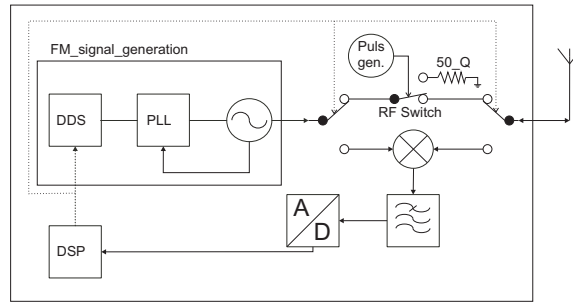
Company	PulsON	DART	Ubisense	Symeo	ScenSor
Frequency (GHz)	3.1-5.3	6.35-6.75	6.0-8.0	5.725-5.875	3.5-6.5
Range (m)	350	50	>160	400	300
Tag Weight	58 g	20 g	580 g	1.4 kg	NA
No. of Tags	1	3500/s	1000	NA	11,000
Refresh Rate (Hz)	8-154	0.01-200	20	25	64 M
Localization	TW-ToF	TDoA	TDoA/AoA	RToF	Tof/TDoA
Accuracy (cm)	2.3	<30	15	10	10
Technology	UWB	UWB	UWB	FMCW	UWB



(a) Micrograph of 77 GHz system built by Ferger et al. for a FMCW radar with 0.1 mm accuracy.



(b) Reader and tag of SELECT project system funded by a EU grant.



(c) Pulsed FM Hardware block diagram realized by Waldmann et al. They chop the FMCW signal to stay with the FCC power requirements.

Figure 2.4: Examples of research UWB indoor positioning systems.

2.2 Research Systems

High accuracy RF system are addressed by many research groups. Table 2.2 shows a brief comparison of such research efforts. Two techniques are used widely with some alteration or combination i.e. wide band FMCW and pulse-based UWB. FMCW radars uses continuous wave that resolve time delay between two system components using frequency difference of echo and receiver oscillator. It is a continuous wave so it drains more power and suffers of multi-path reflection for indoor operation. Many systems are using FMCW e.g. [23] [24] [25].

Pulse-based UWB is time limited repeated signal with small duty cycle and low power consumption. The pulsed nature of the signal makes it easier to remove the multi-path interference that comes later than the line of sight echo. UWB is more suitable for indoors and for systems that require tag with low power consumption. Systems that uses pulse-based technique are [26] [27] [28] [26] [29] [30] [31].

Most systems work at The UWB 3.1 – 10.3 GHz band and 5.8 ISM band. Some pursuit to move up for frequencies 35 GHz [24] and 77 GHz [25] where higher accuracy looks easier to attain.

Recent research achievements show new potentials of FMCW and pulse-based systems. In [25] Ferger et al. built a 77 GHz radar for 2D sensing and they show 0.1 mm accuracy. Fig 2.4a shows the micrograph of the transceiver.

In [23], Waldmann et al. used a pulsed FM signal for localization. The FM signal BW is 1 GHz around 7.5 GHz center frequency. They measured a coaxial cable of length 146 m and obtained accuracy of 7 mm. For a wireless radar configuration they obtained a maximum error of ± 5 cm for a distance of 4 m. The hardware implementation is shown in 2.4c where the FMCW is chopped by a fast RF switch to keep the power under the FCC power requirements.

In [29], the project SELECT supported by an European grant to design a real time localization RFID system, Fig 2.4b, with low-cost and semi passive tags. The system should be UWB-based and compatible with UHF-RFID standards. The system uses

Table 2.2: Research UWB Positioning Systems Summary

Group/Company	System Architecture	Frequency (GHz)	Reported Error	Operating Range
University of Tennessee	Carrier-Based UWB	5.4-10.6	2-5 mm 3D	5 m/Indoor
Waldmann et al.	Pulsed FMCW	7.5	7 mm 1D	4 m/Indoor
D’Erico et al.	Back Scattered UWB	4-5	0.7 m 2D	15 m/Indoor
Georgios et al.	IR-UWB	6-6.5	10 cm 1D	12 m/Indoor
Waldmann et al.	Carrier-Based UWB	7-8	1.7 cm 1D	10 m/Indoor
Meiere et al.	Carrier-Based UWB	22.58-25.7	0.1-2 mm 1D	8 m/Indoor
Ossberger et al.	Impulse-Based UWB	2-7	5-10 mm 1D	5 m/Indoor
Fujii et. al.	Impulse-Based UWB	3.7-5	20 cm 2D	8 m/Indoor
Low et al.	Impulse-Based UWB	3.2-5.2	1 cm 1D	8 m/Indoor
Zetik et al.	Impulse-Based UWB	0.01-5	1.5 cm 2D	2 m/Indoor
Stelzer et al.	FMCW/Interferometry	35	0.1 mm 1D	<1 m/Indoor
Stelzer et al.	FMCW	5.8	10 cm 2D	500 m/Outdoor
Ellinger et al.	FMCW	5.8	18 cm 2D	40 m/Indoor
Feger et al.	FMCW	77	0.1 mm 1D	1.5 m/Chamber

a back scattering CDMA localization scheme and shows 2D localization capabilities of 0.7 m accuracy and 15 m range.

The systems that show mm or sub mm accuracy are [23] that got 7 mm accuracy for a cable length measurements but for 1D wireless measurements they got 10 cm error. In [28], A 25 GHz system is developed and it has 0.1 mm accuracy using a static Kalman filter. They also use PN code with rate of 1.6 GHz compared to 10 MHz pulses for UT system. 1.6 GHz pulse rate means more power requirements. In [32], it is a radar to detect the respiration that also has limited movement. In [24], Stelzer et al. measured using a radar a limited movement of a 5 mm from a smooth surface.

Analog to digital conversion is a key competent of a localization system. The system described by [26], they use Wi-Fi 802.15.4a signal to perform tracking, the receiver consists of an RF front end, and they use an oscilloscope for the analog to digital conversion, the sampling rate is 1 GHz that provides a resolution of 30 cm. In [29], they track a passive RFID tag, they use a CDMA spreading code, the ADC has a sampling rate of 62.5 MHz and 12 bit resolution, the system accuracy is 0.7 m. In [32], they use UWB pulse to detect chest movement, they use a Tektronix sampling oscilloscope to achieve a 2 ps sampling rate. In [27], there is no ADC, they use a comparator to pin out the pulse reception time, the resolution of the system is 0.3 ns. In [31], they also use a sampling oscilloscope. Analog to digital conversion poses a problem as seen, systems either use a sampling oscilloscope that are not feasible for practical system, or a low sampling ADC that is not feasible for high accuracy localization.

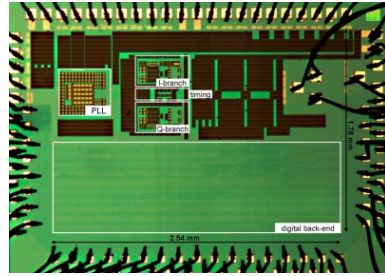
3D localization still can't accomplish accuracy comparable to IR systems. All the UWB systems that showed a similar accuracy are for radar limited vibration-like movement.

Table 2.3: Positioning System Integration on Chip

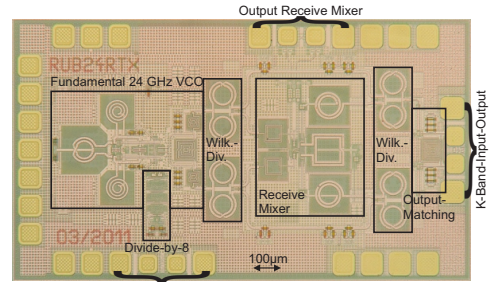
	Bredendiek et al.	Martynenko et al.	Lee et al.	Verhelst et al.	Kao et al.	Hamidian et al.
Technology	MMIC SiGe	0.18 μm CMOS	0.18 μm SiGe	0.13 μm CMOS	90 nm CMOS	0.13 μm CMOS
Application	FMCW	802.15.4a	802.11a	IR-UWB	Micro-Doppler	FMCW
P_{dc}	245 mW	NA	53 mW	4.3 mW	190 mW	42 mW
Error	250 μm	3cm	2.7×10^{-3} BER	1 cm to 1.8 mm	20 μm	Na
BW	8 GHz	3 to 9 GHz	3.1 to 10.5 GHz	500 MHz	NA	250 MHz
Frequency	24 GHz			<1GHz	60 GHz	24 GHz
Range	3 m	10 m	10 m	10 m	2 m	50 m
Chip Area (mm^2)	1.51	4.5	2.3	4.52	0.73	2
Remark	Transceiver	Transceiver	Front-end	Receiver	Transceiver	Transceiver

2.3 Advances and Integration Trends

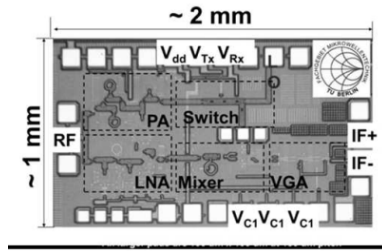
Recently there has been significant advancement in MMIC and CMOS chip designs geared towards UWB and fast time domain processing, some quite variant examples of these efforts are shown in Table 2.3. Ref. [33], for example, is a mono-static FMCW Radar; its transceiver is integrated except for a PLL loop. The system is used to measure the distance of a reflector moving on a linear positioning unit for a 3 m and has demonstrated only 250 μm error, Fig 2.5b. Ref. [34] discusses the design of a 12 channel transceiver capable of a positioning accuracy of 3 cm. It is based on IEEE 802.15.4a for a low data rate with localization capability for sensor networks. Ref. [34] has integrated the whole RF system; but leaving a space on the chip left for digital circuitry integration later on. In [35], a design of UWB receiver direct-conversion front-end that covers the 3.1-10.6 GHz band with a NF of 3.3-5 dB that was integrated with a switchable notch filter, Fig 2.5e. In [36], the authors combined both analog front-end and a digital back-end onto one chip; they used IQ correlator receiver to save energy with a power consumption of only 4 mW for the whole transceiver. They achieved 1.8 mm tracking accuracy over 160 μs averaging time, Fig 2.5a. Ref. [37] shows a 60 GHz Doppler radar transceiver developed for non-contact vital sign detection. It demonstrates the ability to detect 0.2 mm vibration at 2m stand-off distance 2.5d. Ref. [38] is a transceiver for FMCW radar that has a 1.5 mm resolution for a 50 m distance, Fig 2.5c. Clearly we observe in all these MMICs implementations the tremendous space saving; the robustness enhancement of the systems by minimizing the number of interconnection linking the various system components, the extremely low power consumption, and the neat mixing of digital and analog circuitry in one chip.



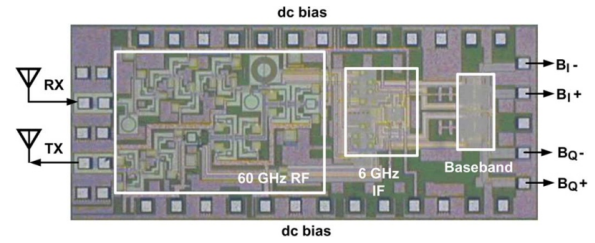
(a) Verhelst et al.



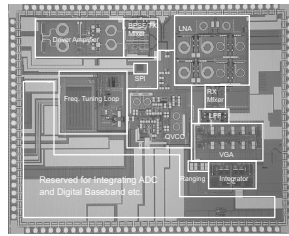
(b) Bredendiek et al.



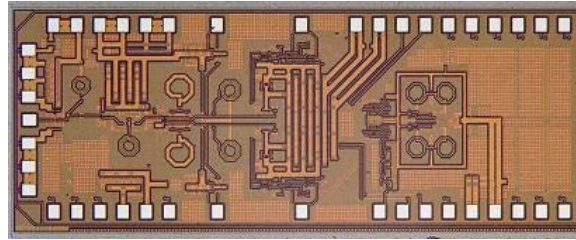
(c) Hamidian et al.



(d) Kao et al.



(e) Zheng et al.



(f) Lee et al.

Figure 2.5: MMIC and CMOS System Integration.

Chapter 3

System Architecture and Problems

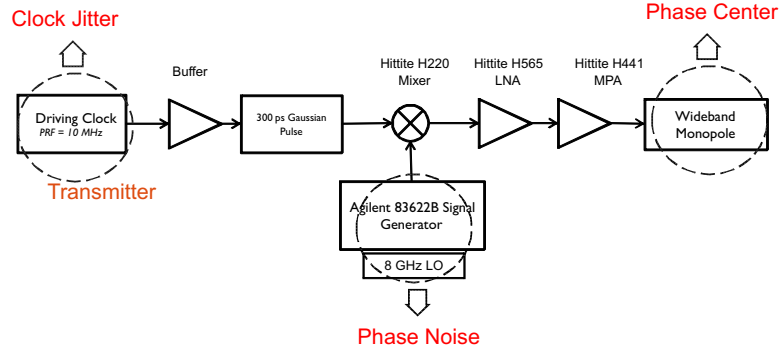
In an effort to improve the accuracy of the current localization system, major hardware blocks were re-examined to guarantee stable operation. Leading edge algorithm was addressed to have higher probability of success. Digital signal processing board was re-evaluated. Fig 3.1 shows the various sources of errors that have been investigated. Table 3.2 shows different sources of errors and their effect on accuracy or the precision of the system.

Table 3.1: Noise Sources Impact on System.

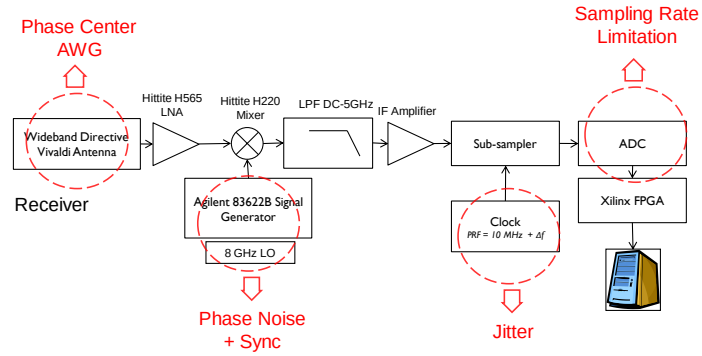
Noise Source	Precession	Accuracy
Clock Jitter	Yes	No
Clock Drift	No	Yes
AWG	Yes	Yes
Phase Center	No	Yes
Phase Noise	Yes	No
Sampling Rate	Yes	No

3.1 I and Q Channels Misalignment

In the receiver side, there has been a noticeable delay between the I channel and Q channel. Typically, the retrieved signal is obtained by squaring the I and Q signals



(a) Transmitter sources of errors.



(b) Receiver sources of errors.

Figure 3.1: Sources of errors in UT positioning system.

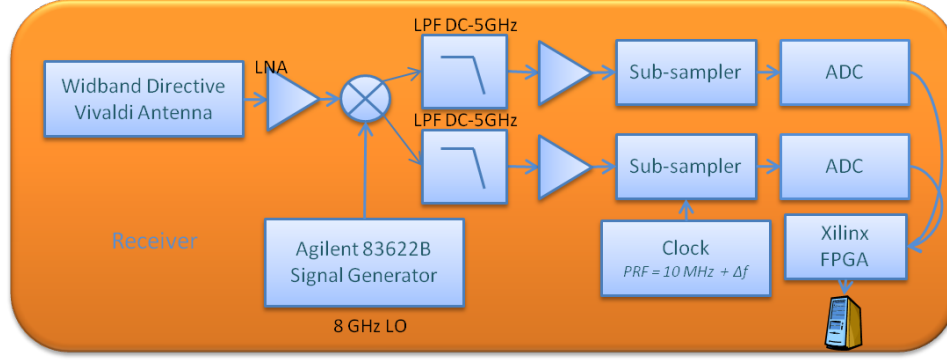


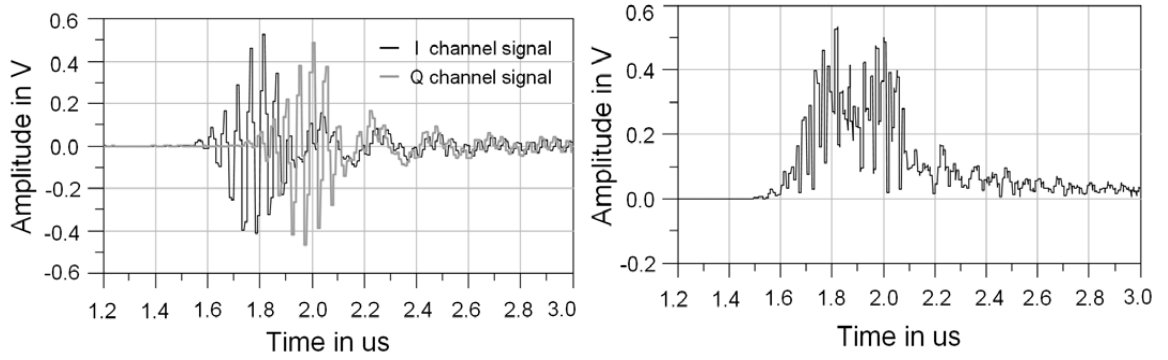
Figure 3.2: IQ receiver block diagram.

and add them in real time, Fig. 3.2. Any random delay or frequency dependent delay would lead to significant retrieved signals error.

Fig. 3.3 shows typical I and Q signals where the relative delay between them is not constant so that we can account for. To study this misalignment problem, we used a Tektronix real time oscilloscope and built a prototype without a sub-sampler, an ADC and FPGA to identify the source of misalignment. It was found out that this misalignment dynamically changes with time and tag position, and it is difficult to compensate or calibrate. Fig. 3.3(a) shows the I and Q signals and Fig. 3.3(b) shows the sum of their squares.

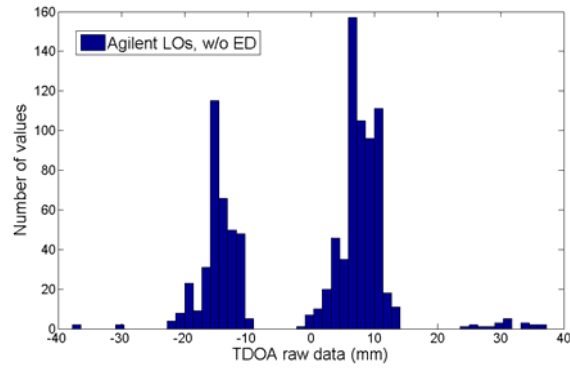
To avoid this misalignment problem, Zhang et al.[17] used only one channel either the Q or the I and were able to retrieve the signal after the mixer and simple filtering. However, the received pulse train of sampled signal had a sinusoidal envelope as seen in Fig. 3.4a. This envelope is due to any slight shift between the two clocks of the transmitter and receiver, and could cause the leading edge readings to go back and forth as seen in Fig. 3.4b. The histogram of such leading edge is shown in Fig. 3.3(c), we can see the leading edge is distributed in two separate heaps.

As a first trial, we looked at averaging the associated leading edge error for a 1000 trial, but the nature of the histogram caused large errors, and the standard deviation was 12 mm which is significantly large error. So. Here we have proposed square detection. Results will be discussed in Section 4.1.



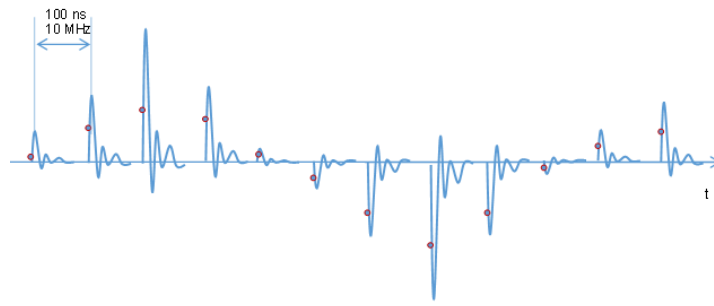
(a) I and Q channels.

(b) The sum of I^2 and Q^2 .

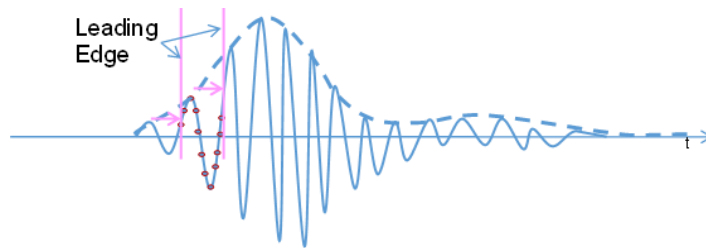


(c) ToA histogram.

Figure 3.3: I and Q channels of the extended received pulse that shows the misalignment between the two channels.



(a) .



(b) .

Figure 3.4: Single channel demodulation: (a) retrieved pulses has a slow sinusoidal envelope corresponding to the frequency shift of transmitter and receiver oscillator; (b) sub-sampled pulse and the triggering edge.

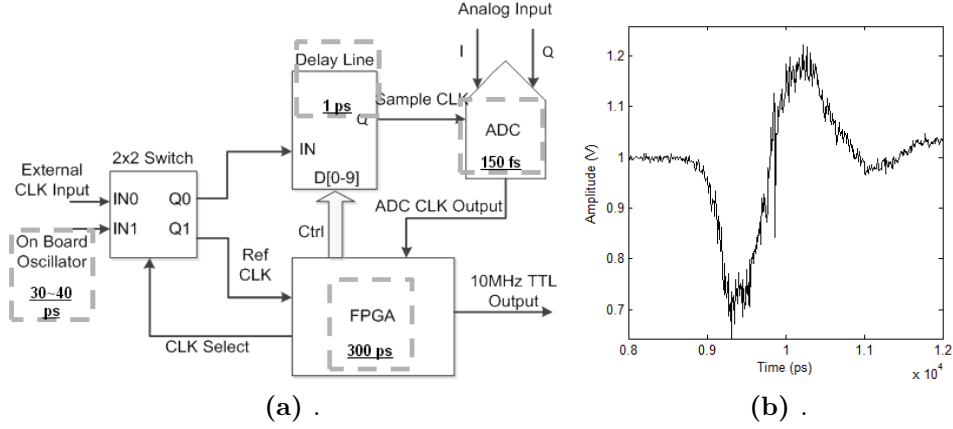


Figure 3.5: Jitter in sampling module: (a) sources of jitter; (b) jitter shows up as spikes in the retrieved pulse.

3.2 System jitter

All jitter sources are small compared to the tag triggering clock, Fig. 3.5a. Table I indicates the FPGA, ADC, delay line, and on board TCXO clock jitter. The Table too has a typical top bench clock jitter as a reference. This jitter in the clock translates into spikes in the sub-sampling as can be seen in Fig. 3.5b.

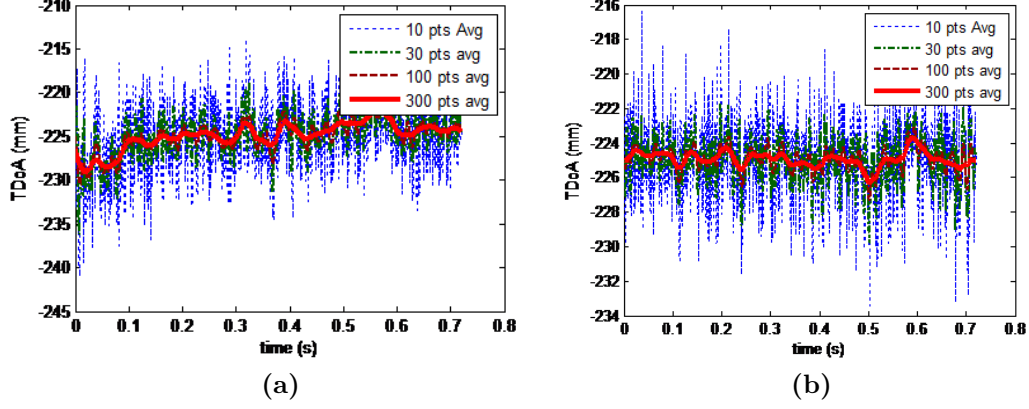
Table 3.2: Sampling Module Jitter Sources.

	Jitter
Top Bench Clock	200 ps
FPGA Output reference Clock	300 ps
ADC	150 fs
Delay Line	1 ps
On-board TCXO	30 ps

Efforts to evaluate this jitter and reduce its effect are major part of our efforts here. As a first step, we measured the TDoA as a function of number of averaged samples. Table 3.3 indicates that upon increasing the number of samples to 300, the STD was reduced from 13.6 mm to 1.494 mm when utilizing a clock with 300ps jitter. Further averaging can help in jitter associated error. Definitely, using better clocks can lead to significant jitter reduction as indicated in Table 3.3 third row and Fig. 3.6b.

Table 3.3: Standard Deviation of TDoA.

STD (mm)	Raw	Avg 10	Avg 30	Avg 100	Avg 300
300 ps Clock	13.6266	3.7054	2.3802	1.7724	1.4939
Top Bench Clock	9.3272	2.1722	1.2740	0.6669	0.4187

**Figure 3.6:** TDoA with different averaging filter lengths: (a) 300 ps clock jitter and (b) top-bench clock.

In this effort, we will investigate further the effect of jitter and develop models and methods to reduce its impact. The jitter in the systems originates at the transmitter and receiver clocks, we used TCXO clocks at both where 10-15 ps jitter is common for this type of clocks.

Moreover, we studied jitter conversion in Step Recovery Diode (SRD) based UWB pulse generators that suffer from jitter caused by AM-to-PM conversion, SRD shot noise and clock jitter. These noise sources significantly impact the accuracy of UWB systems if very high precision ranging/positioning is required.

Also, we study the achievable localization error in the system. A mathematical model and simulation platform are developed to describe the behavior of UWB indoor localization system. A discussion of the dominant reasons for errors that include picoseconds pulsar jitter, sampling clock jitter, sampling rate, and system AWGN is carried. We developed a simple method to calculate the total system jitter, and

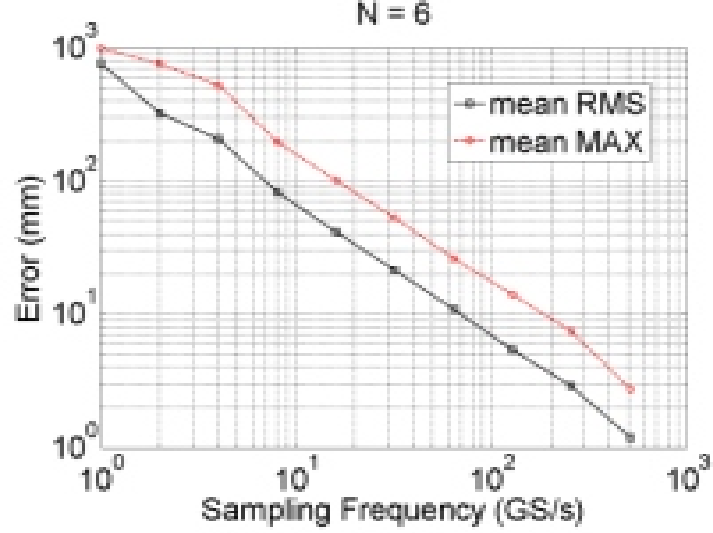


Figure 3.7: Error in 3D positioning as a function of smapling rate [3].

describe error biasing phenomenon as the tag moves approaching one base-station and distancing another.

3.3 High Sampling Rate

In order to achieve a mm 3-D accuracy, we need a high sampling rate. Typically, to achieve such high sampling rate we need to use sub-sampling schemes. For example, if we want 3mm resolution, then we need 10 ps sample spacing, which is equivalent to 100 GSPs sampling rate.

Brandon Merkl [3] showed that, in order to get sub-mm accuracy we need over 512 GSPs as seen in Fig. 3.7. Use of conventional ADCs is not feasible as the current state of the art does not exceed 5-10 GSPs, recently over 40 GSPs by Fujitsu is available which is very expensive. Hence, C. Zhang et al [4] used a sub-sampling mixer where the signal was stretched in time by a large factor. Fig. 3.8 shows the fabricated circuit and the samples signal using this scheme.

This first ADC system uses two clocks. One at 10 MHz and is used to trigger the pulse at the transmitter and the second is 9.999 MHz clock as part of the analog

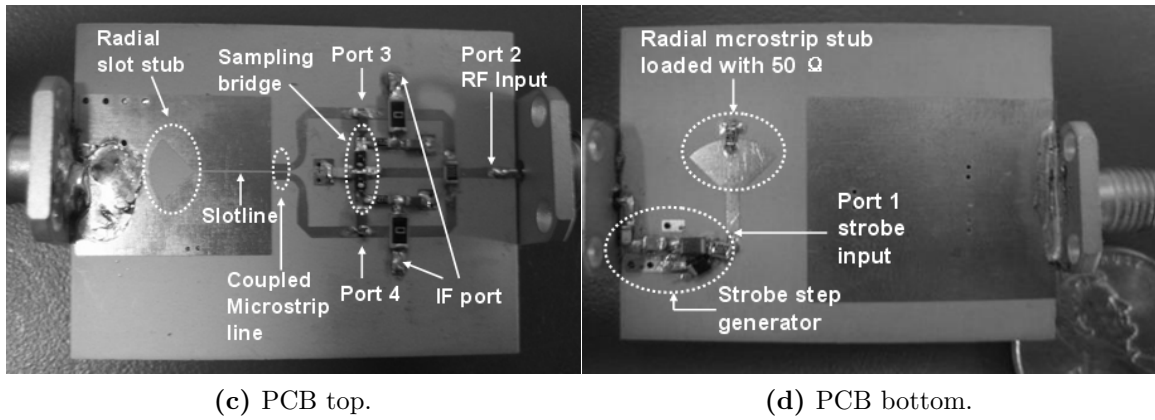
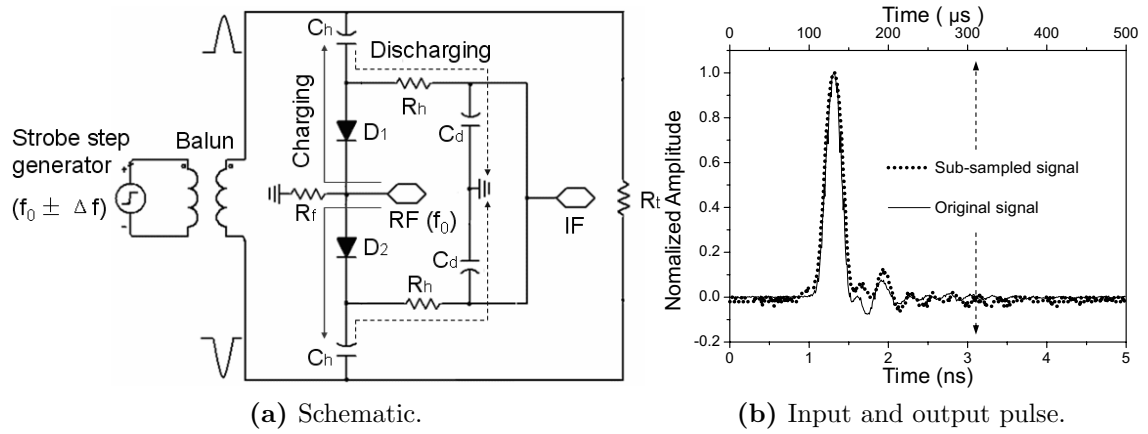


Figure 3.8: Sub-sampler used to extend the pulse and permit sampling by a slow ADC [4].

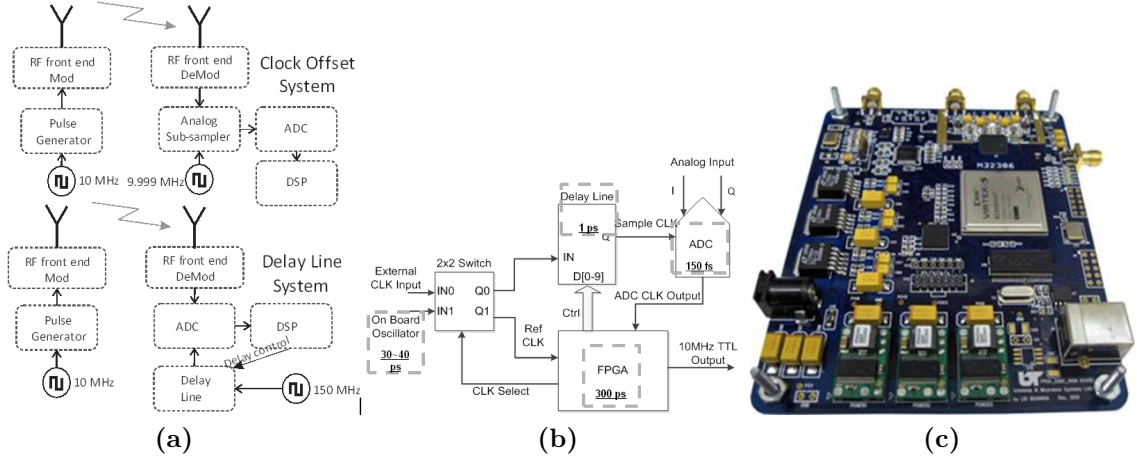


Figure 3.9: Delay Line sub-sampling: (a) system block diagram, (b) jitter sources, (c) sampling module picture.

sub-sampler. The two clocks offset is the key for the sub-sampling and provides the required time shift at the subsequent periods. This is equivalent to expand the signal in the analog domain before implementing ADC. Since the input signal to the ADC is time-expanded, the ADC Analog bandwidth requirement is drastically reduced by such expansion factor. For our system, the original bandwidth is 3 GHz and the expansion factor is 10,000 so the required ADC analog bandwidth is only 300 KHz and that is a clear advantage of such system. However, the usage of such an analog sub-sampling adds noise, requires high signal levels, and limits the expansion factor value to moderate values to guarantee robust performance. Moreover, the need for the 9.999 clock, which is not a standard clock, requires a very precise circuitry to generate a stable precise clock.

Therefore a second system was developed using a delay line system that builds on a delay line chip that can provide delay steps of 10 ps. The 10 ps shift at each original signal pulse repetition rate carries out the sub-sampling process. The system uses standard clocks and no need for precise frequency offset or frequency synthesizers. The system does not use analog sub-sampler and there is no time expansion to the analog signal, subsequently it requires ADCs with a wide analog bandwidth— as wide as the original signal bandwidth.

One downside of this delay line system is that: the available delay line chip distinct steps are not accurate enough and also nonlinear. In our realization of the system, we have used at the receiver side a 150 MHz clock instead of 10 MHz to increase the throughput of the system. The utilized board has a two-channel ADC with a 150 MHz clock, and has a 16 bit resolution. Meanwhile, a USB 2.0 Transceiver chip provides a data transfer rate of 480 Mbit/s, for more details refer to [39].

3.3.1 Jitter

The accuracy of both sub-sampling systems is seriously degraded by both the clock jitter and drift. Additional degradation for the second sub-sampling scheme accuracy is related to the delay line chip non linearity. Impact of these error sources on performance will be discussed in the next section in detail.

The clocks used for sampling at the receiver and for triggering the pulse generator at the transmitter sides are the main contributors for jitters. Moreover, SRD pulse generator augment the jitter, the generated pulse will have more jitter than the SRD triggering clock. As shown in Fig. 3.9b the contributions of other system components are relatively smaller. The jitter distorts the sampled pulse and causes spikes rendering small variation in the retrieved signal shape. This variation translates to randomness in measuring the leading edge of these pulses. As the jitter increases the distortion in the pulse increases and more error in the leading edge is expected. We can observe from Fig. 3.10 how the standard deviation is reduced and that the clock with lower jitter requires less averaging to achieve a sub-mm RMS error. The 200 ps clock meets the 1 mm RMS error line at about 60-70 averaging window filter samples; compared to over a 1000 when using the 300ps clock.

3.3.2 Nonlinearity of the Delay Line

The manner in which we employ the delay line chip is by using a 10 MHz clock for triggering the pulse generator, and a 150 MHz clock for the receiver sampling

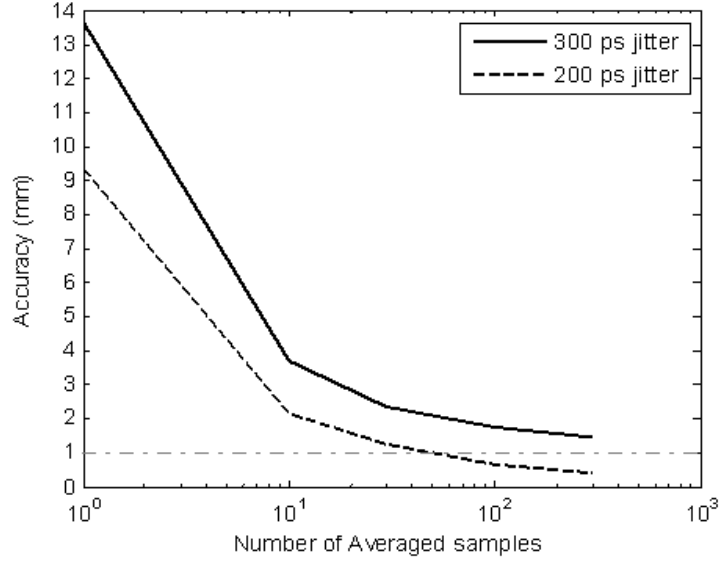


Figure 3.10: Accuracy realized for our system and how they converge with the number of averaging for the two different clock jitters.

circuits. We need 15 sub-periods of the 150 MHz clock periods to reconstruct one pulse with 10MHz repetition frequency. For each sub-period we need a certain number of phase shifts to cover it. A single sub-period is 6.6667 ns. The phase-shifting chip is controlled by a 10 bit word, and the time delay per bit is not binary. It starts with a 10 ps for the LSB but for higher order bits it is not multiple of two e.g. b1 delay is 26 ps and b9 is 4300 ps which deviate by a 6 ps and -820 ps respectively away compared to the binary values. Using these values we need 780 phase shifts to cover the 6.6667 ns sub-period. This nonlinear behavior causes pulse distortion. Typically, a small part of the signal repeats itself, and it corresponds to phase shifts of large numbers that are inaccurately located. This part of the signal repetition causes trespassing over to the next sub-period. Experimentation and trial and error shows that using optimum number of phase shifts per sub-periods could eliminate such distortion. In our experiment 718 phase shifts were used.

Figure 5.1a shows the TDoA of a static tag for different phase shifts. It shows TDoA for 780 and 718 phase shifts. For the 780 there is a dip in the TDoA that causes an

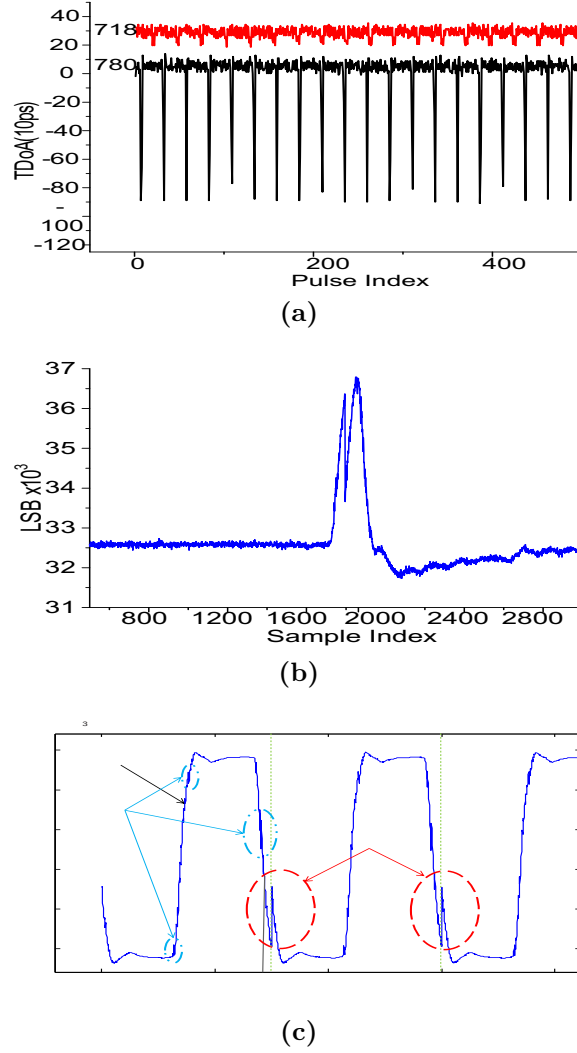


Figure 3.11: Error created using delay-line based sampler: (a) Time difference of arrival error; 780 samples per segment introduces about 80 90 10 ps spike error; 718 samples/segment errors are down to about 100 ps spikes error. (b) Distortion in sampled pulse where small part of the signal repeats itself, where 780 samples/segment exceeds the phase shifts required to cover one sub period time i.e. 6.6667 ns. (c) The same 150 MHz sampling clock fed into the ADC input, 780 samples/segment, shows two main distortions: signal repetition, and high order bits error.

Table 3.4: Systems Comparison.

	Clock offset	Delay Line
Clock Source re-requirements	frequency Synth.	Standard Sources
ADC Bandwidth	Small	Wide
Delay line	No	Yes, but Non-linearity is a problem
Analog sub-sampler	sensitivity problems	None
Throughput	Lower	Higher
effect by Clock Drift	Yes	Yes
effect by Clock Jitter	Yes	Yes

error of about 300 mm. These dips are periodic and coincide with the leading edge crossing the boundary of the two sub-periods. The dips do not disappear completely at 718 phase shifts per sub-period but dips in the 718 case take place when high order bits i.e. 7th, 8th, and 9th changes. The reason is the real time shifts are different than the typical binary values with -200 to -900 ps which results in sampling an earlier part of the pulse.

In this effort, we have addressed this problem. To solve the tremendous error introduced by the non-linearity of the delay-line. We developed a new method that do without the delay-line. We wanted to maintain high through-put. We used a clock with a period $10\text{ ns} + 10\text{ ps}$. The corresponding frequency is a little bit lower than 100 MHz. It acquires 10 samples per pulse period. The block diagram of the system is shown in Fig 4.7.

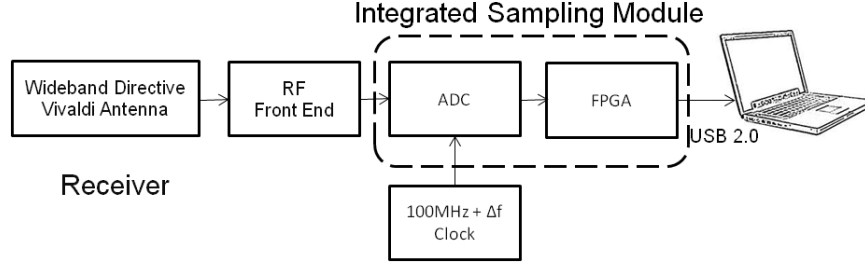


Figure 3.12: Block diagram for direct sample frequency synthesizer digital sub-sampler.

3.4 Leading Edge Algorithm

Leading edge algorithm used by UT positioning system is described in [3]. The received signal $h(t)$ is passed first through a 16-element averaging widow filter.

$$y[t] = \text{avewindow}(\text{abs}(h[t]), 16) \quad (3.1)$$

where $\text{avewindow}(x, n)$ denotes the function which averages the signal for a window size n and $\text{abs}()$ takes the absolute value of the original signal $h[t]$. The averaged signal $y[t]$ then goes through two maximum window filters of sizes n_1 and n_2 samples

$$\text{max}_1[t] = \text{maxwindow}(y[t], n_1) \quad (3.2)$$

$$\text{max}_2[t] = \text{maxwindow}(y[t], n_2) \quad (3.3)$$

where $\text{maxwindow}(x, n)$ denotes the function which returns the maximum for a given window size n . $n_1 = 16$ and $n_2 = 256$. A logical value is obtained

$$r[t] = ((\text{max}_1[t] \times \alpha > \text{max}_2[t]) \text{ and } (\text{max}_2[t] > \text{threshold})) \quad (3.4)$$

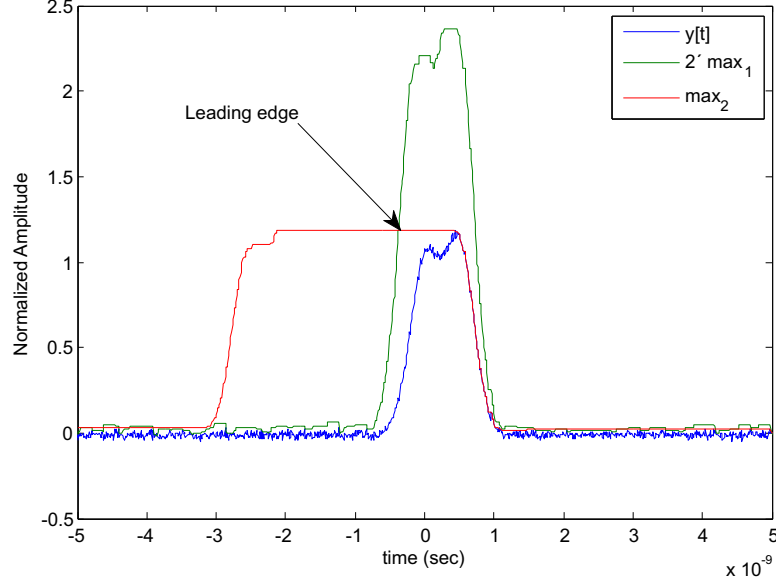


Figure 3.13: Noisy Gaussian pulse with multipath and the leading edge algorithm is applied. The arrow shows the time of the leading edge.

where α is a fixed multiplier currently set to two. *threshold* is established to prevent the noise from triggering the leading edge. Details of the algorithm operation is shown in Fig 3.13.

One problem of such algorithm that it introduces an error in the presence of close strong multi-path signals. In Fig 3.13 we can see the red line y value at the arrow tip equals to the multi-path pulse amplitude and it should equal to the line of sight peak. This kind of error doesn't take place frequently however we still need to alleviate such error.

In this effort, we study the optimum delay to minimize the close multipath error. Also, to modify the algorithm to work with the new sampling module where the data is not real-time as the first system.

3.5 Phase Center

At a certain frequency the phase center of an antenna is the center of the spherical wave transmitted by that antenna. For a UWB antenna receiving or transmitting a

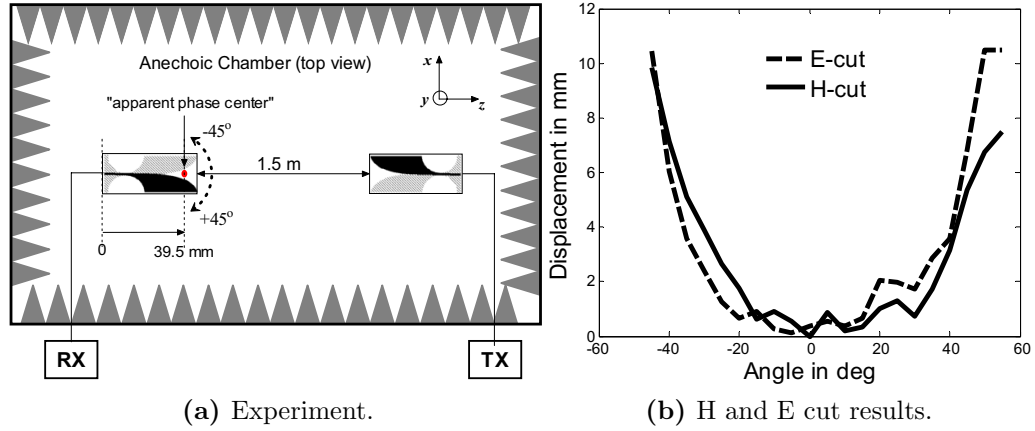


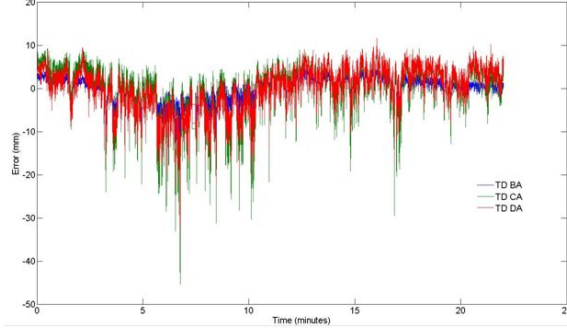
Figure 3.14: Phase center experiment and results [4].

UWB pulse the phase center is the point that the pulse time reference i.e. peak or leading edge is received or transmitted from that point to a sphere surface centered at the same point with same delay.

We have two antennas in our system: a wide band printed monopole for the tag and a directional Vivaldi antenna for the receivers. In [17] experiments were made to characterize the phase center performance of the two antennas. For the printed dipole, the phase center is within 1 mm and has minimum effect on system accuracy. For the receiving Vivaldi antenna an experiment was performed as shown in Fig 3.14a. Two Vivaldi antennas facing each other and one of them was rotated and the phase center error was measured. Fig 3.14b shows the error for both the H and E cuts. We see that about $\pm 30^\circ$ are usable with about 2 mm error and the error is so big for greater angles. 2mm error is still large for our sub-mm accuracy target.

3.6 Clock Drift

Drift is the slow changing in the period of the clock over time. Our system is based on sub-sampling and it is very sensitive to relative drift of the sampling and pulse triggering clock. Fig 3.15a shows the time difference of a 23 minutes for a static tag.



(a) Static tag measured TDoA.

Figure 3.15: Clock Drift effect on TDoA.

In addition to the fast jitter and noise error we can notice a slow error component which is bounded by $\pm 10mm$.

3.7 AWGN

In practical operation, the SNR at each link for a strong UWB pulse typically lies between 20-40 dB. As the SNR degrades below 20 dB and approaches 10 dB and below, the leading-edge detection will fail as it is trying to locate the leading-edge at 1/4th the amplitude of the peak of the received UWB signal which lies below the noise floor of the received signal. Leading edge algorithm ceases to work when the SNR is lower than 10-12 dB. For more details [18].

In this effort, we examine the effect of the AWGN on the error of the localization system.

Chapter 4

System Architecture

Enhancements

To solve some of the problems facing the system we improved the design of some parts of the system. The demodulation method introduced a problem before, we designed a wide-band demodulator that is simple and works in a great way, the one downside is that it requires higher SNR of the received signal to work properly.

The sub-sampling method, we discuss three different sub-sampling methods that we used in our system. They are different in robustness, throughput, and accuracy.

4.1 Self Multiplication Demodulator

The localization system at UT has a non-synchronized carrier of both receivers and Tag. As was shown in section 3.1 a simple architecture would be a square receiver or self multiplication receiver. Most groups build a CMOS or HBT e.g. [40] used HBT Si-Ge process to design a Gilbert cell true multiplier and used for both multiplication and self multiplication operations.

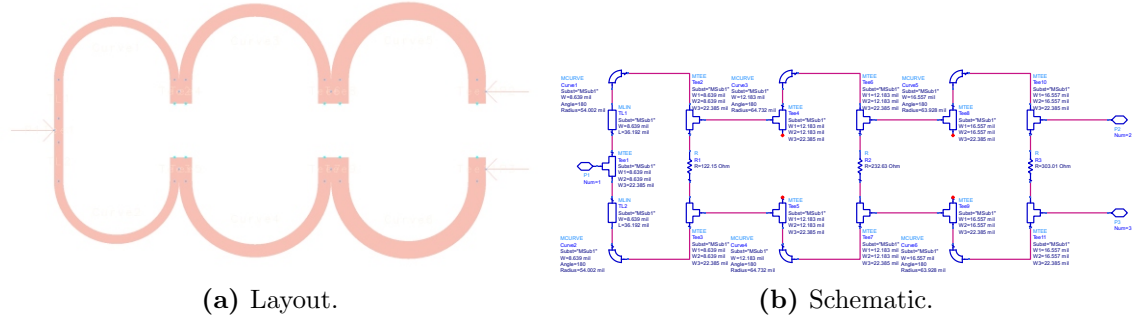


Figure 4.1: Three stage wide-band Wilkinson divider matched to 50Ω at the three ports.

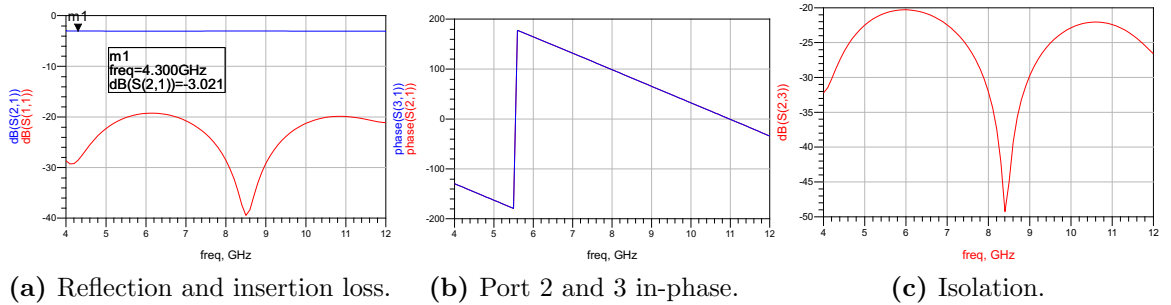


Figure 4.2

At UT we designed a hybrid circuit that consists of a Wilkinson power divider followed by a mixer and then a base-band amplifier. The Wilkinson power divider is a wide-band three stage Chebyshev divider. Schematic and Layout are shown in Fig 4.1 with all the resistor values and micro-strip lengths. The input and output impedance are 50Ω .

Fig 4.2 Shows the S-parameters of the divider. S_{11} is less than $-20dB$. S_{21} and S_{31} are $-3dB$ and are equal. The signals at port 2 and 3 are in-phase. The isolation of port 2 and 3 S_{32} is better than $-20dB$.

The mixer used is *HMC220* by *Hittite* with BW of 5 to 12 GHz. Its layout recommendation is based on GCPW. A smooth transition is designed to move the 50Ω micro-strip to 50Ω GCPW. Two equal sized arms are used to make sure of the complete similarity of the two signals entering the mixer.

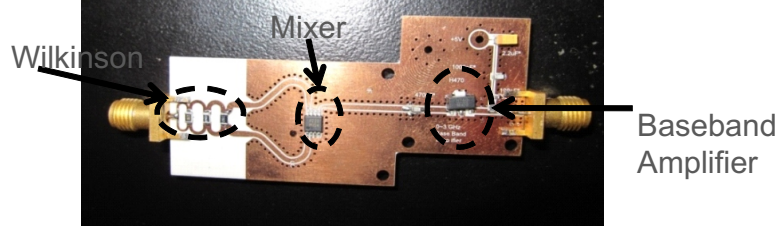


Figure 4.3: Final fabricated and assembled self multiplication mixer.

Finally, we use a *Hittite HMC470* base-band 0–3 GHz amplifier. The purpose of the amplifier is to amplify the output signal before we use a long cable to convey it to the central processing unit. We should notice that there is no fresh carrier feed to one of the mixers RF ports and the signal exiting the mixer is comparatively weak. The self multiplication receiver was built and was successful utilized in retrieving the base-band pulse and solving the problem with using single channel modulation Fig 4.3. We can use the analog sub-sampler after and the low speed ADC. Alternatively we can use the sampler scheme discussed in the following sections.

4.2 Sub-Sampling Techniques for a Time Difference of Arrival Indoor localization System

Sub-sampling is used to alleviate the high sampling rate required for UWB signals. Current commercial direct sampling systems are still too slow or prohibitively expensive for UWB applications. At the University of Tennessee, we developed two different sub-sampling techniques to work with our indoor mm localization system. The two systems suffer numerous shortcomings that prevent them being used in our localization system. The shortcomings are low throughput, non-robustness, non-linearity. A third system is introduced that achieve both high accuracy and high through-put. Changes in the detection algorithm and the frame synchronization are developed to accommodate the new scheme.

4.2.1 Introduction

UWB waveform acquisition is typically performed using two methods: real-time sampling where the entire pulse waveform is acquired in one pass, and equivalent-time sampling where the required samples are gathered over multiple pulse periods. Real-time sampling rate is limited by the aliasing bandwidth of the analog signal. Commercially available systems still have limited performance, Texas Instruments has an ADC chip with two channels. It has a 2.5 GHz analog BW and 1.8 GSPS per channel. One channel can be used with 3.6 GSPS interleaved sampling rate. An example of the research efforts is [41]. A chip fabricated using the IBM-8RF 0.13 μ m CMOS process. It has 6 analog channels and 17.5 GSPS sampling rate for each channels. Word size is 12 bits and Analog BW is 1.5 GHz. However, It still has a sustained readout rate of 50 KHz.

Equivalent-time sampling is an alternative method, it mitigates the high sampling rate required by real-time sampling. The UWB pulse signal is acquired up to the analog bandwidth regardless of the available sampling rate. The necessary number of samples are gathered across several triggers, provided that the signal is repetitive, i.e. quasi static scenes.

One example for equivalent time sampling is where swept time delay processing combined with precise sample and hold gating to reduce the analog to digital converter sampling rate. For example, [42] required 1 Msps to digitize the nanosecond short pulses of 2 GSPS, while retaining the required effective Nyquist sampling rate of 2 GSPS. This method reduces the memory, digital signal processing, and data logging storage requirements significantly as well as the overall cost of the sounder system as described in [42].

Products by major producers are shown in Table I. Sub-sampling has been used previously for real-time significant-bandwidth Oscilloscopes. Last row in table 4.1 shows the capabilities of the board developed at University of Tennessee (UT). The analog bandwidth is 3 GHz, the equivalent sampling rate is 100 GSPS, the sampling

Table 4.1: Commercial Sub-sampling Systems.

Producer	Analog BW	Samp. Rate
Agilent DSO91304A	13 GHz	40 Gs/s
Tektronix DPO70000	33 GHz	100 Gs/s
LeCroy LabMaster 10	65 GHz	160 Gs/s
UT(FPGA, USB2 on-board)	3 GHz	>100Gs/s

time is 10 ps, The total number points required to cover a whole pulse is 10^4 , and the pulse repetition period is 100 ns. Field programmable gate array (FPGA) Virtex 5 is mounted on board for data temporal storage and processing. High speed universal serial port (USB) 2.0 connection is used to transfer the data to the computer for post processing and graphical representation.

4.2.2 Equivalent-Time (Sub) Sampling

In equivalent-time sampling, we utilize slow ADCs to acquire UWB signal. The necessary number of samples is gathered across several periods of the analog UWB signal. The input signal must be repetitive, otherwise distortion is to take place. Here, we will discuss the three sub-sampling systems utilized at UT localization system. We will compare their speed, simplicity, and immunity to clock drift.

Analog Sub-Sampler

The idea of analog sub-sampler is to produce a signal with smaller bandwidth, by time-stretching the signal before it reaches ADC input. Fig 4.4a shows the block diagram of the analog sub-sampler system used at UT. After down converting received signal, we use the analog sub-sampler circuit, Fig 4.4b, to stretch the signal. It samples and holds one point at each pulse period for the whole pulse duration. We use a sampling clock of a period $100 \text{ ns} + 10 \text{ ps}$ to produce equivalent-sampling period of 10 ps. We sample one point per pulse period, we need 10^4 points to acquire a whole pulse. The pulse at the output of the analog sub-sampler has a bandwidth 10^4 smaller than

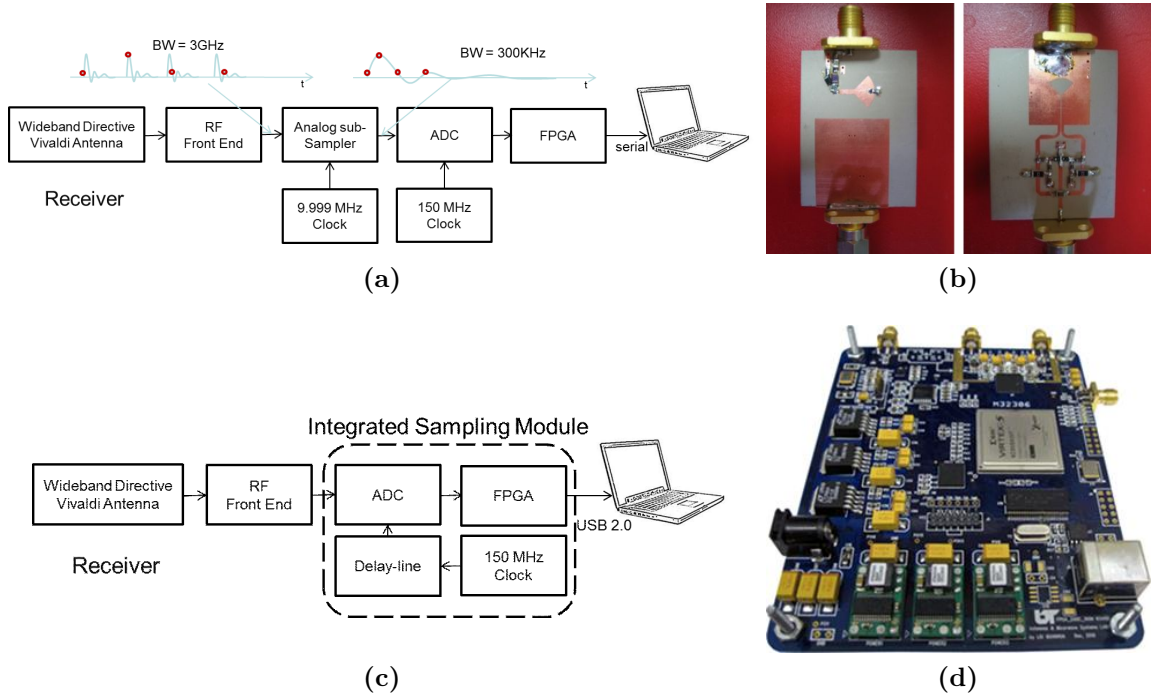


Figure 4.4: (a) and (b) Analog sub-sampler where the pulse is stretched in time and bandwidth is reduced before ADC input. (a) Block diagram showing pulse stretching using the 9.999 MHz that reduces the bandwidth by a factor of 104 suitable for the analog BW of the ADC. ADC has its own 150 MHz clock that operates on the 300 KHz signal larger than Nyquist Rate. (b) Picture of the analog sub-sampler developed at UT [4]. (c) and (d) Delay-line sub-sampler where all the digital back end is integrated and sub-sampling realized digitally. (c) System block diagram showing ADC, FPGA, delay-line, and clock integrated in one board with high speed USB 2.0 computer connection. (d) Picture of the integrated sampling module developed at UT.

the signal at its input. The UT system UWB pulse has a base-band BW of 3 GHz, after the analog sub-sampler the BW is reduced to 300 KHz. The stretched analog signal is then fed to ADC input and sampled at a rate of 150 MHz.

The main advantage of analog sub-sampler is that it alleviates the analog BW requirement of the ADC. A low-cost slow ADC can be used to sample such signal easily. Also the operation of the digital back end (DBE) is simple. Data is received and processed in real-time and no need for memory to save data. The control system for DBE is simpler than its counterpart for the other two systems explained later.

One shortcoming is the low throughput of such system: it uses one sample per pulse. We use 10^4 pulses to produce one pulse and the throughput is 1k pulse/second. Also, the use of a clock with a frequency of 9.99 MHz which is a non-standard crystal oscillator frequency and requires a direct digital synthesizer (DDS).

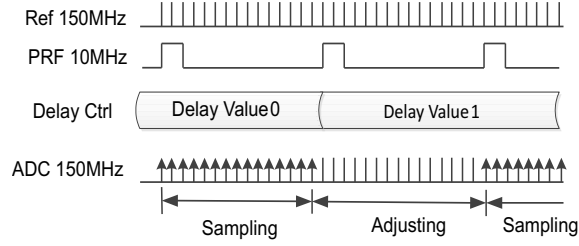
Analog sub-sampler operation is not robust, it requires certain amplitude and frequency for the input signal and the clock to operate correctly. The design of our analog sub-sampler is based on wide band balun with excellent balance over the whole RF bandwidth, which is another challenge for such category of sub-samplers.

Delay-Line Sub-Sampler

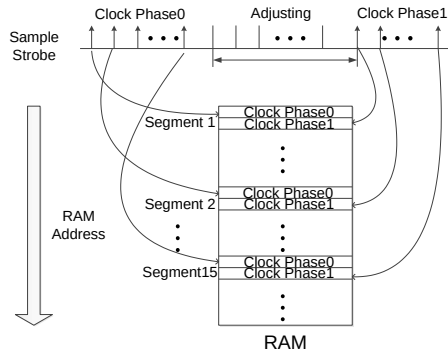
Here we got rid of the analog sampler, we feed the UWB signal directly to ADC input. The ADC required for such design has a wide analog bandwidth of 3GHz. The sampling clock is driven by a 150 MHz crystal oscillator, the UWB signal is sampled 15 times per one UWB period, the Delay line chip is then used to delay the clock by 10 ps and another 15 samples are acquired.

The Memory is divided into 15 segments equal to the number of samples per one pulse period. Each segment corresponds to 6.667 ns of the 100 ns pulse period. Each segment contains ≈ 667 points. However, the segment contains about 700 to 780 point due to delay line non-linearity as discussed later.

The samples are sent to their respective places in the memory allocated on the FPGA. The data are ordered as shown in Fig 4.5.



(a)



(b)

Figure 4.5: Sampling process using delay-line and on-board crystal oscillator. (a) Timing diagram of the sampling clock and the delay. 15 samples are acquired per UWB cycle and the clock is delayed by 10 ps for the next 15 samples. (b) Memory management and samples storage in their orderly place.

After collection of points that cover the whole UWB pulse and all the memory positions are filled. We stop sampling and the data are read sequentially, it is sent to the next stage of processing where we find the pulse time of arrival.

The processed data is sent over USB, the whole pulse or the ToA are sent. USB 2.0 is fast for ToA transmission, It is not fast enough for a whole pulse transmission and we need to control the amount of data transmitted. The on-board USB control chip has a stack that buffers the data before transmission, when it fills up, a USB Flag is set and we use it to stop the data acquisition, until the stack is empty again, Fig 4.6a.

The localization system tag clock is not synchronized to the clock at the base stations. The delay-line sub-sampling is not a real-time operation like its analog counterpart. We can see in Fig 4.6b that the point we start storing the samples is critical for acquiring a correct frame. Frame 1 started at some point within the pulse and the pulse is split between two frames. For a correct leading edge calculation the pulse should take place completely in one frame, frame 2 is an example.

We actively maintain the reference base-station pulse, BS1, at the center of the frame, by following steps in Fig 4.6c. We use the leading edge algorithm to find the arrival time of the pulse relative to the beginning of the frame. If the time of arrival is > 7000 points, we start storing next frame at 1000 point later. If time of arrival is < 5000 points, we start sampling 1000 points earlier.

Delay-line sub-sampling has several advantages. it increases the throughput of the system, In our implementation, it has been increased 15 times. It works without the sensitive operation of the analog sub-sampler. All the clocks used are standard frequencies, they do not require synthesis.

On the other hand, it has some disadvantages. It requires an ADC with wide analog BW, and memory for saving the samples. Operation is not real time, it requires synchronization between frame start and pulse.

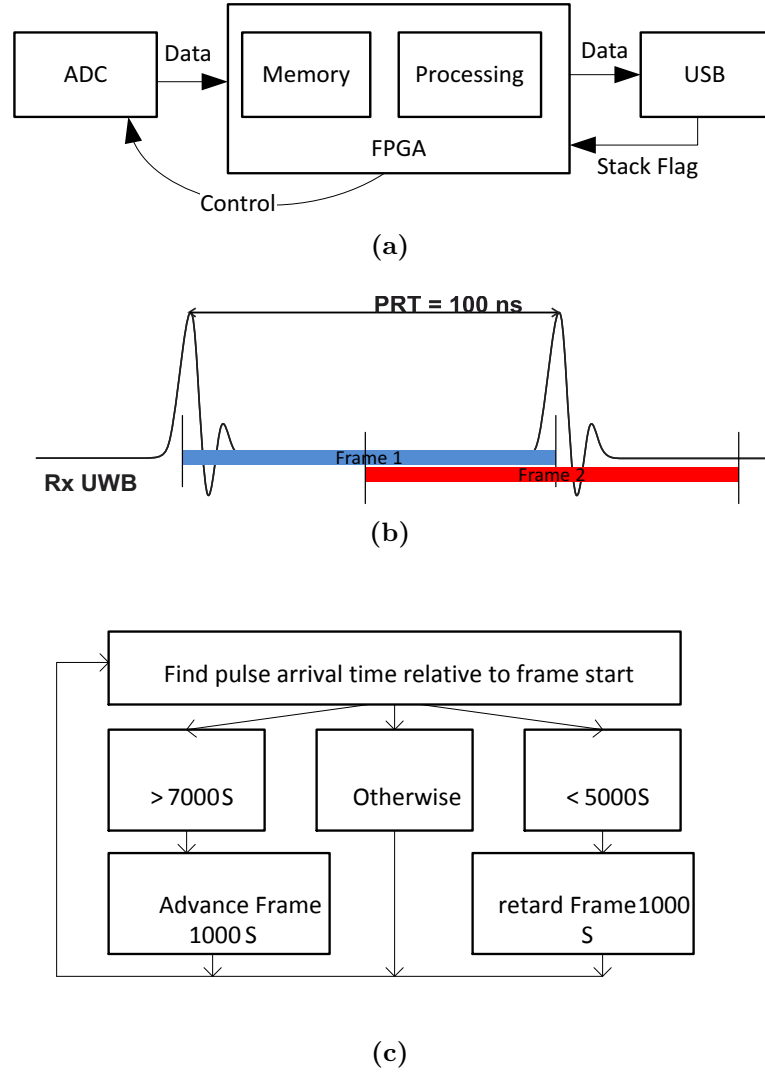


Figure 4.6: (a) FPGA controls the ADC operation based on USB stack availability. (b) and (c) Frame timing position control. (b) For frame 1, pulse is split between two frames and that will result in erroneous ToA. Frame 2 will lead to correct arrival time determination. (c) The frame position is controlled based on the arrival time of the pulse relative to frame start.

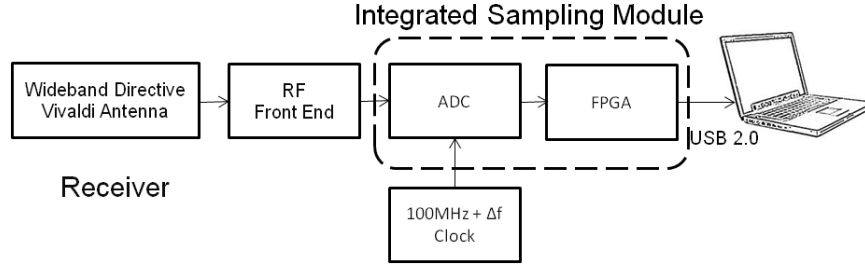


Figure 4.7: Block diagram for direct sample frequency synthesizer digital sub-sampler.

One major shortcoming is the delay-line SY100EP196V itself. It is controlled through 10 bit word, to select the delay in 10 ps steps. The delay-line is not linear, that causes intolerable errors in finding the tag position as explained later.

Direct Sampler with Frequency Synthesis

To solve the tremendous error introduced by the non-linearity of the delay-line, explained later, we developed a new method that do without the delay-line, it maintains high through-put. A clock with a period $10 \text{ ns} + 10 \text{ ps}$ is used. The corresponding frequency is a little bit lower than 100 MHz. It acquires 10 samples per pulse period. The block diagram of the system is shown in Fig 4.7.

Samples positions in memory are found as shown in Fig 4.8. The memory is divided into 10 segments, where segment size is 1000 points.

The samples are stored in memory such that the retrieved pulse points are in correct sequential order when we read them from memory. We receive 10^4 from the ADC. We start by storing sample 0 in segment 0 position 0, sample 1 in segment 1 position 1, and so on. We can use a simple relation to find the segment and position: Segment number = $n \bmod 10$; memory position inside the segment = $n \bmod 1000$, Fig 4.8. Where n is the order the points received by from the ADC.

After storing 10^4 samples, we have covered a whole UWB period, we read the memory where we stored the pulse sequentially, the pulse saved in right order.

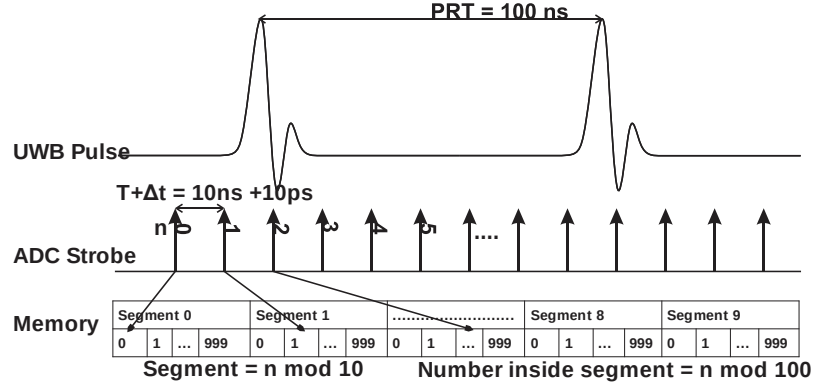


Figure 4.8: Acquisition and storage of samples in memory for a clock of period 10 ns + 10 ps while the UWB signal period is 100 ns. Memory is divided into 10 segments each of 1000 position. In order to produce an intelligible pulse when we read the memory sequentially, the data is written following a certain algorithm.

In general for using this method with a clock of sampling period of $T_s + \Delta t$ and UWB period of T_0 . We divide the memory into $n_s = T_0/T_s$ segments. The number of total points per UWB period is $n_t = T_0/\Delta t$. The number of points per segment $n_{ps} = n_t/n_s$. To find memory address of a sample number n , where n is the order of the sample as it received from the ADC. We find the segment number = $n \bmod n_s$ and the number of the sample inside the segment = $n \bmod n_{ps}$.

This method performs superior to the two other methods. It has high throughput and it does not utilize a delay-line that suffers non-linearity problem. It suffers one problem though that it has a stringent stability requirement of the pulse generation and sampling clock. This error is discussed in section 5.2.3.

Chapter 5

Discussion of Errors in Sub-Sampling Methods

As we pursuit more efficient and simple ways to develop high sampling rate, and low cost systems, we designed two systems: Delay-line sub-sampling and direct sampling with frequency synthesizer. However, we discovered some problems with the two systems that we discuss here.

5.1 Delay-Line Non-Linearity

We used delay-line SY100EP196V by MICREL, it is digitally controlled by a 10 bit word. It has a 10 ps resolution for LSB b_0 . The chip is designed for clock synchronization applications. Bits have delays that deviate their 2^n values, n is bit number, e.g. b_1 and b_9 have delays 26 ps and 4300 ps that deviate 6 ps and -820 ps to their nominal binary values.

Using the delay values provided by the data sheet, the number of phase shifts required to cover one segment of the pulse is 780. Using this number of shifts, acute distortion to the pulse that causes large ToA errors is noticed, Fig 5.1a. In Fig 5.1b a small part

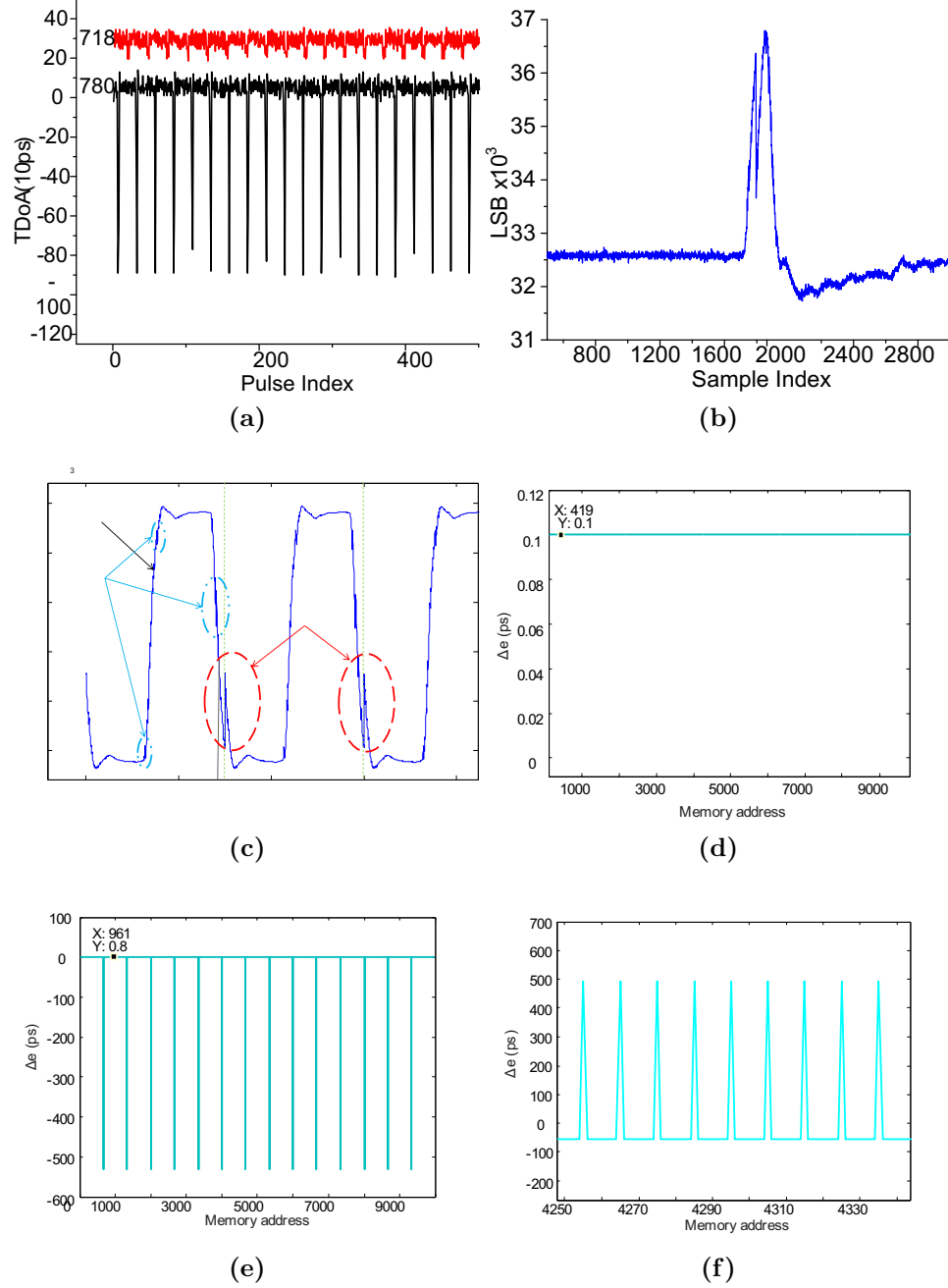


Figure 5.1: Error created using delay-line based sampler: (a) Time difference of arrival error; 780 samples per segment introduces about $80\text{ to }90 \times 10\text{ps}$ spike error; 718 samples/segment reduces error down to about 100 ps spikes error. (b) Distortion in sampled pulse where small part of the signal repeats itself, where 780 samples/segment exceeds the phase shifts required to cover one segment time i.e. 6.6667 ns. (c) The same 150 MHz sampling clock fed to the ADC input, 780 samples/segment shows two main distortions: signal repetition, and high order bits error. Error in equivalent sampling period (d) Analog sub-sampler, (e) Delay-line sub-sampler, and (f) Direct sub-sampler.

of the signal repeats itself. 780 shifts exceed the samples/segment required to cover one segment i.e. 6.667 ns, and it trespass over to the next segment.

In Fig 5.1c we used the same sampling clock as the input for the ADC of the sampling module. We can notice two kinds of distortions: 1- repetition distortion that takes place at segments boundaries, and 2- distortions that manifest when high order bits switch values as we advance the delay-line delay, the new value will have smaller shift, e.g. a delay control word of $(127)_d$ or $(0000111111)_b$ will cause a phase shift of 601 ps, while a control word of $(128)_d$ or $(0001000000)_b$ will cause a shift of 523 ps.

In Fig 5.1a we see the error we get as we utilize two different samples/segment. For 780 samples/segment we have about 80 to 90 sample time, 10 ps, error as a consequence of the segment boundary problem. However when we used the best samples/segment fit, 718, we still have 10 20 sample time error which is unacceptable for our application. The utilization of such delay-lines in accurate sampling is possible. It requires an intensive calibration to find the control word sequence that guarantees incremental delays, and find the precise delay for each control word. After such calibration, we will still have non-uniform sampling that will complicate the system.

5.2 Sensitivity to Clock Drift

Clock imperfections have a great impact on noise, distortion, and error in sub-sampling systems. Total jitter in the system adds an equivalent amplitude noise to the sampled UWB signal. Relative clock drift between the pulse generating clock and the sampling clock causes different forms of errors in the three sub-sampling systems depicted here.

5.2.1 Analog Sub-Sampler

For Analog Sub-Sampler, one sample per pulse, system suffers scaled equivalent sampling period Δt when clocks has a drift. If we have 0.1 ps relative drift between

pulse generation clock and sampling clock; the actual equivalent sampling period will be 10.1 ps while we will base our calculation on one sampling period equals 10 ps.

We have a pulse generation clock period of $T_0 + e_1$, where e_1 is the time drift. The sampling clock has a period of $T_s + \Delta t + e_2$. Let us assume e is constant over the time required to acquire a whole pulse. In presence of time drift the equivalent sample period = $\Delta t + \Delta e$, where $\Delta e = e_2 - e_1$. If the delay time of pulse received by base-station 1 (BS1) is t_1 , and by BS2 is t_2 . The TDoA calculated is $[(t_1 - t_2)/(\Delta t + \Delta e)] \times \Delta t$ and we have a percentage error of $\Delta e/(\Delta t + \Delta e)100\%$. An example if we have an error $\Delta e = 1$ PPM of the clock period, 100 ns, we will end up with 1% error in the TDoA. In Fig 5.1d, we can see the error Δe which is a constant.

5.2.2 Delay-Line Sampler

In delay-line sampler it is a little bit more complicated. Fig 5.1e shows the error Δe as a function of the sample number in the sequence they are read and processed. For this figure $e_2 = 0.05ps$ and $e_1 = -0.05ps$. Notice that two neighboring samples in one segment are away by 15 sampling clocks and each are at consecutive UWB pulse. Hence, the error is $T/T_s \times e_2 - e_1 = 15 \times 0.05 + 0.05 = 0.8ps$. Moreover, all the drift accumulates at the segment boundary and we have a break that shows as a spike. The spikes in equivalent clock period show as a signal distortion at the segment boundaries: missing part of the signal for $-\Delta e$, and repetition error, similar to Fig 5.1b, for $+\Delta e$.

5.2.3 Direct Frequency Synthesizer

Fig 5.1f shows the error using the third sub-sampling method. The spikes are more frequent, once per 10 samples. The time difference between neighboring samples is larger, they do not belong to consecutive pulses anymore. Clock drift error is more pronounced than the two aforementioned methods.

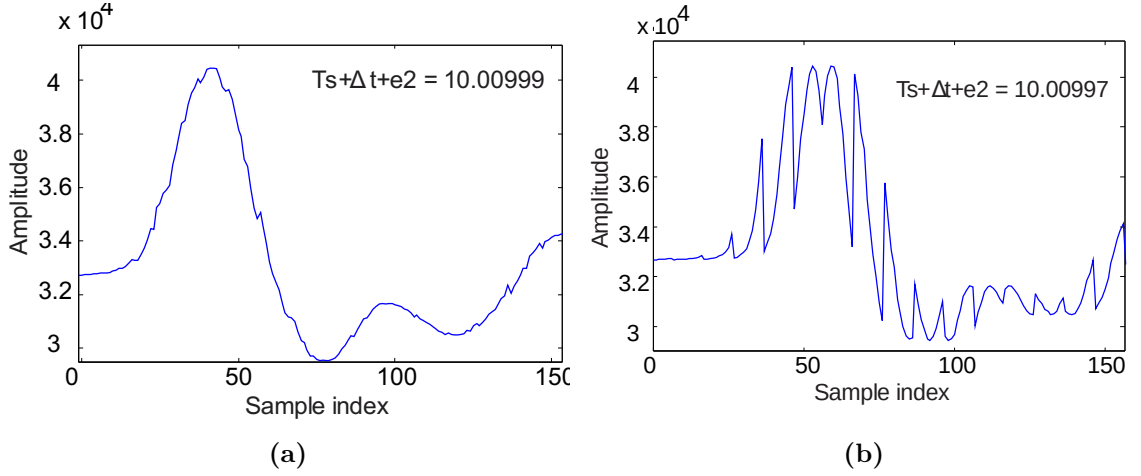


Figure 5.2: Distortion in UWB pulse experiment for direct synthesizer method: (a) with sampling clock period of 10.00999 ns the distortion in pulse is minimized; (b) sampling clock period of 10.00997 the distortion has tremendous amplitude.

The distortion that takes place at the spikes can be used to find the clock rates that will minimize such error. Sampling clock frequency can be tuned to minimize drift error. Fig 5.2a shows a sampling clock with period 10.00999 ns shows almost no clock drift distortion, while Fig 5.2b shows intolerable distortion with a period of 10.00997 ns. That is just 20 fs change.

5.3 Conclusion

Real-time sampling rate is still insufficient for high speed applications. A good alternative is equivalent time sampling. At UT we have developed three equivalent time sampling systems. Table 5.1 shows a comparison of the three systems.

First system alleviates the requirement on ADC BW, it utilizes simple FPGA code. However, it has a very low throughput. The clock Drift will cause an error that we cannot notice on the sampled pulse. The system requires a separate analog sub-sampler circuit and a non-standard clock frequency.

Table 5.1: Sub-Sampling Techniques Comparison.

Sub-sampler	Analog	Delay-Line	Direct + Freq. Synth.
ADC Analog BW	Small	Large	Large
ADC Speed	Small	Small	Small
Sens. to Jit.	RX+TX	RX+TX	RX+TX
Sens. to Drift	smallest	medium	highest
RX complexity	high	simple	Medium
Throughput	Low	High	High
FPGA code	Simple	Complex	Complex
Non-Lin. prob.	Non	High	Non

The second system simplifies the receiver chain. It removes the need for the analog sub-sampler and the non-standard clock. It increases the throughput of the system as well. The delay-line chip suffers though large non-linearity errors that makes it unsuitable for high accuracy applications.

Third system uses the same hardware for the second system. It increases the throughput of the system. It uses non-standard clock frequency.

The second and third systems require a wide analog bandwidth ADC as wide as the received analog signal. They also require complex FPGA code for control and storing. The jitter impacts the three systems in the same way where the total jitter equals the sum of the transmitter and receiver clock jitter in the square sense.

The third system is more sensitive to the clock drift. However this sensitivity is easily visualized in the sampled signal and that can be used to tune out this clock drift by real-time monitoring such error. System three supplies high throughput while maintaining lowest accuracy issues.

Chapter 6

Towards Integrated UWB Localization Systems Using MMICs and Mixed Signal Components for Low Power Consumption and Fast Processing

First generation UWB precise localization systems have been successfully demonstrated by many groups. Most of these developed systems were based on hybrid components and separate digital development circuit boards for digital signal processing. But these discrete components are mostly heavy, bulky, and energy hungry. Recently, many MMIC circuits have been developed and present new opportunities for evolving low cost, compact, and significantly reduced power consumption systems opening the door for a new set of UWB applications. Here, we present our efforts to replace some of these hybrid components by recently developed MMIC chips, and an integrated digital module developed by ULM University and UT respectively. Similar performance was achieved but rather with significantly reduced

power consumption, much smaller footprints, and higher throughput. Details of such integration will be presented here.

6.1 Introduction

At the University of Tennessee (UT), we have been involved in developing a low cost, compact, and precise localization UWB system. Real-time 3D localization accuracy in the range of few mms has been demonstrated [43]-[30]. Such high accuracy is needed for wide range of applications including surgical navigation, sensitive asset tracking, and high precision tool manufacturing.

UT First generation system design was based on off-the-shelf components and hybrid assembly. UWB positioning system consists of one transmitter (tag) or more, and multitude of base stations (receivers). Typically, at least two receivers are used for 1D localization, 3 base stations for 2D localization, and 4 base stations for 3D. However, redundancy in the number of base stations should improve the localization accuracy. The UT transmitter is comprised of a narrow pulse generator of 300 ps using a step recovery diode (SRD), subsequently this pulse modulates an 8 GHz VCO through a mixer, and next the signal is amplified using a medium power amplifier. The pulse is periodically produced using a 10 MHz clock. In the receiver side, the received signal is amplified using an LNA block; later an energy detection mixer is used. The pulse signal is retrieved using a sub-sampling scheme [43]-[30]. This localization system is generally bulky, and energy hungry even though mm accuracy was achieved.

Recently there has been significant advancement in MMIC and CMOS chip designs geared towards UWB and fast time domain processing, some quite variant examples of these efforts are shown in Table 6.1. Ref. [44], for example, is a mono-static FMCW Radar; its transceiver is integrated except for a PLL loop. The system is used to measure the distance of a reflector moving on a linear positioning unit for a 3 m and has demonstrated only 250 ?m error. Ref. [45] discusses the design of a 12 channel transceiver capable of a positioning accuracy of 3 cm. It is based on

Table 6.1: Integrated Designs Performance.

	Technology	Application	P_{dc}	Error	BW	Range	Area	Remarks
Boch [44]	MMIC SiGe	FMCW	245 mW	250 μ m	8 GHz@24GHz	3 m	1.51 mm^2	Transceiver
Sing [45]	0.18 μ m CMOS	802.15.4a	NA	3 cm	3 to 9 GHz	10 m	4.5 mm^2	Transceiver
MIT [35]	0.18 μ m SiGe	802.11a	53 mW	2.7e-3 BER	3.1 to 10.5 GHz	10 m	2.3 mm^2	Front-end
Belg [36]	0.13 μ m CMOS	IR-UWB	4.3 mW	10 to 1.8mm	0.5@1GHz	10 m	4.52 mm^2	Receiver
Florida [37]	90 nm CMOS	Micro-Doppler	190 mW	20 μ m	NA@60GHz	2 m	0.73 mm^2	Transceiver
Berlin [46]	0.13 μ m CMOS	FMCW	42 mW	NA	0.25@24 GHz	50 cm	2 mm^2	Transceiver

IEEE802.15.4a for a low data rate with localization capability for sensor networks. Ref. [45] has integrated the whole RF system; but leaving a space on the chip left for digital circuitry integration later on. In [35], a design of UWB receiver direct-conversion front-end that covers the 3.1-10.6 GHz band with a NF of 3.3-5 dB that was integrated with a switchable notch filter.

In [36], the authors combined both analog front-end and a digital back-end onto one chip; they used IQ correlator receiver to save energy with a power consumption of only 4 mW for the whole transceiver. They achieved 1.8 mm tracking accuracy over 160 μ s averaging time.

Ref. [37] shows a 60 GHz Doppler radar transceiver developed for non-contact vital sign detection. It demonstrates the ability to detect 0.2 mm vibration at 2m stand-off distance.

Ref. [46] is a transceiver for FMCW radar that has a 1.5 mm resolution for a 50 m distance.

Clearly we observe in all these MMICs implementations the tremendous space saving; the robustness enhancement of the systems by minimizing the number of interconnection linking the various system components, the extremely low power consumption, and the neat mixing of digital and analog circuitries in one chip.

In an effort to reduce the circuit size and power consumption in our current system, UT in collaboration with Ulm University has replaced some components by MMIC RF components that were developed at Ulm University for both the UWB tags and receivers. We have also integrated the digital backend into one multilayer board instead of using various evaluation boards for the ADC and FPGA. We mounted the ADC, digital delay line, FPGA, and high speed USB using a PCB multilayer board. Integration adds in particular to the reliability of the system, saves on its power consumption, facilitates practical utilization, and enhances the portability of such a system.

In this paper we will describe in detail the transmitter front-end in section 6.2, the receiver front-end in section 6.3, the sampling circuits implementation in section 6.4,

Table 6.2: Pulse Generators Comparison.

	SRD pulse generator	MMIC chip
Pdc	1008 mW	6mW
Impulses voltage	1 Vpp	250 mVpp
FWHA	300 ps	300 ps
Frequency spectrum	5 11 GHz	3.5 8.4 GHz

in section 6.5 we show experimental measurements results, and we conclude in section 6.6.

6.2 Transmitter Front End

The first generation non-coherent UWB positioning system currently being used for indoor positioning at UT has been discussed in detail in [43]-[30]. However, the power requirement of the transmitter (or tag) is over 1 W—which restricts the use of this system in only low power applications. Fig. 6.1a outlines UT current discrete tag which utilizes a Hittite 506 VCO, a Hittite 441 medium power amplifier MPA as well as a Micrometrics MSD700 step recovery diode-based pulse generator. The VCO operates at 8 GHz, mixed with a 300 ps FWHA narrow pulse generated by the SRD circuit. The modulated signal in the range of 5 GHz to 11 GHz is amplified using a MPA and is fed to a monopole antenna. Picture of the discrete tag is shown in Fig. 6.2a and the generated pulse is shown in Fig. 6.13.

Recently Ulm University developed UWB MMIC chips that can impact our transmitter and receiver design. The block diagram of a SiGe MMIC-based UWB transmitter developed by Ulm University is shown in Fig. 6.1b. An integrated board design with the SiGe MMIC at the feed point of a UWB dipole antenna is shown in Fig. 6.3. This integrated MMIC chip is comprised of a Schmitt trigger, a current mirror, and a quenched cross-coupled LC oscillator; more details on the MMIC design can be found in [47]. MMICs were realized using an inexpensive Si/SiGe HBT technology using MIM capacitors, and 4 types of resistors as well as 3 metallization layers. All devices

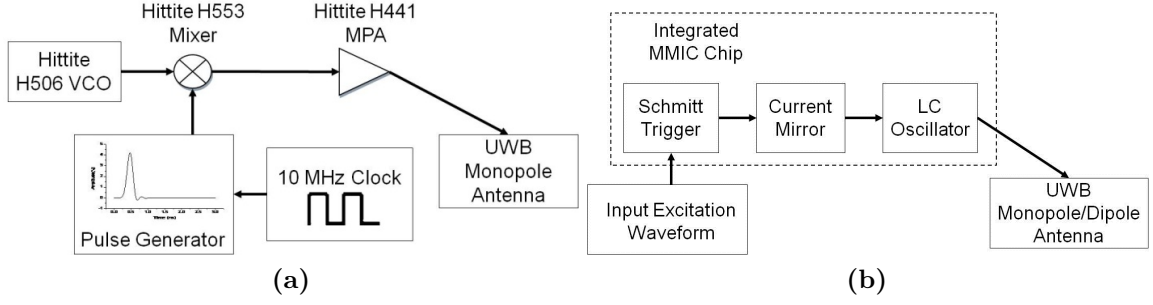


Figure 6.1: Block diagram of UWB transmitter front-ends: (a) discrete, (b) integrated into a MMIC chip.

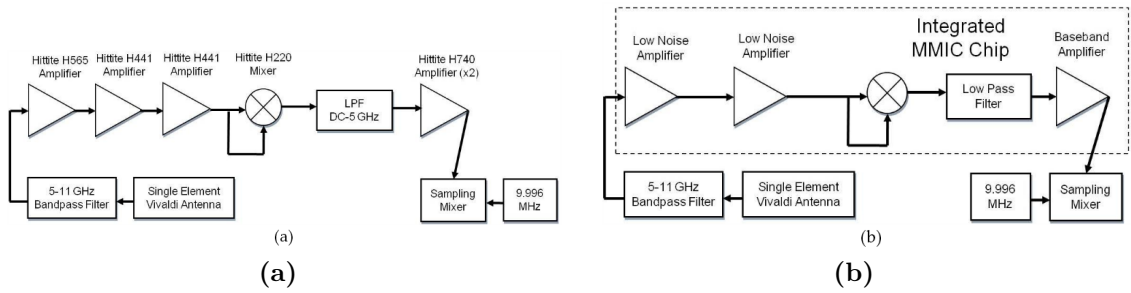


Figure 6.2: Block diagram of UWB receiver front-ends: (a) discrete, (b) integrated into a MMIC chip.

were fabricated on a low resistivity 20 cm. For the transmitter MMIC design, a current spike generation circuit, controlled by an RC charging circuit, is used to trigger an LC oscillator. The spike generation circuit allows a repetition rate well in excess of 1 GHz, but we used it here for only 10MHz. Meanwhile, a deliberate asymmetry and a parallel resistor are introduced to the oscillator core for fast startup and quenching off, generating impulses of sub-nanosecond duration and a large 10 dB bandwidth. Fig. 6.5a is a microphotograph of the designed differential impulse generator circuit. The total power consumption of the chip is only 6 mW at a 1.5 V supply voltage. The maximum power spectral density (PSD) is below the FCC limit of -41.3 dBm/MHz, and it has a 10 dB bandwidth of 4.9 GHz from 3.58.4 GHz.

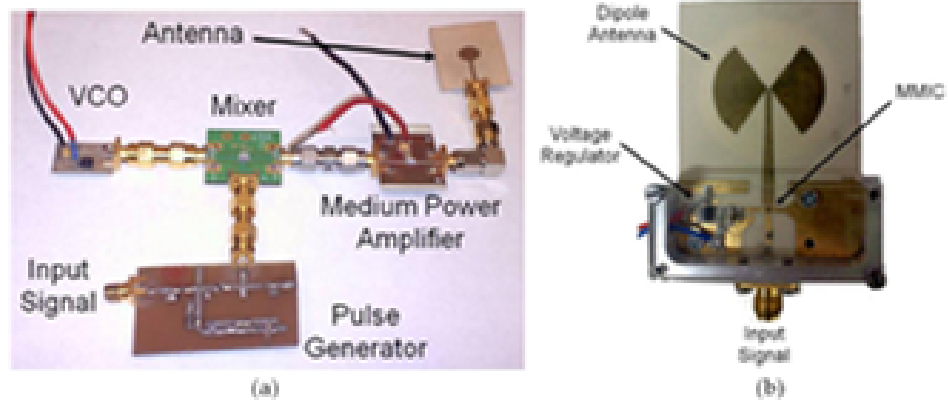


Figure 6.3: UWB transmitter front-ends: (a) discrete, (b) integrated into a MMIC chip.

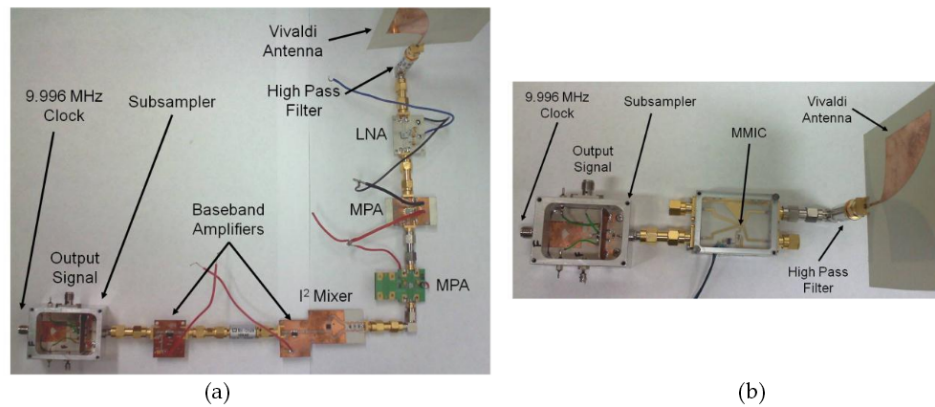


Figure 6.4: UWB receiver front-ends: (a) discrete, (b) integrated into a MMIC chip.

6.3 Receiver Front End

A block diagram of the previously utilized discrete UWB non-coherent receiver is shown in Fig. 6.2a. It includes a directional Vivaldi antenna, a band-pass filter, three stages of amplification using Hittite H565 and 441 amplifiers, a squaring mixer using Hittite H220 mixer, a low-pass filter DC-5GHz, a baseband amplification using Hittite H740 amplifier, and a subsampling mixer. Fig. 6.4 shows a picture of this receiver chain. The main drawbacks of this discrete receiver include power consumption (2.15 W load requirements) and relatively large size, more design details are given in [30]. Alternatively, MMIC circuits can be utilized here as well. Fig. 6.2b shows a block diagram of the MMIC-based receiver where discrete amplifiers, squaring mixer, and a low-pass filter components have been replaced by an integrated SiGe MMIC chip. The core of the energy detection receiver is the squaring circuit which is based on a Gilbert cell four quadrant amplifier comprising two differential stages in parallel with cross-coupled output, complemented by a low pass filter and a differential output buffer. An LNA stage is used to provide an adequate signal level before mixing. The LNA micrograph is shown in Fig. 6.5b, and it measures 0.43 mm x 0.61 mm. Fig. 6.4 shows a picture of the UWB non-coherent receiver using the integrated SiGe MMIC front-end. More information on the design of the MMIC non-coherent receiver front-end can be found in [5]. This developed MMIC receiver provides a significant reduction in the RF front-end size and total power consumption including the DC-DC converter losses from more than 3 W to around 190 mW.

6.4 Design Implementation of Compact Sampling Module

A UWB impulse system typically requires an extremely high sampling rate that could be very expensive to implement. Equivalent time sampling has been used as an alternative [42]-[4]; its strategy is to reconstruct a complete input waveform

by progressively shifting the sampling clock timing after each signal cycle and accumulating captured samples during certain input signal cycles.

In our previous work, the equivalent time method has been successfully implemented to achieve mm indoor localization system [43]-[30]. However, this previously developed prototype has some limitations which have significantly degraded the system performance. The previous system utilized separate evaluation boards for ADCs and FPGA which have incompatible interfaces. Thus, twisted wire pairs were used for interconnection and they not only brought un-robustness and crosstalk issues but also limited the bandwidth of the sampled data, Fig. 6.6.

In order to improve the system performance and maintainability, we have completely redesigned the high speed data acquisition module by successfully integrating ADCs and FPGA in a 4-layer printed circuit board (PCB) [48]. The photograph of the newly designed compact sampling module is shown in Fig. 6.8. In addition to increase the capability of detecting very weak signals the 9-bit ADC has been replaced by a 16-bit ADC in the new module, which has significantly enhanced the system dynamic range with a 10ps capture resolution that is equivalent to a 100 GS/S sampling rate.

6.4.1 Compact Sampling Module Architecture

The detailed block diagram of our novel compact sampling module is shown in Fig. 6.9. The module uses a 2x2 switch to control the clock selection. It can work with the on-board 150 MHz crystal oscillator clock to get 15 samples per pulse or external clock; we currently use the external clock port with a clock rate of 100 MHz and 10 samples per pulse. A USB 2.0 transceiver using the commercial chip CY7C68013 is also implemented in the module and used to upload the digitized data to a computer. It is noted that designing a wideband ADC front end circuit is critical to achieve a high performance in the data acquisition module. Using either an amplifier or a transformer is a typical way to drive ADC differentially [49].

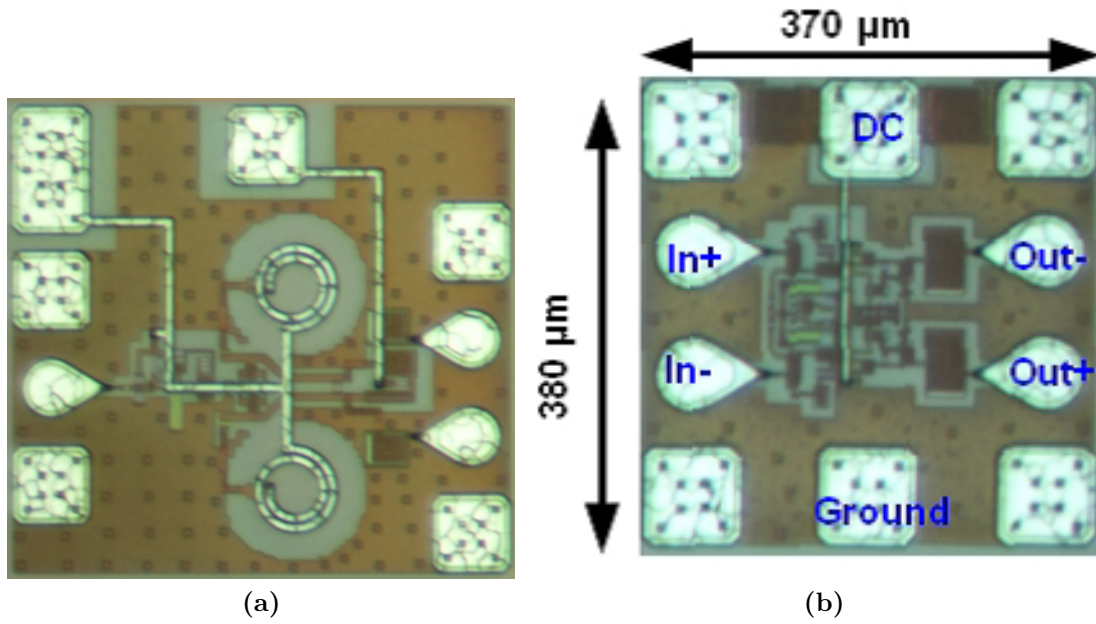


Figure 6.5: Micrograph of the MMIC chips utilized in UT localization system: (a) differential impulse generator, (b) differential LNA.

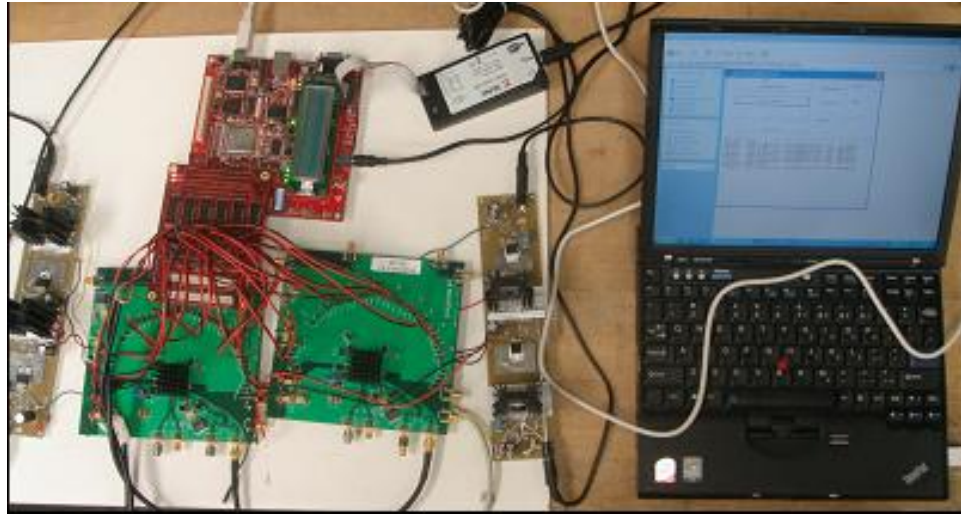


Figure 6.6: Old prototype that used separate evaluation boards. It suffered cross-talk, un-robustness, and limited bandwidth.

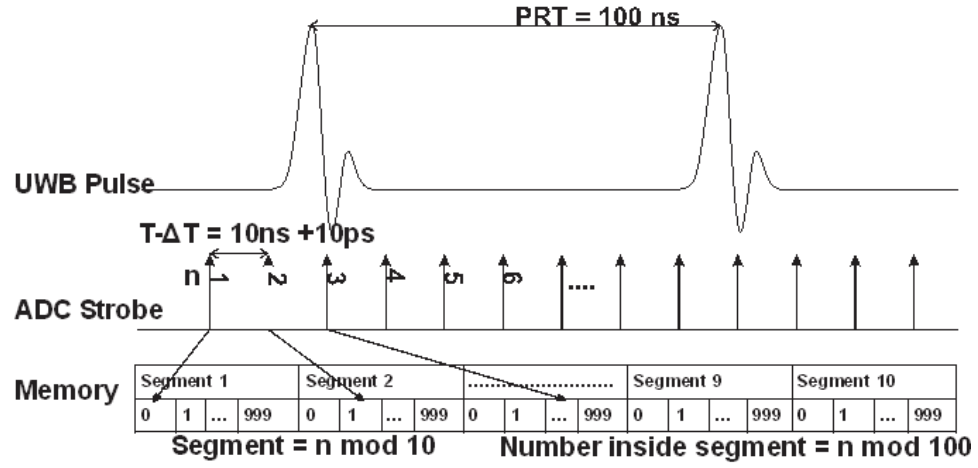


Figure 6.7: Graphical representation of the equivalent time sampling scheme.

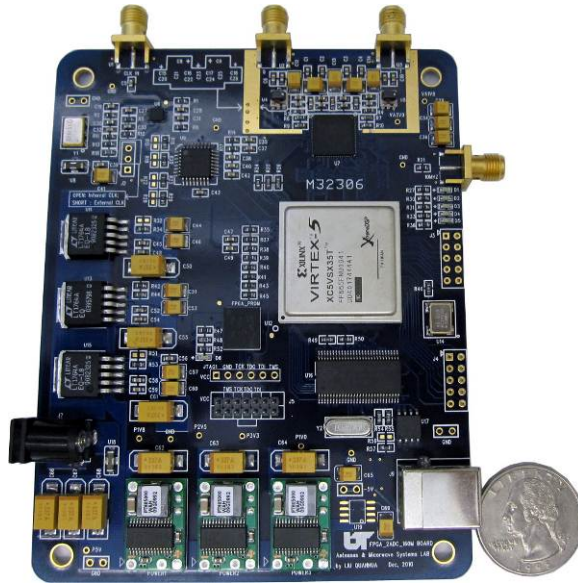


Figure 6.8: Photograph of newly developed sampling module, integrating a dual channel ADC, a Xilinx Virtex-5 FPGA, a delay line chip, and USB2.0 transceiver in a 4-layer PCB board.

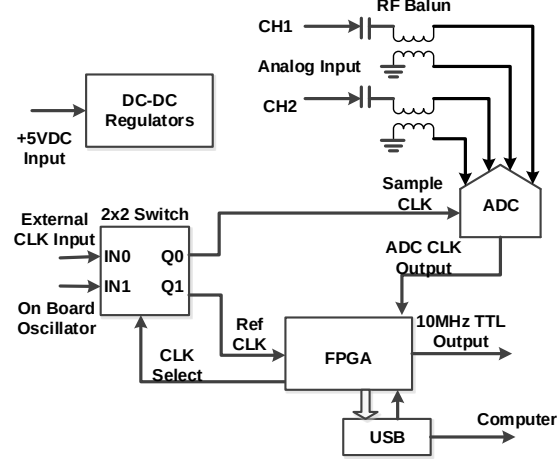


Figure 6.9: Detailed block diagram of the novel compact sampling module. The module provides two analog input channels, CH1 and CH2.

6.4.2 Data Acquisition Technique and FPGA Implementation

The subsampling process is used to circumvent the requirements for a high sampling rate of 6 GHz necessary for the 3 GHz signal based on Nyquist. The subsampling scheme exploits the periodicity of the sampled signal where one sample at least is acquired per pulse. It requires 10,000 point to reconstruct a single pulse.

The acquisition technique is illustrated by the graphical representation in Fig. 6.7. In order to reconstruct a complete UWB pulse using the equivalent time sampling scheme, it utilizes a train of pulses that are assumed invariable in shape. We successfully utilized a sub-sampling scheme that achieves high throughput and acceptable precision and is based on using a sampling clock with a sampling time $T + \Delta t$. The samples are stored in the memory in their corresponding location. The parameter Δt represents the real sampling interval of the equivalent time sampling scheme. In our system, we used an external clock with a 10 ns T and a 10 ps Δt , which is selected based on the preference of the application.

In a typical mode, Δt is set to 10ps which renders an equivalent sampling rate of 100 GSPS. The sampling clock period $T + \Delta t = 10\text{ns} + 10\text{ps}$ that corresponding to

clock frequency of 99.9000999 MHz. The memory is divided into 10 segments which represent the ratio of pulse repetition rate PRT and T. Each segment contains 1000 memory position with total memory size of 104 equal to the total number of pulse points. We start by storing sample 0 at segment 0 memory location 0; sample 1 at segment 1 position 1 and so on. A general equation for the segment number = $n \text{ mode } 10$, and memory location inside the segment = $n \text{ mode } 1000$, where n is the order of the samples received from the ADC. By following this scheme to fill the memory we will acquire the whole pulse in 103 received pulse periods and the samples will be saved in their right position in memory.

After the signal is sampled, we can either send the raw data to the computer and perform all the computation there, or process it first and send it later on. The on-board processing consists of low-pass filtering the raw UWB pulse to get rid of noise and sampling imperfections, and finding the ToA of the pulse through leading edge algorithm. The board uploads the data to a computer with a throughput rate of 27 MB/s. A high data uploading rate can significantly increase the system update data rate, which is of great importance in real-time detection scenario.

6.4.3 Signal Integrity (SI) Considerations in PCB Design

Several challenges need to be addressed when designing a mixed analog and digital PCB with high system clock speed and input analog frequency. The most common design issues affecting SI include impedance control, crosstalk, power/ground planes, and signal routing [50]. Especially for this mixed signal PCB design, the problem is even more critical as the input analog signal reaches 2.7 GHz and the system clock frequency approaches 100 MHz.

The most straightforward method in improving SI is to physically isolate the various components groups on the PCB. In our design, the clock, data converter circuit, the power supply and high speed logic are put in separate sections of the PCB to avoid any noise-coupling among them, as shown in Fig. 6.10.

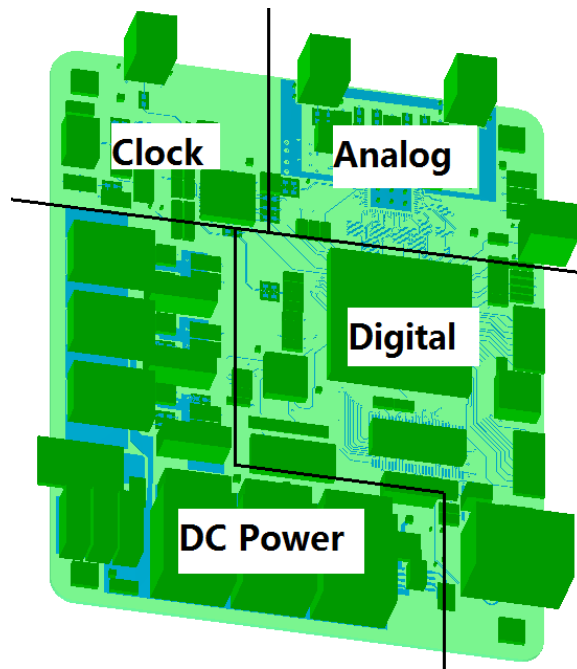


Figure 6.10: Layout plan of the designed PCB, putting clock, data converter circuit, power supply, and digital logic control in separate sections of the board.

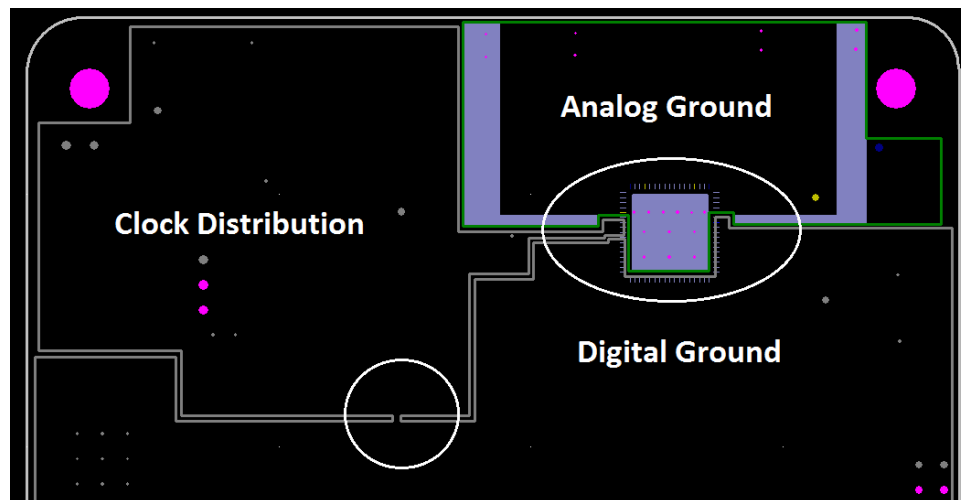


Figure 6.11: Strategy to split the ground plane into three regions: analog ground, digital ground, and clock distribution.

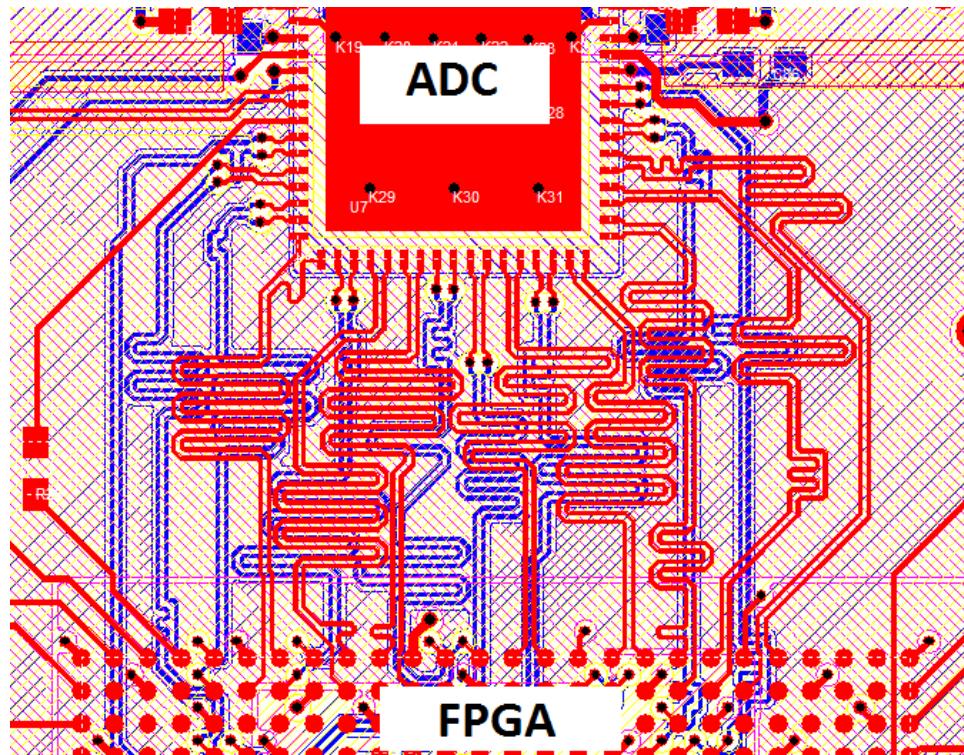


Figure 6.12: Equal length accordion-shaped lines are used to connect ADC output nets with FPGA input pins in the routing.

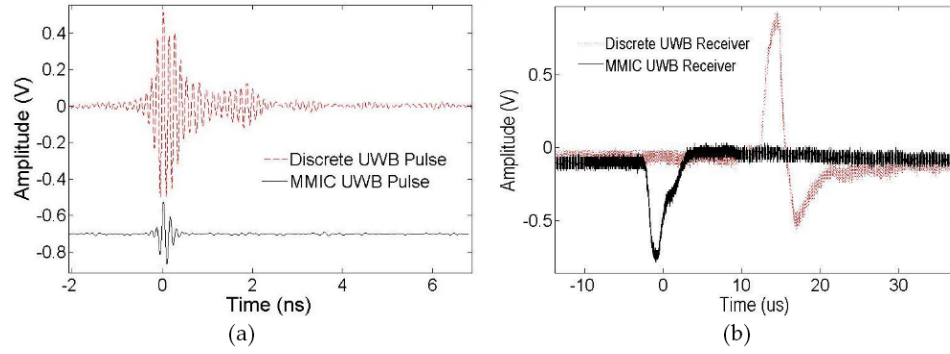


Figure 6.13: Measured transmitted UWB signals: in red UWB discrete pulse generator; in black MMIC UWB integrated generator.

Using a multilayer PCB in the design also helps in improving the SI performance, in terms of achieving solid power and ground planes and reducing the signal coupling and crosstalk. In our implementation, we used relatively low cost 4-layer FR4 PCB. For a mixed signal circuit design, the digital ground usually brings more noise than an analog one. The ground plane of the compact sampling module is partitioned very carefully into analog, digital and clock sections, as shown in Fig. 6.11.

The 16-bit ADC chip ADC16DV160 supports dual channel. The digital data is provided via dual data rate outputs and the logic standard utilizes a low-voltage differential signaling (LVDS). This results in only 16 pairs of LVDS signals. Termination of LVDS is not necessary at the FPGA input because Xilinx FPGA integrates digitally controlled impedance resistors inside the device. All these features have greatly minimized the PCB routing area. In the PCB layout, accordion-shaped lines are used to connect ADC output data nets with FPGA to equalize their lengths, as shown in Fig. 6.12. The equal length makes ADC signals arrive at the FPGA input pins at the same time, thus it can prevent logic errors in FPGA programming.

6.5 Experimental Results

A real-time oscilloscope with a 13 GHz bandwidth was used to record the output signals. The measured impulses for the MMIC generator with peak to peak amplitude

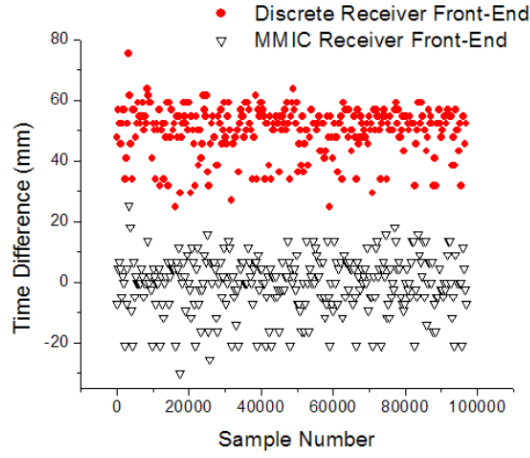


Figure 6.14: Raw time difference static data for two discrete front-end receivers versus two MMIC receivers in millimeters with MMIC data offset to zero for illustration.

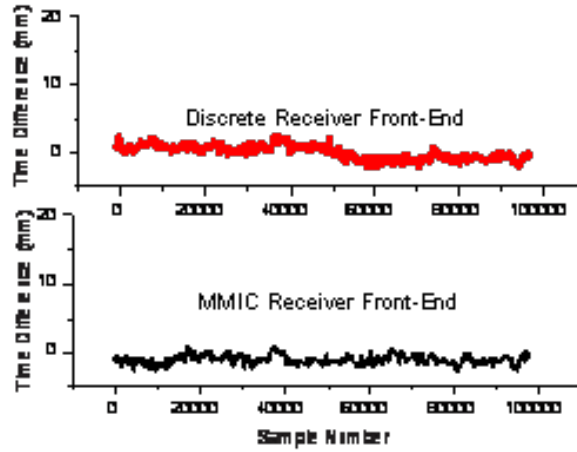


Figure 6.15: Time difference static data for two discrete front-end receivers versus two MMIC receivers in millimeters after applying a 300 sample averaging window.

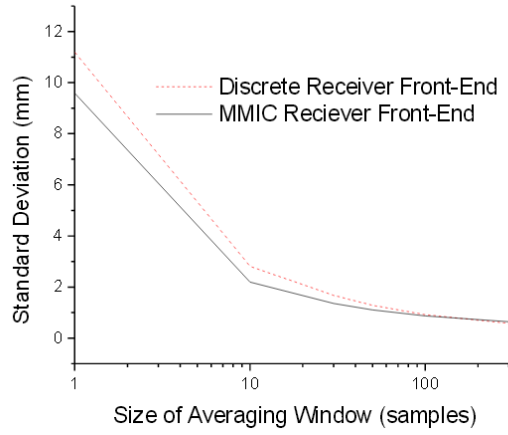


Figure 6.16: Standard deviation of static time differences comparing two discrete receiver front-ends to two MMIC receiver front-ends with a variable averaging window size.

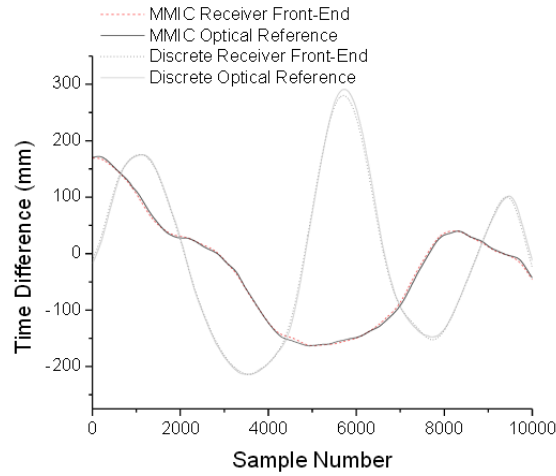


Figure 6.17: Dynamic time differences in millimeters as the tag is moved freely in the view volume comparing two discrete and two MMIC receiver front-ends. An optical tracking system provides 3-D real-time reference data.

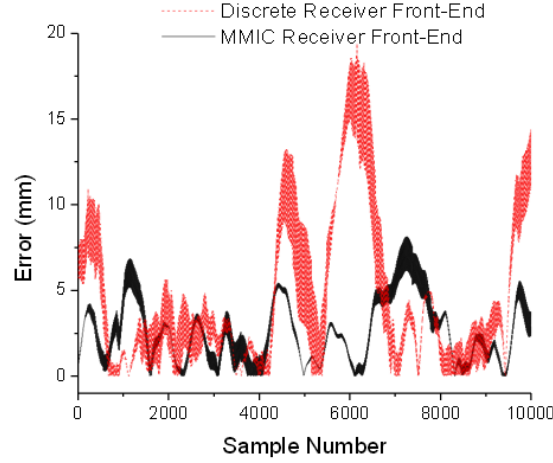


Figure 6.18: Ranging errors in the dynamic time differences shown in Fig. 6.17; when comparing the UWB time difference data to the optical (ground truth) time difference data.

of 210 mV while 1 V for the discrete tag, and a full width at half maxima of an envelope of 300 ps are shown in Fig. 6.13.

Static and dynamic real-time experiments were undertaken to compare the high accuracy localization performance with discrete and MMIC front-ends. The leading-edge of the UWB pulses was located via a FPGA algorithm. The time difference is used in a time difference of arrival algorithm and represents the difference in samples as measured by the FPGA between two channels. This sample difference is then converted to millimeters using the sub-sampling period Δt . Fig. 6.14 shows raw static data comparing the time difference of two discrete and two MMIC front-end receivers. The raw standard deviations are 11.2 mm and 9.59 mm for the discrete and MMIC receivers respectively. Fig. 6.15 shows the same data after applying a moving averaging window of length 300.

Fig. 6.16 shows how the standard deviation decreases for larger averaging windows with no difference between discrete and MMIC receivers.

Fig. 6.17 shows a dynamic experiment where a tag moves freely around the view volume causing dynamic changing of the time differences. The optical tracking system is calibrated to the UWB tag and all four UWB receivers to provide 3-D real-time

reference data. As shown in Fig. 6.17, the UWB and optical systems follow identical trends within a few millimeters.

Fig. 6.18 shows the absolute difference between the time differences for the UWB positioning system versus the optical positioning system. The MMIC receivers have a RMSE of 2.56 mm while the discrete receivers have a RMSE of 4.47 mm over all 10,000 samples.

6.6 Conclusion

UWB systems performance has significantly improved in the last few years. Efforts are underway to develop MMIC chips and multilayer boards solutions to replace previous discrete designs. MMIC chips include the pulse generator, pulse shaping circuit, and the medium power amplifier. The receiver chip could include an antenna, LNA, and energy detection circuit. Meanwhile, digital signal processing is handled by a multilayer board integrating the sub-sampler and an A/D converter.

Preliminary results are very encouraging, where the performance of the discrete and MMIC receiver front-ends are very similar in both static and dynamic experiments, showing the potential of MMIC front-ends in future systems targeting high accuracy indoor positioning while reducing cost, size, and power consumption. However, integrating MMICs into the UWB transmitter and receiver chains will significantly reduce power consumption and size.

Additionally, digital back end integration made the system much more robust by eliminating the wire connections among different digital modules. It also made feasible to send higher data rate to the computer which increased the system throughput by an order of magnitude. Typically, more throughputs improve the system dynamics and enable the utilization of longer post processing filters.

Definitely, efforts in MMICs should continue to develop lower jitter pulse generators, lower noise figure receivers, and integrating wide band antennas. Meanwhile, development of faster, lower cost A/D converters and samplers will significantly

impact real time localization systems as it is still today the bottleneck in developing affordable systems.

Chapter 7

Modeling And Jitter Improvement of SRD Based Systems

Step Recovery Diode (SRD) based UWB (Ultra Wide Band) pulse generators suffer from jitter caused by AM-to-PM conversion, SRD shot noise and clock jitter. These noise sources significantly impact the accuracy of UWB systems if very high precision ranging/positioning is required. Jitter behavior caused by the transmitter and receiver is mostly detrimental in the equivalent time sampling receiver. So a mathematical model for simulation of the jitter and amplitude variation effect in the equivalent time sampling technique has been developed and used in SystemVue [51] simulations. A criterion as an estimate of system accuracy is defined as Signal to Distortion Ratio (SDR) used. Similarly, a model for AM and PM noise analysis for an SRD based UWB pulse generator is developed that was validated experimentally. In addition, SRD shot noise contribution on output jitter was evaluated using the proposed model. Based on these models, methods to reduce the output jitter of the system have been recommended. Simulation showed that clock jitter and SRD shot noise led to pronounced output jitter, with shot noise are the primary cause. For a typical SRD based UWB pulse generator, an output jitter of around 3 psec has been achieved using some improvement techniques based on the proposed method,

compared to a 15 psec jitter before improvement. These measured results are in good agreement with our predictions.

7.1 Introduction

Ultra-wideband (UWB) wireless technology has stirred great interest because it provides high resolution and low cost implementation in the time domain [52]. UWB covers many applications ranging from biomedical systems such as monitoring of human vital signs [53][54] to security applications such as see through wall systems and sensitive assets tracking [55][56]. Its feature of high resolution can be utilized in UWB radars to achieve high accuracy in ranging and precise 3D-positioning [57][53]. These UWB systems use very narrow pulses, rendering the pulses retrieval in receivers as one of the system operations bottlenecks. The narrow pulse/wideband sampling requires the use of expensive components or advanced signal processing techniques for digital conversion. Using high sampling rate analog to digital converters (ADC) for direct conversion is limited by current ADC technology or the prohibitive cost of ultrafast ADC chips. As a result, other alternative techniques, such as interleaving multiple analog to digital convertors with relatively low sampling rates or sub-sampling have been proposed. The time interleaved technique [58] uses relatively inexpensive processors with moderate speeds, but it requires complicated analog circuitry for the interconnection of multiple ADCs. Another technique, adapted here, uses equivalent time sampling, a method requiring only moderate speed ADCs [59]. In this technique, the system dynamics are slightly compromised in exchange for achieving a low cost system. However, as will be discussed in section II, this technique requires a very stable pulse stream the subject of our study in this chapter. To achieve high resolution, we used picosecond pulses and relied on a simple step recovery diode (SRD) electronic circuit that features nonlinear behavior [60; 61; 62] to generate these picosecond pulses. However, SRD based UWB pulse generators suffer from jitter noise. Different techniques can be applied to analyze the noise

[63]. These analysis techniques could be classified into two general categories: the conversion matrix approach [63; 64] including its extensions [65], and the harmonic balance approach [63; 64]. However these techniques only provide a tool for analyzing the noise in the circuit and cannot offer an intuitive view on the contribution of the different noise sources in the Pulse Generator (PG) output jitter. Therefore in this chapter we develop an analytical formulation to better quantify the effect of different noise sources on SRD based UWB pulse generator. Then two techniques are presented to reduce the jitter at the output of pulse generator as well. This chapter is organized into 5 sections. In section 7.2, the fundamentals of the equivalent time sampling technique and noise effects will be studied. In Section 7.3, an analytical approach and a mathematical model for noise analysis in the UWB PG circuit will be developed and investigated. In section 7.4, measurement results compared to simulation results will be discussed and in section 7.5 conclusions based on simulation and experiments will be developed.

7.2 Noise Effect in Equivalent Time Sampling Technique

Equivalent time sampling is a simple technique that requires re-transmitting identical pulses, i.e. the periodic repetition of transmitting and receiving the same pulse as shown in Fig. 7.1. So jitter reduction can improve the distortion of the reconstructed pulse using this technique. In this section effect of different noise sources on reconstructed

pulse using this technique will be simulated and studied. In Equivalent Time sampling technique, the sampling period in the receiver is set with an offset equal to the desired sampling resolution; typically small offsets result in a high resolution for reconstructing the pulse. In a basic equivalent time sampling technique, just one sample per transmitted pulse is taken as shown in Fig. 7.1, requiring low receiver

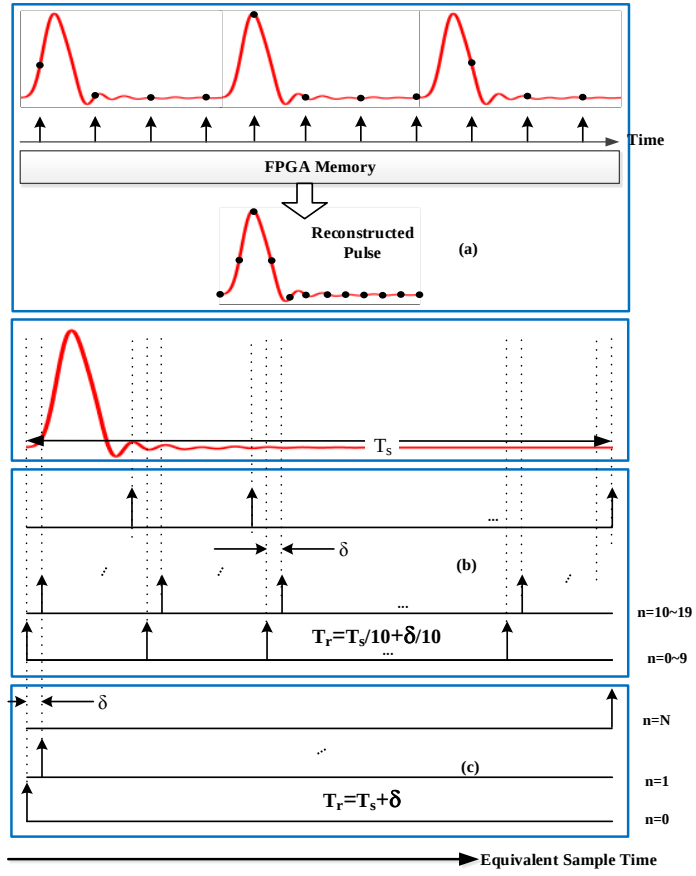


Figure 7.1: The equivalent time sampling timing diagram [8].

sampling frequency. As shown in Fig. 7.1 the sampling moments $n(T_s + \delta)$ result in equivalent $n\delta$ sampling moments due to pulse repetition with period T_s . As an example, if a pulse with repetition period (T_s) of 100nsec is sampled with a clock with 100.01 nsec period (T_r) (i.e. clocks are displaced by 10ps), then after taking 10,000 samples the transmitted pulse will be reconstructed with 10 psec sampling resolution. These sampling moments are shown in Fig. 7.1; considering the first sampling point as the reference point of the reconstructed pulse, the next sampling moment will be slightly shifted; consequently the sampling point as shown in Fig. 7.1 corresponding to $n = 1$ will be achieved. It is clear that the number of samples required for a complete pulse reconstruction (N) in this method is the transmitter repetition period over the sampling resolution. Therefore, in this technique the exact repetition time of the pulse in the transmitter and receiver sampler are key parameters in determining the pulse reconstruction accuracy. Any jitter of either the transmitter or receiver clock will significantly affect this accuracy. As an extension of the above basic sampling technique implementation, we have designed an advanced, more complex and faster system [59] shown in Fig. 7.1. In this system, instead of taking 1 sample per received pulse, we take 10 samples per pulse and store these samples in their appropriate bins to reconstruct the original pulse; thus this method is 10 times faster than the basic method. It should be noted that, in this case, as the number of points per pulse is 10, for 10 psec sampling resolution, then the receiver clock offset must be reduced to 1 psec offset from the transmitters clock.

7.2.1 Mathematical Model of Equivalent Time Sampling

To model and analyze equivalent time sampling without losing the generality of the problem, we have analytically described the process and investigated the impact of various parameters on performance. Assuming the transmitter pulse repetition frequency is $1/T_s$, the transmitted pulse train can be expressed as

$$s(t) = \sum_{n=-N}^N A_n p(t - nT_s - J_{nt}) \quad (7.1)$$

in which the function $p(t)$ is an ultra-wideband pulse generated by the pulse generator, J_{nt} is the transmitter jitter and A_n is the amplitude variation of the pulse generator. Since the pulse width is very small compared to repetition period, the amplitude variation of the pulse is modeled by the pulse repetition dependent amplitude (A_n). Using the equivalent time sampling technique, this pulse will be sampled with a clock slightly shifted from the transmitter. So the sampled pulse at the receiver ($r(t)$) can be written as

$$r(t) = s(t) \times \sum_{m=-N}^N \delta(t - mT_r - J_{mr}) \quad (7.2)$$

in which J_{mr} and T_r are receiver clock jitter and period respectively and $\delta(t)$ is the delta Dirac function. Through mathematical manipulation of (7.2), we have J_{kt} and J_{kr} , the captured phase noise terms at a specified sampling time, represented in (7.3) with new index k . Since the difference between T_s and T_r is very small, the system sampling resolution could be designed to be tens of GSps.

$$r(t) = \sum_{k=-N}^N A_k p(k(T_s - T_r) - J_{kt} - J_{kr}) \times \delta(t - kT_r) \quad (7.3)$$

Equation (7.3) clearly shows the sampling resolution by the presence of the $(T_s - T_r)$ term combined in the UWB pulse $p(t)$. Based on [66], both the transmitter and receiver jitter can be considered as Gaussian distributed random phenomena with standard deviation defined by the phase noise specifications of the clocks [67][68]. So the transmitter and receiver jitter, given that they are uncorrelated, could be augmented and equivalently modeled in one clock in either the transmitter or the receiver with a combined jitter standard deviation of

$$\sigma_J = \sqrt{(\sigma_{J_r}^2 + \sigma_{J_t}^2)} \quad (7.4)$$

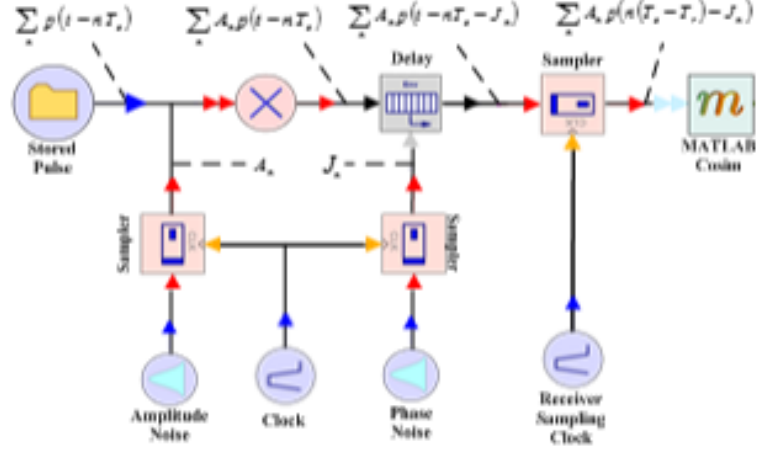


Figure 7.2: The equivalent time sampling block diagram in SystemVue.

This equivalent jitter noise causes distortion in the reconstructed signal and will be modeled in the next section using the SystemVue [51] tool. But before using this technique for simulation, a criterion as a measure of reconstructed signal accuracy is required. Defining r as sampling resolution and $r(t)$ as captured signal, (7.3) can be rewritten as

$$r(t) = \sum_{k=-N}^N A_k p(kr - J_k) \times \delta(t - kT_r) \quad (7.5)$$

which can be easily extended as

$$r(t) = \left[\sum_{k=-N}^N A_k p(kr) + \sum_{k=-N}^N A_k p'(kr) J_k \right] \times \delta(t - kT_r) \quad (7.6)$$

In (7.6) the first summation term represents the signal term and the second summation term represent the distortion or noise term. The Gaussian signal shape can be expressed as:

$$p(t) = A e^{-t^2/(2w^2)} \quad (7.7)$$

in which w is the half amplitude Gaussian pulse width. Therefore since the second term in (7.6) is dependent on the pulse derivative expressed in (7.7) and consequently

the pulse width (w), the noise/distortion ($n(t)$) power will be dependent on pulse width. To normalize this dependency we define the Signal to Distortion Ratio (SDR) of the reconstructed as

$$SDR_{ETS} = (T/2Kw)^2 \frac{1/T \int_T s^2(t)}{1/T \int_T n^2(t)} \quad (7.8)$$

in which w , the half amplitude Gaussian pulse width, normalizes the noise power and (7.8) $n(t)$ is the difference between ideal signal and distorted signal. In (7.8) the pulse period (T) unit is nsec and pulse width (w) unit is psec. The constant K is defined equal to 1000 as a scaling factor to simplify number presentation. The denominator in (7.8) is the difference between the original and reconstructed pulse, which can be interpreted as reconstruction distortion.

7.2.2 SystemVue Simulation of Equivalent Time Sampling

To show the effect of noise in pulse reconstruction, an equivalent time sampling receiver is implemented in SystemVue and both amplitude and phase noise effects on pulse reconstruction are studied. All amplitude variation of the received pulse is referred to as AM noise and all the phase or timing variations of the received pulse are referred to as PM noise.

The SystemVue tool provides the ability to simulate a communication system at any level, ranging from a behavioral modeled circuit used in a communication system to signal processing and detection techniques simulation and evaluation. The simulation block of our system is illustrated in Fig. 7.2. To simulate the equivalent time sampling technique, a Gaussian shaped UWB pulse with 300 psec width (Fig. 7.1 pulse) is exported from ADS [69] (the output of circuit simulation which will be studied in more detail in section 7.3) to SystemVue with a high sampling resolution.

The amplitude variation (A_n) is represented by a Gaussian distributed random variable, sampled with a clock with period T_s , and then multiplied by the pulse stream. This sampling of noise at the transmitter side synchronizes the amplitude

noise samples and equivalent jitter stated in (7.4) with the transmitter repetition period. It can be inferred from equations (7.2) and (7.3) that the phase noise is equivalent to a random delay in the pulse. Therefore the pulse train is delayed by a Gaussian distributed discrete random value.

In this simulation the amplitude noise is a Gaussian distributed random variable with mean of 1 and standard deviations shown in Table I. Jitter is a zero mean Gaussian distributed random variable with standard variations also specified in Table I. Finally, the pulse train in the model is sampled with the receiver clock with a period T_r with an ideal sampler without jitter – meaning that all phase noise sources have been collectively embedded in the transmitter based on (7.4) and shown in Fig. 7.2.

The details of the equations governing the simulation are shown in Fig. 7.2. In this simulation, the pulse repetition period of the transmitter is 100 nanoseconds and the sampling period of the receiver is 10.001 nanoseconds, giving an equivalent sampling rate of 10 GHz. Since in this method 10 points per pulse are captured, the sampling resolution is $(10T_r - T_s)$.

Both AM and PM noise that have been accounted for in the model cause signal distortion when reconstructing the pulse, as indicated in Fig. 7.3.

Given that we are using typical clocks (TCXO) in the transmitter and receiver, the equivalent jitter in pulse reconstruction will be assumed to be around 7 psec in our simulation. In Fig. 7.3 the effect of only PM noise in the transmitter with a standard deviation of 7 psec (jitter) is plotted, which in the frequency domain gives a signal to distortion ratio (SDR) of about 12dB. In Fig. 7.3 AM noise of 3% resulted in a similar SDR level, manifested in pronounced pulse ripples. In Fig. 7.3 the effect of pure AM and pure PM noises are compared in the frequency domain, in which the reconstructed signal SDR is calculated using mathematical definition of SDR_{ETS} (7.8) implemented in SystemVue.

In Table I, the quantified effect of AM and PM noise in pulse reconstruction is reported. Note that in SystemVue simulations of the AM noise of the transmitter, the received pulse level is not constant within the reconstruction time period. The level

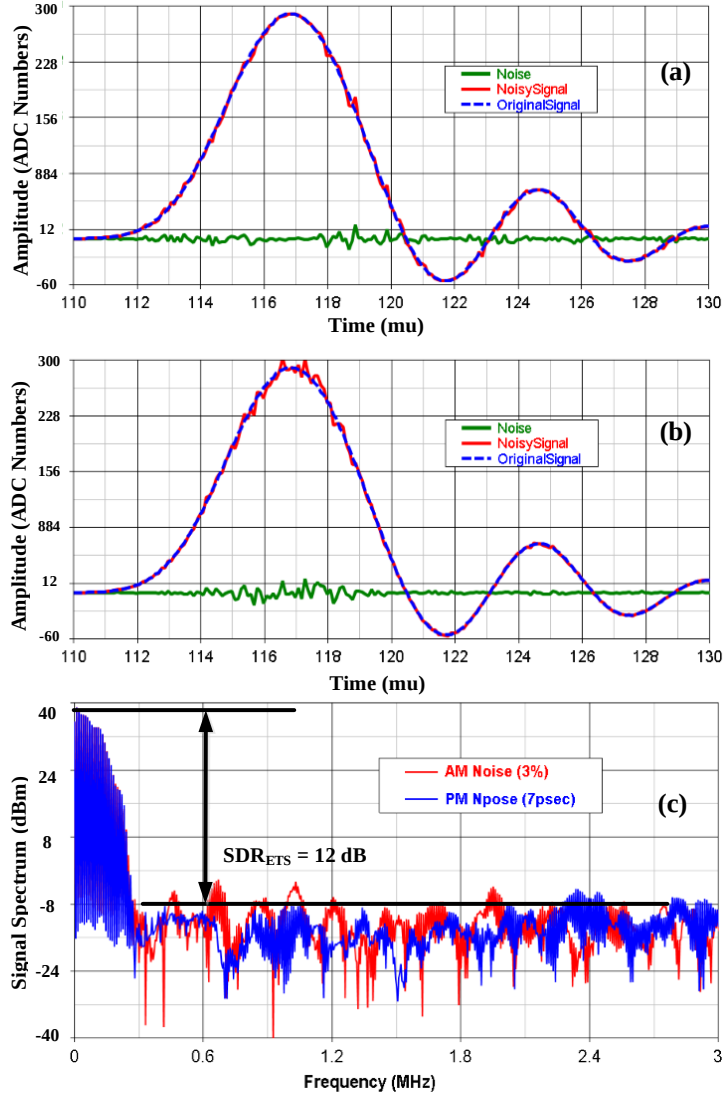


Figure 7.3: Reconstructed noisy/distorted pulse shape in time domain caused by PM noise (a) and AM noise (b) and their spectral domain representation (c).

Table 7.1: AM and PM Noise Effect on Equivalent Time Sampling.

AM Noise %	PM Noise (psec)	SDR_{ETS} (dB)
3	-	12
5	-	8
10	-	3
15	-	1
20	-	-4
-	3	18
-	5	15
-	10	9
-	15	5
-	20	3

variation could be related to any parameter variation in the propagation channel or transmitter. These simulations reveal that the noise in the output of the UWB pulse generator has a pronounced effect, and achieving maximum stability in amplitude and timing (phase) of this pulse stream in the receiver before sampling is essential. For this specific example, a 7ps PM and about 3% AM noise leads to an SDR of approximately 12dB.

It should be mentioned here; since in our UWB localization system we need to reach sub-millimeter accuracy – which is beyond the signal bandwidth – we need to use the leading edge of the pulse as a timing reference. Since location accuracy is proportional to timing accuracy and timing accuracy depends on reconstructed pulse distortion, maximum SDR values or equivalently minimum distortion on the reconstructed pulse stream is required.

As discussed before, all these generated noises in the reconstructed pulse come from utilizing equivalent time sampling instead of a direct sampling technique. The noise in the reconstructed pulse in an equivalent time sampling system could be considered as source noise that the whole system (regardless of its application from RADAR to localization) could be affected. Typically, the SNR/SDR defines the accuracy floor for the studied system. Subsequently, enhancement of the pulse reconstruction process leads to higher system accuracy.

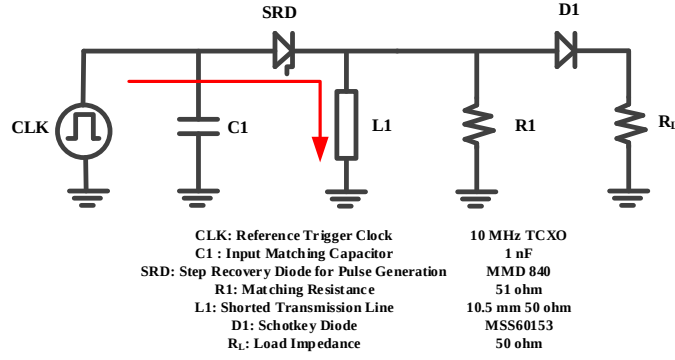


Figure 7.4: SRD Based UWB Pulse Generator Circuit.

To improve the reconstructed pulse SDR, pulse amplitude stabilization in the receiver could be easily addressed using an appropriate wideband AGC.

In case of using AGC, it must have a fast response time with appropriate bandwidth. Hence, in this chapter, we have focused on the pulse generator jitter (phase stabilization) problem which appears in the receiver.

7.3 Nonlinear Noise Modeling in UWB Pulse Generator

Jitter improvement on UWB pulse generator circuit, requires modeling of jitter generation mechanism and proposing some improvement techniques based on the model developed. The circuitry for a UWB pulse generator is depicted in Fig. 7.4[60]. In this circuit, during the positive cycle of the clock (steady state) the forward biased SRD is charged and conducts. When the clock polarity is reversed, the SRD discharges until all stored charges are completely depleted. At this point (recovery), an abrupt very short pulse (step) is generated; that is utilized for generating the UWB pulse (Fig. 7.5). This mechanism is discussed in detail in [60], but in this chapter we will focus on circuit noise analysis.

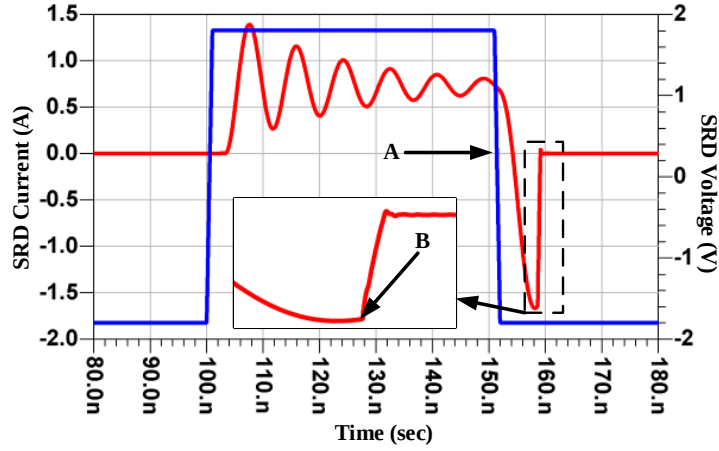


Figure 7.5: Clock and SRD Current Signals in UWB Pulse Generator (A: discharge start time, B: Discharge finish time or current jump moment).

To analyze the jitter and noise sources in this circuit, additive noise to the clock will be investigated and the impact of both AM and PM noise sources on the jitter will be studied. For AM noise analysis, the trigger clock is assumed to be a rectangular pulse stream without any jitter and for PM analysis, the trigger clock is assumed to have very stable and noise-free amplitude. In our analysis of AM and PM noise conversion to output jitter of the source, the conversion phenomena (AM-to-PM) is accounted for as well and assumed to occur in the SRD. This assumption is correct since the only function of the Schottky diode (seen in Fig. 7.4) is pulse shaping, affecting only the amplitude shape of the output.

7.3.1 PM Noise

As shown in Fig. 7.5, the main source of timing uncertainty or jitter is the uncertainty in the exact occurrence time of both instants A and B. As discussed before, B is the point at which the SRD completely discharges and the instant the SRD abruptly changes from the on-state to the off-state. Given that the clock determines the point (A) at which the discharge starts, and the discharge duration (relaxation time) is determined by the stored charge in the SRD (which depends on semiconductor

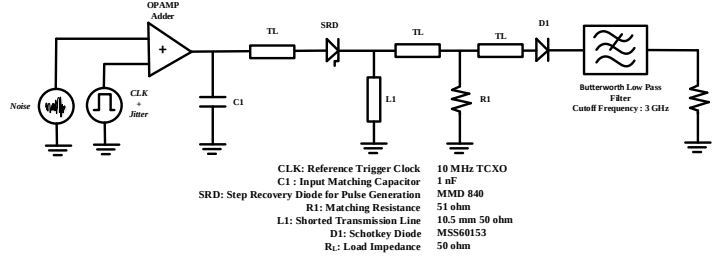


Figure 7.6: Pulse Generator Simulation Schematic used in ADS Simulation.

material properties), the only uncertainty is point A. In this case it is determined by the zero crossing of the triggering clock (as seen in Fig. 7.5) and affected by jitter. In other words, the clock jitter caused by the PM noise of the reference oscillator will be translated degree by degree to the PG output jitter. The relationship between clock phase noise and jitter is previously studied in [70]. Here, we use ADS for its simulation. The ADS simulation of this pulse generator circuit (Fig. 7.6) and jitter analysis of the output in MATLAB [71] verify this discussion. The waveform shown in Fig. 7.7 is a result of triggering a UWB pulse generator using a clock with 10 picosecond jitter (standard deviation).

To extract the output jitter, we imported the output of this PG circuit from ADS to MATLAB. Results show that the standard deviation of the pulse jitter is very close to the source jitter (9.80 picoseconds) and no amplitude fluctuations are discernible (Fig. 7.7).

To find the jitter of the imported pulse stream, a threshold of the pulse at half amplitude is defined in MATLAB and the points at which the pulse crosses this threshold is defined as the pulse occurrence time. These results are consistent with the fact that the clock jitter affects only the timing of the clock zero crossing (point A), and has no effect on the amplitude variation of the output waveform.

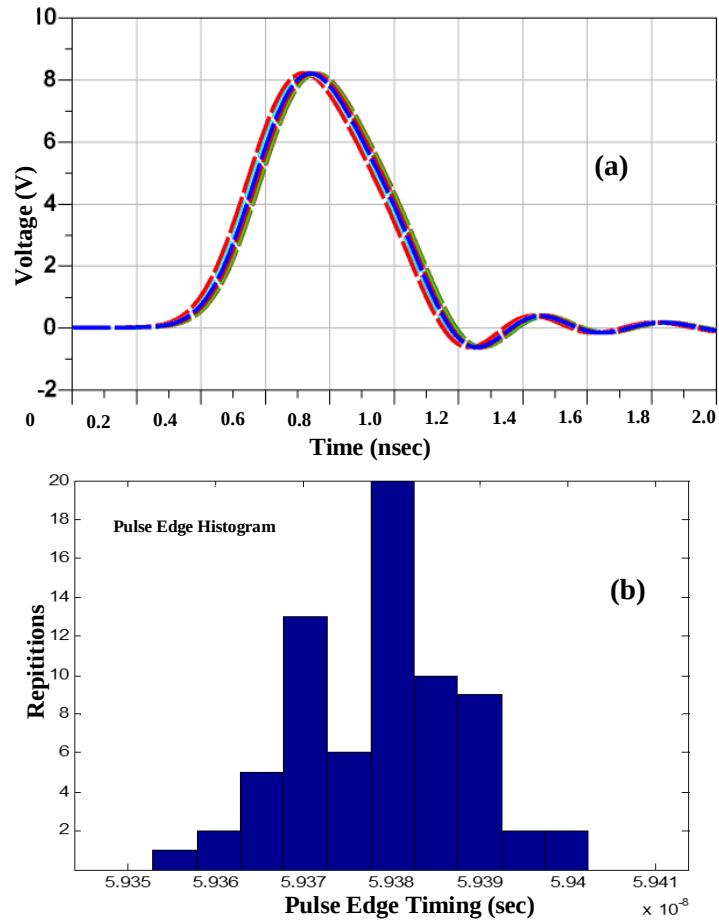


Figure 7.7: Clock PM Effect in output waveform shown in ADS (a) and pulse edge histogram in MATLAB (b).

7.3.2 AM Noise

Referring back to the circuit of Fig. 7.4, during the positive cycle of the clock, the carriers are injected into the semiconductor regions of the diode and the diode is changed into a conductor. After the semiconductor regions saturation or device forward bias, all amplitude variations of the clock will be manifested in relevant SRD current variations.

The relationship between the amplitude variations of the clock voltage and SRD current could be simulated using circuit analysis, but the aim of this chapter is to find the relationship between the amplitude variations and phase variation of the UWB pulse. Since the main source of pulse generation is the SRD current, conversion of AM noise to PM noise takes place within the SRD device. Therefore the focus will be to find a relationship between the amplitude noise and phase noise in SRD current. Based on the fact that the charge stored in the SRD during positive cycles of the clock is equal to the charge discharged during the negative cycles of the clock, we can extract the amount of charge stored in the SRD during the positive cycles of the clock by using the following equation:

$$Q_I = \int_{t=A}^{t=B} i_{SRD}(t)dt \quad (7.9)$$

in which points A and B are the instants defined in Fig. 7.5 where the discharge starts and finishes. The charge injected to establish forward bias is independent of the excitation signal and can be extracted from the SRD model [72]. As shown in Fig. 7.8, any slight AM fluctuation of the SRD current is converted to PM variation of the UWB pulse. In Fig. 7.8 it should be noted that the AM variations of the SRD current are very small compared to current itself. In addition, part of their frequency content is filtered by different elements on the path of the clock to the SRD. Therefore it is difficult to graph its current variation before the jump.

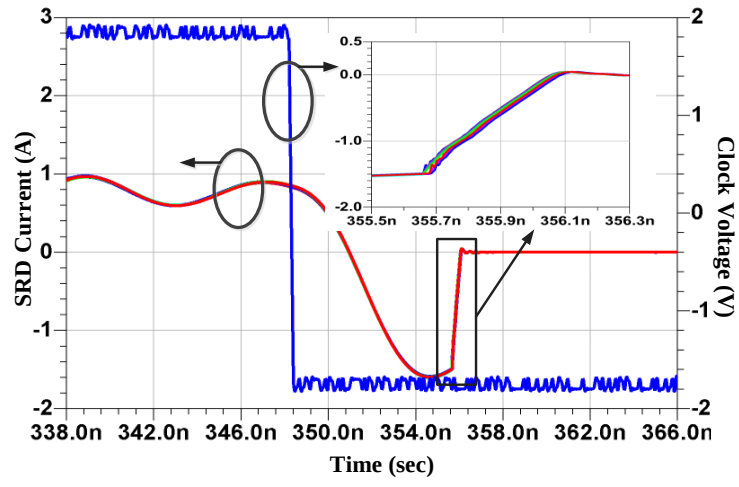


Figure 7.8: Simulation of AM Noise effect in UWB Pulse Generator Circuit in ADS
- AM noise of 200mVpp with 7GHz bandwidth.

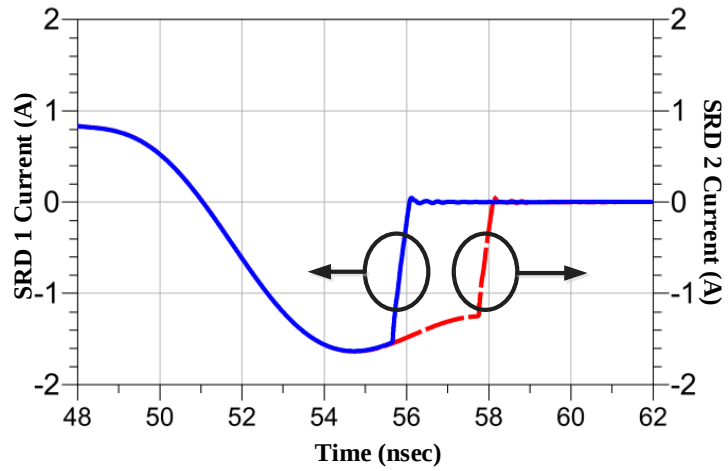


Figure 7.9: SRD Current in for first circuit and second circuit invoking SRD with more TL.

To make the SRD AM noise clearer AM lock noise is added. To analyze the source of AM-to-PM conversion phenomenon, we assume that the AM variation in the SRD current is given by:

$$i_{SRD,noisy}(t) = [1 + \mu(t)]i_{SRD}(t) \quad (7.10)$$

in which $\mu(t)$ is time dependent amplitude variation of the SRD current due to amplitude variations of the clock source. Since the charge stored in the device during the forward bias cycle is constant and it is assumed that the trigger clock has no jitter, then there is no uncertainty in the zero crossing point of the trigger pulse. Then equation (7.9) can be re-written in the general form given below:

$$Q_I = \int_{t=A}^{t=B+\delta t} [1 + \mu(t)]i_{SRD}(t)dt \quad (7.11)$$

in which δt is the resulting time deviation. Since the SRD minority carrier life time is less than the diode forward bias time, meaning the SRD is fully charged to its steady state before snap back, Q_I in (7.9) and (7.11) are equal. By expanding equation (7.11), we have

$$Q_I = \int_{t=A}^{t=B+\delta t} i_{SRD}(t)dt + \int_{t=A}^{t=B+\delta t} \mu(t)i_{SRD}(t)dt \quad (7.12)$$

By expanding the integration limits in (7.12) and combining with (7.11) we have

$$Q_I = Q_I + [1 + \mu(B)]i_{SRD}(B)\delta t + \int_{t=A}^{t=B} \mu(t)i_{SRD}(t)dt \quad (7.13)$$

Assuming $\mu(t) \ll 1$, (7.13) can be reduced to

$$i_{SRD}(B)\delta t = \int_{t=A}^{t=B} \mu(t)i_{SRD}(t)dt \quad (7.14)$$

which states that the noise charges are due to the accumulated noise component of the current. For simplicity, if the amplitude variations of the SRD current are replaced by

an average value $\delta\mu$, manipulating (7.14) and using (7.9) we reach a simple relation between $\delta\mu$ and δt :

$$\delta t / \delta \mu = Q_I / (i_{SRD}(B)) \quad (7.15)$$

which states that the parameters affecting the AM-to-PM conversion in UWB PG circuit are determined by the SRD physical parameters (charge stored during forward bias Q_I and peak discharge current, $i_{SRD}(B)$).

For verifying the developed equations, another UWB PG circuit using a different diode was simulated in ADS. For this circuit a new SRD with a minority carrier life time (TL) of 15 nsec (50% more than the previous SRD TL) is used. The SRD current in the two circuits are plotted in Fig. 7.9. Both circuits are excited with a similar clock with the same AM noise level; the resulting pulse waveforms are displayed in Fig. 7.10. In Fig. 7.10(a) the resulting jitter due to AM noise is 13.9 picoseconds (standard deviation), and in Fig. 7.10(b), 27.85 picoseconds. This is due to the increase in the stored charge inside the SRD (shown by Q_{I1} and Q_{I2} in Fig. 7.10c). Also, there is less current at the jump point for the second SRD ($i_{SRD}(B)$). As illustrated in Fig. 7.10(c), the AM-to-PM conversion in the second circuit is twice the AM-to-PM in the first circuit, as predicted by Eq.(7.15). Subsequently, one of the key parameters to decrease the AM-to-PM conversion in SRD pulse generator is the minimization of the stored charge of the device. This conclusion can be inferred from the developed model too, and should be considered when selecting the SRD type.

In addition, based on Eq. (7.14), the PG jitter caused by AM noise depends on the SRD current. This current has a repetition frequency specified by the reference clock of the circuit. Hence this noise conversion relation is sensitive to the noise frequency. Another feature of the circuit that could be inferred by this time-dependent model and Eq. (7.14) is the down-conversion of the high frequency components of the AM noise mixed with the clock harmonics.

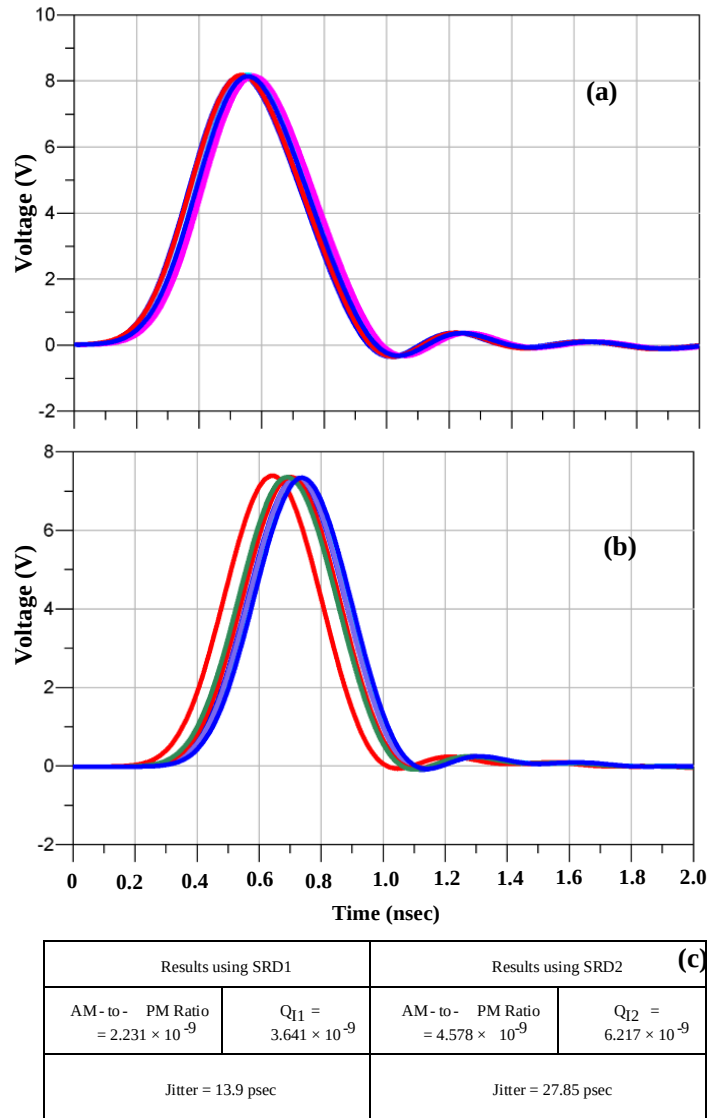


Figure 7.10: Output waveform jitter for circuit using SRD1 (a) , SRD2 with more TL (b) and results of AM-to-PM model calculations (c) performed in ADS using two selected SRDs using jitter free clock with AM noise of 200mVpp and 7GHz Bandwidth.

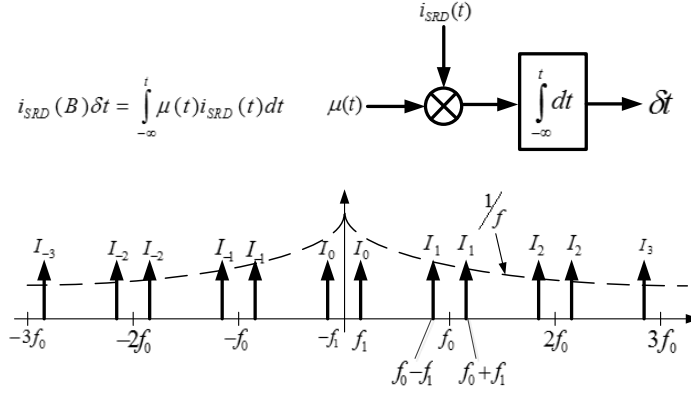


Figure 7.11: Frequency domain interpretation of the proposed jitter model.

This feature could be more intuitive when (7.14) is interpreted in the frequency domain (Fig. 7.11). By multiplication of two signals ($\mu(t)$ and $i_{SRD}(t)$) with different frequencies, mixed products of both will be generated in the frequency domain. Since integration is like a low pass filter in the frequency domain, only the low frequency or the difference frequency components will pass through and show up in the output. This highlights the effects of the $(f - nf_0)$ (in which f_0 is the clock frequency and n integer multiples of the clock frequency) term in the AM-to-PM frequency spectrum. So the jitter response for different frequencies will have a periodic nature. To show this frequency dependent feature of the AM noise conversion, the model proposed by (7.14) will be manipulated in the frequency domain. Since the SRD current is a periodic signal, the integration boundaries can be embedded in the SRD current by multiplying a rectangular pulse train on the SRD current and changing the integral boundaries to infinity.

$$i_{SRD}(B)\delta t = \int_{t=-\infty}^{t=+\infty} \mu(t)i_{e,SRD}(t)dt \quad (7.16)$$

in which $i_{e,SRD}(t)$ is the product of SRD current and a rectangular pulse train. The equivalent SRD current is still periodic and assuming a single tone sinusoidal AM noise, (7.16) can be rewritten in frequency domain as

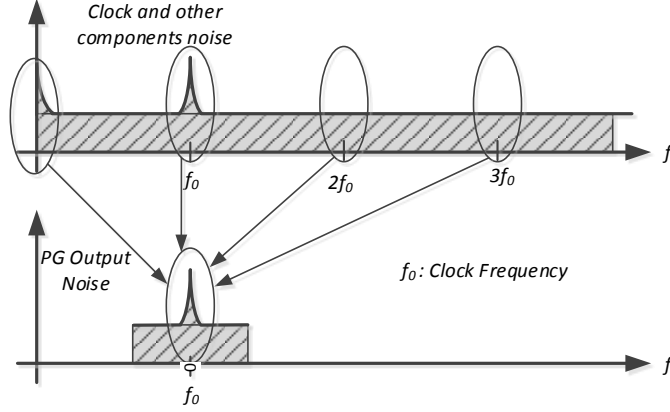


Figure 7.12: AM-to-PM Spectral conversion in UWB Pulse Generator.

$$F(\delta t) = \frac{1}{i_{SRD}(B)} \frac{1}{j2\pi f} \times \sum_n I_n \delta(f - nf_0 - mf_0 - f_1) \pm I_n \delta(f - nf_0 + mf_0 + f_1), \frac{-f_0}{2} < f_1 < \frac{f_0}{2} \quad (7.17)$$

in which the I_n terms are Fourier expansions of $i_{e,SRD}(t)$ (Fig. 7.11) at nf_0 frequency components. The noise frequency is assumed to be $mf_0 + f_1$. Finally, integration implements a low pass filter. The boundaries defined for f_1 in (7.16) do not add any limitations on the model and noise signals with frequencies more than $f_0/2$ can still be modeled by (7.17). Total RMS (Root Mean Square) jitter will be proportional to the sum of the amplitude of all the terms, shown below as

$$J = \frac{1}{\sqrt{2}} \sum_{n=-N}^N \frac{I_n}{nf_0 + mf_0 + f_1} + \frac{I_n}{nf_0 - mf_0 - f_1}, \frac{-f_0}{2} < f_1 < \frac{f_0}{2} \quad (7.18)$$

Equation (7.18) reaches its minima at

$$f_1 = nf_0 \quad (7.19)$$

because the function $|1/(x+a) + 1/(x-a)|$ is ascending for $x > 0$ and descending for $x < 0$. Based on the boundaries of f_1 from (7.17), the jitter will reach its maxima at $f_1 = f_0/2$. This is because the mixing feature and can be rewritten generally as

$$f_1 = \frac{2n+1}{2}f_0 \quad (7.20)$$

This periodic feature will be verified in the measurements section of the AM-to-PM conversion. It is completely analogous to the phase noise generation model in oscillators modeled by Hajimiri [73] and Demir [74]. As with these models this time-variant feature of the circuit causes the frequency conversion of the noise described graphically in Fig. 7.12. Measurement results will verify this feature of the circuit. This frequency conversion, similar to microwave oscillators, can cause up-conversion of noise sources with $1/f$ spectrum, along with down conversion of high frequency noise if present in the circuit. It can be seen that other noise sources add to or even dominate the output jitter, depending on their power and spectrum.

7.3.3 Shot Noise

As shown in Fig. 7.12 and predicted by the model, different noise sources, ranging from interference to thermal noise, can affect the output jitter. In the circuit used for picosecond pulse generation, during the positive cycle of the clock, the SRD conducts a current through a short circuited transmission line to ground. The current is primarily limited by the intrinsic resistance of the SRD. Thus the SRD current is very large (in the order of an ampere, as shown in Fig. 7.8) and will cause relatively large shot noise based on the shot noise equation discussed in [75].

Thus it is expected that after removing interference signals from the clock pin, shot noise will be the dominant contributor on output jitter. Reducing the SRD current will reduce the output jitter. This will be verified in section 7.4. Additionally, based on the proposed model, the shot noise spectrum (which has a $1/f$ noise spectrum)

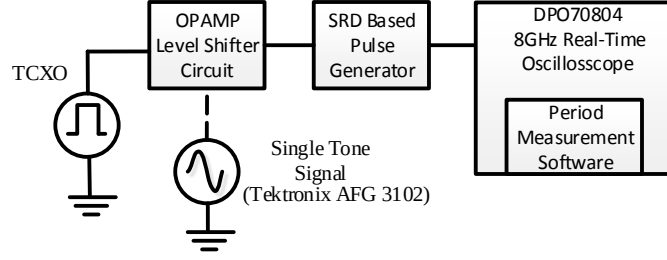


Figure 7.13: Measurement Setup.

will be up-converted around the trigger clock frequency (f_0) and add to other types of noise.

7.4 Measurements

To validate the developed model, jitter of fabricated pulse generator at different conditions will be measured and the results will be discussed. To measure the jitter in the UWB PG output, we used the Tektronix PDO70804C oscilloscope period measurement option. This real time oscilloscope has an 8GHz analog input bandwidth and an 8 bit ADC in its input, with a sampling rate of 25 GHz. Therefore, the quantization noise due to the oscilloscope itself may cause problems and is studied in Appendix A. The jitter measurement setup is illustrated in Fig. 7.13. A single tone signal with variable frequency is injected into the clock signal through an OPAMP adder/amplifier as a noise source.

7.4.1 AM-to-PM Conversion Measurement

To measure the AM-to-PM conversion of the pulse generator and to validate our model, the circuit of Fig. 14 was fabricated. The op amp pair provided a convenient add function as well as a low impedance source, necessary to drive the SRD. The

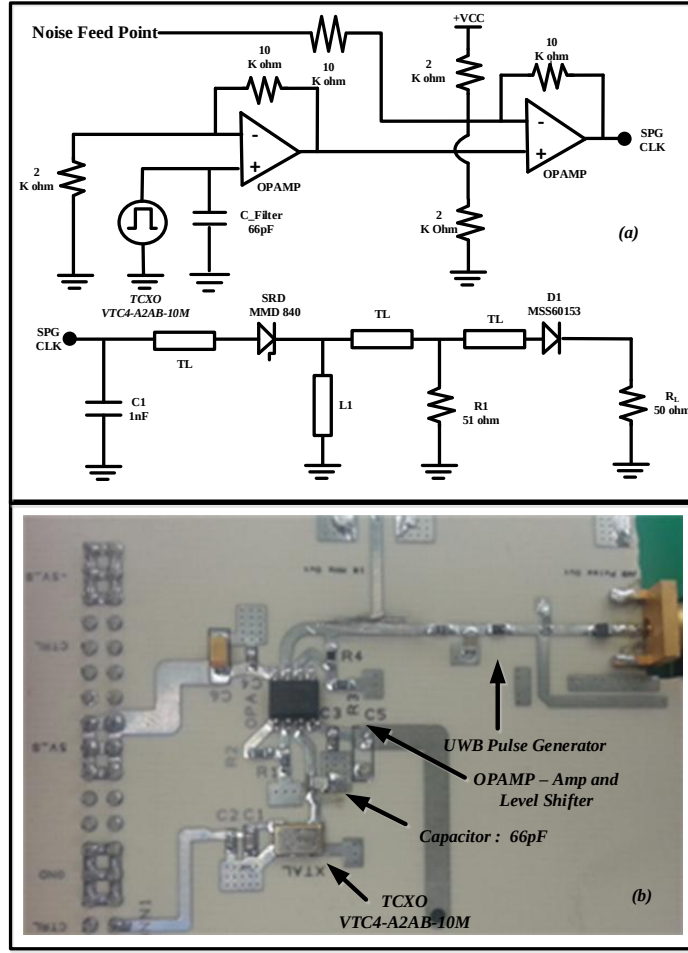


Figure 7.14: Schematic (a) and photograph (b) of the fabricated pulse generator.

signal fed into the circuit was generated by a Tektronix AFG 3102 with a 20mV peak amplitude sine wave at different frequencies.

The horizontal axis in Fig. 7.15 is the frequency of sinusoidal noise added to the clock signal and the vertical axis is the resulting RMS jitter at the PG output. The reference clock used in this circuit had 3.3 v peak amplitude and a phase noise of 1.6 psec, resulting in jitter in the PG output even in the absence of the AM noise.

As expected from the proposed model, the 1MHz signal had the same effect on the output jitter as 11MHz or 9MHz. This is due to noise down- conversion. The measurements show that the output jitter of the PG at frequencies equal to the

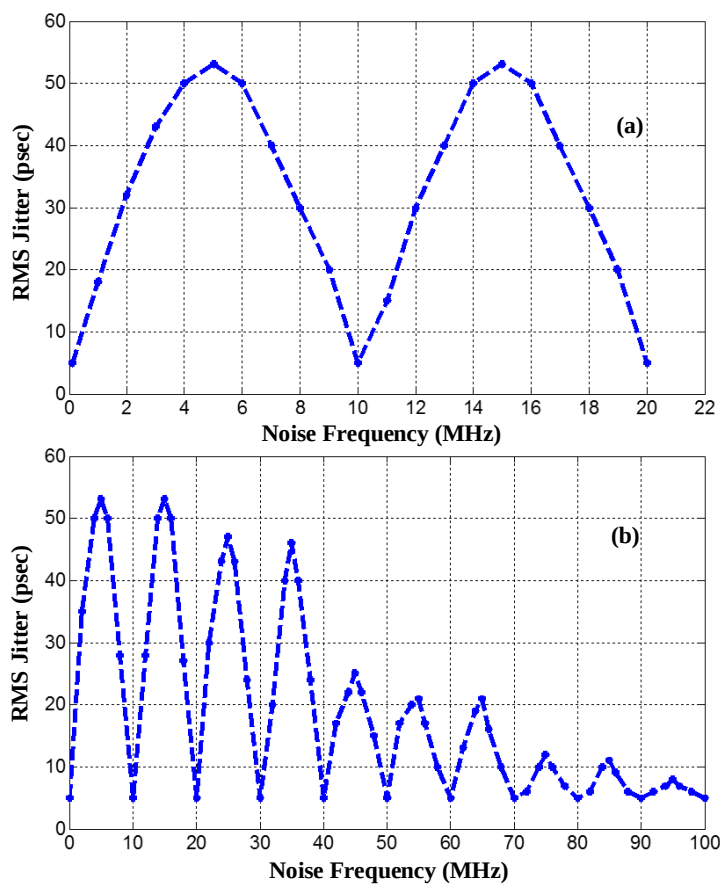


Figure 7.15: AM-to-PM Noise measurement Results at lower frequencies with higher frequency resolutions (a) and at higher frequencies (b).

harmonics of the clock frequency reaches a null, as predicted from the proposed model for single tone noise in equations (7.16) to (7.20). Hence, because of the TCXO phase noise and other noise sources, a non-zero AM-to-PM conversion floor is reached as seen in Fig. 7.15.

To justify these features of the circuit using the model, it should be noted that, similar to [73], terms of the harmonic mixture will give a zero frequency term that does not show up in the output jitter. The DPO70804 captured pulse (Fig. 7.16(a)) and measured jitters under two extreme conditions (5 MHz noise and 10 MHz noise) are shown in Fig. 7.16(b) and (c) respectively. Fig. 7.16(b) and (c) are period measurement snapshots. Since the period jitter is very small compared to the signal period, it is not possible to visually show the jitter effect on signal snapshot window of Fig. 7.16(a). The periodic feature of AM-to-PM discussed above does not repeat at higher frequencies (different peak point), since at higher frequencies (harmonic orders greater than 3) the frequency response of other circuit components, like the OPAMP, will dominate. However, the repetitive nature of the system (having a null at the clock harmonic points and peaks between them) still holds and shows up in the measurements (Fig. 7.15(b)). In this figure, the peak jitter is determined by the noise amplitude of 20 mV. In the fabricated circuit, given that the TCXO clock does not have a square waveform, we used high gain OPAMP based amplifiers to make a square shaped trigger pulse.

Generating a short pulse results in a wideband (4 GHz) signal source. This could couple to the TCXO clock and be fed-back to the SRD after amplification through the OPAMPs. To suppress this noise and to prevent unwanted oscillations, we used capacitors before the rectangular pulse generation for low pass filtering. Since at this point a low number of clock harmonics was present, large capacitors were used, lowering the cut-off. After amplification of the clock, additional capacitance was carefully selected to remove generated higher order harmonics.

The experiment showed that in the absence of injected noise and without using a capacitor on the clock pin of the TCXO, output jitter was 15 picoseconds. Jitter

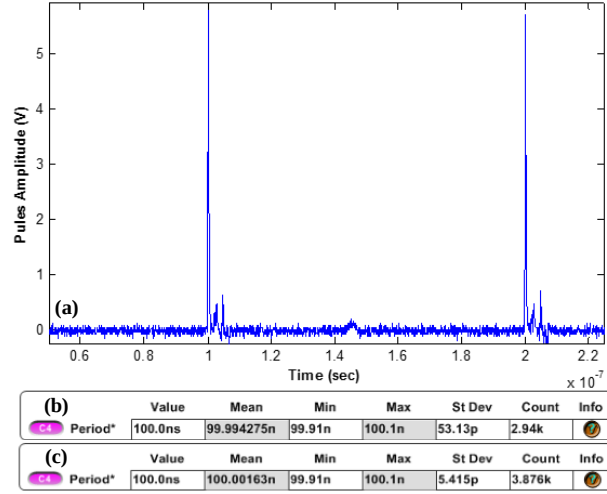


Figure 7.16: Captured pulse stream using DPO70804 (a) and period measurement screenshots with 5 MHz-20 mVpp (b) and 10 MHz-20 mVpp added signal as amplitude noise.

was reduced to 5 psec after inserting a 66 pF capacitor. To estimate the value of the capacitor, the associated cut off frequency of the output circuit was set to the first harmonic of the clock; i.e. 10MHz. So

$$C = \frac{1}{(2\pi f_c R_{out})} = \frac{1}{(2\pi \times 10MHz \times 250\Omega)} \approx 63pF \quad (7.21)$$

in which $R_{out} = 250$ is the output resistance of the TCXO measured in the lab.

7.4.2 Measurement of Shot Noise Effect

It is known that shot noise in the circuit studied above is a function of the SRD current, and the current passing through the SRD depends on the triggering clock voltage level. A triggering clock level of 5 V caused a jitter floor of 5 psec. By changing the clock amplitude level from 5 V to 3.3 V, the current passing through the SRD was reduced, resulting in an output jitter of 3.5 psec instead—an improvement by a factor of 1.4, close to $5/3.3=1.51$.

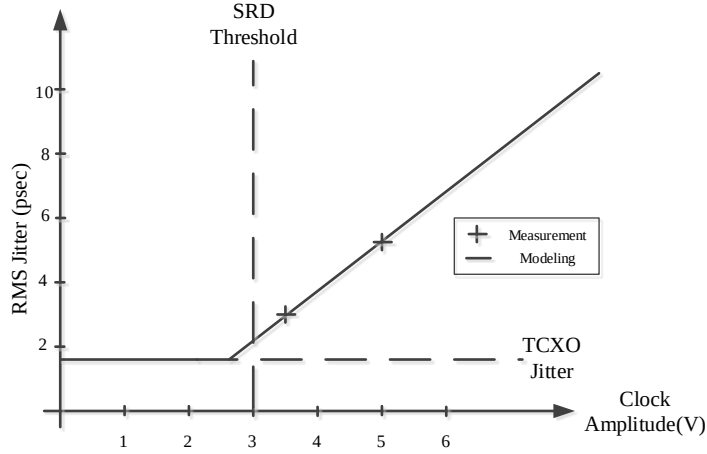


Figure 7.17: SRD based UWB Pulse Generator RMS jitter versus Shot noise contribution and jitter floor.

During the forward bias of the SRD, the current passing through the SRD is a relatively large current (in the order of an ampere). However, the clock voltage cannot be reduced below the barrier voltage of the diode required to push the SRD to its on and off states. So the minimum shot noise is associated with minimum SRD current, i.e. using the lowest clock voltage level.

However, even though minimal voltage was used, the minimum current was relatively still high, leading to relatively large shot noise. It can be inferred that the 3.5 psec measured overall noise comes mostly from the shot noise conversion of the SRD. The shot noise source is bigger than the other noise components (the clock phase noise and thermal noise are typically less than 1.6ps), so shot noise dominates.

In summary, in order to reduce the jitter caused by SRD shot noise, we need to reduce the clock triggering voltage to its bare-minima. This will lead to lower SRD current and lower shot noise. This limiting factor is shown in Fig. 7.17 with the vertical dashed line identifying the minimum voltage level that the clock can meet to generate a UWB pulse, while keeping the shot noise level as low as possible. In this figure output jitter versus trigger clock amplitude is shown while the jitter floor in the circuit is limited by the clock jitter and diode barrier voltage.

So in design and part selection of the SRD, the barrier voltage and TL should be as low as possible and the clock jitter should not dominate the jitter associated with the shot noise. In the case of our circuit, because of the presence of the Schottkey shaping diode at the output, decreasing the clock level lower than 3.3 V causes an exponential decrease of the output amplitude. Beyond this level, the quantization noise of the oscilloscope (Appendix I) dominates the jitter measurements

7.5 Conclusion

To achieve a very stable UWB pulse generator in association with an equivalent time sampling receiver, amplitude and phase noise of UWB pulse generator should be minimized. To model the system, the SystemVue tool proved to be a powerful and flexible tool, showing the importance and effects of these noises in an equivalent time sampling receiver. In the SystemVue model, we augmented the transmitter jitter and receiver sampler jitter. This simulation quantitatively showed the importance of these noise sources in equivalent time sampling. They can be largely avoided if direct conversion is used instead. In these simulations new quantitative criterion as a measure of pulse distortion for UWB pulses sampled by ETS technique is provided and used.

Typically, jitter (PM Noise) is produced by the clock itself, but it was discovered that in an SRD based UWB pulse generator, serious AM-to-PM conversion could lead to significant jitter as well and must be addressed. So a mathematical model was developed to quantitatively analyze the output jitter.

This model can accurately show the frequency conversion feature in jitter of SRD based pulse generators as well as dependency of jitter to SRD physical features. Based on our developed linear time variant model for this AM-to-PM conversion, we found two techniques to reduce the output jitter. First, use a capacitor to decouple the interference signals from the circuit, and secondly, drive the SRD with low voltages to decrease the current passing through the SRD.

The first method was developed during our validation experiment. It was shown that in the presence of a very wideband signal in the circuit, the AM-to-PM conversion process causes large jitter in the pulse generator output. This usually dominates the jitter caused by the clock phase noise and SRD shot noise. Suppression of these amplitude interference signals early-on, and a decoupling capacitor, would help in reducing output jitter.

For the second method, it was found out that after removing amplitude interferences from the clock, shot noise passing through the SRD is the dominant source of output jitter. To limit this noise source, a trigger clock with lower voltage levels was used. The threshold voltage of the SRD was the limiting factor in reducing the shot noise effect.

The model also can predict the effect of TL of SRD at the output jitter. Based on this model the selected SRD should have minimum TL as well as low barrier voltage. In general, the reference clock jitter determines the jitter floor of the output, but it is usually dominated by the shot noise of the SRD. In the circuit used in this chapter, by using a capacitor at the clock pin of the TCXO and reducing the SRD current, the output jitter dropped from 15 psec to 3.5 psec.

7.6 Appendix I : Estimation of Quantization Noise Error in Jitter Measurements

Since jitter can be considered as the standard deviation of a signal period, as indicated in DPO70804C manual for measuring the signal period, the DPO70804C considers a trigger level at one point and determines (extracts) the time of the next point signal, or the interpolations of the signal, that again pass this trigger level. It then calculates the time difference between these two successive triggering points as the signal period. So, we assume that the signal variation between the two sampling

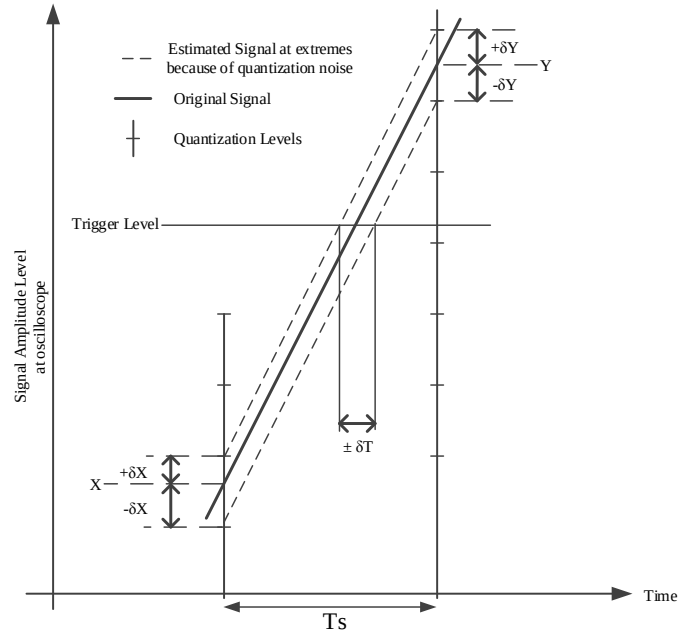


Figure 7.18: Quantization Noise effect on jitter measurements.

points is completely linear. This happens when the sampling rate is high enough compared to signal bandwidth.

As depicted in Fig. 7.18, because of quantization at the sampling points, error exists between the limits shown by the dashed line. This will cause an error on trigger time estimation affecting period measurement. Using a simple linear representation, it can be shown that

$$\delta T = (-1/XT_s)/(1 + Y/X)^2(\pm\delta X) + (-Y/X^2T_s)/(1 + Y/X)^2(\pm\delta Y) \quad (7.22)$$

in which X and Y are the signal levels at two successive sampling points before and after the trigger level. This equation can be approximated by equation (7.23) if Y/X is large,

$$\delta T/T_s = (-Y^2/X^2)/(1 + Y/X)^2(\pm\delta Y/Y) < (\pm\delta Y/Y) \quad (7.23)$$

and consequently

$$\delta T < \pm \delta Y / (Y / T_s) \quad (7.24)$$

Therefore, with an 8-bit oscilloscope quantization and a 25 GHz real-time sampling rate, the period measurement accuracy will be less than 30 femto seconds if an appropriate pulse slope is used. For the UWB pulse generated by our PG, the pulse slope is 2.4 v/65.5 psec. As a result, the jitter caused by quantization noise for this case will be as follows:

$$\delta T \approx (10/2^8 V) / (2.4/62.5 Vps) \approx \pm 1 psec \quad (7.25)$$

adding to the PG output jitter. But since the jitter measurements for the fabricated pulse generator are more than 3 psec, the 1 psec oscilloscope accuracy is adequate.

Chapter 8

Accuracy Assessment

In this chapter, we estimate the achievable localization error in an ultra wide band (UWB) precise positioning system. The system is based on time difference of arrival of narrow pulses to multitude of base-stations. A mathematical model and simulation platform are developed to describe the behavior of UWB indoor localization system. Limits on the location accuracy as a function of the parameters of the UWB system are described. A discussion of the dominant reasons for errors that include picoseconds pulsar jitter, sampling clock jitter, sampling rate, and system additive white Gaussian noise (AWGN) is presented. We show a simple method to calculate the total system jitter, and describe error biasing phenomenon as the tag moves approaching one base-station and distancing another. Design curves are provided to determine the required specifications of the various system components to achieve a certain positioning accuracy.

8.1 Introduction

Advances in UWB and other enabling technologies have resulted in higher achievable accuracy for wireless sensor networks, which has opened up new applications including smart medical instruments, surgical navigation, and asset tracking. To realize the potential of these applications, additional research is needed to develop system-level

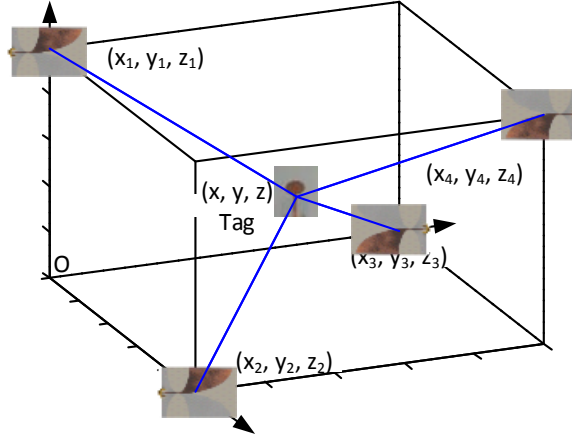


Figure 8.1: 3D localization system at University of Tennessee: four directive Vivaldi antennas connected to the base-stations at the corners of a cube to receive the RF pulses. Omni-directional printed dipole is utilized to transmit the RF pulse. Central processing unit is used to measure the time delay that the pulse takes to reach the base-stations.

design tools and comprehensively quantifying the impact of error sources on overall system accuracy. The potential exists to change the accuracy of these indoor wireless localization systems to millimeter and even to sub-millimeter accuracy.

However, indoor sub-mm to mm accuracy systems still face numerous challenges. The challenges include the noise and sensitivity of the UWB receiver, multi-path, antenna phase-center variation, time scaling, jitter, and degradation due to overall system calibration. For example, when analyzing the sensitivity of the UWB receiver built at the University of Tennessee to AWGN and signal to noise ratio (SNR), the leading-edge detection algorithm implemented on field programmable gate array (FPGA) [76] must be re-examined in detail to understand the limitations of the system in terms of ranging accuracy. The leading-edge detection algorithm fails when the UWB pulse peak SNR drops to around 10-12 dB, leaving the leading edge near the noise floor.

Both the accuracy (localization bias), and the precision (variance) of a tag position measurement in a UWB localization system depend on noise generated from the active/passive system circuit components, and the techniques used to filter them out. They include system jitter, AWGN, and analog-to-digital-converter (ADC) errors.

These are functions of the sampling rate and digital filter size as well. Another set of errors stemming from the propagation effects, like multipath and antenna phase-center, will not be discussed here, and could be estimated based on results of [76][77][30][78]. The first set will be thoroughly investigated here, except for ADC noise that is much less than other sources.

The goal of this chapter is developing a mathematical model and a simulation platform, verified by empirical measurements, to describe the overall augmented error in localization due to jitter, AWGN, and sampling rate. For simplicity, a one-dimensional (1D) case will be considered. Extending results to three-dimensional (3D) case is straightforward.

In section 8.2, the chapter starts by describing the system construction. It describes its transmitter, receiver radio frequency (RF) front-end and digital back end, which includes the sampling method i.e. equivalent time sampling. This part also describes the detection algorithm used i.e. leading edge and the triangulation method i.e. time difference of arrival TDoA.

Next, the jitter and AWGN impact on the system accuracy and precision is addressed. Jitter effect on the system is not straightforward though. Hence, for better understanding, section 8.3 describes the jitter in the system and its temporal and frequency domain characteristics. Simulation and measurement are also performed to support findings in this section.

In section 8.4 and 8.5, a theoretical and computer model are built to study the system performance, as the signal is contaminated by the jitter and AWGN.

Section 8.6 shows the theoretical model and simulation results where results are supported by measurements. We conclude in section 8.7.

8.2 System Description

UWB based systems have been discussed in numerous publications, e.g. [79][80][81]. The system at the University of Tennessee [76][77][30][78] is a UWB narrow pulse

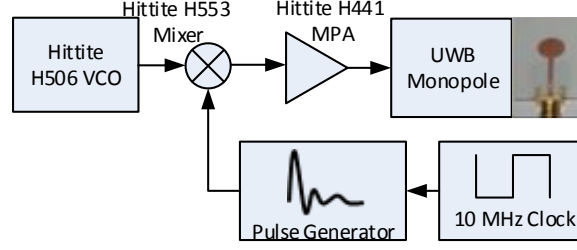


Figure 8.2: Tag transmitter block diagram: Gaussian pulse generator triggered by a 10 MHz clock, VCO Hittite H506 output of 8 GHz is mixed using Hittite H553 mixer with the pulse and amplified using a Hittite H441 medium power amplifier, and an omnidirectional monopole antenna is used to transmit the pulse.

localization system, comprised of a transmitter and numerous receivers, Fig. 8.1. The transmitter, the tag, has a picosecond pulse generator controlled by a clock. It has a power amplifier and a wide-band omni-directional antenna as well. In the receiver side, it has a wide-band antenna, RF frontend, a sampler, and an ADC. When time difference of arrival (TDoA) concept is used, the number of receivers is at least four for 3D positioning. In case of 1D, two receivers suffice.

8.2.1 Construction

The developed system is an indoor localization and tracking system, built to achieve accuracy and precision in the one mm range. The use of TDoA alleviates the need for transmitter-receiver clock synchronization, since the system uses wireless tag. The four receivers i.e. base-stations have four separate RF front-ends, close to the antennas to improve the signal to noise ratio. The four base-stations signals are gathered to one board, for analog to digital conversion and processing. The antennas are positioned in predefined places. The system utilizes an active tag to transmit a $\tau = 300ps$ Gaussian pulse $g(t)$ (8.1), τ is the full width at half maximum (FWHM). The pulse repetition frequency is 10 MHz . The tag produces a train of pulses $s(t)$ described by (8.2). $T_0 = 100ns$ is the pulse repetition period.

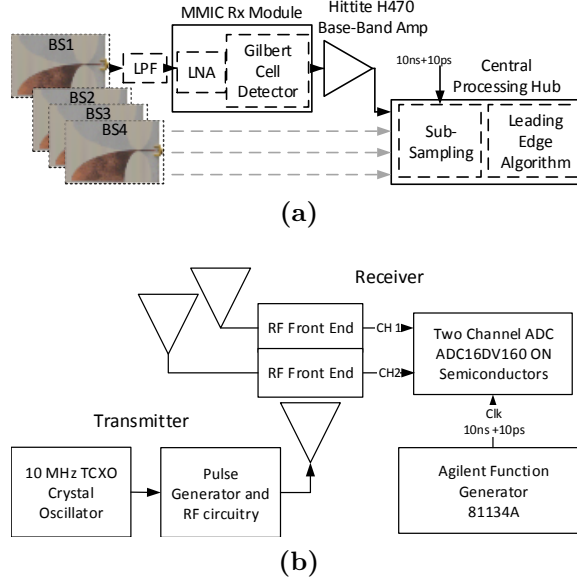


Figure 8.3: System receivers architecture: (a) four base-stations connected to a central processing hub. Single receiver chain consists of an analog low pass filter LPF, MMIC receiving module: LNA, square law detector based on a Gilbert cell four quadrant multiplier developed by ULM University [5], and Base-band Hittite H470 amplifier. Central processing hub digitizes the pulses, and finds the TDoA using a leading edge algorithm. (b) The Clocking diagram of transmitter and receiver, transmitter uses 10 MHz TCXO crystal oscillator. The four received base-stations signals are fed to two ADC16DV160 chips with two channels each i.e. four in total. The Two ADC chips use the same external clock generated by Agilent function generator of sampling time 10 ns + 10 ps. The transmitter and receiver clocks are not synchronized.

$$g(t) = e^{-4\ln(2)(t/\tau)^2} \quad (8.1)$$

$$s(t) = \sum_{-\infty}^{\infty} g(t - mT_0) \quad (8.2)$$

In Fig. 8.2, the base-band pulses are up converted using an 8 GHz oscillator, amplified, and transmitted using printed dipole. For reception, Fig. 8.3, four base-stations with predefined positions receive and down convert the signals. The signals from the four base-stations are then sent to the central processing hub for sub-sampling. The sampling takes place at the receiver by a clock with a period of 10 ns+10 ps, it is not synchronized with the transmitter clock. The system equivalent sampling period is the difference of the receiver and transmitter clocks periods, i.e. $T_s = 10ps$. The high stability of the receiver and transmitter clocks is critical to maintain such difference invariable. The time of arrival (ToA) is found using the leading edge algorithm. Finally, a TDoA algorithm is employed to triangulate the tag position.

8.2.2 Leading Edge Algorithm

To find the exact ToA of a received pulse, a leading edge algorithm (LE) is used. It is an implementation of constant fraction discriminator (CFT) algorithm. It was shown to have better performance in multipath environment compared to peak detection [76], Fig. 8.4. The leading edge algorithm was optimized to avoid close multipath errors.

The LE algorithm starts with the ADC output, where we apply a digital low pass filtering (averaging filter), that we will call signal filter in this chapter. It reduces the noise especially caused by imperfection in the sampling process. A real-time maximum filter is used for two copies of the pulse, one of them delayed. Max and Max16 are the pulse after the maximum filter and the delayed pulse after the maximum filter respectively.

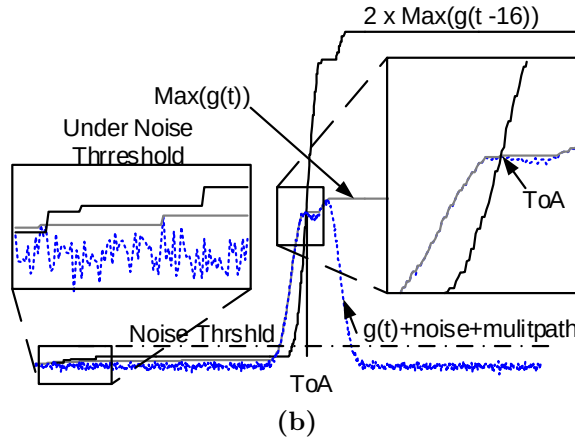
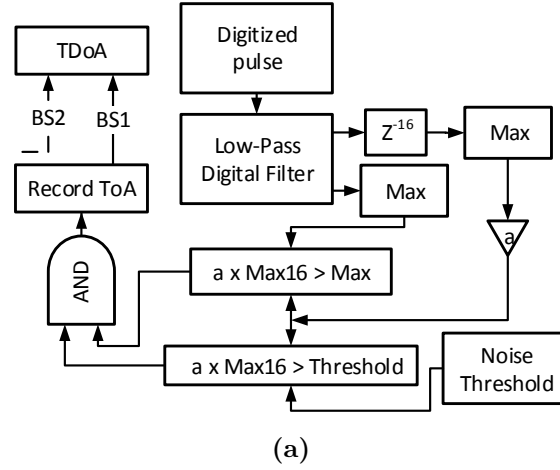


Figure 8.4: Leading edge algorithm: (a) block diagram, and (b) application on a Gaussian pulse tainted with noise and multipath. The digital pulse is low-pass filtered then it is duplicated into two copies one is delayed by 16 samples periods. Both copies are fed into a maximum filter. The delayed branch is multiplied by a . The delayed branch is compared to the direct branch and to a noise threshold. If the delayed branch is greater than both then the time is recorded as the ToA. Two ToAs are subtracted to find TDoA.

$$Max(m) = \max(g(1) : g(m))$$

$$Max16(m) = \max(g(1) : g(m - delay))$$

To find the time of arrival ToA, we wait until the following inequality takes place, the time is recorded as the ToA of the pulse. A noise threshold level is used to avoid false triggering by the noise, Fig. 4(b).

$$(aMax16 > Max)AND(aMax16 > Noise)$$

Where $a = 2$ and $delay = 16$ is employed for the current system. Interested readers can refer to [76] for more details. At the processing unit, comprised of an FPGA and a computer, the ToAs are collected and the TDoA is estimated. Final TDoA measurements can be subsequently improved by using post filters applied on TDoA values.

Leading edge algorithm accuracy, however, is significantly affected by the presence of jitter. Typically, different sources of jitter include clocks jitter, pulse generator jitter, and sampler jitter. Clocks jitter originates from both the triggering clock of the pulse generator, and the sampling clock at the receiver. In the following, we will develop a mathematical model for the leading edge algorithm, but first we will discuss the nature of jitter noise in implemented sub-sampling scheme.

8.3 Jitter Error In Sub-Sampling Systems

In a direct sampling system, the transmitter jitter does not add to the distortion of the pulse. In fact, the transmitter jitter simply cancels when TDoA algorithm is used, as transmitter jitter just adds the same random delay to all receivers. However, in our system where an equivalent time sampling system is used, the transmitter jitter must be accounted for too, as it will not be automatically canceled. There is no correlation

between receiver and transmitter clocks jitters, they are not synchronized, and jitter is assumed Gaussian [82]. Consequently, the jitters of the transmitter and receiver add in a mean square sense (8.3).

$$\sigma_t = \sqrt{\sigma_{tr}^2 + \sigma_{rx}^2} \quad (8.3)$$

Where σ_t is the total jitter, σ_{tr} is the transmitter jitter, and σ_{rx} is the receiver jitter. Transmitter jitter includes transmitter clock jitter and pulsar jitter as well.

The addition can be explained by noting that one sample is captured per transmitted pulse period, while there are random delays of both the sampling clock and the transmitter clock, these errors are independent and will be different from one sample to another. Thus, the transmitter random delay is not the same for the whole pulse anymore, i.e. in the sub-sampling case, the TDoA cannot eliminate the random delays by the transmitter.

To account for the jitter effect, the total time jitter $j(t)$ for a signal $g(t)$ will be translated into amplitude voltage noise $n_j^g(t)$, that can be estimated using (8.4) [83] as a first order approximation of Taylors series, though higher order terms need to be added for higher accuracy. The amplitude of $j(t)$ is random with a normal distribution that has a zero mean, σ_t^2 variance, and white spectrum.

$$n_j^g(t) = \frac{dg(t)}{dt} j(t) \quad (8.4)$$

For a Gaussian pulse and assuming ergodic jitter $j(t)$ process, the time average of the noise power p_{nj}^g of (8.4) can be found over the period $-\tau$ to $+\tau$, where τ is the pulse width and $E()$ is the statistical expectation. The integration is almost equal to integration from $-\infty$ to $+\infty$.

$$p_{nj}^g = E \left[\frac{1}{T_o} \int_{T_o} (n_j^g(t))^2 dt \right] \quad (8.5)$$

$$p_{nj}^g = \frac{\sigma_t^2}{2\tau} \int_{-\infty}^{+\infty} \frac{dg(t)^2}{dt} dt \quad (8.6)$$

$$p_{nj}^g = \frac{\sigma_t^2}{\tau^2} \sqrt{\frac{\pi \ln(2)}{2}} \quad (8.7)$$

To find the frequency spectrum $P_{nj}^x(f)$ of the noise caused by the jitter of an arbitrary signal $x(t)$, we can use (8.8) [84]. It is the convolution of the jitter power spectrum $P_j(f)$ with the power spectral density $P_x(f)$ of the signal affected by the jitter, multiplied by the square of the frequency to represent the differentiation in the time domain.

$$P_{nj}^x(f) = [(2\pi f)^2 P_x(f)] * P_j(f) \quad (8.8)$$

Eq. (8.8) indicates that $P_{nj}^x(f)$ has a white spectrum, since one term of the right hand side convolution, i.e. $P_j(f)$, is a constant function of frequency, because jitter is assumed white Gaussian. Consequently, the amplitude noise caused by the jitter is white noise as well.

We can use (8.8) to find an expression for the noise power spectrum caused by the jitter in $s(t)$ i.e. $P_{nj}^s(f)$. $s(t)$ is practically important since it is the signal that could be physically measured. Alternatively, we can use (8.7) to find the average noise power in $s(t)$ i.e. p_{nj}^s and Parseval's identity (8.9), and that $P_{nj}^g(f)$ is white to find $P_{nj}^s(f)$. Both methods will yield the same result. Where $DUT = 2\tau/T_0$ is the duty cycle and $f_o = 1/T_o$.

$$\frac{1}{T_o} \int_{-T_o}^{T_o} |x(t)|^2 dt = \int_{-\infty}^{\infty} |X(f)|^2 df \quad (8.9)$$

$$p_{nj}^s = pnj^g \times DUT = \frac{\sigma_t^2}{\tau} \sqrt{2\pi \ln(2)} \quad (8.10)$$

Since we are dealing with a sampled signal, a discrete Fourier transform (DFT), i.e. fft, would be more suitable for our case. A sampling frequency f_s results in frequency spectrum span that extends from $-f_s/2$ to $f_s/2$. Using Parsevals identity for periodic signals (8.9), we get $P_{nj}^s[k]$ (8.11) (8.12) the discrete power spectrum of $n_j^s(t)$. k is the discrete frequency index.

$$P_{nj}^s[k] \times f_s = p_{nj}^s \quad (8.11)$$

$$P_{nj}^s[k] = \frac{\sigma_t^2 f_o}{\tau f_s} \sqrt{2\pi \ln(2)} \quad (8.12)$$

However, lets emphasize here that the noise resulting from the jitter is concentrated at the time when the pulse exists, a concentration factor is $1/DUT$. Jitter will cause more error if AWGN and jitter have same average power, or same spectrum amplitude, because jitter exists solely when the pulse exists while AWGN exists all the time.

In addition, the jitter noise depends on the amplitude of the sampled pulse that can be shown by just multiplying $g(t)$ by an amplitude term.

To empirically measure the jitter amount in the received signal, an equation will be deduced that describes a ratio r of the pulse spectrum maxima at $f = 0Hz$ to the noise floor that depends on the jitter power σ_t^2 , the pulse repetition rate f_o , and pulse width τ . Since for our system f_o and τ are known values, the jitter in the system can be estimated. For the sampled Gaussian pulse (8.13), $\tau_n = \tau/T_s$.

$$g[n] = e^{-4\ln(2)(\frac{n}{\tau_n})^2} \quad (8.13)$$

$$e^{-4\ln(2)(\frac{n}{\tau_n})^2} * \delta_{N/m}[n] \xleftrightarrow{DFT^N} \tau_n m \sqrt{\frac{\pi}{4\ln(2)}} e^{-\frac{(\tau_n k)^2}{4\ln(2)}} \delta_m[k] \quad (8.14)$$

The pulse train $s[n]$ corresponding DFT [85] is shown by (8.14). Where N is the total number of points used to calculate the DFT, m is the number of pulses exists in such N points, and $\delta_i(n)$ equals one when $n = .., -2i, -i, 0, i, 2i$, and zero otherwise. The power spectral density (PSD) of a signal $x[n] \xleftrightarrow{DFT} X[k]$ [19] and it is the same relation used by Matlab (8.15).

$$PSD = \frac{(\frac{X[k]}{N})^2}{\Delta f} \quad (8.15)$$

Where $\Delta f = f_s/N$ is the resolution of the DFT . To find r , the amplitude of the PSD of the Gaussian pulse train $s[n]$ will be used at $k = 0$ (8.16)-(8.17).

$$PSD(s[n])_{k=0} = \frac{\tau^2 f_0^2}{\Delta f} \frac{\pi}{4\ln(2)} \quad (8.16)$$

$$r = \frac{PSD(s[n])_{k=0}}{P_{nj}^s[k]} \quad (8.17)$$

$$r = \frac{\tau^3 \sqrt{2\pi} f_0 N}{\sigma_t^2 (4\ln(2))^{3/2}} \quad (8.18)$$

This relation can be used to calculate the system jitter from the spectrum of the sampled pulse train $s(t)$ for a given τ and f_0 .

Fig. 8.5 shows simulation results of the localization system, simulation platform is explained in a later section, where fft length N is 213, and the pulse repetition rate f_0 is $100MHz$. For example, for $1ps$ total jitter $r = 70.8dB$, while for $10ps$ jitter $r = 50.8dB$ which show very good agreement with (8.18).

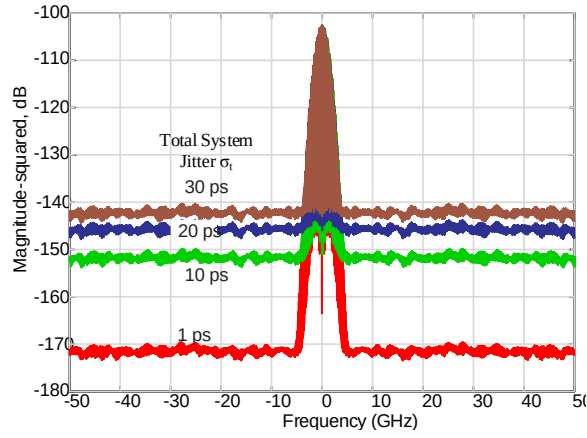


Figure 8.5: Power spectral density of simulated sampled Gaussian pulses. 1, 10, 20, and 30 ps are used for the total system jitter σ_t . Pulse repetition rate is 100 MHz. Fast Fourier transform is of length N equal 213, pulse width τ is 300 ps, and normalized pulse amplitude $A = 1$. Ratio r of the peak to the noise floor agrees very well with (8.18).

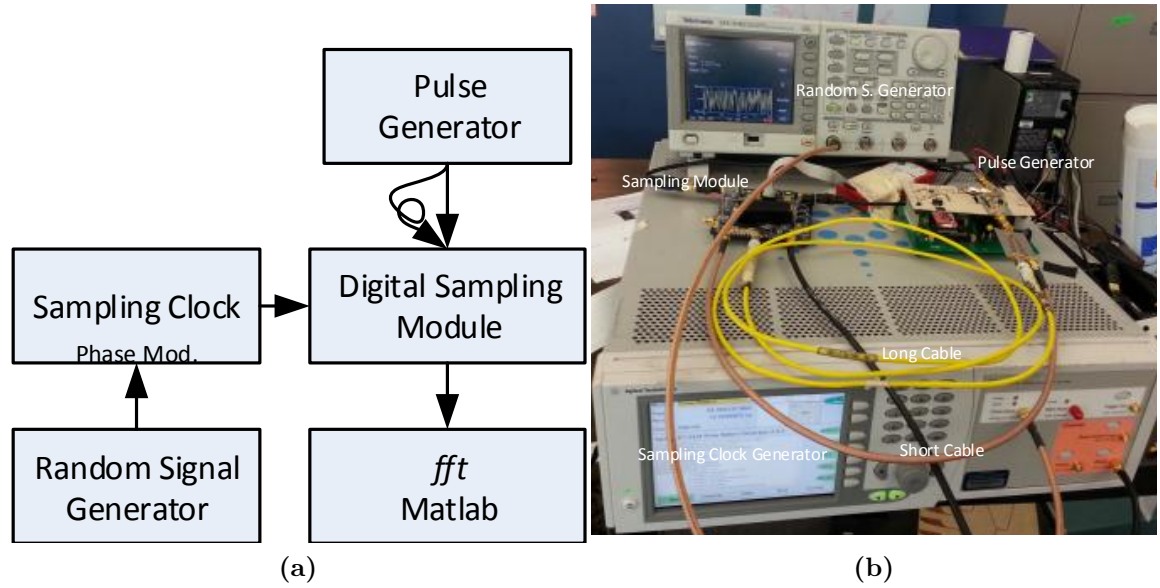


Figure 8.6: Block diagram and picture of the experiment used to measure Gaussian pulses at different sampling clock jitter. Without the fft block we obtain the time domain pulse Fig. 8.7a, and with fft we get the PSD shown in Fig. 8.7b.

Table 8.1: Measured Jitter and Resulting Noise in Gaussian Pulses

Sampling (RX) Clock Jitter (ps)	Measured r (dB)	Back calculated Jitter (ps)	$\sqrt{\sigma_{tr}^2 + \sigma_{rx}^2}(\sigma_{tr} = 15ps)(ps)$
3	37	15.4	15.2
20	32	27.5	25
40	27.5	46.2	42.7
50	25.5	55	52.2

To validate our results, we used the experiment setup shown in Fig. 8.6. In this experiment, the pulse generator is connected, after splitting the pulse into two copies using a wide-band Wilkinson splitter, to the digital sampling module that works based on the sub-sampling technique. Meanwhile, two cables with different lengths mimic the different ToA delays. The sampling clock jitter is controlled by modulating the phase of the sampling clock using a random signal generator. It was swept starting from 3 ps, the minimum, to 50ps. The tag clock has a measured jitter of 15ps. The resulting sampled time domain pulses, spectrum, ToA, and TDoA were saved.

Fig. 8.7a shows the time domain measured Gaussian pulses as the sampling clock jitter was varied for the values 3, 20, 40, and 50ps. We notice how the sampled pulses get noisier as the clock jitter increases. For the total jitter, the transmitter and the sampler clock jitter should be added. Fig. 8.7b shows the *PSD* of pulses shown in Fig. 8.7b. Noise floor looks white which supports the initial assumption of white Gaussian jitter, and it increases with increasing jitter. Ratio r is independent of the pulse amplitude.

Table 8.1 summarizes these results. Column one shows receiver (sampling) clock jitter-independent variable. Last column shows the total jitter of the system, obtained using (3) and 15 ps measured transmitter jitter. Second column shows the ratio r read from Fig. 8. Third column shows the total jitter σ_t calculated using (8.18).

The values of the total system jitter are close to that calculated using (8.18) if we consider transmitter jitter. The simulation results are in very good agreement with (8.18) while measurements are within 5% error. The discrepancy arises from the

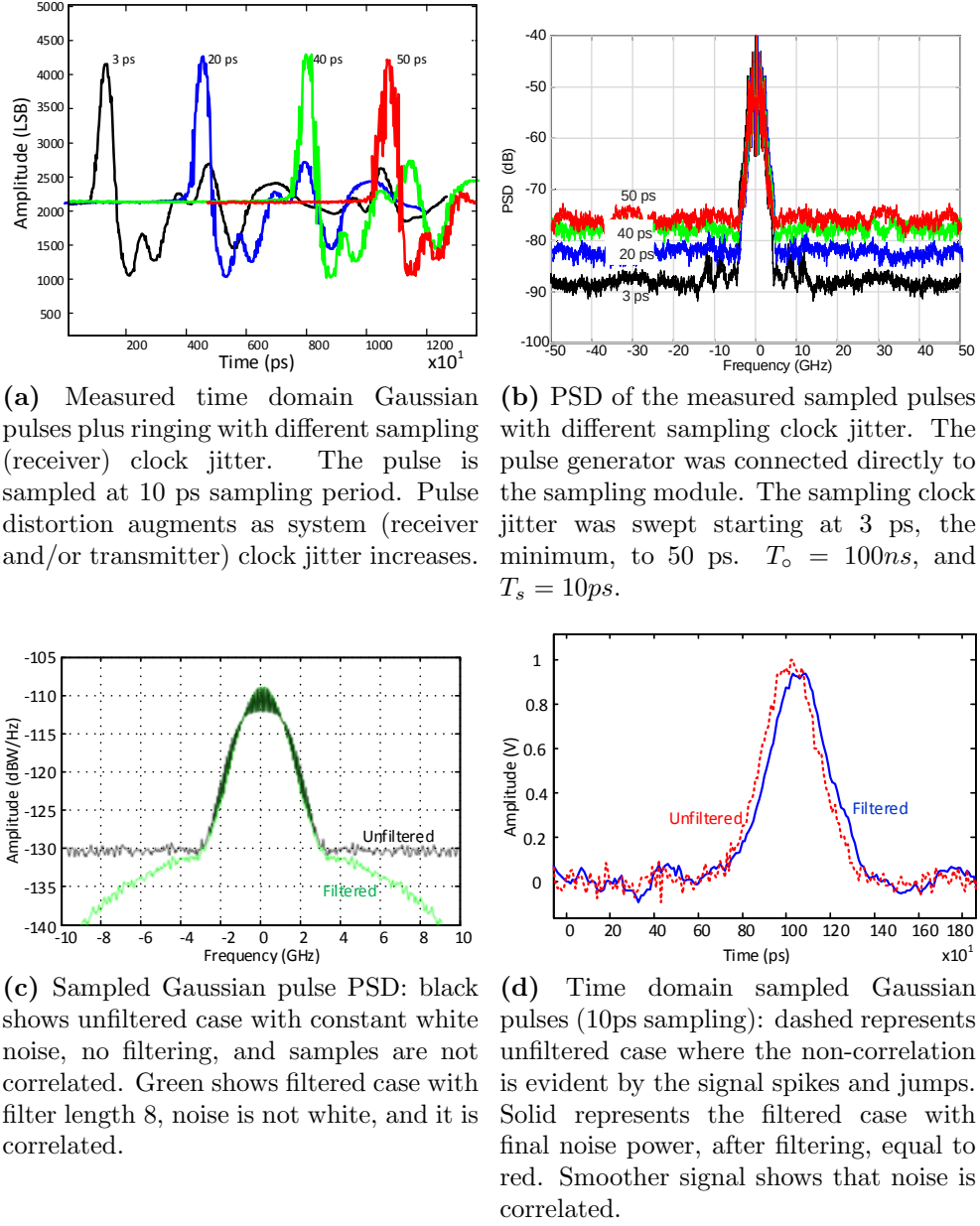


Figure 8.7

background noise is not a perfect straight line to measure clearly the ratio r , the Gaussian shape is an approximation, and that we ignore the real pulse generator ringing.

In summary, the total jitter in the system can be found by two methods. 1- measuring the receiver and transmitter jitters, and find the root of the sum of the squares, but that requires accurate instruments to measure the jitter, and does not take into account other sources of jitter in the receiver and transmitter, i.e. jitter added by the pulse generator, or by the ADC. 2- Sampling the pulse and using the PSD to find the total jitter, which is much simpler and easier. A time domain method is also possible, but we used the spectrum to show that the jitter caused amplitude noise has a white spectrum.

Notice that to find the jitter we connected the pulse generator directly to our sampling module, and neglected AWGN effect, as it is significantly lower.

8.4 Leading Edge Detection Mathematical Model

ToA of a Gaussian pulse can be found by simply using a constant threshold. However, for a fixed threshold, there will be an error in ToA when the pulse amplitude changes, as we move the tag further and closer to the receiving antenna. To circumvent this problem, we use a leading edge algorithm that is based on CFT. It dynamically changes the threshold value based on the amplitude of the received pulse, and keeps a half threshold ratio fixed all the time. That means a pulse received of amplitude A is compared to a threshold level of $A/2$. The error analysis should be similar to the case of received pulses of invariable amplitude and constant threshold, and will be adopted here.

Before the leading edge algorithm, Fig. 8.8, a moving average filter with a length l is applied to reduce the noise. The noise of raw samples is uncorrelated. However, it becomes correlated with the use of a low-pass (averaging) digital filter, signal filter.



Figure 8.8: Block diagram of the digital processing that takes place inside the FPGA. The raw sampled pulse is fed to a low-pass (averaging) filter to get rid of out of band noise (jitter, AWGN,). The leading edge algorithm is used to find the ToA. Post filter is used to decrease the final timing error.

Such filter decreases the noise power (variance) by a factor l as will be discussed later on. Meanwhile, the noise becomes band-limited, not white, as the filter limits the bandwidth. Additionally, the noise at consecutive samples becomes dependent as well.

Finally, A post-processing filter is applied on TDoA values to further reduce its error by using a moving average filter of length l_p .

Fig. 8.7c shows the spectrum of a filtered and unfiltered pulse, it shows how the noise at the unfiltered case is almost straight-line indicating white noise. On the other hand, the filtered case noise is affected by the filter, and it is not white anymore.

Fig. 8.7d shows the time domain of a pulse for two different cases. The filtered case has noise $n(t)$ and uses an averaging filter of length $l = 8$, so the noise power after filtering is $n(t)/\sqrt{8}$. The unfiltered case, the signal has noise $n(t)/\sqrt{8}$ with no filtering, i.e. both cases have the same noise power. We can notice that the unfiltered case has spikes, and the filtered case is smoother. In Fig. 8.7d, although the noise power was adjusted to be the same for the two plotted pulses, a smoother pulse indicates that the noise at different samples is correlated. Hence, there is a need for different treatment for the two cases.

We will discuss the leading edge error in two sections: one for the simple case of unfiltered (uncorrelated) noise and the second for filtered (correlated) noise. Second case can be applied to uncorrelated noise by setting the signal filter length to one.

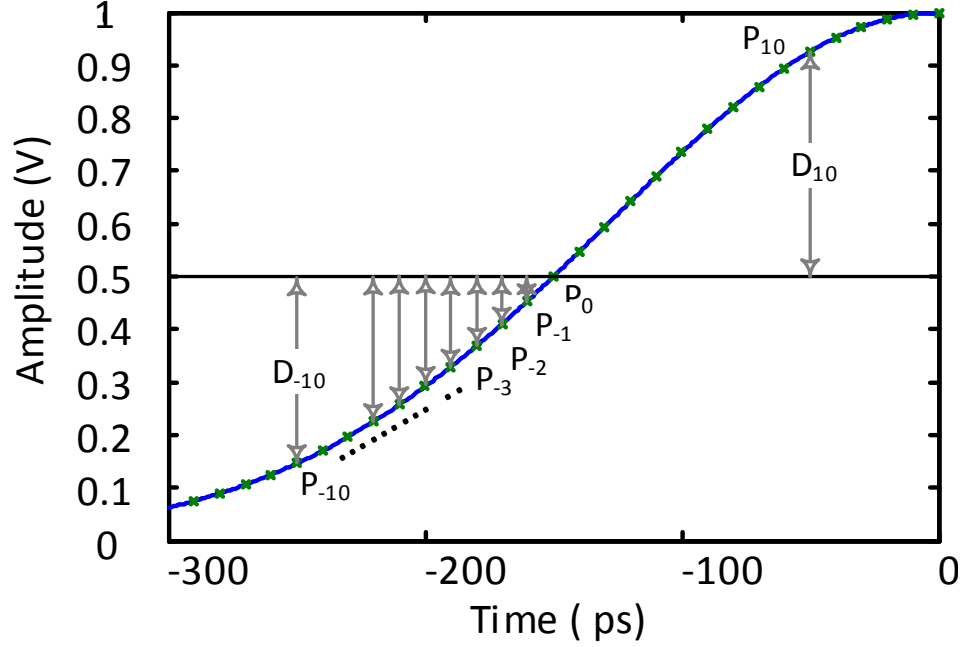


Figure 8.9: leading edge of the pulse showing noise amplitude to hit threshold (0.5). A constant threshold of half is equivalent to LE algorithm when we receive pulses with varying amplitude.

8.4.1 Unfiltered Case (Uncorrelated Noise)

In this section, the error of the leading edge algorithm is addressed. The error types are precision and accuracy errors i.e. variance and bias errors. The probability density function of the leading edge algorithm process is found based on the probability of first success. The probability of first success is based on the AWGN and jitter noises at each point of the leading edge of the pulse. The probability density function (*PDF*) is used to find the expectation and variance of the LE.

The well-known probability equation that describes the probability of the first success occurrence at the m^{th} trial if the success rate is q_i is used (8.19). Q_{le} is the leading edge probability.

$$Q_{le}(m) = q_m \prod_{i=1}^{m-1} (1 - q_i) \quad (8.19)$$

For our application, notice Fig. 8.9, as we move back in time from p_o , the distance between the pulse and the threshold increases. That means for a certain noise power the probability to hit the threshold is going to decrease. The probability monotonically decreases until it is negligible at a certain point. Going back ten points, i.e. time samples, seems adequate for our noise range analysis. The point -10 is used as the start of the probability product in (8.19). The reference point here is where the pulse amplitude equals half and it is at time $-\tau/2$ back from the pulse peak. The success rate, i.e. hitting the threshold level at each of these points, can be found using (8.19), q_i is found using (8.20).

$$\begin{aligned}
q_i &= Q(n(t) > 0.5 - g(kT_s)) \\
&= 0.5 \operatorname{erfc}\left(\frac{D_m}{\sqrt{2}\sigma_n^m}\right) \quad m < 0 \\
&= 1 - 0.5 \operatorname{erfc}\left(\frac{D_m}{\sqrt{2}\sigma_n^m}\right) \quad m \geq 0
\end{aligned} \tag{8.20}$$

Where Q is the probability and D_m is shown in Fig. 12. We will use (8.19) to study the statistical behavior, i.e. variance, and mean, of the unfiltered case.

8.4.2 Filtered Case (Correlated Noise)

In case of dependent trials, a joint distribution is used to find the probability of hitting the threshold (8.21).

$$\begin{aligned}
Q_{le}(m) &= Q(p_{-10} = \text{fail}, p_{-9} = \text{fail}, \dots, p_m = \text{success}, p_{m+1} = \text{don't care}, \dots) \\
&= f_X(X_{-10} < D_{-10}, X_{-9} < D_{-9}, \dots, X_m > D_m, X_{m+1} < \infty, \dots)
\end{aligned} \tag{8.21}$$

Where $Q_{le}(m)$ is the probability of leading edge taking place at sample m , X_n is random variable represents noise amplitude at each point. X is defined as

a multivariate normal distribution (8.22), μ and Σ are the mean and covariance matrices.

$$X \sim \mathcal{N}_m(\mu, \Sigma) \quad (8.22)$$

$$\mu = [E[X_1], E[X_2], \dots, E[X_m]] \quad (8.23)$$

$$\Sigma = [Cov[X_i, X_j]] \quad i = 1, 2, \dots, m; j = 1, 2, \dots, m \quad (8.24)$$

The distribution density f_X in (8.21) for random multivariate normal variable X is defined by .

$$f_X(x_1, x_2, \dots, x_k) = \frac{1}{(2\pi)^{k/2} |\Sigma|^{1/2}} e^{-\frac{1}{2}(X-\mu)^T \Sigma^{-1} (X-\mu)} \quad (8.25)$$

Assuming the noises at all the points are identical, with zero mean $\mu = [0, 0, 0, \dots, 0]$ and variance σ_n^2 , then the covariance matrix Σ can be constructed.

For a moving average window filter with length l , $s_f(mT_s) = \frac{1}{l} \sum_{i=m-l}^{i=m} s(iT_s)$ is the filtered signal, and $n_f(mT_s) = \frac{1}{l} \sum_{i=m-l}^{i=m} n(iT_s)$ is the filtered noise. The variance of the filtered noise can be found as follows: the noise at different samples are independent before filtering, the variance of the sum of independent variables equals the sum of its variance, then the variance is given by (8.27), which indicates that the noise power is reduced by $1/l$.

$$Var(n_f(mT_s)) = E[n_f^2(mT_s)] = \frac{1}{l^2} E\left[\sum_{i=m-l}^{i=m} n^2(iT_s)\right] \quad (8.26)$$

$$Var(n_f) = \frac{1}{l^2} \times \sum_{i=m-l}^{i=m} \sigma_n^2 = \frac{1}{l} \times \sigma_n^2 \quad (8.27)$$

To build the covariance matrix, we use (8.28), d is the distance between the two points under covariance operation. Since $n(iT_s)$ and $n(jT_s)$ are independent for $i \neq j$,

only the terms with $i=j$ will have expectation of σ_n^2 and the final covariance terms are found using (8.29).

$$\begin{aligned} \text{Cov}\left(n_f(mT_s), n_f((m+d)T_s)\right) &= E\left[n_f(mT_s) \times n_f((m+d)T_s)\right] \\ &= \frac{1}{l^2} E\left[\sum_{m=m-l}^{n=m} n(iT_s) \times \sum_{j=m+d-l}^{j=m+d} N(jT_s) \right] \end{aligned} \quad (8.28)$$

$$= \frac{1}{l^2} (l-d) \sigma_n^2 \quad (8.29)$$

An example for this calculation: let us assume six consecutive points and a filter length of $l = 4$, the covariance matrix is given by (8.30).

$$\Sigma = \begin{bmatrix} \frac{\sigma_n^2}{4} & \frac{3\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} & \frac{\sigma_n^2}{16} & 0 & 0 \\ \frac{3\sigma_n^2}{16} & \frac{\sigma_n^2}{4} & \frac{3\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} & \frac{\sigma_n^2}{16} & 0 \\ \frac{2\sigma_n^2}{16} & \frac{3\sigma_n^2}{16} & \frac{\sigma_n^2}{4} & \frac{3\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} & \frac{\sigma_n^2}{16} \\ \frac{\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} & \frac{3\sigma_n^2}{16} & \frac{\sigma_n^2}{4} & \frac{3\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} \\ 0 & \frac{\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} & \frac{3\sigma_n^2}{16} & \frac{\sigma_n^2}{4} & \frac{3\sigma_n^2}{16} \\ 0 & 0 & \frac{\sigma_n^2}{16} & \frac{2\sigma_n^2}{16} & \frac{3\sigma_n^2}{16} & \frac{\sigma_n^2}{4} \end{bmatrix} \quad (8.30)$$

The equal noise at all the points is justified for the AWGN noise. It is less accurate for the jitter noise though. To get a more accurate model for the jitter noise, a different noise power at each point according to (8.4) should be used. While a second Taylor series expansion approximation should be utilized as it will be more accurate for large jitter values.

We also assumed that one sampling instance will coincide with p_o , Fig. 12, this is inaccurate though, because the pulse arrives at arbitrary time. In order to account for that, the leading edge probability was calculated for different sample points shifts, and the result was averaged.

Subsequently, the last step is to translate the variance error, and mean square error in the leading edge time of two base-stations to a TDoA error. Since TDoA is $LE_2 -$

LE_1 , where LE is the leading edge time and the subscript designate the base-station number. The errors for the two leading edges times are independent even if the two channels have some noise in common, since the LEs take place at different times, and generally larger than the filter size. The mean square error in the TDoA can be found using (31).

$$Var[TDoA] = Var[LE_2 - LE_1] = Var[LE_2] + Var[LE_1] \quad (8.31)$$

8.5 Simulation Frame Work

In parallel to analytical analysis, a Matlab Simulink, Fig 8.10, was used to simulate two-channel system, where we can introduce common jitter to both channels and independent AWGN to each as well. LE and TDoA are the final outputs. The simulation block diagrams start by a generator, it generates a train of Gaussian pulses, it branches into two similar pulse trains, their amplitude is 1 V. A gain stage controls the pulse amplitude at each channel separately.

The gain block is followed by a fractional delay stage, where the pulse can be delayed by a fraction of a sample time. The delay is controlled by a uniform random number generator. This delay stage reflects the physical system, where the pulse generation and the sampling process are not synchronized, and the pulse generation time relative to the sampling instant changes in a random way. This delay is subtracted at the end of each channel when finding the leading edge time.

The AWGN noise and the jitter effects are addressed by using two normal random number generators. The first is added directly to the amplitude of the pulse to replicate the effect of AWGN. The second represents the jitter, it controls the sample and hold clock delay. Sixteen-bit quantization stage and a moving average filter, we can control its length, comes next.

The final stage is the leading edge stage that uses the algorithm described earlier. The output of that stage presents the number of samples passed since the pulse is initially

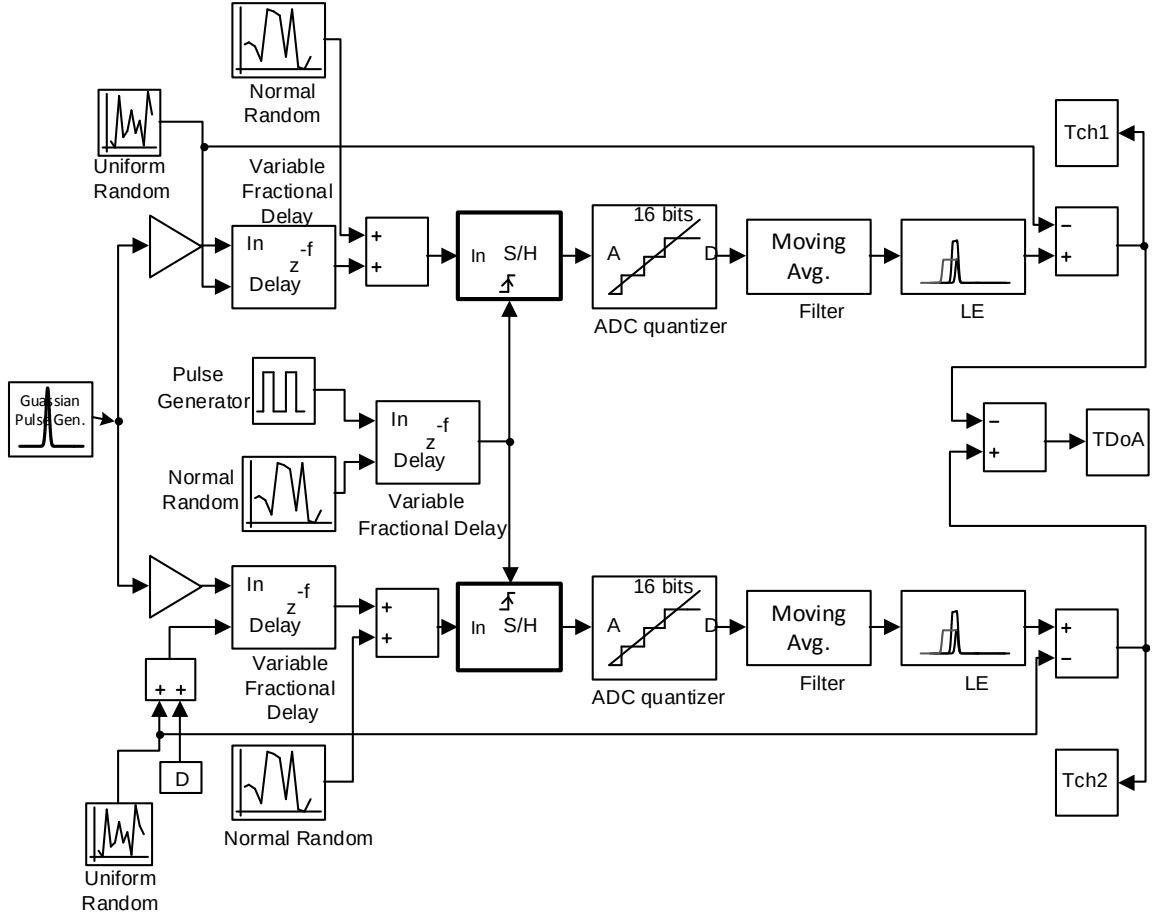


Figure 8.10: Simulation framework that simulates clock jitter, AWG, ADC word size, filter size effects, and sampling rate. It uses Matlab Simulink. We collect the ToA and TDoA for long runs and find the variance and expectation to compare with measurements and mathematical model.

generated until it reaches the leading edge stage. The random delay of the Gaussian pulse that was added earlier is subtracted from the final leading edge. $LE_1 = t_{ds} + e_1$ and $LE_2 = t_{ds} + D + e_2$ where t_{ds} is the inherent delay of the simulation blocks. e is the error caused by jitter, quantization, sampling, and AWGN for each channel. D is the delay introduced for the second channel to represent the difference in arrival time of received pulses, and to insure the error caused by the jitter is independent similar to the practical system.

The TDoA is found by subtracting the leading edge times $TDoA = LE_1 - LE_2$ and $TDoA = D + e_2 - e_1$. The simulation will output ToA of each channel and TDoA. We collect long runs of points to find the variance and mean. Results of this simulation will be used to validate our empirical and experimental results in the following section.

8.6 Results and Discussion

This section will present some of our simulation and measurements of the whole system. In general, jitter and AWGN with same noise power result in a close leading edge error, but not the same since jitter to amplitude noise conversion is not equal at all pulse points but is dependent on the signal slope (8.4), while the AWGN is invariant all the time.

Henceforth, we will represent AWGN with an equivalent jitter amount that produces the same average power in 2τ period (8.7), 1ps is equivalent to $11.6\mu w$. We will show the effects of system noise and imperfection on the realized accuracy. We will compare the analytical simulation and the mathematical model and compare them to measurements.

8.6.1 TDoA Expectation (mean) (Accuracy error)

CFT systems are designed to produce accurate timing information from analog signals of varying heights but with the same rise time. This is done by splitting the input

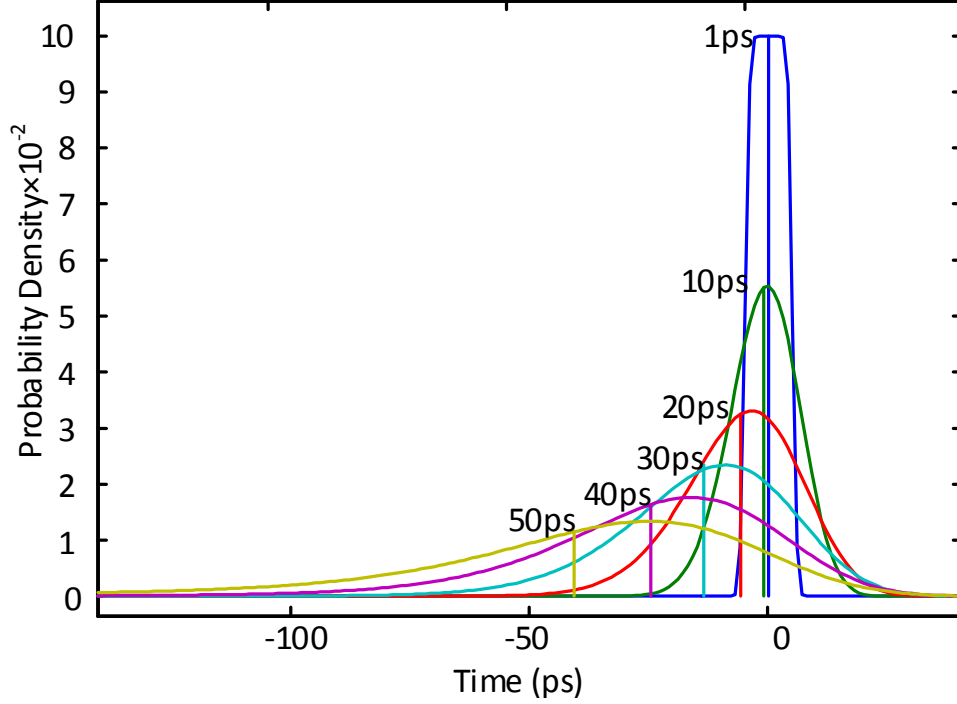


Figure 8.11: PDF of LE time as the AWGN noise is changed starting at 1ps up to 50 ps. Expected ToA, mean, changes by 40 ps upon 50 ps change in AWGN level.

signal, attenuating (amplifying) half of it and delaying the other half, then feeding the two halves into a fast comparator CFT triggers a timing signal at a constant fraction of the input amplitude. The trigger always appears before the true maximum of the pulse. This offset should be a constant offset and independent of the amplitude. However, in our measurements, we saw a slight shift increase. It appears as the noise level increases, and the CFT appears to lag in time. Fig. 8.11 shows the probability density function of the leading edge time for the unfiltered case. We observe about 40 ps movement in the expected value, shown by the vertical line, when the AWGN increases from 1 to 50 ps. Post-processing filters will not overcome this kind of error. It is crucial for a high accuracy system to keep the expected value of ToA unchanging. The impact on system performance is pronounced in case of AWGN noise. Typically, jitter value at the receiver is the same for all the channels, and expected value change will be nulled as TDoA is used. For AWGN, the SNR changes as we move the tag inside the volume.

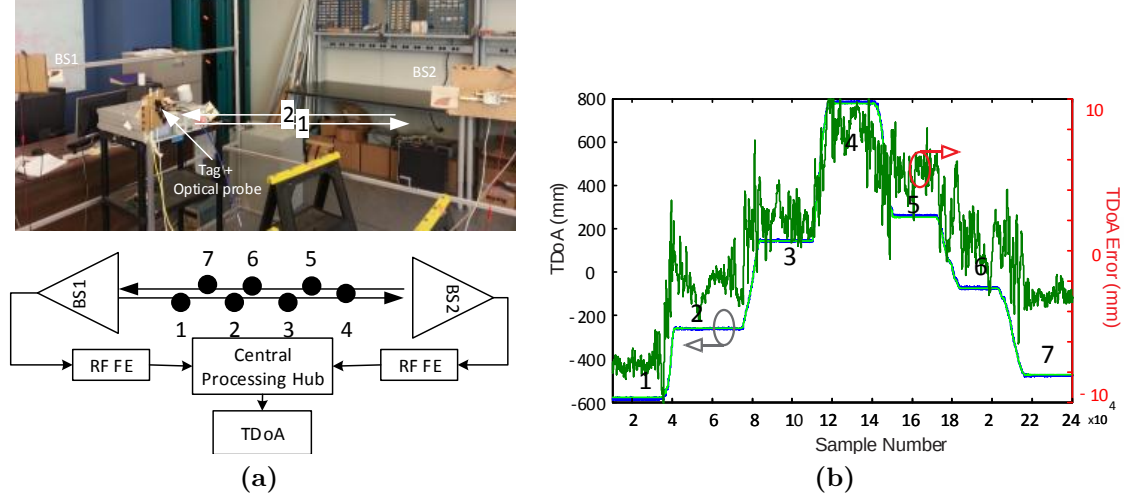


Figure 8.12: (a) Picture of an experiment where we move the tag and optical probe, then we measure the error. (b) Measured TDoA of experiment in part (a), LE2 LE1 in blue as we move the tag from BS2 to BS1 and return it again. TDoA error in green shows positive deviation as we go from BS2 to BS1 while SNR2 decreases and SNR1 increases. Inverse behavior is noticed as we return to BS2.

An experiment was performed to verify the simulation and the mathematical model prediction of expectation change as the noise changes, Fig. 8.12. We used two base-stations with facing antennas. The two antennas are about 2 m away. A tag was moved from position 1, closer to base station one (BS1) antenna, to position 4, closer to BS2 antenna. The Tag was moved back again to position 7 closer to BS1. The tag was moved on the straight-line connecting BS1 antenna and BS2 antenna. The left ordinate axis in Fig 8.12b shows the TDoA of the tag in mm.

When we move from position 1 to 4, SNR1 of BS1 decreases and LE1 expected time retreats (moves backward). SNR2 increases and LE2 expected time advances. A reverse effect takes place when moving from position 4 to 7. The total expectation or bias error, for $TDoA = LE2 - LE1$, is bias error of LE2 minus bias error of LE1, thus the bias error in the TDoA will increase as we move from position 1 to position 4 and decreases as we move back to position 7.

Fig. 8.12b shows the measurements data of the UWB system and optical measurement system of 0.3 mm accuracy as a ground truth. The TDoA values are post filtered with

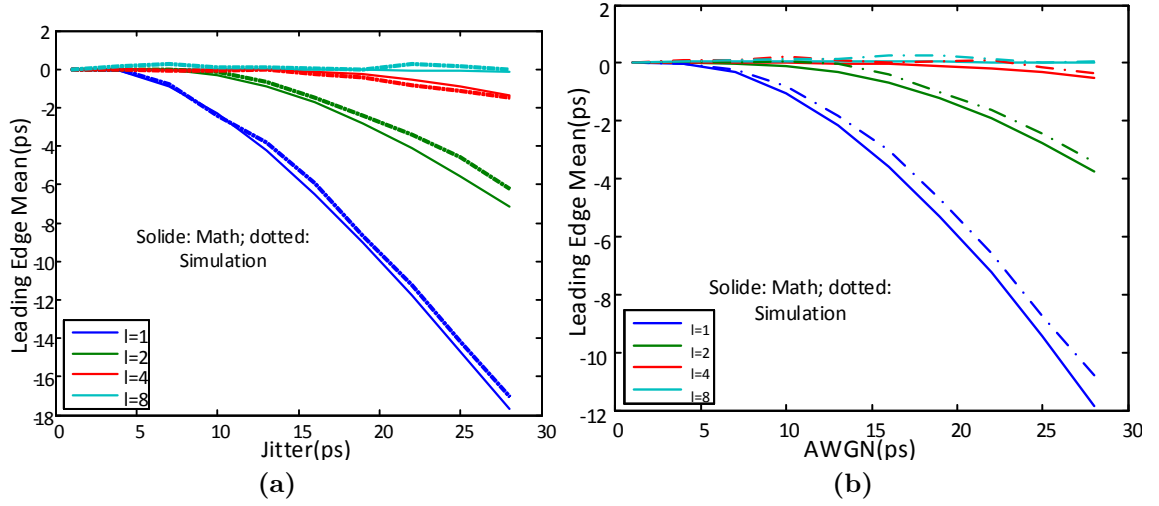


Figure 8.13: Relative expected value or mean for LE time and filter effect. Longer signal filter improves the mean bias error. X-axis represents (a) jitter, and (b) AWGN in equivalent jitter.

an averaging window filter of length 100 to isolate the expected value. Fig. 15(b) right ordinate axis depicts the deviation of the UWB measurements as we move. It starts with a bias error of -8 mm at position 1 closer to BS1 and increases to 10 mm at position 4 closer to BS2. It then retreats to about -3 mm at position 7. Results are consistent with the mathematical and simulation models, where a shift in expected value is present as the SNR changes.

In Fig. 8.13, the expectation of the leading edge time is shown as a function of clock jitter and AWGN using simulation platform and mathematical model, i.e. expectation of (21), they show very good agreement. TDoA expected value behavior is found by subtracting expected value for two base-stations. The mean value bias error decreases as signal filter size increases.

8.6.2 TDoA error (Variance)

Leading edge error, variance of (21), is sensitive to clock jitter and AWGN. Error lessens as the filter size increases. Fig. 8.14 depicts that behavior and shows agreement of both mathematical model and simulation. Fig. 8.15 shows

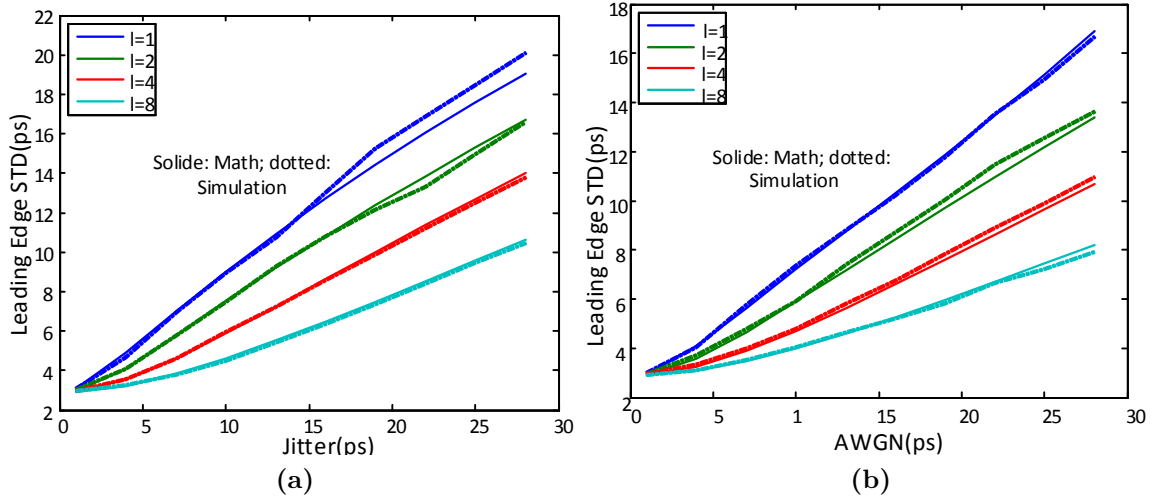


Figure 8.14: Error in LE edge ToA with different filter size. (a) jitter. (b) AWGN, the x-axis shows the AWGN level in equivalent jitter ps.

measurements, we varied the sampling clock jitter and measured the corresponding LE error. Fig. 8.15 shows the error vs. the total jitter back calculated from pulse spectrum using (8.18).

Measurements show agreement with both mathematical model and simulation. They indicate that for a 15 ps jitter and for a filter length 8, a leading edge error of about 6 ps is estimated. Definitely lower system jitter would lead to a lower LE error.

8.6.3 Sampling Rate

Fig. 8.16 shows that increase in sampling period T_s increases the error, i.e. variance of (21). The minimum LE mean square error for a given sampling period T_s , without post-processing filter, is fixed and independent of the signal filter length, it is given by $T_s/\sqrt{12}$. The minimum error conforms to the standard deviation of a uniform random variable, and that describes the random manner the pulse is received with respect to sampling instances.

Fig. 8.17 explains the signal filter length limitation. Maximum length that improves the LE time error is $l \times T_s \approx \tau$. For our system $\tau = 300ps$, and for sampling time 10

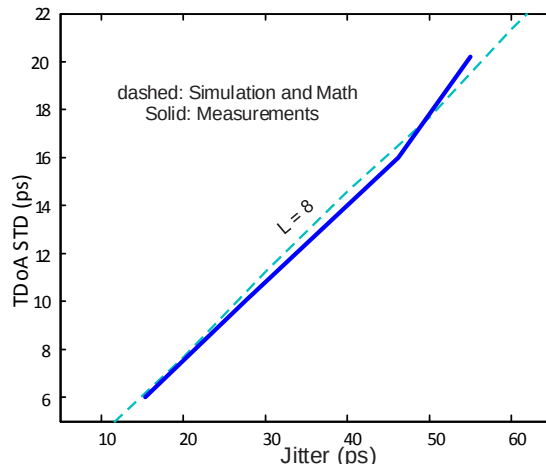


Figure 8.15: Measurements of the error vs. the total system jitter. It shows good conformation with the mathematical model and simulation platform. The low-pass digital signal filter used length is 8.

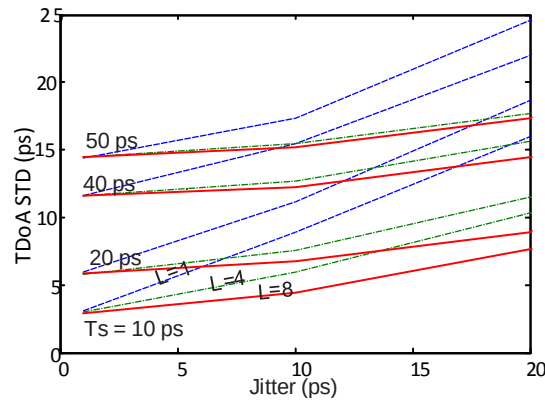


Figure 8.16: Simulation shows that the sampling rate limits the minimum error. It also shows that a filter length of 8 adds almost no improvement compared to 4 for 50 ps sampling time.

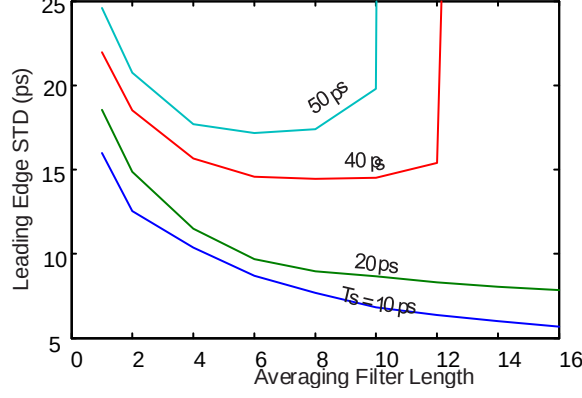


Figure 8.17: Filter size impact on LE time error or variance with different sampling rates. It shows that low-pass signal filter length increase improves LE time error with upper limit that filter length times sampling time almost equal to Gaussian pulse FWHM $l \times T_s \approx \tau$. Jitter = 20 ps and AWGN = 0.

ps a filter length of up to 32 can be used. For 50 ps maximum filter size is about 6. That explains why filter of length 8 have almost no improvement over 4 in Fig. 17 for $T_o = 50ps$.

8.7 Conclusion

A method to measure the total jitter in high accuracy Gaussian pulse systems by using the sampled power spectral density is developed. The results are dependent on a certain CFT algorithm described, and they could be applied to constant threshold for constant amplitude pulses or similar algorithms. A mathematical model and simulation platform are introduced to describe the error of a localization system. The model predicted the jitter, AWGN, and sampling rate caused errors.

It explained a phenomenon of error in localization that changes with distance. It was shown that the change in SNR as we move the tag around the volume leads to a shift in the expected value of the ToA of the pulse, it cannot be overcome using a post filter, and the signal filter reduces this error though. We also showed that the minimum error is proportional to the sampling time, with our implementation of the

leading edge algorithm. An interpolation method can be used to alleviate this lower limit.

A compromise exists though between the dynamic independent update rate of the system and the error of TDoA given a specific AWGN and jitter in the system we can use bigger post filters to reduce the error that is going to reduce the independent update rate as well.

To measure the total jitter in the system, a measurement of each component time jitter is required utilizing accurate instruments that are expensive. Here, we presented an easy way to measure the total jitter in the system using the digital spectrum, fast Fourier transform, of the sampled pulse.

Moreover, the mathematical model/simulation could expect the mean square error caused by AWGN and jitter. Jitter and AWGN have similar spectrum but different temporal properties i.e. jitter is highest when the signal slope is maximum. Consequently, similar AWGN and jitter noise powers cause different errors. The measurement was in excellent agreement with the models.

We also found out that the signal averaging filter length is limited and the increase in filter length over this limit worsens the accuracy achieved. New type of filters, i.e. correlation filter, could be used to overcome this limitation.

Chapter 9

Discussion and Design Guidelines

In this chapter, we will have a general discussion of the localization system errors and potential remedies. we will wrap up with design guide based on the models that were developed through the dissertation.

9.1 System Errors and Remedies

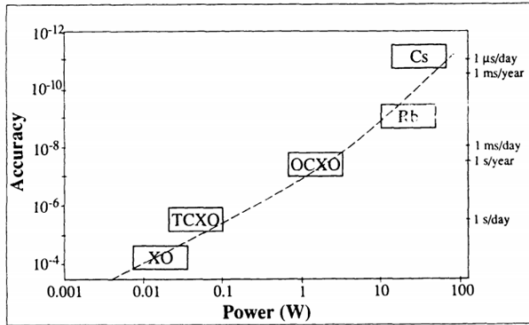
The system suffers from errors that can be categorized to either accuracy or precision errors. Accuracy errors can be divided into time variant and location based errors. A general discussion of the remedies and future work are addressed in the following sections.

Table 9.1: Noise Categories

Error Source	Type	Remarks
Jitter	Precision	
AWGN	Precision	
Quantization	Precision	
Clock Drift	Accuracy	Time based
Phase Center	Accuracy	Position based
AWGN	Accuracy	Position based
Multipath	Accuracy	Position based



Figure 9.1: Atomic clock on chip by MicroSemi.



(a)

	Quartz Oscillators			Atomic Oscillators		
	TCXO	MCXO	OCXO	Rubidium	RbXO	Cesium
Accuracy* (per year)	2×10^{-6}	5×10^{-8}	1×10^{-8}	5×10^{-10}	7×10^{-10}	2×10^{-11}
Aging/Year	5×10^{-7}	2×10^{-8}	6×10^{-9}	2×10^{-10}	2×10^{-10}	0
Temp. Stab. (range, °C)	5×10^{-7} (-55 to +85)	2×10^{-8} (-55 to +85)	1×10^{-9} (-55 to +85)	3×10^{-10} (-55 to +68)	5×10^{-10} (-55 to +85)	2×10^{-11} (-28 to +65)
Stability, $\sigma_y(t)$ (t = 1 s)	1×10^{-9}	1×10^{-10}	1×10^{-12}	3×10^{-11}	5×10^{-12}	5×10^{-11}
Size (cm ³)	10	50	20-200	800	1200	6000
Warmup Time (min)	0.1 (to 1×10^{-6})	0.1 (to 2×10^{-8})	4 (to 1×10^{-8})	3 (to 5×10^{-10})	3 (to 5×10^{-10})	20 (to 2×10^{-11})
Power (W) (at lowest temp.)	0.05	0.04	0.25 - 4	20	0.35	30
Price (~\$)	100	1,000	2,000	8,000	10,000	40,000

* Including environmental effects (note that the temperature ranges for Rb and Cs are narrower than for quartz).

(b)

Figure 9.2: (a) Relationship between accuracy and power requirements (XO=simple crystal oscillator; TCXO=temperature-compensated crystal oscillator; OCXO=oven-compensated crystal oscillator; Rb=Rubidium frequency standard; Cs=Cesium beam frequency standard). (b) Crystal and atomic oscillators comparison, after [6].

9.1.1 Clock

Crystal oscillator are based on quartz. It has high quality factor and presents a stable frequency determining component in the oscillator circuit.

The main drawback of crystal oscillator is that the frequency is dependent on the temperature change. There are three types of crystal oscillators based on what mechanism used to deal with that problem. XO (crystal oscillator) does not have temperature control of any kind. TCXO uses a temperature dependent reactance to counter the effect of the temperature on the crystal. OCXO uses a small oven to maintain the crystal temperature as invariant as possible.

As an example TXCO and OCXO from Conner Winfield. The sizes are 7x5x2 mm, and 9x14x9 mm respectively. The typical jitter values are 3, and 0.5 ps. The frequency stability vs temperature is from -20 to 20 ppm/c, and -1 to 1 ppm/c. Their power consumption is 20 mW, and 2.5 W respectively. The price of the OCXO is about 20 times the TCXO. The OCXO size is big and consumes high power for a tag design, It will add much to the price of multi-tag system, it can be used though for the receiving module to improve its performance.

Atomic clocks has superior performance to crystal oscillators, they are used for GPS system. Big size and high price are the prohibiting factors for using it in an indoor localization system. However, Atomic clock on chip Fig. 9.1 by MicroSemi looks a good potential candidate. The price is still high, hundreds of dollars. the size is 40x35x11 mm, and the power consumption is 120 mW. MicroSemi claims two orders of magnitude better performance than OCXO.

Fig. 9.2a shows the accuracy dependence on power,[6] it is a 1991 technical report but its data can be used for comparison. For high clock stability and long time operation OCXO or Cesium atomic clock should be used, TCXO with 1 s/day Accuracy is large compared to 1 ms/day OCXO and 1 μ S/day for the atomic clock. In Fig. 9.2b [6], OCXO based oscillators have the best short term stability (Allan Variance) σ_y of 1^{-12} of the nominal frequency, beating atomic clocks. Also, Cesium based atomic oscillators have the best accuracy performance of 2^{-11} /year, three orders of magnitude better than OCXO and five orders of magnitudes better than TCXO.

9.1.2 Sampling

UWB signal has a wide bandwidth, it requires high sampling rate, 6 Gsps is the minimum Nyquist rate, University of Tennessee system case. Direct sampling introduces the least noise to the system. The jitter of the receiver clock, an expensive OCXO can be used, will contribute to the received pulse distortion not the transmitter jitter. Remember that for sub-sampling systems the total jitter that distort the pulse

is $\sqrt{\sigma_t^2 + \sigma_r^2}$, and for a direct sampling system it will be just σ_r . However a 6 Gsps is beyond the commercial state of the art, Texas Instrument has an ADC with 4 Gsps and 12 bit resolution.

One hurdle in the way of using direct sampling is the dependence of the resolution and precision on the sampling time. For direct sampling the sampling time will be so large under the current leading edge algorithm. One more stage should be added before the leading edge algorithm to rebuild or interpolate the pulse points. Another problem is that higher frequency operation, narrower pulse, and larger bandwidth is a desired evolution to the system for better precision/accuracy, ADC speed will not be able to catch up with the demanding analog signal bandwidth.

For higher sampling rates, an equivalent sampling method should be used, where a low speed ADC is used to achieve the high sampling rate for periodic signals. However, more attention should be given to fix various distortion by the sub-sampling process. For some cases, i.e. delay line sub-sampler, efforts to calibrate and measure the true delay times should be pursued based on non-uniform samples to reconstruct the pulse. Compressive sensing has been investigated by Depeng [86] for localization system and preliminary theoretical results are very promising and would allow few measurements to reconstruct the pulse using low rate ADCs. Efforts are under way to prototype such system.

9.1.3 AWGN Mean Error

AWGN impacts both precision and accuracy. Filtering can improve precision. Accuracy problem is that the pulse appears to arrive earlier as its SNR deteriorates. For the current system a dynamic amplification/attenuation system should be added to maintain same SNR for the whole volume. Moreover, new demodulation techniques are another option to improve SNR performance of the system. Correlation receiver is a good option, a fresh locally generated at the receiver copy of the pulse is used to

recover the received pulse. Also, using long integrators to find maximum correlation point removes most of the noise in the signal.

9.1.4 Accuracy Errors

Accuracy errors, e.g. antenna phase center, AWGN shift error, multi-path, and clock drift, are hard to alleviate. one solution for that problem is to calibrate the whole dynamic volume to account for all the accuracy errors present.

Alternatively each error can be addressed separately. Antenna phase center for example, we can improve the phase center stability by adding rods, or lenses. For the clock drift, a static tag in a multi-tag system can help to resolve that problem. Multi-path errors can be reduced by using narrower pulse and higher carrier frequency.

9.2 Design Guide

There are two filters in the system: signal filter and post processing filter. Signal filter is a digital filter that is applied to the digitized pulse to remove AWGN and sampling noise, the upper limit of the filter length is $l \times T_s \approx \tau$. Post processing filter is used for the TDoA to increase the system precision. For the post processing filter, longer filter increases precision of the system. However, longer filters will make the system response slower. Furthermore, position filtering cannot overcome the system accuracy problems.

Systems designers that desire to achieve a certain 1D error e with an independent update rate U . He/she can start by choosing a post-processing filter of length l_p , it will reduce the

TDoA error by $\sqrt{l_p}$. Then the actual system update rate is $U_a = U \times l_p$ to keep the same independent update rate U , U_a is the update rate before the post-processing filter. The error for a single channel of the system e_i is the sum of errors caused by AWGN and jitter in root mean square sense. Either the simulation platform or the

Table 9.2: Error Contribution

Error Source	Position error (mm)	Conditions	
Clock Drift	20	30 minutes	Accuracy
AWGN Mean	20	1.4 m range	Accuracy
Clk Jit+Pulse Gen.	1	-	Precision
Phase Center	4	$\pm 40^\circ$	Accuracy
Sampling Rate	1	$T_s = 10ps$	Precision

mathematical model can be used, given the AWGN, jitter, and filter length, to find such single channel error. The 1D TDoA error equals the sum of the two channels errors, i.e. $= \sqrt{(e_1^2 + e_2^2)}$. The error e is in time units. To convert it to distance, we multiply by c , the speed of light.

The ToA bias error introduced in section VI A. can be determined by finding the maximum and minimum AWGN noise using the system power/noise budget. We then find the shift in the expected value associated with each channel. For 1D case, the bias error should be twice that of a single channel.

Meanwhile, to use the mathematical model we start with (8.25). You need to fill the Σ matrix. For AWGN, σ_n^2 is the same for all the points, it represents the AWGN power. Care should be taken though as the analysis was based on normalized pulse amplitude.

For jitter to fill the Σ matrix, you can assume a constant noise power for all pulse points and use the average power (8.7). You can also use Taylor linear approximation (8.4) for different noise power at pulse points. Second order Taylor approximation can also be used for results that are more accurate. Notice that SNR and LE error arising from certain jitter is based on normalized pulse and should be the same for pulses with different amplitude.

9.3 Map to Millimeter Accuracy

The sources of error contribute to the final localization error. The contribution of errors based on experimental results is shown in Table 9.2.

One path to achieve sub-mm accuracy that summarizes prior discussion is:

Sampling

- Use a direct sampling to get rid eliminate transmitter jitter that uses small low cost clock. Until direct sampling becomes viable, compressive sensing or sub-sampling are more realistic.
- Direct sampling will improve throughput to apply longer post processing filters to further improve precision.
- Use more complicated pulse retrieval filters/algorithms to remove precision dependence on high sampling rate.

Clock

- A high-end clock OCXO/Atomic should be used at the receiver, based on how long the system would operate without calibration.

Demodulation

- Use more sophisticated methods i.e. correlation, to maintain stable and good SNR over the whole volume.

Volume Calibration

- Procedures to calibrate the whole volume should be developed.

Chapter 10

Conclusion

The study of error sources in a 3D localization system is addressed in the dissertation. Our goal is to produce sub-mm precision/accuracy system, so the need to search for and learn the mechanisms of tiny errors formation that could be avoided/eliminated in UWB systems.

Pulse generator is one source of jitter that contributes to augment the total system jitter and the final system positioning error. Jitter in the triggering clock translates directly to jitter in the pulse, clock jitter to AM noise conversion is not noticed. Amplitude to phase conversion mechanism takes place at the SRD pulse generator, it is proportional to the SRD intrinsic charge, AM noise to jitter conversion is periodic in the frequency domain with a period equal to the pulse repetition frequency. A capacitor can be used to decouple the interference signals from the SRD circuit, it reduced the jitter produced by the SRD. Also, decreasing the triggering clock amplitude will reduce the shot noise, the amplitude reduction is limited by the minimum triggering voltage of the SRD.

To achieve high accuracy localization system, a high sampling rate is required. Real-time sampling rates are still limited for feasible application in our system. Three equivalent-time sampling alternatives were compared in this dissertation with respect to their Throughput, ADC analog bandwidth, system complexity, firmware

complexity, and sensitivity to clock imperfections; preference is given to the third method. Definitely, direct sampling is a needed but it is like a dream at this point, or very very expensive, other solutions like compressive sensing should be pursued. System integration adds significantly to the robustness of the system. MMIC chips have been developed to contain the whole system: Whole receivers and transmitters. The chips might have the antennas on-board. Digital back-end is integrated to one multi-layer board, it contains the ADC, FPGA, power, and USB logic. Integration increases the system reliability and decreases power consumption in large numbers, no loss in system accuracy/precision is noticed.

The performance of the system can be assessed for two cases: 1D and 3D only problems. 3D case will suffer the 1D problems in addition to problems like antenna phase center variation. jitter and AWGN are the main errors in 1D case. AWGN causes an accuracy problem, where there is a bias shift as we move the tag around the volume and the SNR of the received signal changes. Also, the total jitter in a sub-sampling system was shown to equal to the sum of the jitter in the transmitter and receiver in a mean square sense, and it can be measured by noting the spectrum of the received pulse.

In summary, the research in the future should include:

- Better sampling schemes like either direct sampling or compressive sampling.
- Use of high stability and low jitter clocks, like atomic clocks that their price has dropped significantly.
- Develop correlator receivers for better pulse reconstruction.

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Vita

Essam Elkhoully was born 1981 in Tanta, Egypt. Tanta is located 58 miles north of the capital Cairo and 81 miles southeast of Alexandria. He obtained his bachelor degree in 2003 at Tanta University and he was the top of his class through the five years of his engineering study. He obtained his master degree in 2009 at Tanta University.

He moved to the USA in 2009 to start his PhD studies with professor Aly Fathy. He worked for the antenna and microwave group until he graduated in 2014.

His parents Abdelkadir Elkhoully and Samia Khalid has six children Reham, Essam, Assmaa, Reem, Amr, and Sarah Elkhoully and six grandchildren. Essam is a husband to Dounia Baiya and a father to Lillian Elkhoully.