A High Frequency Wireless Power Transfer System for Electric Vehicle Charging Using Multi-layer Non-uniform Self-resonant Coil

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Abstract

Abstract—Wireless EV (Electric Vehicle) charging is an emerging technology with rapid development in the past decade. Compared to wired EV chargers, wireless power transfer (WPT) enables safe and unobtrusive charging for EVs.

This work proposes high frequency wireless charging using a self-resonant (SR) coil at several megahertz. A multi-layer self-resonant coil structure is proposed, allowing high quality factor coils to be fabricated from layers of inexpensive copper foil and dielectric film. Additionally, the self-resonant coil utilizes its interlayer capacitance for resonance, eliminating the external compensation capacitor and shrinking the overall volume of passive component to increase the power density. Comparing to other self-resonant coils in the literature, it exhibits the characteristics of achieving high quality factor and high inductance simultaneously.

Prototype coils with 200 mm radius are fabricated and tested, achieving quality factor over 450 at 3 MHz. The fabricated air-core coil structure is low-cost and lightweight, with 200 mm radius, 3 mm thickness and only 2 oz copper traces.

The power stages, including GaN (Gallium Nitride) transistor based inverter and SiC (Silicon Carbide) diode based rectifier, are designed with emphasis on reduction of PCB (Printed Circuit Board) layout parasitics. Experimental tests show 95.2% dc-dc efficiency with 6.6 kW power transferred across a 100 mm coil-to-coil distance. The power density is 52.5 kW/m^2, without need for any external compensation components. This work validates the concept of high frequency compact WPT system for EV.

Practical shielding design is proposed for the WPT system with self-resonant coils, considering the high frequency parallel resonance effect. Complete coil pads are fabricated and assembled, incorporating the ferrite cores, PTFE (Polytetrafluoroethylene) spacer, and aluminum plate. The system is validated with shielded SR coils, achieving 92.3% DC-DC efficiency and 7.1 kW/dm^3 volumetric power density. This work demonstrates the first 6.6-kW WPT system using compact self-resonant coils with practical shielding implementation.

The concept of proposed multi-layer self-resonant coil is extended to other possible structures. Different multi-layer self-resonant coil structures are compared and analyzed, giving design guidelines for their capabilities at different system operating frequencies.

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CHAPTER 1. INTRODUCTION

1.1 Introduction to Electric Vehicles

With the increasing public awareness of the environmental impact of greenhouse gas emissions, electric vehicles (EVs) have drawn worldwide attention as the potential successor to gasoline vehicles. While a full electric vehicle produces no emission from the tailpipe, a more comprehensive evaluation would include the global warming emissions associated with the electricity generation for charging an EV. Fig. 1 compares the EV global warming pollution emissions in the United States in 2015 and 2019. On the map, the miles per gallon (MPG) number represents the equivalent fuel economy rating of driving the average EV based on the same standard for gasoline vehicles in each U.S. electricity grid region. The calculation analyzed emissions from the whole process, including natural resources extracting and transportation, power plant emissions, transportation to filling stations, along with the combustion from the tailpipe.

As shown in Fig. 1(a), the U.S. average electric vehicle emission economy was 68 MPG in 2015. Although there exists variation between different grid regions mainly due to the mix of electricity sources, the lowest MPG area still reaches the equivalent of 35 MPG, which is 21% higher than the average 29 MPG of a new gasoline vehicle in that year [1].

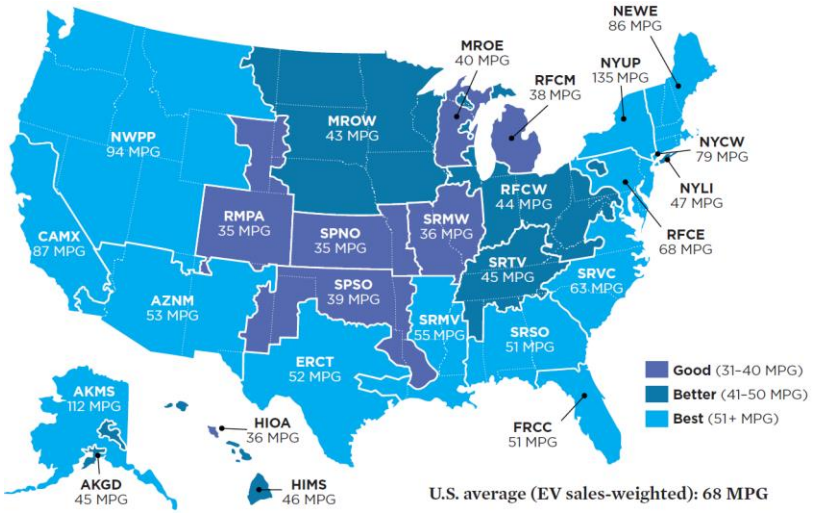
The advantage of driving an EV to avoid the impact of climate change is becoming more dominant each year. By the year 2019, with the fast penetration of renewable energy like hydropower and wind to replace coal and natural gas in the electric grid and improved efficiency of EVs, the average MPG jumps to 88, a 30% increase in only 4 years. California, whose environmental regulations are often set as the standard for U.S.

automakers, reaches 122 MPG with 40% improvement [2]. Note that from 2015 to 2019, the average new gasoline vehicle MPG is only slightly increased from 29 to 31, excluding trucks, as reported by Environmental Protection Agency (EPA). EVs still have great potential to dramatically cut global warming emissions with cleaner electricity grid and more advanced EV manufacturing.

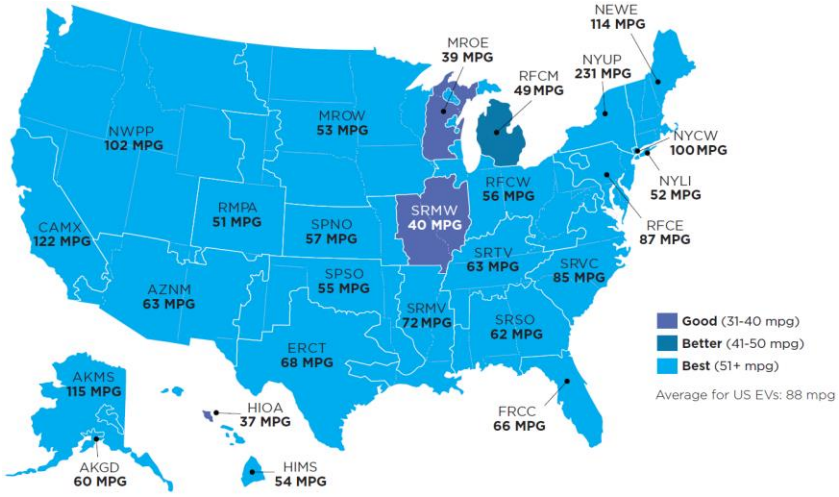
For the purposes of both environmental protection and carbon emission reduction, governments around the world have announced national or regional commitments to improve their EV penetration in the transportation sector, whose policies are strong drivers of the EV market in early growth. Fig. 2 gives the estimated EV sales share in some of the major automobile markets based on the different current and future government ambitions for the EV market. There is no doubt that basically all major markets will embrace the EV rapidly in the next 10-20 years [3]. The rest of world is approximated as following the average of the leading markets with a 10-15 year delay.

Morgan Stanley gives the global EV market size in detailed numbers as shown in Fig. 3. In 2017, sales of new electric cars reached a record volume of 1 million units [4]. From the year 2015 to 2025, the EV unit sales are anticipated to have a 37% compound annual growth rate (CAGR). By the year 2050, the total number of EVs will reach one billion, globally.

Infrastructure, like charging stations are also critical to support sustainable EV market growth. For example, the 100 most populous metropolitan areas in U.S. are studied in Fig. 4 to evaluate the gap between the existing public and workplace charge stations in 2017 and the expected demand for new charging infrastructure in 2025 to charge more than 3 million EVs at that time based on the market growth rate, government policies, and



(a)



(b)

Fig. 1. Equivalent EV global warming pollution ratings in the United States (a) 2015 [1], (b) 2019 [2]

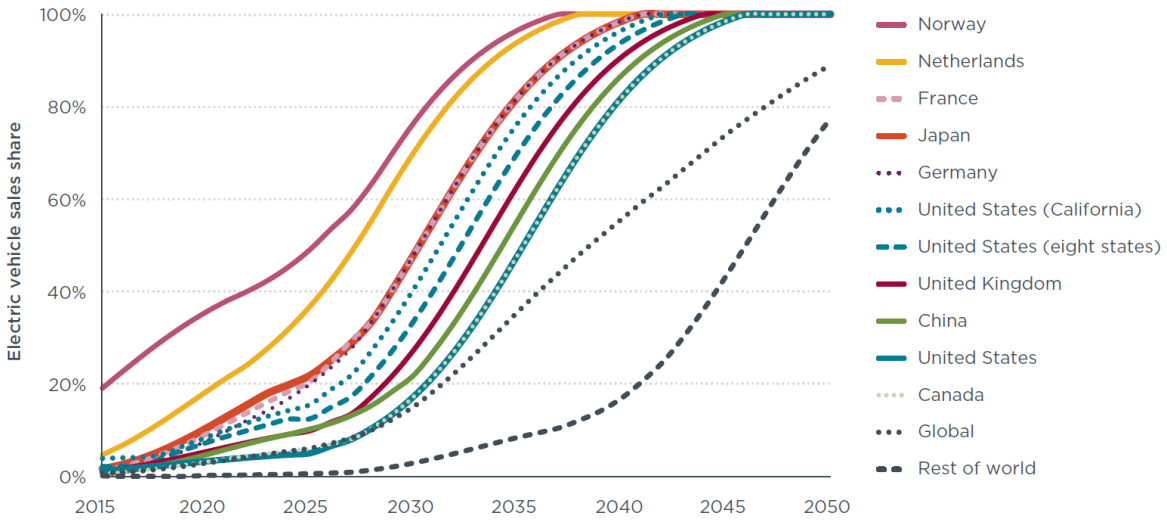


Fig. 2. Share of EV in new passenger vehicle sales [3]

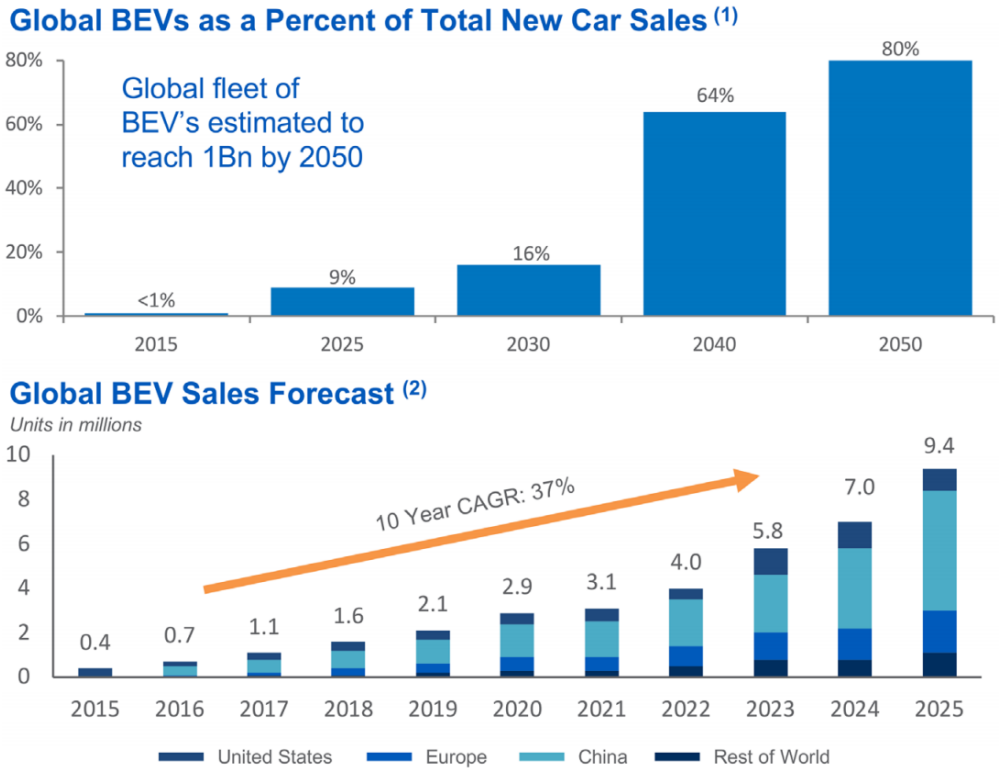


Fig. 3. Global EV market review and forecast [4]

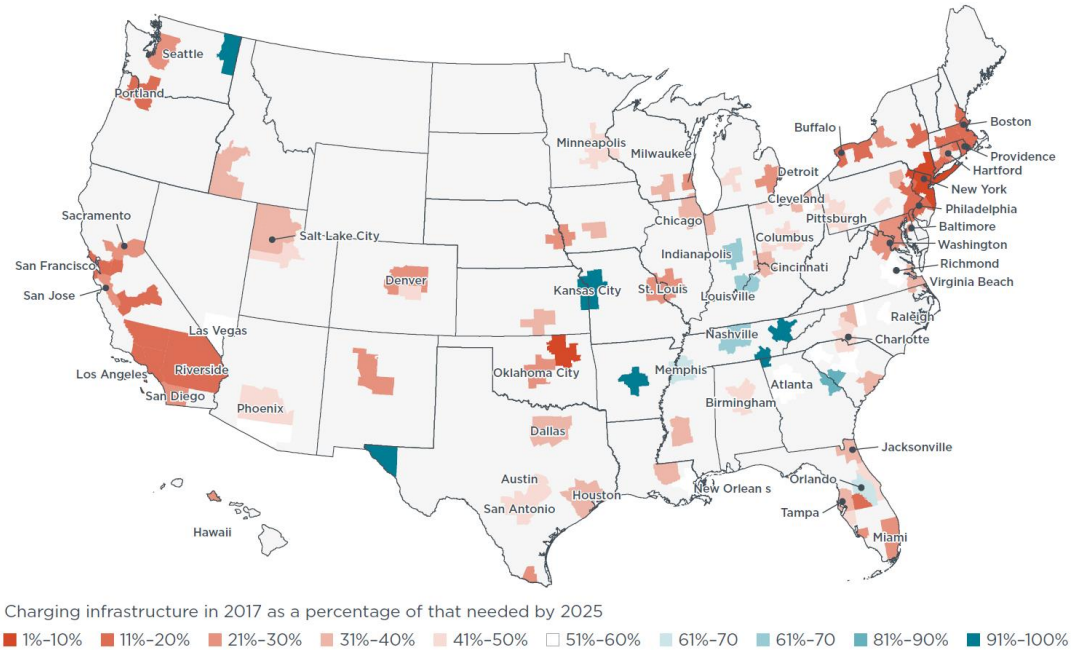


Fig. 4. EV charging infrastructure in 2017 as a percentage of that needed by 2025 in U.S. by metropolitan area [5]

and emerging charging behavior patterns [5]. The red shaded area means that there is more than 50% of new infrastructure shortage, which happens in 88 of 100 total surveyed areas. Considering the continually expanding EV market in the future, much more charging infrastructure is demanded for rapid growth, especially in California and the Northeast where high EV uptake is expected in the next couple of years. Worldwide, McKinsey reported that in the next 10 years, $50 billion investment will be needed to install more than 40 million chargers in U.S., China, and EU to fill that gap, as shown in Fig. 5 [6].

Categorized by the power rating, there are three different levels of charging based on Society of Automotive Engineers (SAE) International as shown in Fig. 6 and summarized in TABLE I [7]-[8]. Level 1 uses the standard 120 VAC household wall plug charging. Level 2 increases the charging voltage to 200-240 VAC and can be installed either at home or in public parking spots with similar wiring for an electric clothes dryer. The power rating are 1.2-1.8 kW and 3.3-22 kW for Level 1 and Level 2, respectively. The average cost of a Level 2 charger used at home is less than $1000. For workplace or public, the infrastructure price is increased to $3000 to $5000 [6]. Many current EVs on the market use Level 2 charging, including the Chevrolet Volt, a Plug-in Hybrid vehicle (PHEV), at 3.3 kW and the Nissan Leaf at 6.6 kW.

To further increase the charging speed to less than 20-30 mins to compete with gasoline vehicles, Level 3 utilizes DC fast charging at 400-1000 VDC with more than 50 kW charging power. Accordingly, DC fast charging station requires proper planning and installation by the local utility company considering the expensive equipment and extreme power requirement. Depending on different power ratings, the price of a DC fast

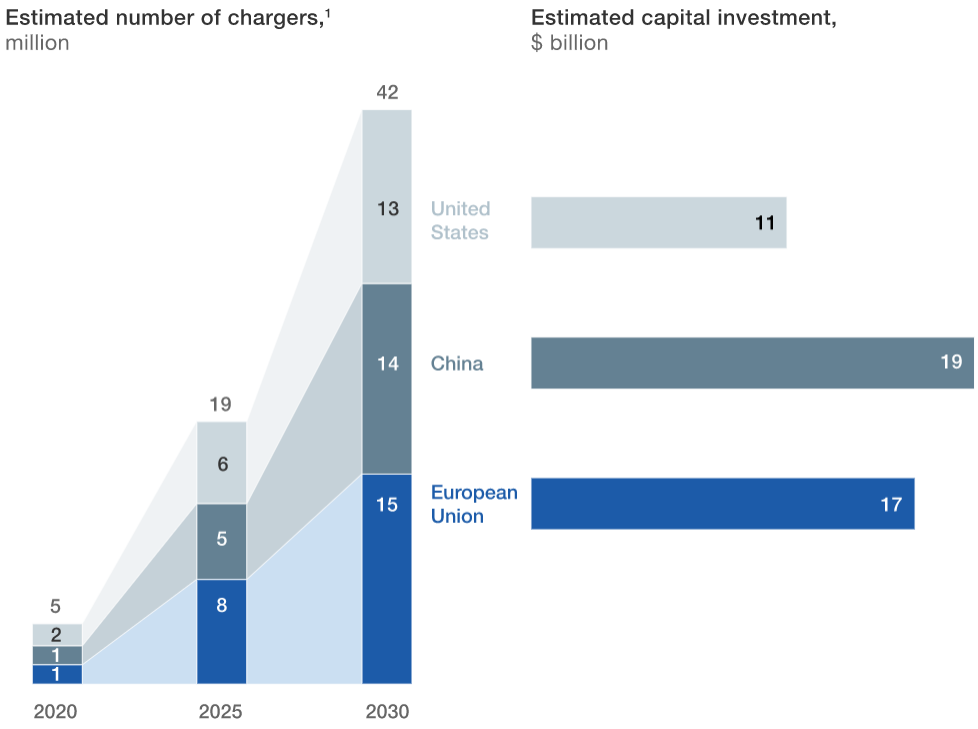
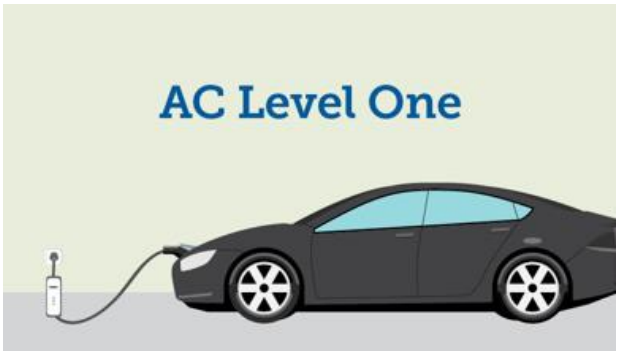


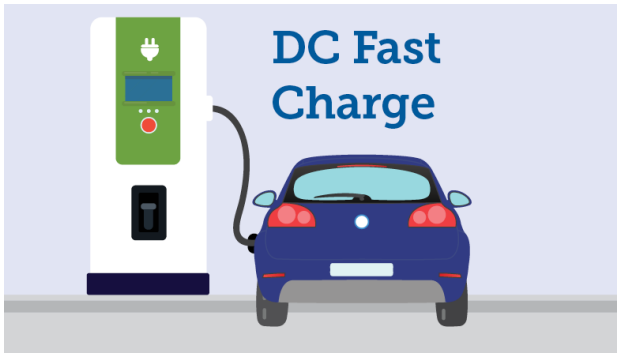
Fig. 5. Charging infrastructure 2020-2030 in U.S., China, and EU [6]



(a)



(b)



(c)

Fig. 6. SAE standard on different EV charging ratings (a) level 1 (b) level 2 (c) DC fast charging [8]

TABLE I. EV charging levels by SAE International

@SAE	Voltage	Power	Miles per hour	Setting
Level 1	120 V AC	1.2-1.8 kW	3-4 miles	Simple household AC plug charger
Level 2	200-240 V AC	3.3-22 kW	10-70 miles	At home or public parking
DC fast	400-1000 V DC	50 kW or more	150-1000 miles	Expensive equipment installed by local utility

charger starts at $25,000 and can be higher than $200,000 for larger capacity [6]. A typical public EV charging station is illustrated in Fig. 7 for Level 2 and DC fast charging [9].

1.2 Wired EV Charging to Wireless EV Charging

In contrast to conventional wired EV chargers, wireless power transfer (WPT) allows EV battery charging without a physical, cable connection in a safe, robust, and unobtrusive way. As shown in Fig. 8 and Fig. 9, the wireless charging coils are buried underground, allowing the charging station footprint to be reduced. In addition, charging plugs, which can be easily damaged or cause electric safety concern without supervision, are no longer required [13]. By dynamically charging the EV on the highway while running, the battery size on EV can be largely reduced.

Based on the report from Grand Review Research, the entire wireless charging market reached $1.87 billion in 2014 globally. Wireless charging can be applied in different areas including automotive, consumer, industrial, healthcare, defense and others as shown in Fig. 10. Among all the sectors, wireless EV is relatively new and still in its early R&D phase with rapid growth. The global wireless EV charging market is projected to reach a market size of over $234 million by 2027 from an estimated $16 million in 2020, growing at about 47% rate annually [14]-[15].

In October 2020, SAE published its first standard J2954 on WPT for EVs, allowing charging power up to 11 kW over a 250 mm air gap with up to 94% efficiency as listed in TABLE II [16]. The standard also outlines the parking assistance for EV that makes autonomous parking and charging available. Together with J2954, J2847/6 is published recommending the communication protocols between EVs and charging stations.

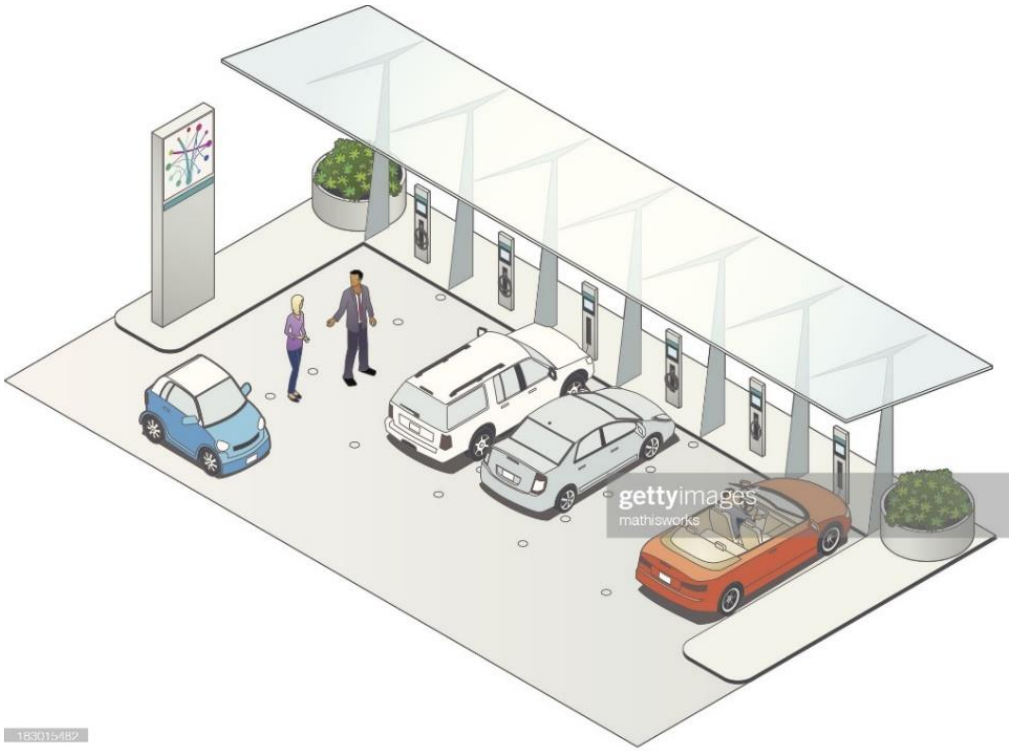


Fig. 7. Typical public EV charging station for level 2 or DC fast charging [9]



Fig. 8. Wired EV charging infrastructures [10]-[12]



Fig. 9. Wireless EV charging infrastructures [4]

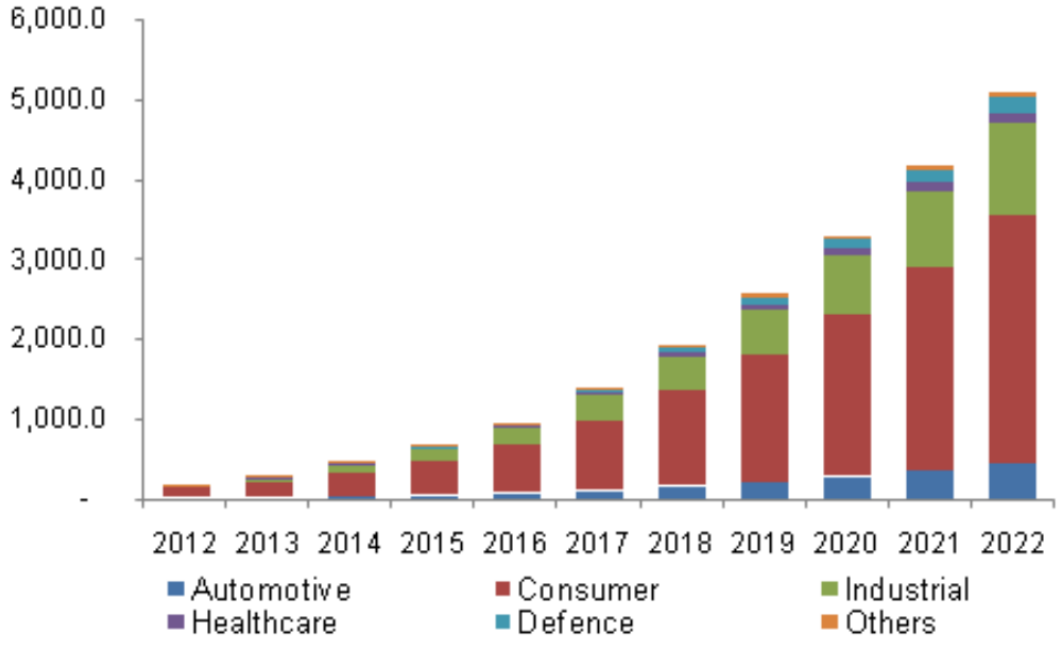


Fig. 10. U.S. wireless charging market by application 2012-2022 [15]

TABLE II. Wireless EV charging standard by SAE International [16]

Common frequency band	WPT1	WPT2	WPT3	Minimum efficiency
85 kHz (81.39-90 kHz)	3.7 kW	7.7 kW	11 kW	85%

A typical structure of WPT system for EV is shown in Fig. 11. From the transmitter pad buried underground, power is transferred wirelessly to the receiver pad, which is installed beneath the chassis of EV. High leakage flux exists spatially due to the large air gap ranging from 100 mm to 250 mm approximately, which is the major difference comparing with conventional closely-coupled high frequency transformer in wired EV charger. Compensation networks are normally applied together with the charging pads to cancel out the reactive power and improve the power transfer capability in this loosely-coupled circuit. To guarantee high efficiency power transfer, a high frequency inverter is required between AC utility line and transmitter pad, and a rectifier is needed on the car to rectify the high frequency AC voltage received from the receiver pad and charge the battery. Communications between the transmitter and the receiver are usually required for power transfer optimization and pad misalignment control.

1.3 Wireless EV Charging Industrial Practices

The leading companies and research groups for wireless EV charging include WiTricity, Halo, Momentum, HEVO, PLUGLESS, and KAIST, with their products' specifications summarized in TABLE III. In 2007, a group of scientists in MIT successfully delivered 60 W at 40% efficiency over a 2 m distance between coupled coils of 30 cm radius. They co-founded WiTricity later on as a spin-off company from MIT. WiTricity has been working closely with major automakers like BMW and Hyundai by licensing its intellectual property and has demonstrated a series of wireless charging prototypes for next generation vehicles. In 2018, BMW introduced the world's first EV sedan that is factory equipped with wireless charger using WiTricity's techniques, 530e iPerformance.

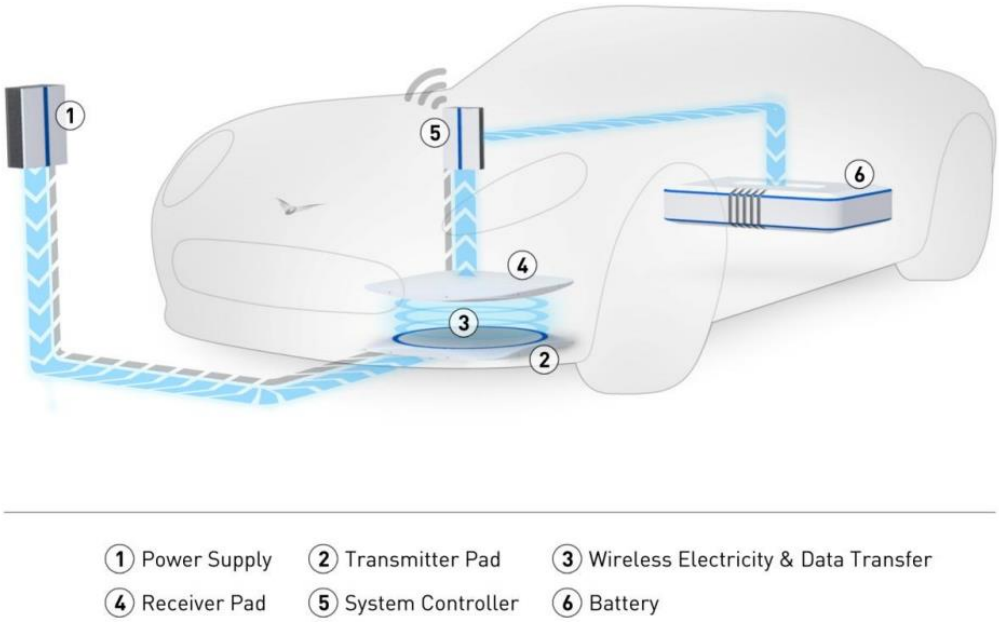


Fig. 11. A typical WPT system on EV [17]

TABLE III. Industrial wireless EV charger specifications [18]-[24]

Company	Frequency	Airgap	Power rating	Efficiency
WiTricity	145 kHz	180 mm	3.6-11 kW	90-93%
Momentum	NA	610 mm	50-200 kW	NA
HEVO	85 kHz	305 mm	1-10 kW	>85%
PLUGLESS	20 kHz	152 mm	3.3-7.2 kW	89%
WiPowerOne	85 kHz	200 mm	27 kW	80%

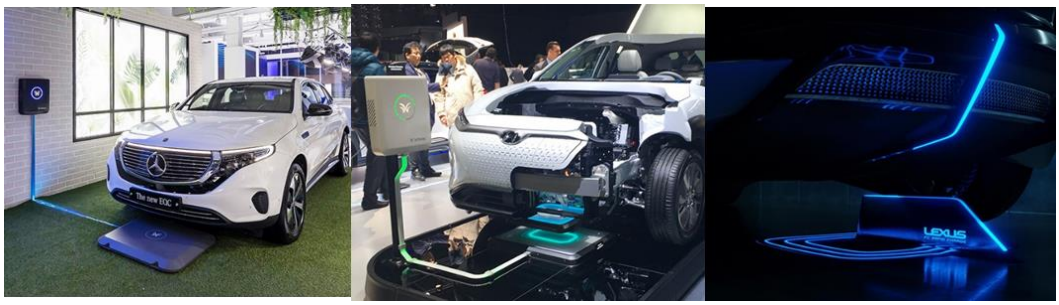
Qualcomm's Halo has been collaborating closely with the University of Auckland and has developed a number of coil pad geometries suitable for wireless EVs, including the patent for the double D coil pad. In 2019, it was acquired by WiTricity with its over 1500 patents or patent applications [18].

Momentum is a Philadelphia based company focusing on higher-power vehicles in applications like public transit, delivery vans, and auto fleets. It is currently working with Link Transit for a 5-year contract in Washington state to provide wireless charging systems for Link Transit's growing fleet of electric buses [19]. Recently, WiTricity filed a patent infringement suit against Momentum in December 2020 to cut the sales of any unlicensed products in Momentum [20].

HEVO and PLUGLESS focus more on supplying finished goods directly to customers. HEVO is a startup in Brooklyn, New York, and its first contract from NYU Office of Sustainability allows the deployment of manhole-like wireless EV charger in New York city in 2014 [21]. PLUGLESS provides wireless charger with 3.6-7.2 kW power rating and allows customers to directly install the charger on their vehicles. The supported models include Telsa S, BMW I3, and Nissan LEAF [22].

Diagrams of wireless chargers from different companies are compared in Fig. 12.

Compared to the stationary WPT practice mentioned above, dynamic WPT allows EVs to charge continuously during running. The research team from Korea's Advanced Institute for Science and Technology (KAIST) has been working on the demonstration project of dynamic WPT bus for over a decade. In 2018, a spin-off company from KAIST, WiPowerOne, was founded specializing in manufacturing wireless charging infrastructures. Fig. 13 shows the electrical bus serving as the shuttle on KAIST campus.



(a)



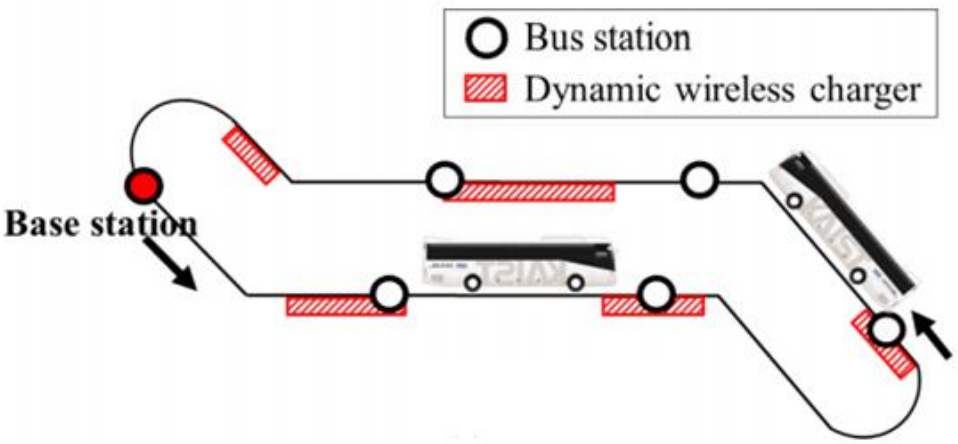
(b)





(c) (d)

Fig. 12. Commercially available wireless chargers (a) prototypes from WiTricity (b) electric bus from Momentum (c) Manhole-like charger from HEVO (d) customized charger from PLUGLESS [18]-[22]



(a)



(b)

Fig. 13. WiPowerOne dynamic wireless charging electrical bus (a) dynamic WPT scheme (b) power track under construction and in operation [23]

Still, the high cost of infrastructure and complicated installation is one of main obstacles for the development of dynamic WPT [23].

1.4 Summary on Current Wireless EV Charger Limitations

In the practical application of wireless EV charging, there is usually 100-250 mm airgap between the transmitter pad underground and the receiver pad beneath the vehicle chassis. This unique requirement makes WPT system efficiency relatively low compared to the wired EV chargers with similar power ratings. The state-of-the-art EV WPT charger from WiTricity gives only 90-93% efficiency, which brings challenge in both energy costs and thermal management design of the system. For a better power transfer with higher efficiency, the couplers size is often larger than 500 mm in diameter, inevitably increasing the material cost and total weight. Fig. 14 and TABLE IV gives the specifications of WiTricity WiT-3300 wireless EV charger with 3.3 kW output over 180 mm airgap. The diameter of both transmitter pad and receiver pad is 500 mm, weighting 12.5 kg each.

Accordingly, the construction footprint is large, and the installation cost is high. For instance, PLUGLESS offers 3.6 kW and 7.2 kW wireless charging systems for $5,999 and $12,999, respectively [22]. The large initial cost becomes one of the main obstacles for the deployment of wireless EV charging [26].

Considering all the factors above, high efficiency, high power density, lightweight WPT systems with low cost are imperative for increased adoption of wireless EV charging.

1.5 Dissertation Outline

The dissertation is organized as follows. Chapter 2 provides the detailed review on the state-of-the-art WPT system design, which leads to the motivations for high frequency coil



Fig. 14. WiTricity WiT-3300 wireless EV charger [25]

TABLE IV. WiTricity WiT-3300 specifications [25]

Specs	**Value**
Operating frequency	145 kHz
Output power	0.3-3.3 kW
Transmission distance	180 mm
Transmitter pad	500 mm x 500 mm x 37.5 mm, 12.5 kg
Receiver pad	500 mm x 500 mm x 37.5 mm, 12.5 kg
Inverter assembly	220 mm x 330 mm x 130 mm, 4.2 kg
Receiver assembly	200 mm x 280 mm x 7 mm, 3.6 kg

structure in WPT system for EVs. In Chapter 3, the attempted high frequency coil designs in the literature utilizing self-resonant coil are discussed in detail, and a multi-layer non-uniform SR coil with high quality factor and high inductance characteristics is proposed. Chapter 4 presents the inductance and capacitance modeling process for the proposed coil, demonstrating its design process through geometry optimization. Chapter 5 gives the system-level optimization, incorporating results of the optimized coil design. Chapter 6 presents the fabrication process and experimental measurements of a prototype system. Chapter 7 presents the shielding design for the proposed coil. Chapter 8 discusses the generalized multi-layer coil with different structures. Chapter 9 concludes the dissertation.

CHAPTER 2. REVIEW ON STATE-OF-THE-ART WPT SYSTEMS AND MOTIVATIONS FOR HIGH FREQUENCY WPT SYSTEM

With the unique requirement of long-distance power transfer at several hundred millimeters, it is challenging to have compact wireless EV charger design with high efficiency. To better facilitate the understanding of WPT systems and to expose the design challenges, a thorough literature review is conducted for state-of-the-art WPT systems suitable for EV charger application.

2.1 Introduction on Wireless Charging Techniques: IPT vs CPT

2.1.1 Inductive Power Transfer

Based on the different coupling mechanism between transmitter side and receiver side of the WPT system, there are two types of WPT techniques as candidates for high power wireless EV applications: Inductive Power Transfer (IPT) and Capacitive Power Transfer (CPT) [27]-[30]. As shown in Fig. 15, IPT is based on inductive coupling of a magnetic field between two coils. Controlled by a varying current source in the primary side coil, a predominantly magnetic varying field is generated between the coils, and the distance is generally much smaller than a wavelength. Such near-field magnetic coupling induces voltage on the secondary side coil, and energy is transmitted through the large air gap between two coils.

Since the successful demonstration of 60 W power delivery over 2 m distance by MIT scientists in 2007 [28], the IPT based EV has developed rapidly in the past 14 years. Some of the typical IPT systems for EV are illustrated in Fig. 16 [32]-[35]. For most of the current coil designs, Litz wire is used extensively instead of the conventional solid AWG wire for

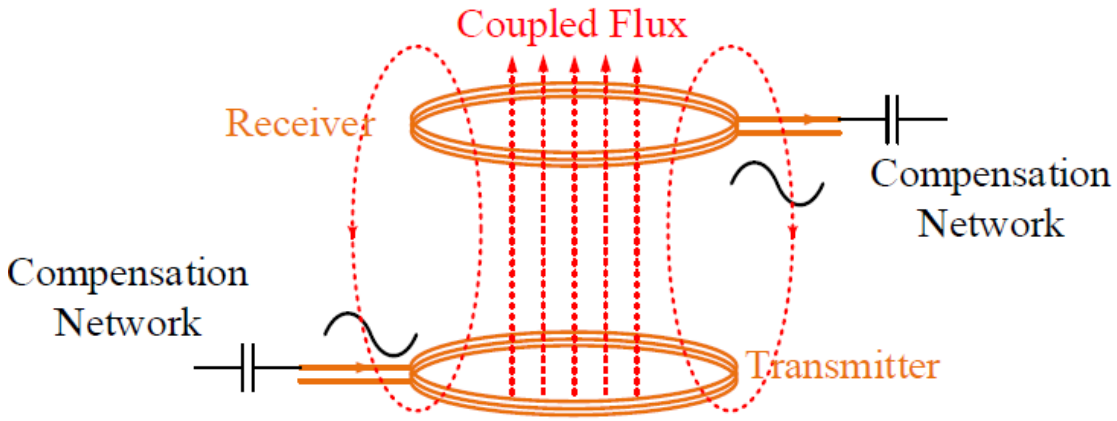
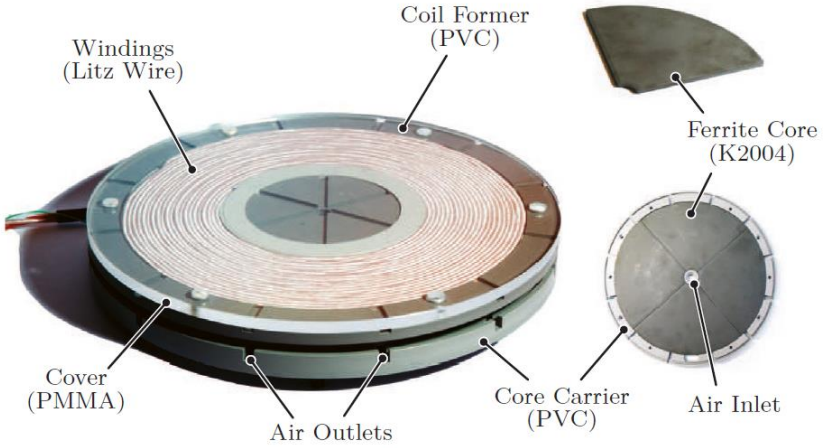
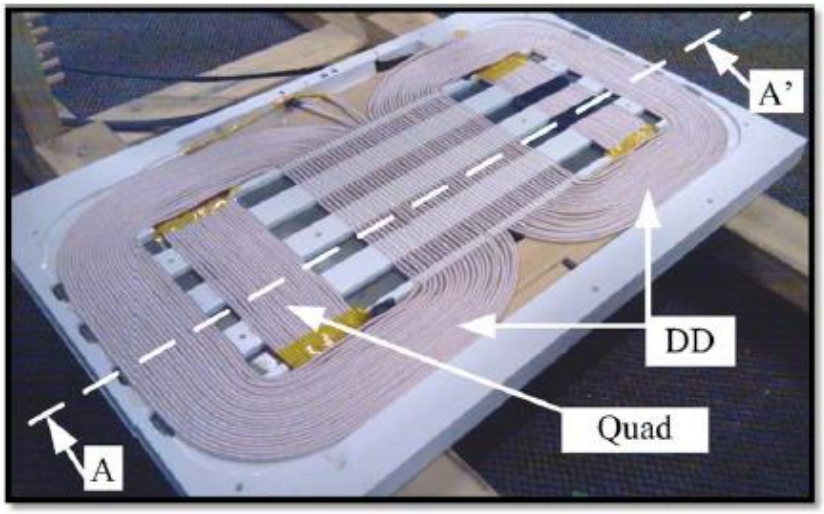


Fig. 15. Inductive coupling [31]



(a) 210x210 mm^2, 52 mm, 5 kW, 100 kHz, 96.5% from ETH [32]



(b) 540x800 mm^2, 200 mm, 2 kW, 20 kHz, NA from University of Auckland [33]

Fig. 16. Some of the typical IPT pad structure (pad size, power transfer distance, power rating, operating frequency, and DC-DC efficiency)

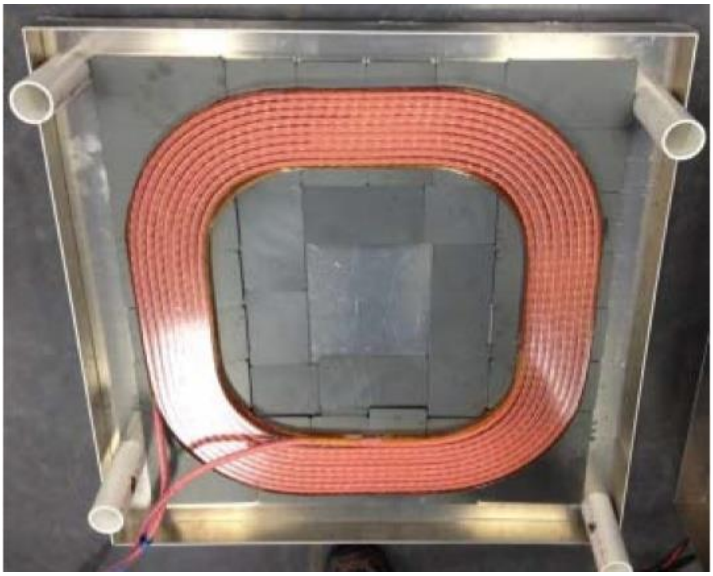


Fig. 16. continued (c) 640x640 mm^2, 162 mm, 12 kW, 23.5 kHz, 95.1% from ORNL [34]

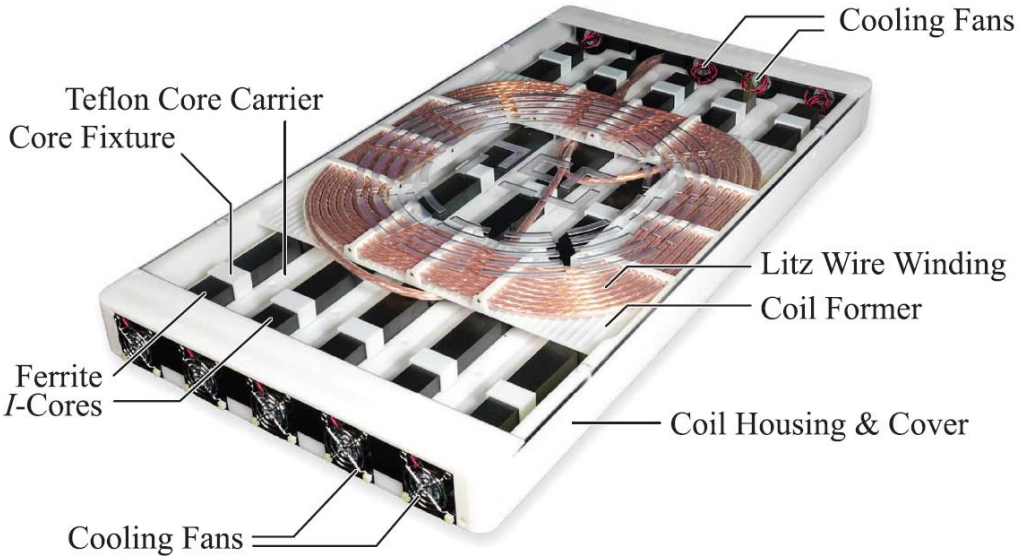


Fig. 16. continued (d) 410x760 mm^2, 160 mm, 50 kW, 85 kHz, 95.8% from ETH [35]

its capability of reducing high frequency eddy current loss. Different coil pad structures have been explored to provide the largest coupling possible between two couplers. Usually, magnetic cores like ferrite plates or bars are applied to better channel the flux around the coil and improve the inductance and coupling.

By paralleling four high power couplers, a 1 MW IPT system for high-speed trains was reported in [36]. The measured efficiency is 82.7% over 50 mm airgap when delivering 827 kW. A very high power density design at 200 kW/m^2 is presented in [37] with a three-phase resonant network with extensive utilization of Litz wire and ferrite.

Despite different design approaches and power ratings, the common structure of the coil pad for IPT requires Litz wire windings and ferrite cores. With higher power and larger airgap, larger coil pad with more windings and cores are demanded. The operating frequency is often limited below several hundred kHz to avoid excessive ferrite and winding losses.

2.1.2 Capacitive Power Transfer

The second technique is Capacitive Power Transfer (CPT), where energy is delivered through coupled metal plates instead of coupled inductors. An electrically coupled pair of metal plates are required, and each plate-pair will form a capacitor. When excited by an ac source, energy is transmitted through these contactless plates.

Compared with IPT, CPT features favorable characteristics including lightweight and cost-effective design. It does not require expensive high frequency Litz wires or heavy magnetic cores, which aids the high frequency design to reduce the weight of passive components.

However, CPT suffers from two major issues: low coupling capacitance and high

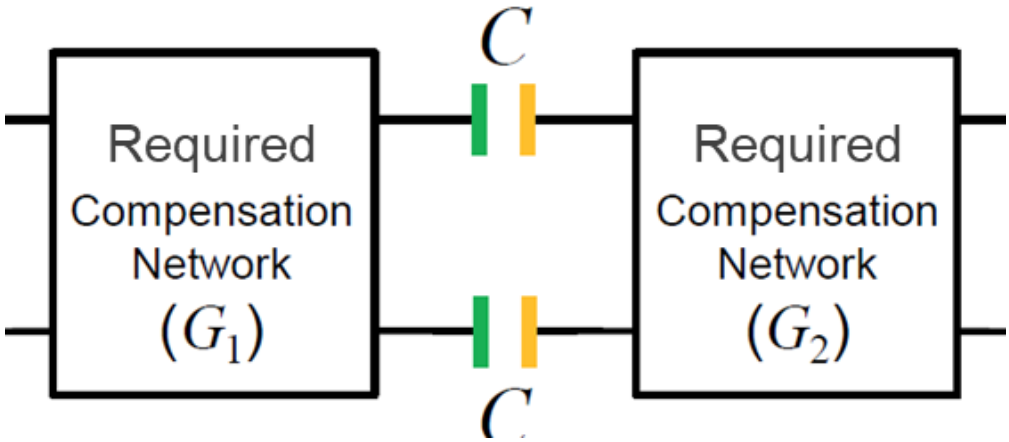
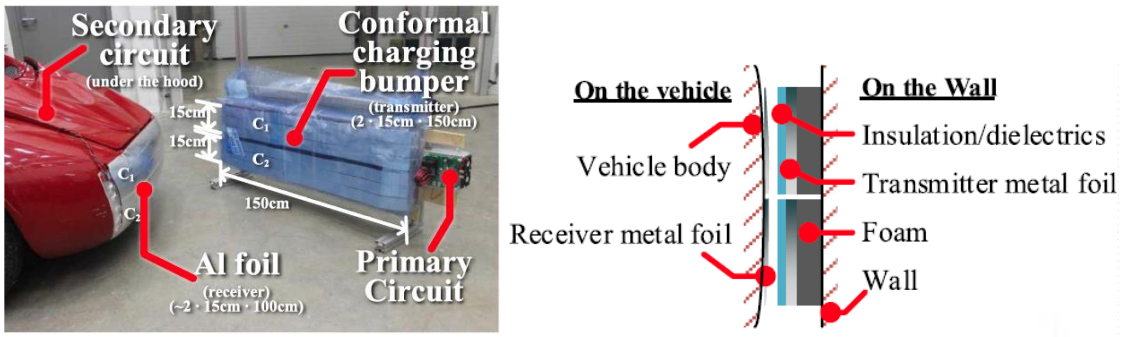


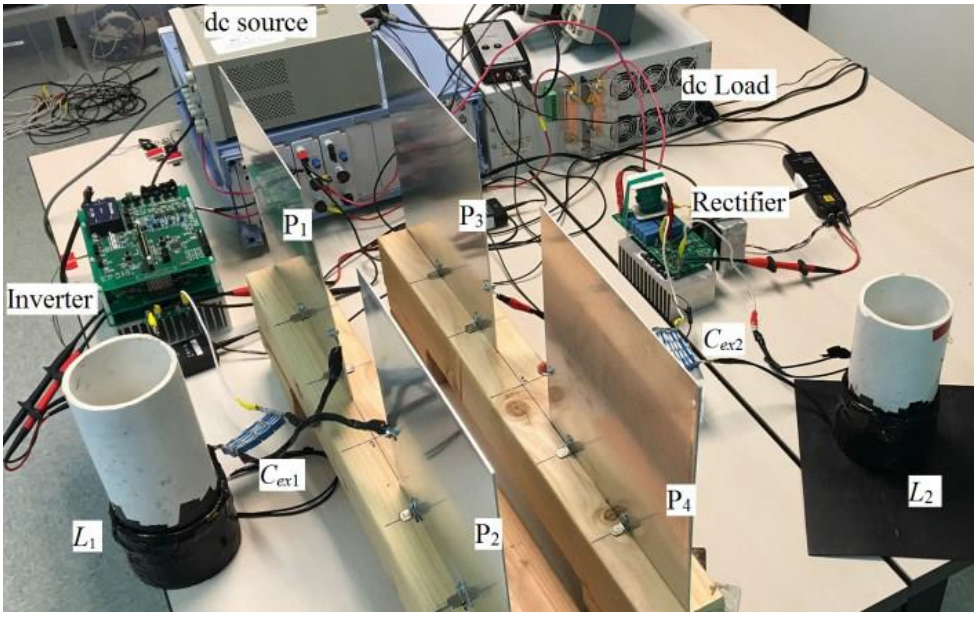
Fig. 17. Capacitive coupling [41]

fringing field. Capacitive coupling requires a relatively large coupling area to achieve large coupling capacitance, imposing a design challenge on high power density. For high power EV applications with a large air gap, the transmission efficiency is low due to the low coupling capacitance between the paralleled plates [38]-[42]. Fig. 18 gives some state-of-the-art CPT system designs and their generated capacitance between plates is within the range of dozens of pF only. To compensate, MHz operating frequency is required to reduce the impedance in the power flow of the circuit, which directly imposes a design challenge for the high power, high frequency converters. In addition, relatively large-valued inductance is required at μH range at MHz frequency for resonance, leaving a design challenge for high value, high quality factor inductors at high frequency. Considering the factors above, the power density of CPT systems is not comparable to IPT systems. Work in [45] provides a concept to integrate IPT and CPT systems, but power density is still not comparable to IPT systems. By operating at 13.56 MHz, [46] further increases the power density of the capacitive link, but two large, specially-designed toroidal interleaved-foil coupled inductor with 200 mm diameter are used to reduce the magnetic loss in the compensation network, which will cut the claimed power density by half if the volume of these inductors is included.

The high fringing field at the edge of coupled metal plate pairs is another concern for CPT because of electric field exposure limits on the human body [47]-[48]. As shown in Fig. 19 for a 150 W, 1.5 MHz CPT system, there exists coupling capacitance between the four Aluminum plates, and they can be simplified as a two-port model, with self-capacitance C_{in1} and C_{in2}, and equivalent mutual capacitance C_M. The derived self-capacitance is 129.8 pF with only 2.8 pF (2.16%) coupling coefficient. To have a high



(a) 1500x150x2 mm^2, 0.1 mm, 1 kW, 530 kHz, 88% from University of Wisconsin-Milwaukee [43]



(b) 300x300x2 mm^2, 180 mm, 150 W, 1.5 MHz, 70% from SDSU [44]

Fig. 18. Some of the typical CPT pad structure (pad size, power transfer distance, power rating, operating frequency, and DC-DC efficiency)

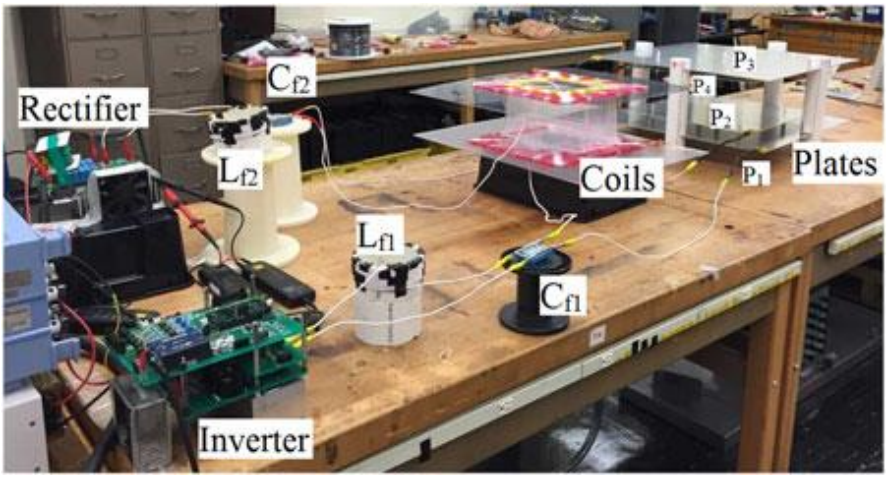


Fig. 18. continued (c) 610x610+300x300 mm^2, 160 mm, 2.84 kW, 1 MHz, 94.5% from SDSU [45]

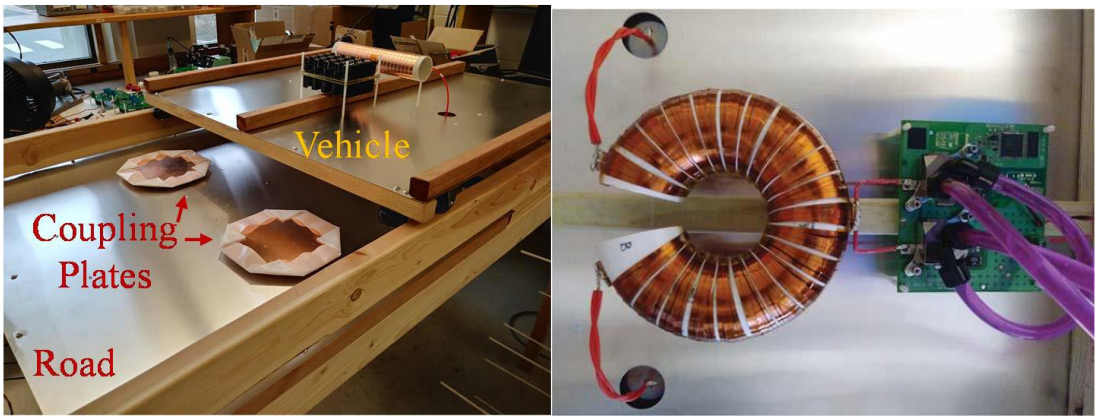
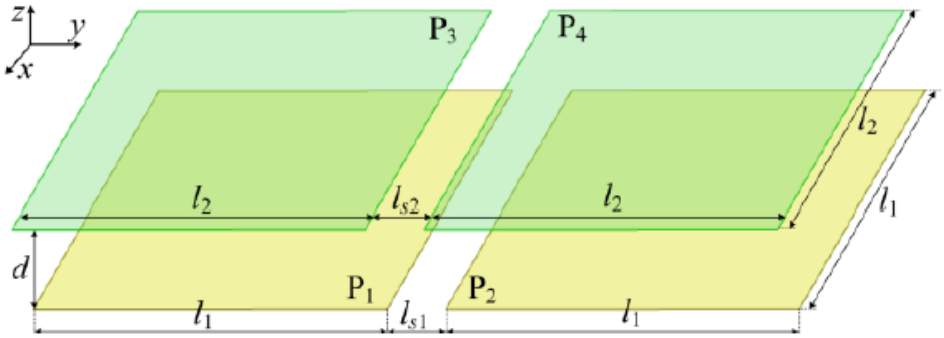
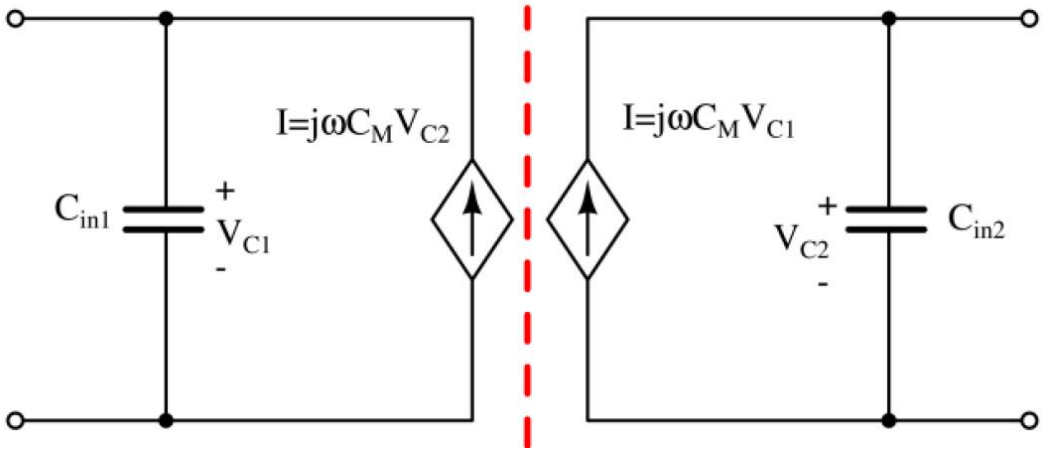


Fig. 18. continued (d) 220x220x2 mm^2, 120 mm, 3.75 kW, 13.56 MHz, 93% from Cornell [46]



(a)



(b)

Fig. 19. A 150 W, 1.5 MHz CPT system (a) structure of capacitive coupler (b) equivalent two-port model [44]

power transfer to the secondary side, the plate voltages are resonated into several kilovolt range. With 3 kV/mm air breakdown voltage, there is no concern for arcing if the distance between plates is large enough.

However, due to the small coupling and high fringing on the edge of plates with high voltage, there is high electric field not just between the main coupled plates (P_1 and P_3, P_2 and P_4) but also between the leakage coupled plates (P_1 and P_2, P_3 and P_4), which may cause EMI concern. The maximum field strength near the plate is 10.6 kV/m, which is much higher than the 550 V/m IEEE C95.1 electric field strength safety standard at 1.5 MHz. A 350 mm safety clearance is needed for this 150 W CPT system as shown in Fig. 20. With potential higher power transfer at higher frequency for EV application, leakage electric field around the CPT plates will be even higher than the safety standard.

2.1.3 Summary

Fig. 21 summarizes power rating and transfer distance for different IPT and CPT systems for various applications including EV. The empirical relationship within this figure indicates the general trend for IPT and CPT application domains. For most of the IPT systems, the power and transfer distance could be large which is suitable for EV applications. On the contrary, CPT is generally applicable for small-gap regions. Both IPT and CPT can achieve >90% efficiency in their own application areas. There are some research groups focusing on wireless EV charging over large airgap using CPT technique recently, and their designs will be plotted and compared with other state-of-the-art IPT systems in Fig. 22.

Fig. 22 plots the state-of-the-art WPT systems for EV charger applications, with the power ranging from serval hundred watts to kilowatts and the switching frequency ranging

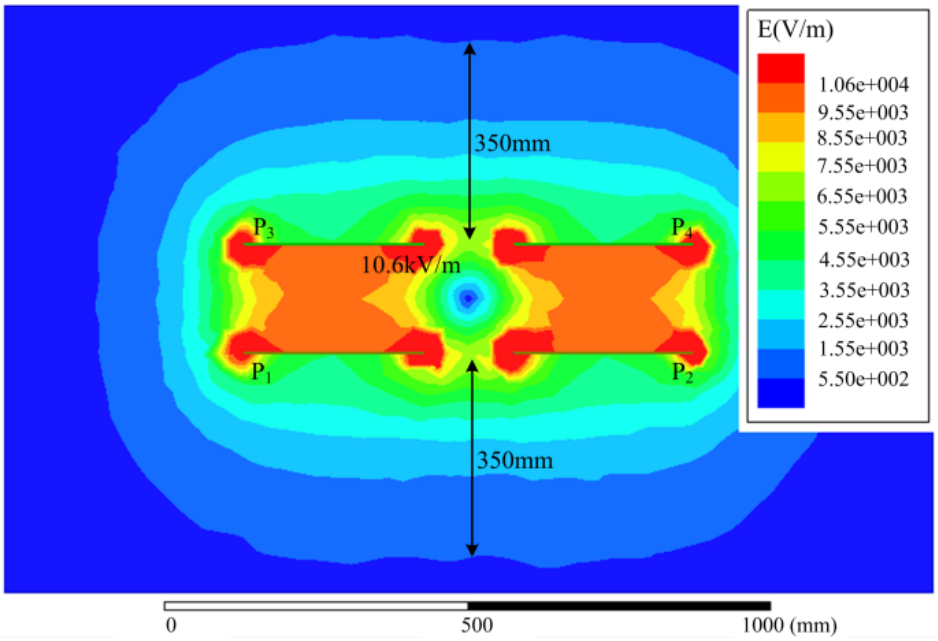


Fig. 20. Electric fields emission around the capacitive coupler for a 150 W, 1.5 MHz CPT system [44]

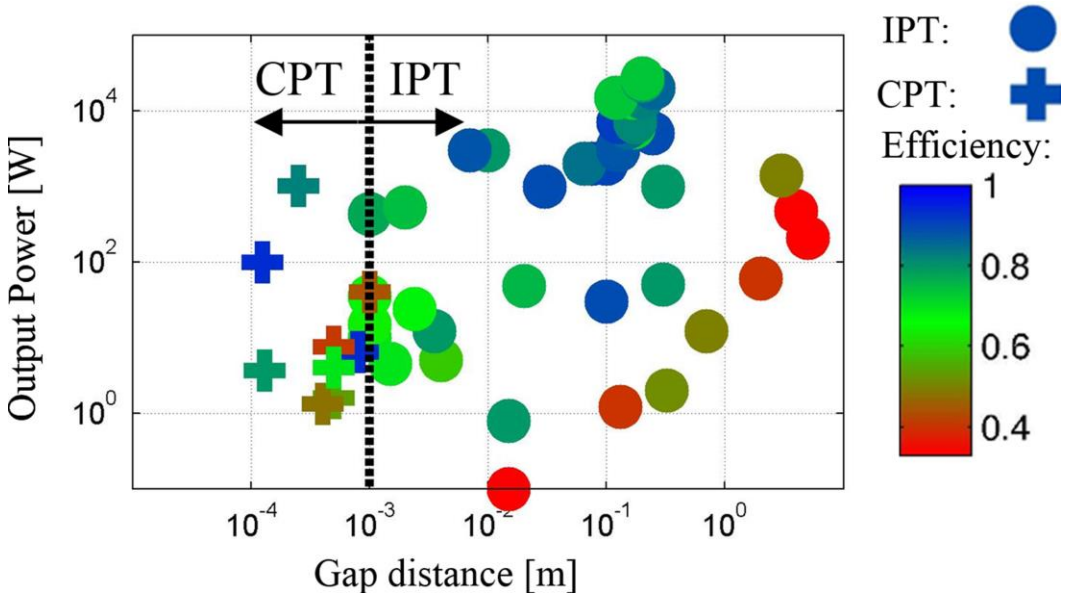


Fig. 21. Output power versus airgap for IPT and CPT systems [41]

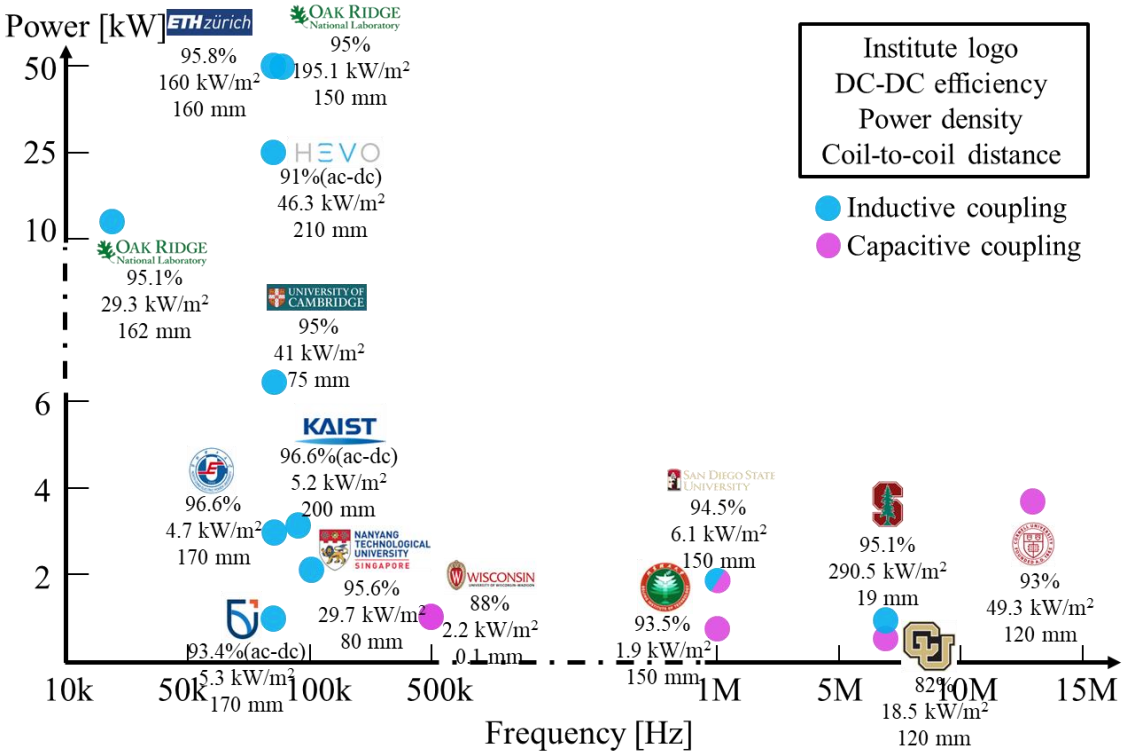


Fig. 22. State-of-the-art WPT systems for EV charging

from tens of kilohertz to several megahertz. The color of each dot represents the WPT technique applied. Critical performance specifications are also labeled, including system DC-DC efficiency, coil power density and power transfer distance. Inductive power transfer systems have power rating up to tens of kilowatts, but most use frequencies below 100 kHz [49]-[56]. Since there is no high frequency core loss and winding loss, capacitive power transfer systems tend to work in higher frequency range in order to increase coupling between the metal plates but have limited power density and power rating.

The main characteristics of IPT and CPT are summarized in TABLE V.

In summary, IPT is a relatively mature technology for WPT systems for EV chargers with air gap up to dozens of centimeters. However, it should be noted that the efficiency and power density of IPT systems are still limited by low coupling between the transmitter coil and receiver coil due to the large air gap. This issue is currently addressed by using more Litz wire windings or heavier magnetic cores and having larger coils up to 400 mm-600 mm in radius to gain larger inductance value and higher coupling coefficient. However, the efficiency and power density are often sacrificed, and overall manufacturing cost is inevitably increased. Moreover, the fringing magnetic field around the coil should be controlled with the safety margin for human body, and it is strongly dependent on the coil design in terms of coil size, current rating, operating frequency.

Based on the reviewed contents above, although IPT is more dominantly applied for EV applications, there are still many design challenges for any high efficiency, high power density, low cost and robust WPT system. The design challenges for IPT system are detailed in the following section.

TABLE V. IPT and CPT techniques comparison

Technique	Advantage	Disadvantage
Inductive coupling	1. high power 2. large transfer distance	1. cost of windings and cores 2. heavy magnetic cores 3. frequency limitation due to winding and magnetic losses
Capacitive coupling	1. lightweight 2. low-cost metal plates	1. low capacitance coupling 2. low power density 3. high frequency compensation design 4. safety concern for high fringing electric field

2.2 Design Challenges of Current IPT System for EV and Motivations for High Frequency Coil Design

2.2.1 Efficiency limitation by coupling and coil quality factor

By the application requirement of wireless EV, the air gap between transmitter coil and receiver coil ranges from 100 mm to 250 mm, leading to the coupling coefficient lower than 0.3 in most cases. The impact of the coupling coefficient on system performance is analyzed theoretically with the system circuit model to reveal the key factors determining system efficiency in this section.

As shown in the Fig. 23, different from the conventional isolated DC-DC converters for wired EV charger, there is now a large air gap for the high frequency transformer. Since the gap is usually several hundred millimeters for EV application, magnetic coupling coefficient k is largely reduced, resulting in reduced efficiency due to more reactive power in the reduced magnetizing inductance. For isolated DC-DC converters, load-dependent behavior can be avoided by introducing a compensation capacitor at transformer primary side to resonate with the leakage inductance to have load-independent characteristic. However, for many WPT applications including EV charging, the relative position of primary coil and secondary coil is often changing dynamically. And the changing coupling coefficient means varying leakage inductance, making it impossible to dynamically compensate the leakage inductance and keep constant resonant frequency. As a result, new compensation networks are required for both transmitter coil and receiver coil to solve this issue. The most straightforward type, series-series (SS) compensation network, is briefly analyzed here to give its working principle [32].

In Fig. 23, one capacitor is connected in series at both transmitter side and receiver side,

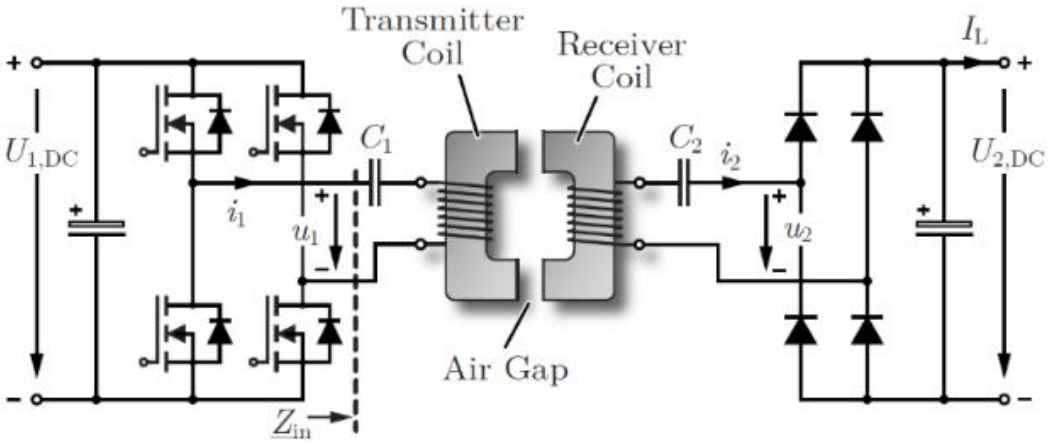


Fig. 23. Series-series compensated WPT converter [35]

and the corresponding fundamental frequency model is derived as in Fig. 24. The two coils are modeled with controlled voltage sources and two lumped inductors. Note that the circuit model is based on fundamental frequency analysis. High order input voltages are assumed to be filtered out by the resonant network, and the diode bridge rectifier is modeled as an equivalent load resistor $R_{L,eq}$. In reality, for considerations like control and soft-switching, converters will not run right at the coil resonant frequency as assumed in the fundamental frequency model. Still, it is adequate for the efficiency evaluation in a broad way. Since the output power and current relationship are derived as,

$$P_o = \frac{1}{2}|i_2|^2 R_{Leq} \tag{1}$$

$$\frac{i_1}{i_2} = \frac{j\omega L_2 + \frac{1}{j\omega C_2} + R_2 + R_{Leq}}{j\omega M} \tag{2}$$

It can be concluded that any net reactance on the secondary will increase i_1 with more loss on R_1, and any net reactance on the primary will not affect loss but increase the v_1 amplitude. As a result, the capacitance value of C_1 and C_2 are selected to resonate with the constant self-inductance of two coils, respectively,

$$f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{L_1 C_1}} = \frac{1}{2\pi}\frac{1}{\sqrt{L_2 C_2}} \tag{3}$$

Since the impedance of resonant networks are cancelled out, the remaining circuit can be solved easily with input impedance,

$$Z_{in} = \frac{\omega_0^2 M^2}{R_{L,eq}} \tag{4}$$

which is purely real, giving coupling-independent behavior of the circuit. This is the major advantage of SS compensation network since resonant frequency will remain constant with

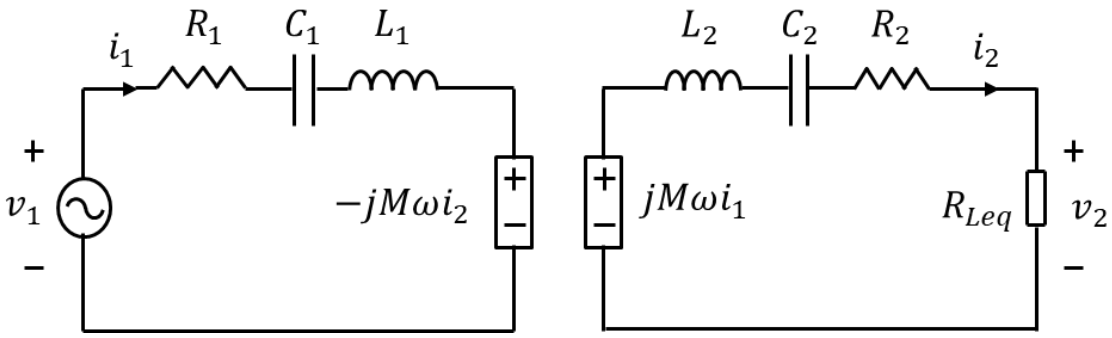


Fig. 24. Fundamental frequency model of series-series compensated WPT system

changing position of coils.

For the given WPT system, the maximum efficiency it can achieve has been analyzed,

$$\eta = \frac{I_2^2 R_{Leq}}{I_1^2 R_1 + I_2^2 R_2 + I_2^2 R_{Leq}} = \frac{1}{\frac{\alpha + \frac{1}{\alpha} + 2}{k^2 Q_1 Q_2} + \frac{1}{\alpha} + 1}, \text{with } \alpha = \frac{R_{Leq}}{R_2} \tag{5}$$

$$Q_1 = \frac{\omega L_1}{R_1} \qquad Q_2 = \frac{\omega L_2}{R_2} \tag{6}$$

where Q_1 and Q_2 are the quality factor of transmitter coil and receiver coil, and k is the coupling coefficient between the two coils. Under the condition that,

$$\frac{\partial \eta(\alpha)}{\partial \alpha} = 0 \tag{7}$$

$$\frac{\partial^2 \eta(\alpha)}{\partial^2 \alpha} < 0 \tag{8}$$

$$\eta_{max} = \frac{k^2 Q_1 Q_2}{\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right)^2} \tag{9}$$

When

$$\alpha = \frac{R_{Leq}}{R_2} = \sqrt{1 + k^2 Q_1 Q_2} \tag{10}$$

with a higher Q or k, the maximum efficiency can be increased. Note that this analysis is not dependent on specific type of compensation network and is as a general formula to evaluate the maximum converter efficiency.

As shown in the equation for system maximum efficiency (10) which is plotted in Fig. 25, with higher quality factor coil design, the system maximum efficiency can be improved. However, the system maximum efficiency is inherently limited by the coupling coefficient [57][58].

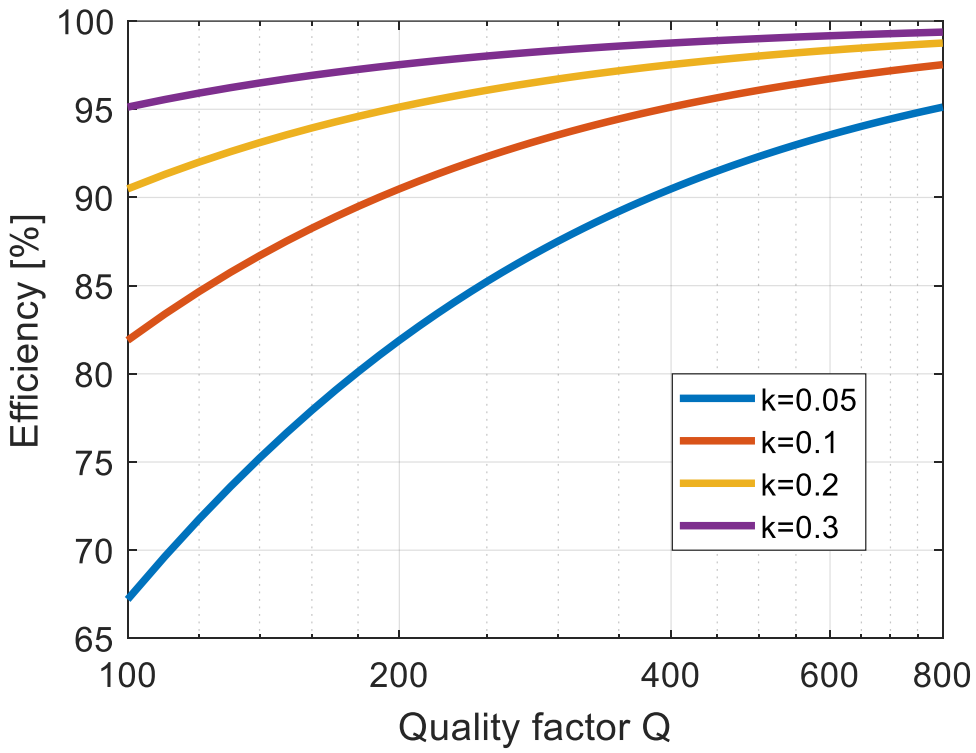


Fig. 25. Theoretical maximum system efficiency between two coils [57]

There are many other possible compensation networks made of different combinations of passive components in series or in parallel with transmitter and receiver coils. Based on the very different system performance requirement for varied applications, different compensation networks are utilized to achieve specific goals, including increase power transfer ability, minimize the VA rating of the power source, and achieve soft-switching of devices [59]-[61]. Reference [61] gives a systematic comparison of four common compensation schemes in IPT systems in terms of maximum efficiency, maximum power transfer, load-dependence, coupling-dependence, and allowance of no magnetic coupling characteristics. There are many other compensation networks proposed for other benefits [62]-[67]. For example, LCL compensation gives a constant induced voltage at secondary side suitable for multiple pickups systems. Although there are a number of configurations for compensation networks, the transmitter coil and receiver coil are still the unchanging component in the WPT system. The two key parameters, k and Q, directly determine the maximum possible efficiency of a WPT converter.

Since coupling coefficient is mostly defined by the size of the coil and coil-to-coil distance, coil quality factor Q is the critical design variable that has direct impact on system maximum efficiency for any given coil geometry. If a coil can be designed to resonate at higher frequency while the ESR remains low, the quality factor is increased. In the past, pushing for high frequency system has been mentioned in many papers for wireless power transfer but is seldom implemented for detailed and mature design beyond hundreds of kHz [30][57][68]. The main limiting factor is the high frequency loss associated with the Litz winding and ferrite cores.

In addition to the possible improvement of quality factor Q, higher frequency could be

beneficial for system design. Based on the fundamental frequency model in Fig. 24, Fig. 26 and Fig. 27 give the calculated system voltages and currents, assuming an optimal coil-to-coil efficiency at 98.02%, with output power P_o = 6600 W, two coils quality factor Q = 500, and coupling coefficient k = 0.2. Note that I_1 and I_2 have the identical values at the optimal coil-to-coil efficiency point. Compared to the 100 kHz IPT system, higher frequency operation at MHz range allows higher input and output DC voltages and lower coil currents due to the changing optimal load resistance in Fig. 28, which is suitable for high efficiency power stage design if enabling high voltage GaN transistors with fast switching capability are used. Alternatively, for the same voltage and current, small coil inductance design is needed, allowing a possible coil weight and volume reduction.

2.2.2 Coil with Large Size and Heavy Weight

Due to the relatively large air gap between transmitter and receiver coil, low coupling is expected, and power transfer capability is low. To increase the overall efficiency, the coil structure should provide the largest coupling possible to avoid any reactive energy associated with the leakage flux. Considering the charging station space, the coil pad should be low-profile and light-weight, and good mechanical stability is needed so that its structure remains intact when coil pad is buried underground. In this section, coil designs are reviewed including their pad geometries and adopted magnetic materials.

(a) Coil Pad Geometry

The circular pad is the most common type and has been studied extensively in recent years for EV [69]. According to [70], a new term, height of the fundamental flux, is invented to describe how far the most of flux can reach above the coil, which determines the coupling between pads. It is claimed that by the nature of magnetic field, the height of

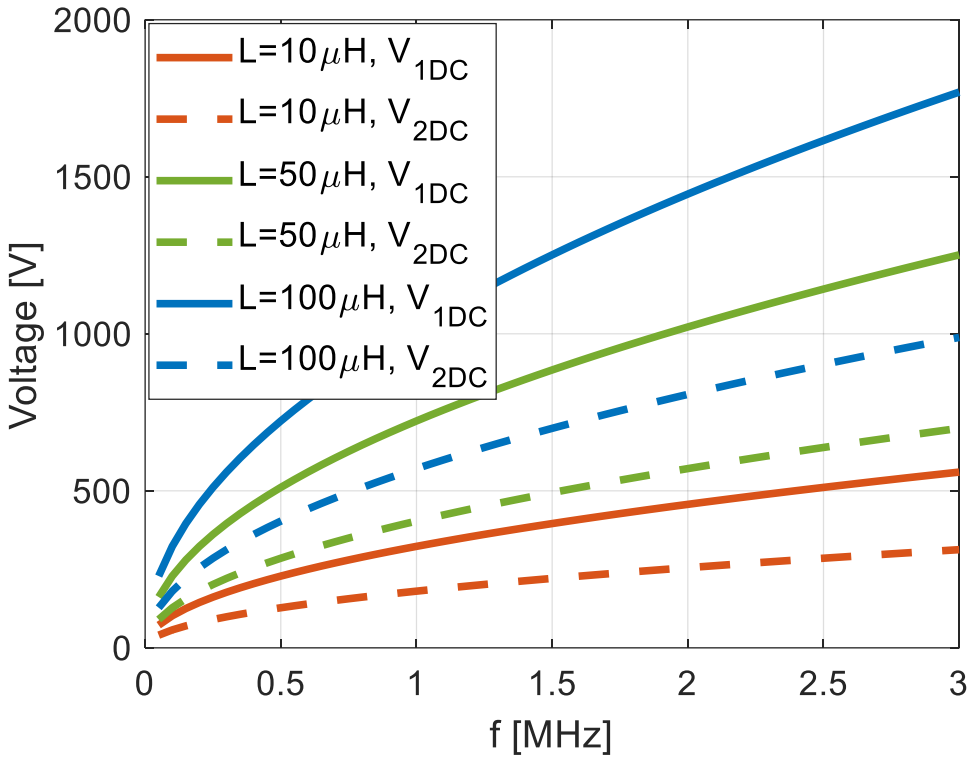


Fig. 26. Calculated inverter input and rectifier output voltages vs. frequency and coil inductance

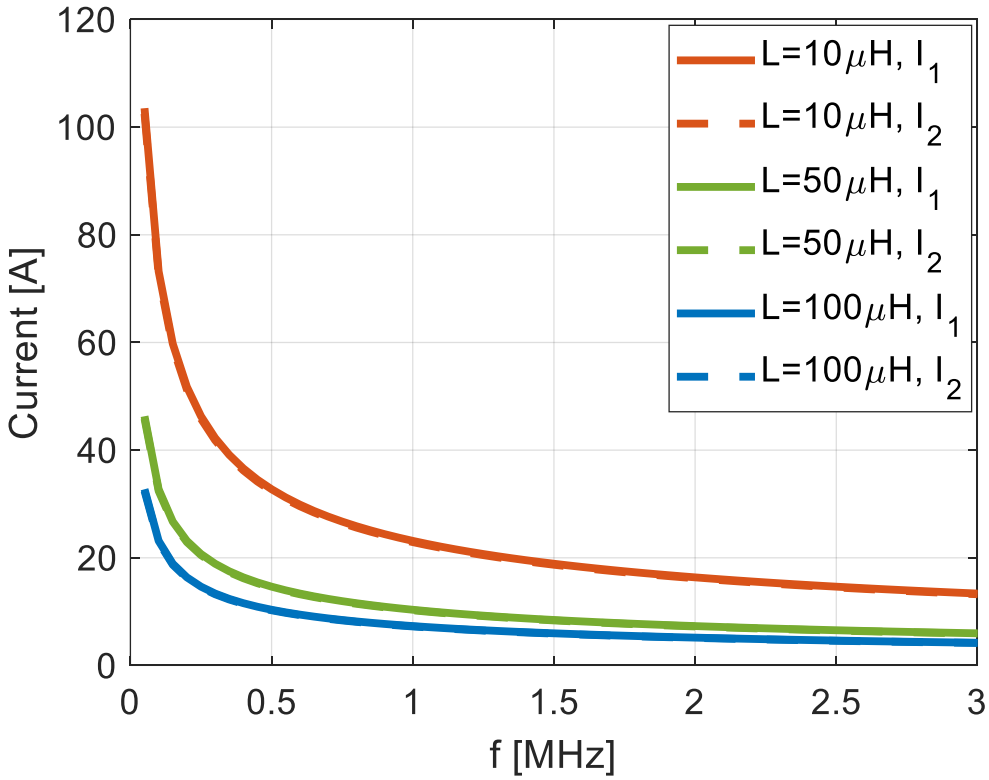


Fig. 27. Calculated primary and secondary side currents vs. frequency and coil inductance

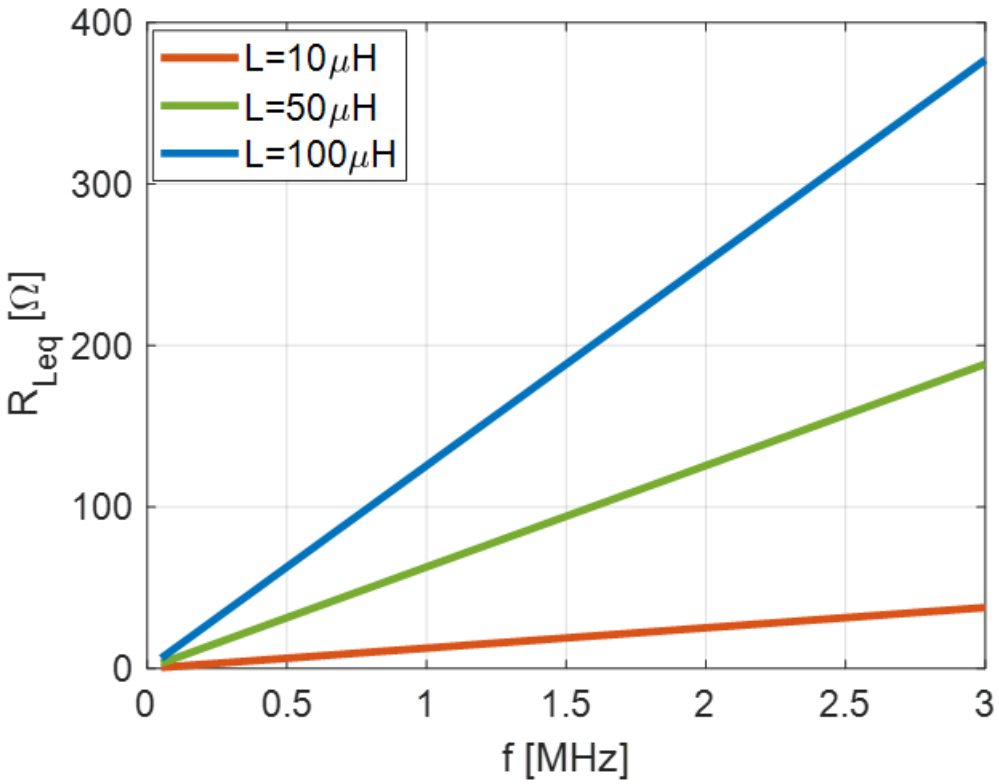


Fig. 28. Optimal load resistance vs. frequency and coil inductance

the fundamental flux path is about one-fourth of the pad diameter as shown in Fig. 29 in the circular pad, which limits the air gap length between transmitter and receiver coil. When the airgap between couplers is about a quarter of the coil diameter, typically the coupling coefficient is close to 0.2. In other words, an increment unit of height requires about four increment units of pad's diameter.

To overcome such limitation and increase the height of the fundamental flux path, [71] proposed a flux-pipe structure as in Fig. 30: the coil is wound on an H-shape long ferrite bar. This structure essentially doubles the preferred flux path to half of the coil pad length. In other words, with given air gap distance, the coupling between two coils will be larger, resulting higher system efficiency if designed properly at same coil dimension constraint. However, observing the flux lines in Fig. 30, for each coil, half of the total flux generated will impose coupling for power transfer, and the other half facing the back of pad is not useful and will generate leakage inductance. This so-called double-side flux distribution naturally wastes half of the flux and cause more burden for shielding effort. When shielding is added, extensive loss is generated, and the quality factor drops dramatically.

In summary, the circular coil has the desirable single-sided flux distribution, with most of the flux utilized for power transfer. Usually, an aluminum cover is applied at bottom of the pad as shielding to prevent extra loss in surrounding metal materials, but it has no impact on efficiency improvement since it works only on the leakage flux. Still, the height of the fundamental flux path is limited compared with flux-pipe structure.

To solve the issue for both circular pad and flux-pipe, and to improve the misalignment tolerance, the DD pad is invented, with better misalignment performance with larger charge zone [72][73]. Instead of using a vertically wound coil, now two D-shape coils are placed

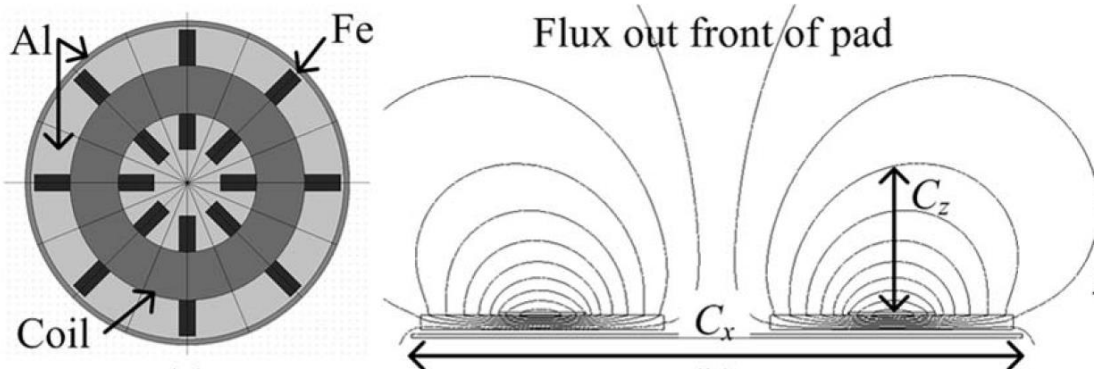


Fig. 29. Layout of a circular pad and its flux lines on the cross section [69]

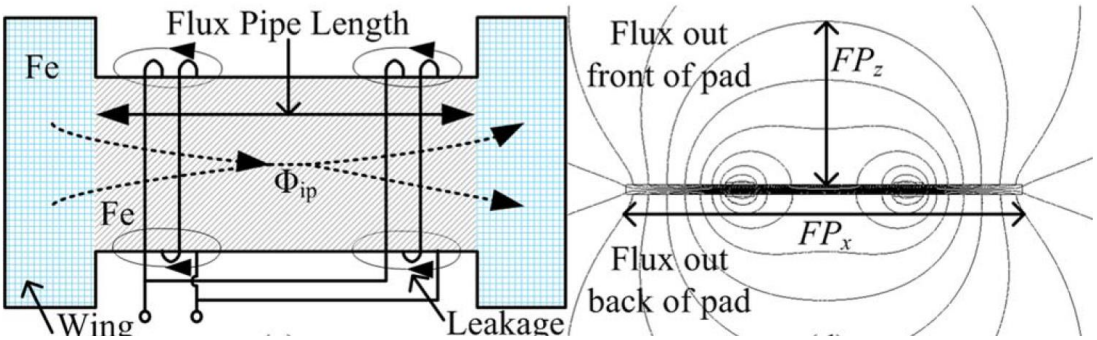
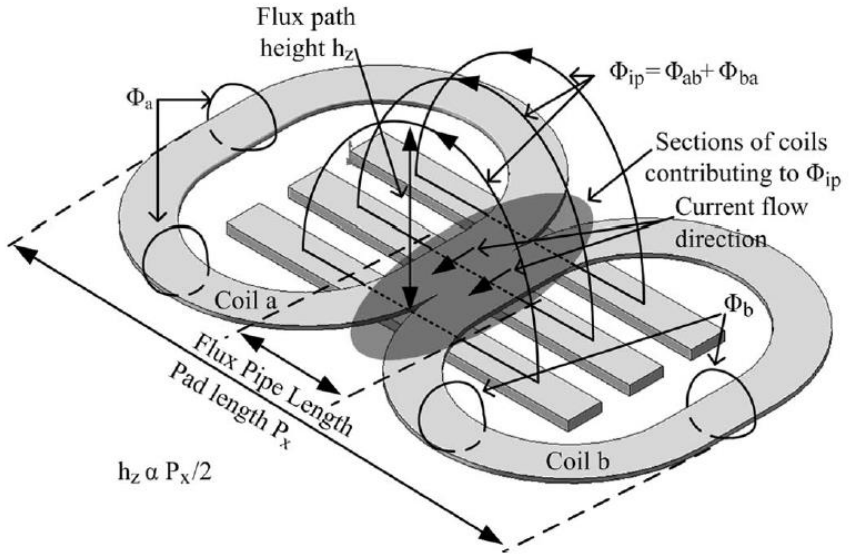


Fig. 30. Layout of a flux-pipe and its flux lines on the cross section [70]

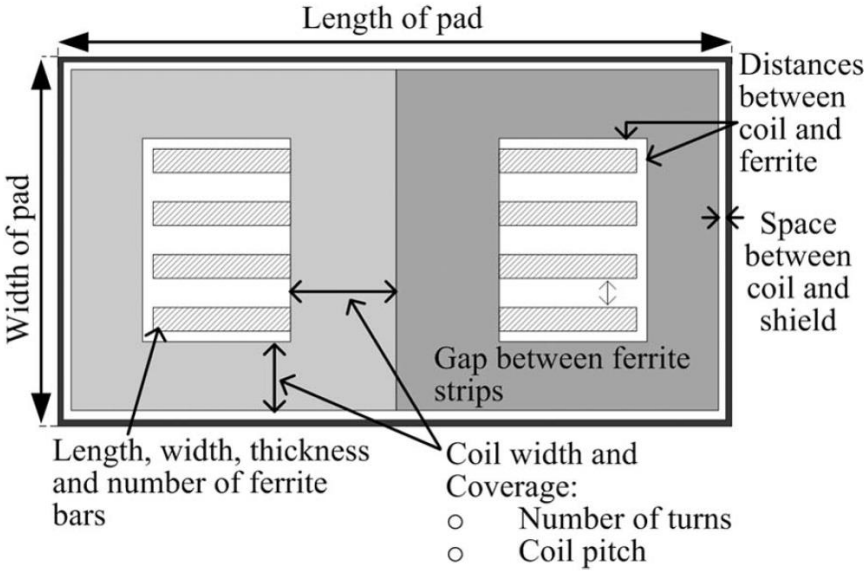
horizontally. At the center of a DD pad, an equivalent flux-pipe is formed by connecting two coils in parallel electrically, and in series magnetically. In this way, the fundamental flux height will be proportional to half of the pad length. Consequently, the length of the pad should be made as long as possible to increase the coupling, while the width of the pad needs to be small to avoid extra copper loss. This design concept results in the double D shape structure in Fig. 31. Note that no major flux will be generated on the back of coil, and aluminum shielding loss for leakage flux will be small.

Under the x-axis (front-to-rear of car) misalignment condition, the DD pad suffers from a null position, where the coupling coefficient drops to zero. As shown in Fig. 32(c), all the flux generated from transmitter coil will enter and exit from one D coil at the receiver side, resulting in no induced voltage at the secondary side. The flux picked up by the other D coil is negligible due to the far distance. Such characteristic makes the DD pad sensitive to the x-axis misalignment. In order to compensate, an extra quadrature (Q) coil at the receiver side is shown in Fig. 32(a). At null position, the changing flux in the Q coil will induce voltage instead of the DD pad. Its symmetrical position makes sure that it is magnetically decoupled with the DD pad of receiver, and they can be tuned separately and then work together as the receiver pad.

Fig. 33 gives the comparison result of power transferred with different coil pads under varying horizontal offset. The air gap is 200mm, primary current is 23A, and switching frequency is 20 kHz. Compared with DD pad, DDQ can clearly increase the power transfer capability at null position with x-axis offset. Note that Q pad has no compensation ability for y-axis misalignment. For similar reason, the circular pad also has a null position, at about 40% of pad diameter offset. At zero offset, the intrinsic low coupling coefficient



(a)



(b)

Fig. 31. DD pad: (a) simplified model (b) final structure [72]

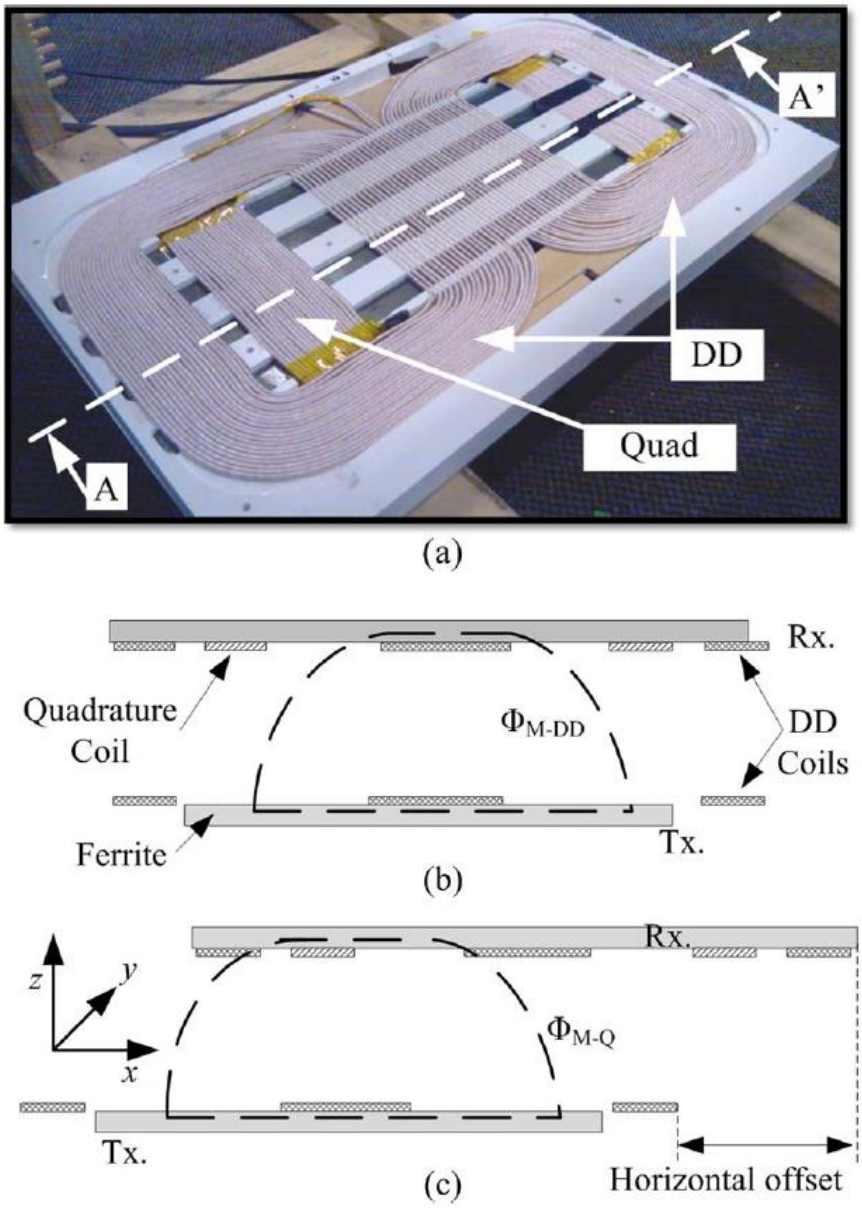
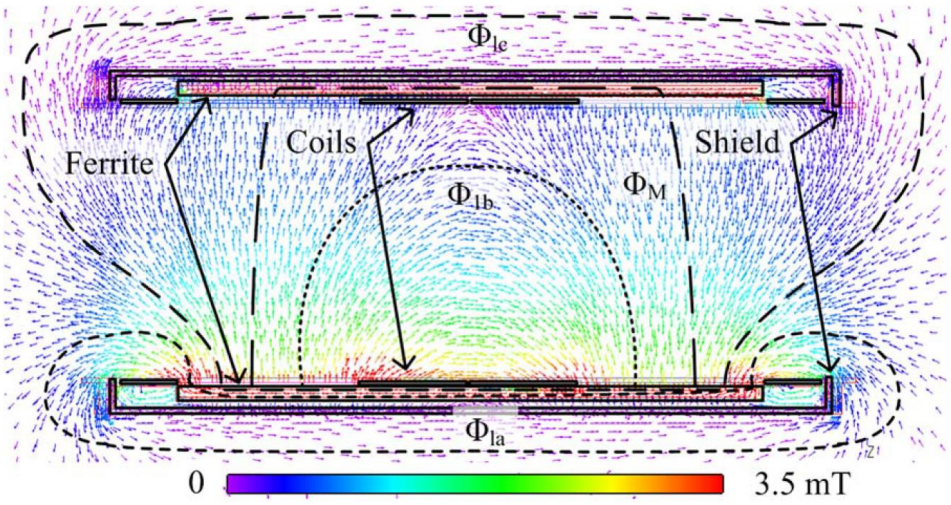
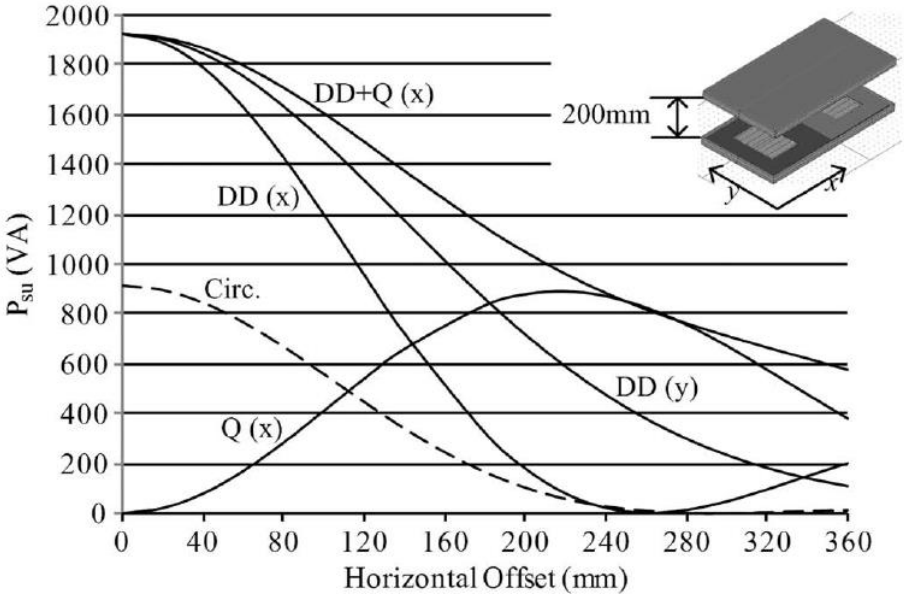


Fig. 32. DDQ pads (a) Coil structure (b) horizontally x-axis aligned position (c) horizontally x-axis misaligned null position [72]



(a)



(b)

Fig. 33. (a) Cross section view of DD pad flux distribution (b) misalignment tolerance comparison for circular pad, DD pad and DDQ pad [72]

leads to the relatively low power transfer of circular pad. However, it should be noted that the extra Q coil will generate more copper loss and power converter loss, since an additional paralleled rectifier is needed for the Q coil. Moreover, when parked, it is easy to tune the front-to-rear misalignment by simply driving forward or backward, while door-to-door misalignment is more critical and not convenient to adjust.

The comparison of different coil structures has also been conducted in other papers as shown in Fig. 34 [74]. However, all the comparisons mentioned above either focus on coupling coefficient only or lack system level optimization.

In reality, for the system design, the fundamental flux height is not the only critical factor that has influence on the system efficiency and power density. For instance, higher copper loss in DD coil may outweigh its advantage in high coupling coefficient in terms of system performance. To have a fair and comprehensive comparison on the system performance using different coil pad structure, a multi-objective optimization is developed in [75] considering the tradeoffs between conflicting design parameters. The pad geometries under analysis are shown in Fig. 35. The geometrical parameters related to windings and ferrites are considered based on the defined range in TABLE VI. The optimization region is also bounded by maximum winding current density, maximum core flux density, maximum core loss density, and minimum system efficiency (>93%).

A total of 3000-4000 designs are computed from TABLE VI and the result is shown in Fig. 36. With the higher coupling coefficient for a given coupler size, the copper winding loss is lower because of the low driving current under the same power output. Although more ferrites are required for the circular pad for the same power density, the average flux density in the ferrite strips is relatively low, leading to the lower core loss as depicted in

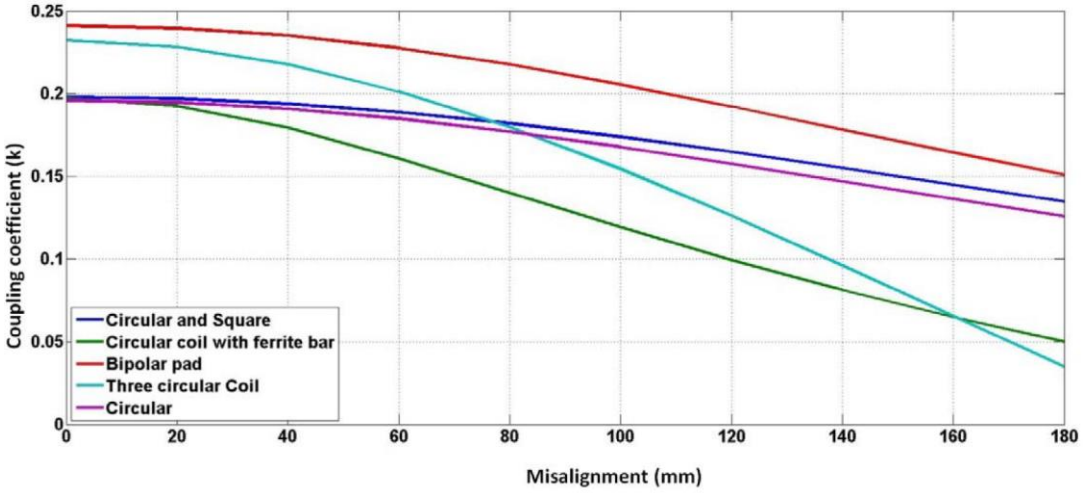
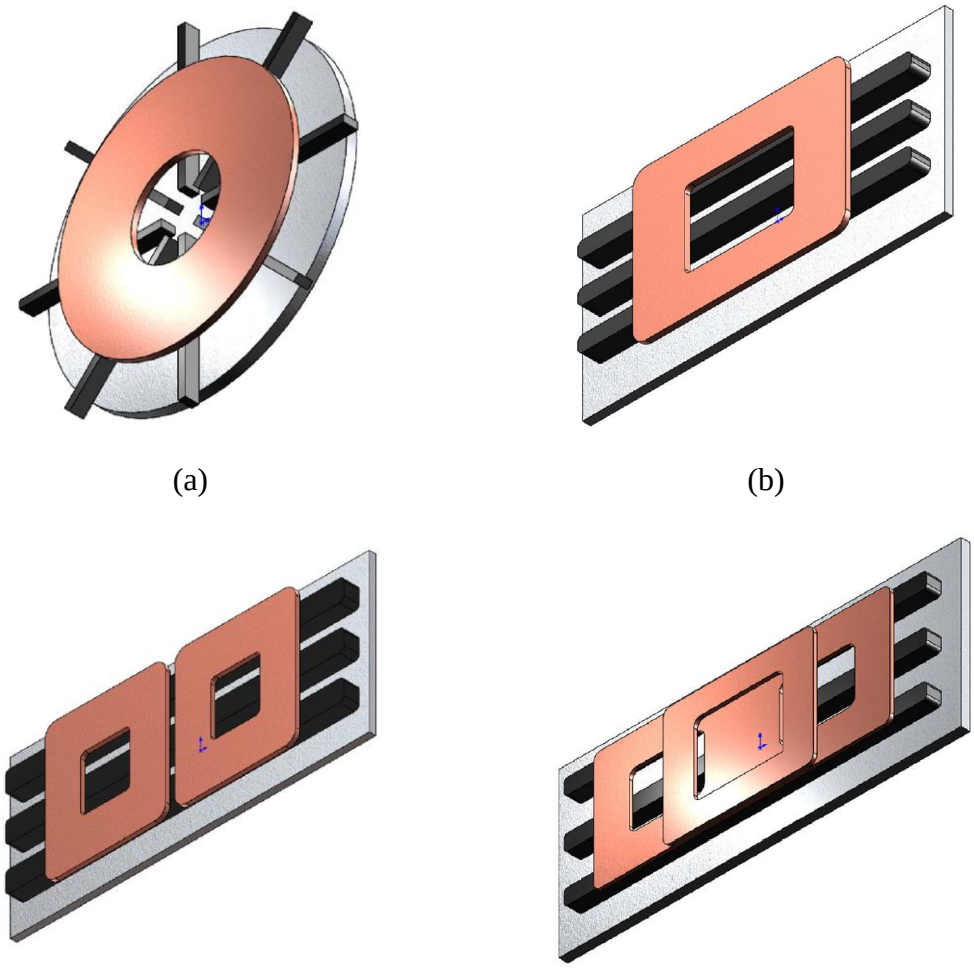


Fig. 34. Comparison of coupling coefficient for different coil geometries [74]



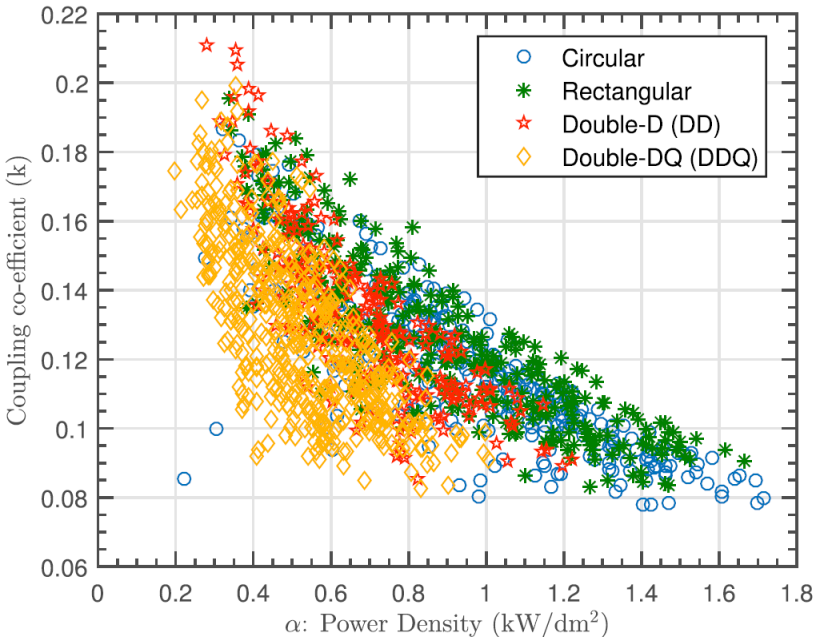
(a) (b)

(c) (d)

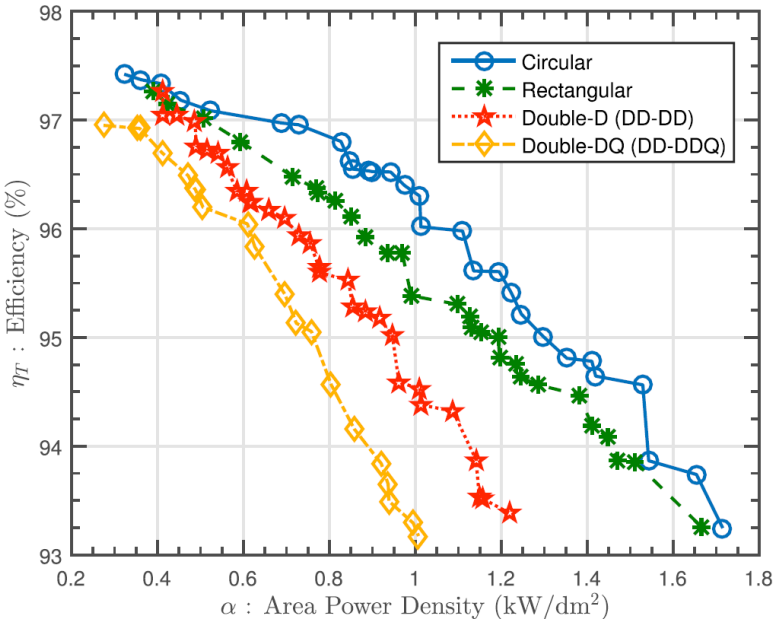
Fig. 35. Coil pad candidates for comparison [75]

TABLE VI. Design optimization range for coil parameters [75]

Variable	Symbol	Unit	Range			
			DD-DD	DD-DDQ	Rect	Circ
Number of turns	N_{T}, N_{R}	-	15-60	15-60	20-65	20-65
Number of turns in Q coil	N_{Q}	-	-	15-60	-	-
Diameter of litz wire	d_{litz}	mm	2.4 - 4.8	2.4 - 4.8	2.4 - 4.8	2.4 - 4.8
Inner length	l_{i} , r_{i}	mm	10-35	10-35	10-75	10-75
Inner width	w_{i}	mm	10-35	10-35	10-75	-
Ferrite thickness	h_{fe}	mm	5-35	5-35	5-35	5-35
Ferrite width	w_{fe}	mm	15-45	15-45	15-45	15-45
Gap between ferrites[2]	w_{ag}	%	20-100	20-100	20-100	-
Length of ferrite [3]	l_{fe}	%	50-120	50-120	50-120	50-120
Number of ferrites	n_{fe}	-	1-7	1-7	1-7	2-12



(a)



(b)

Fig. 36. Optimization results (a) coupling coefficient vs area power density (b) system efficiency vs. area power density [75]

Fig. 37. Considering the two factors above, the circular pad has the highest efficiency and power density. Although the conceptual argument on the fundamental flux height indicates that DD and DDQ pads should have higher coupling, that conclusion was simply based on the analysis with case studies.

Reference [75] also discussed the important performance factors including misalignment and stray field as shown in Fig. 38, and the results are as follows [76]:

a. Circular pad has highest coupling factor and power density under the perfectly aligned condition.

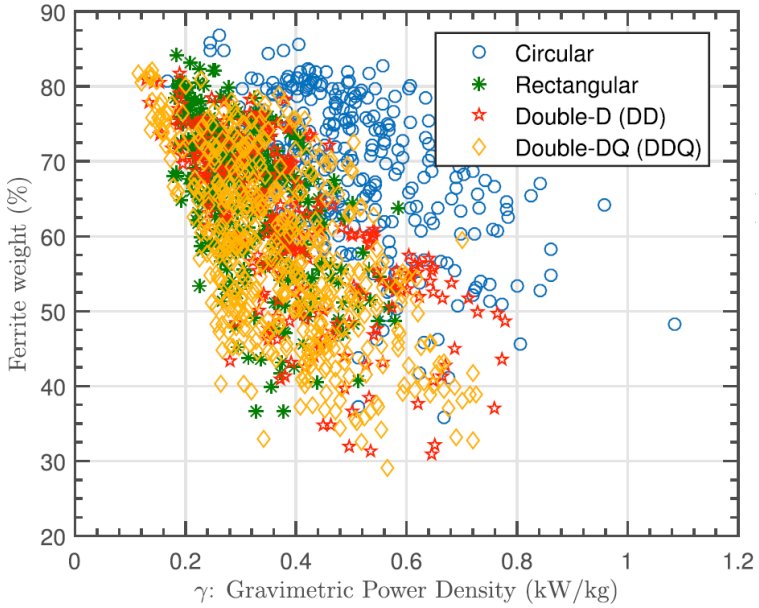
b. With most usage of ferrites and least usage of copper windings, the circular pad has the lowest ferrite and winding loss, leading to the highest system efficiency.

c. Polarized pads including DD and DDQ give better misalignment performance in the longitudinal direction.

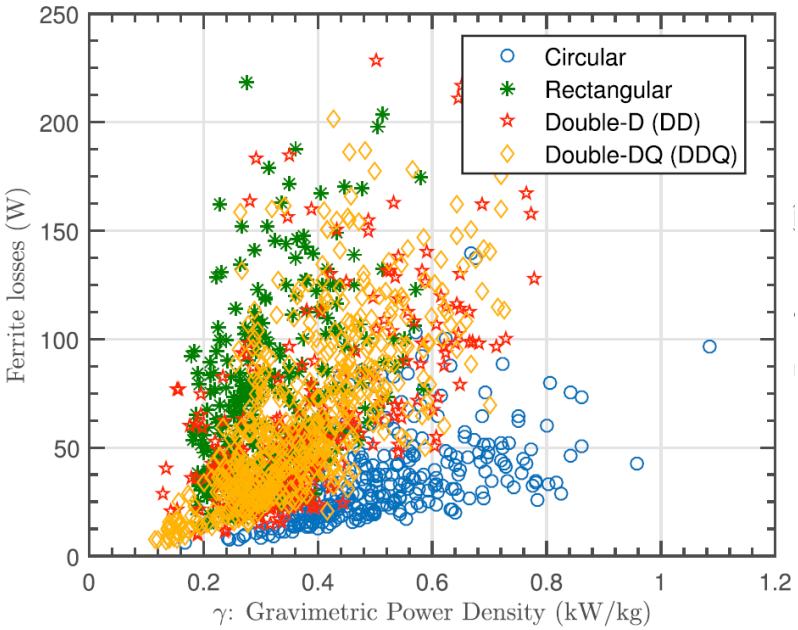
d. Both circular and rectangular pads have lower stray field densities compared to polarized pads.

(b) Magnetic Material

For most current WPT systems for EV charging, the switching frequency is around 100 kHz. Accordingly, low core loss ferrites are applied for their low cost. Moreover, because ferrites are fabricated by pressing and sintering of iron oxides, they have the isotropic material property. This is important because the magnetic field between two coils has a spatial orientation, and the direction has a large variation throughout the magnetic core. In contrast, tape wound cores are anisotropic. When a flux with the direction orthogonal to the lamination exists, it will generate huge eddy current loss [77]. It is in fact the same reason why litz wire is preferred over the laminated copper foil as the winding material.

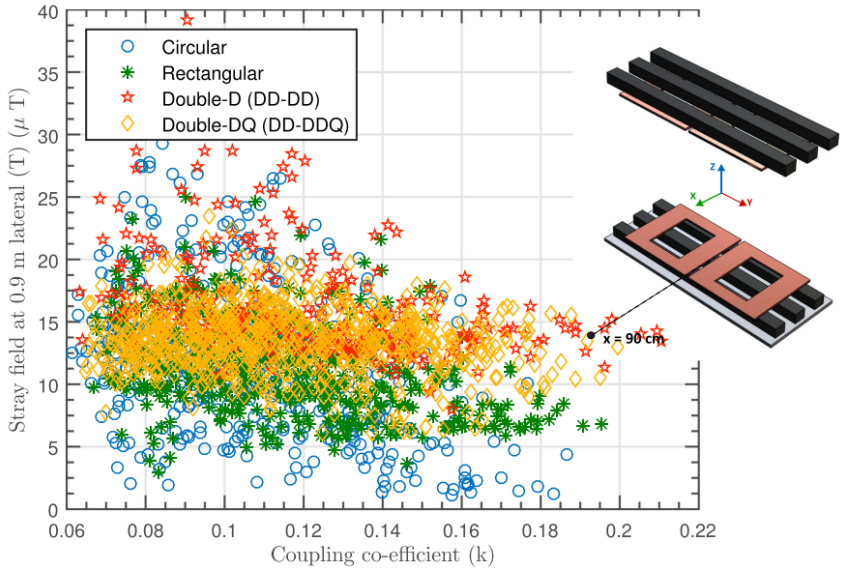


(a)

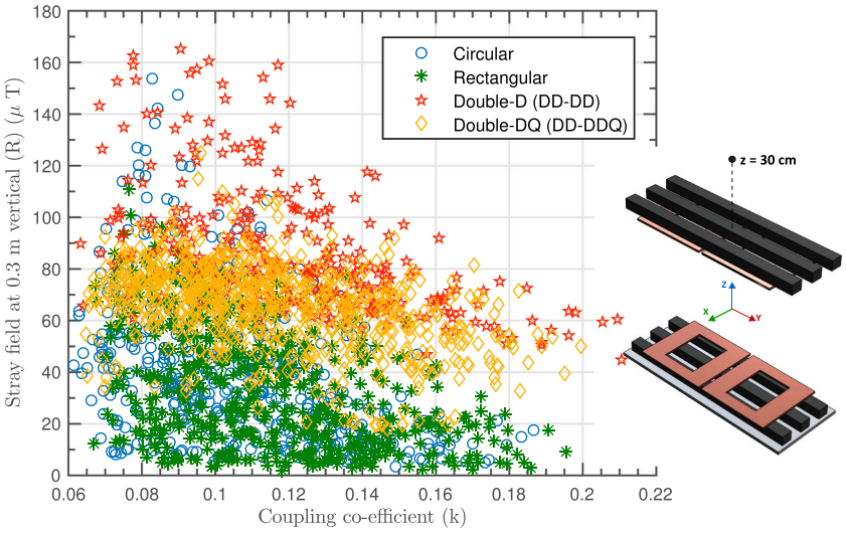


(b)

Fig. 37. Optimization results (a) ferrite weight as percentage vs. gravimetric power density (b) ferrite losses as percentage vs. gravimetric power density [75]



(a)



(b)

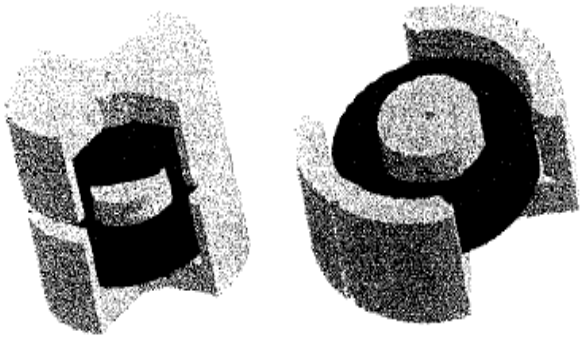
Fig. 38. Optimization results (a) stray field 0.9 m lateral from the transmitter coil center (b) stray field 0.3 m vertical from the receiver coil center [75]

The most common magnetic cores utilizing pot cores [78], U cores [79][80] or E cores [81][82] are not suitable for EV application for their excessive thickness or fragility to bury underground as shown in Fig. 39. Moreover, the flux coupling area is quite small compared with the size of coil pad, making it very sensitive to the horizontal misalignment.

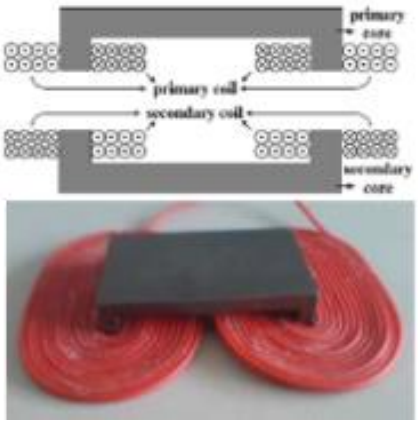
As a result, magnetic core is more often used to constrain the flux path beneath the litz winding. In Fig. 40, the leakage flux below the winding is channeled through the ferrite plate. The inductance and coupling can be increased, and excessive energy loss can be avoided in the surrounding materials.

Knowing that adding ferrite is beneficial for better flux distribution, the remaining issue is the structural design of ferrites. However, the analytical solution is usually not feasible considering the complexity of the flux distribution. In fact, the magnetic field is strongly influenced and shaped by winding and magnetic core together, and it can only be solved practically in situations where there are no magnetic cores. As a result, finite element analysis (FEA) is used in most of the reviewed papers and verified with measurement results. In the following part of this section, several examples are reviewed to show the simulation-aided design trade-off process. Despite coil pad structures being different in the examples, a shared ferrite core design methodology is common among them.

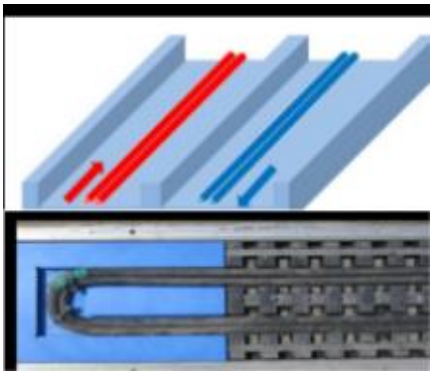
The most straightforward parameters of ferrite core are the diameter and area. To investigate the optimal diameter of ferrite plate, the simulated coupling coefficient under different ferrite plate diameters is drawn in Fig. 41(a). Two rectangular coils with diameter of 450 mm and 250 mm are used at primary side and secondary side, respectively. The air gap is 150 mm and a whole plate of ferrite is assumed. Larger size of ferrite plate can help increase the coupling coefficient with diminishing benefit for length much greater than the



(a)



(b)



(c)

Fig. 39. Litz wire with (a) pot core (b) U core (c) E core [78]-[82]

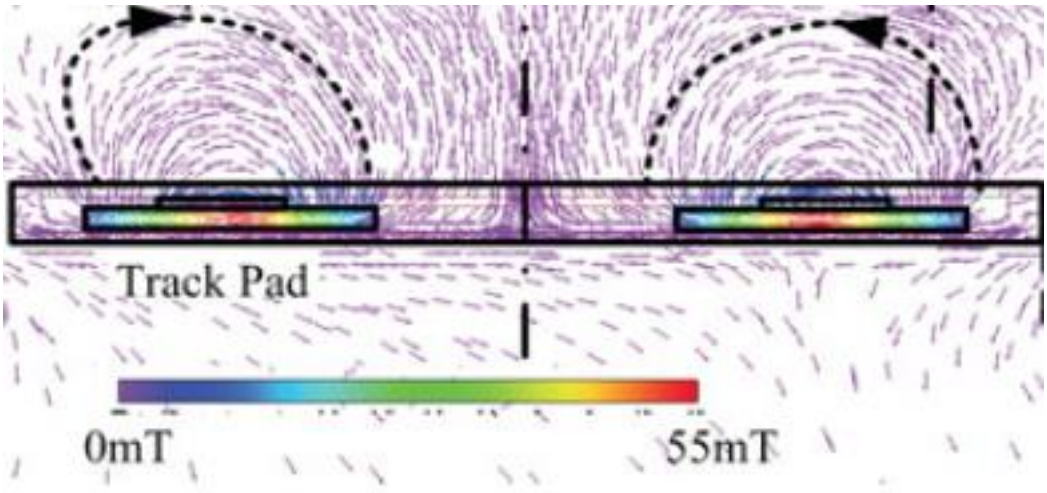
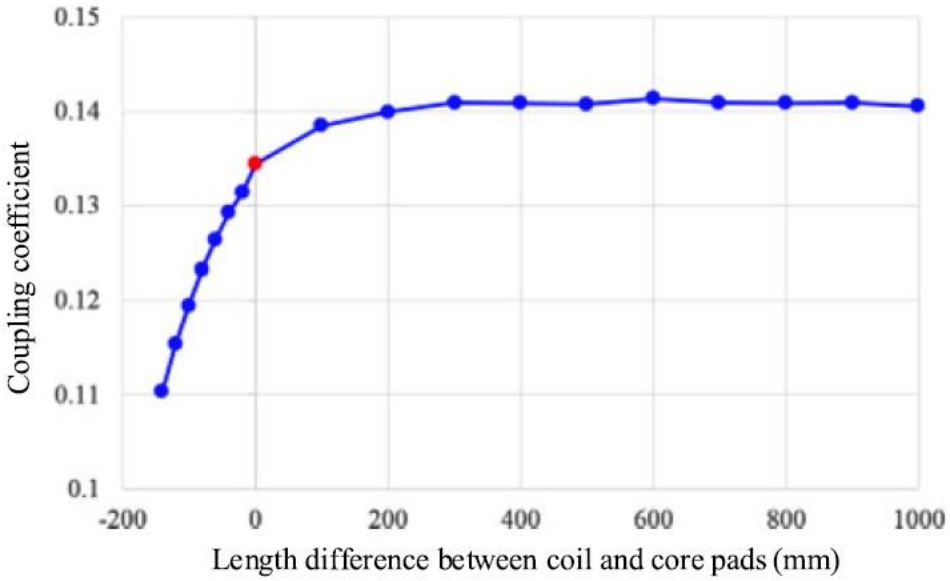
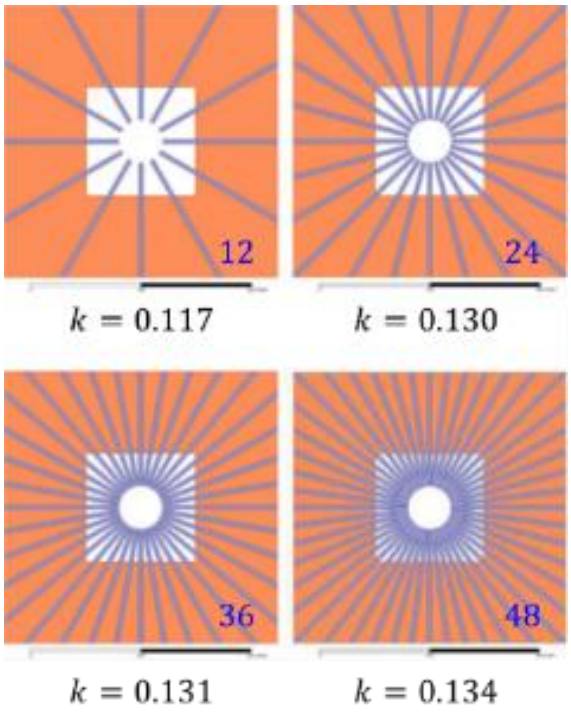


Fig. 40. Flux distribution of a circular litz winding with ferrite plate below [69]



(a)



(b)

Fig. 41. (a) Effect of length difference between coil and ferrite core (b) effect of different number of ferrite bars [83]

coil diameter. A good trade-off design point should have the core plate diameter comparable to the coil pad size. Fig. 41(b) provides the analysis of number of ferrite bars. Instead of using a whole plate, ferrite bars are widely used to make a trade-off between weight and coupling. With the fact that coupling coefficient is limited at 0.136 with the ferrite plate, it is not feasible to select a large number of ferrite bars for the sole purpose of increasing coupling.

Specifically, the length, width, thickness, and number of ferrite bar can be studied by changing the interested variable. Fig. 42 presents the power transferring capability of different ferrite bar geometry parameters for a circular coil pad. Although all the parameters can help increase the coupling, it provides the guideline for geometry design since increasing bar length has the most benefit and increasing thickness has the least. To further investigate different ferrite arrangements, a number of ferrite bar topologies are compared in Fig. 43. Although (d) and (e) have lower power transfer capability, they have the best utilization of ferrite bars since long bars increase the flux density above the pad and narrow bars enable a more efficiently guided flux around the coil.

Fig. 44 exhibits another ferrite bar design example in DD coil pad. The length and width of ferrite bars are tuned to locate best coupling and maximized power transfer. The purple shaded area is preferred as the design target since it has the greatest slope, indicating an efficient ferrite material employment.

Different coil pads including rectangular, circular and DD have been discussed in this section, it is clear that same FEA-assisted method is shared for ferrite core design on diameter, size, bar pattern, in order to improve the coupling within the size and weight limits.

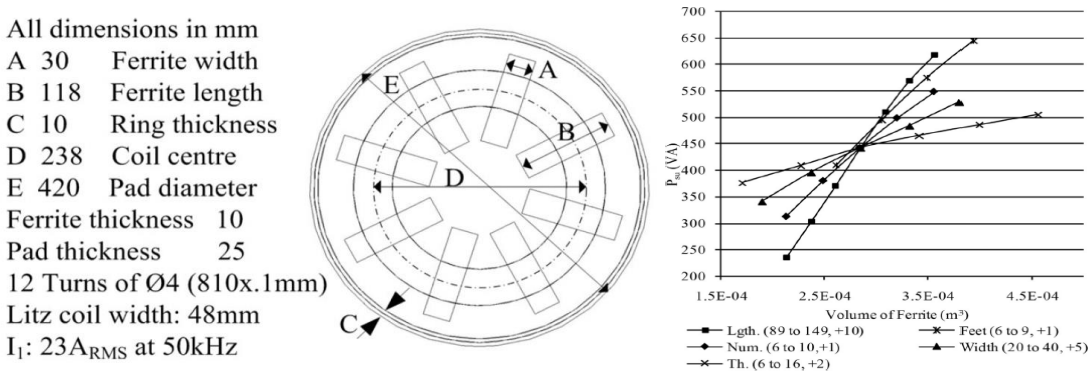


Fig. 42. Volumetric comparison of ferrite bar parameters [69]

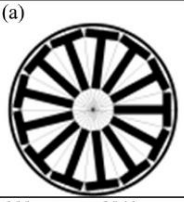
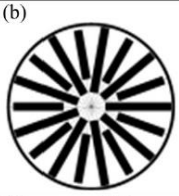
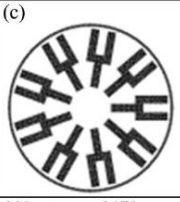
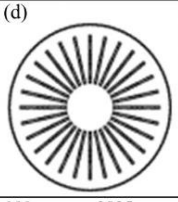
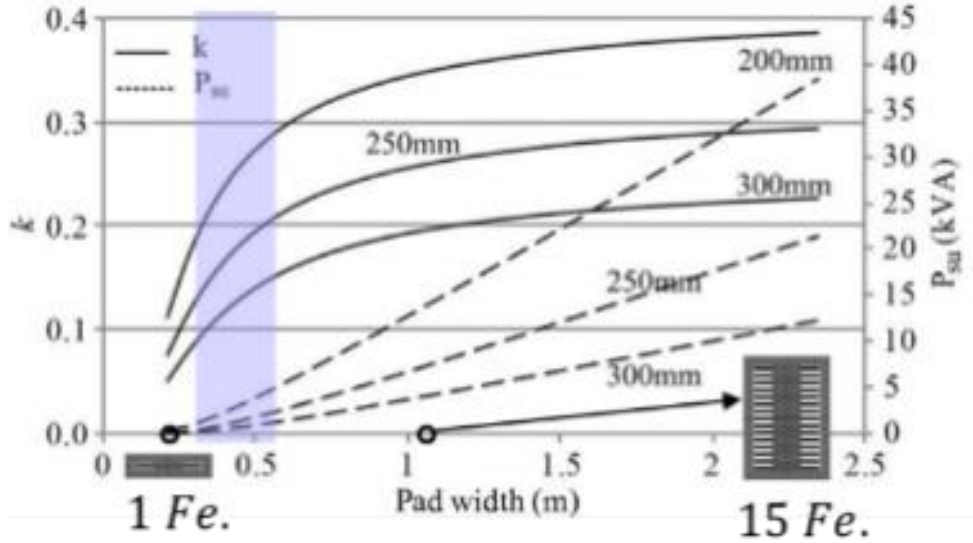
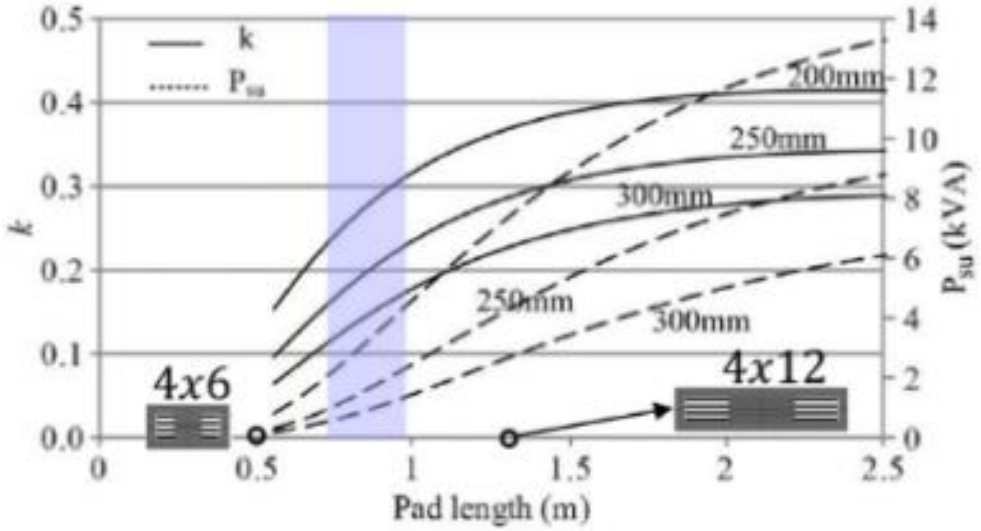
Pad Topology	(a)	(b)	(c)	(d)	(e)
					
P_{su} at given Separation (VA)	100mm 3841 150mm 1236 200mm 435	100mm 3832 150mm 1212 200mm 420	100mm 3479 150mm 1102 200mm 383	100mm 2825 150mm 868 200mm 293	100mm 2480 150mm 775 200mm 264
No. of bars	32.5	31.5	33	21	18
Use (VA/cm^3)	3.34	3.44	2.98	3.80	3.89

Fig. 43. Comparison of different ferrite bar arrangements [69]



(a)



(b)

Fig. 44. Variation in ferrite for a DD pad: (a) width (b) length [72]

(c) Ferrite-less Approaches

To have a more compact and cost-effective coil design with less ferrite, efforts have been made on windings in Fig. 45 and Fig. 46. Different from leveraging an efficient ferrite layout, [49] applied two more additional intermediate coils at the primary side to have an efficient coil space utilization. Still, the system can only deliver 3.3 kW output power with 800x800 mm^2 coil dimension. Reference [84] proposed a ferrite-less DD coil pad to avoid using large quantities of brittle ferrite cores. To prevent any potential crack of the ferrite due to the high forces from the roadway and corrosion of Aluminum plate, the transmitter side coil is ferrite-less and Al-less, with an additional reflection winding to attenuate the stray field. With 40% reduction in coupling and more than 50% reduction in primary side inductance, the primary side current is increased significantly. With 980x750 mm^2 transmitter pad dimension and 175 mm airgap, the primary and second side RMS currents are 97 A and 130 A respectively, and the system DC-DC efficiency is only 89% at 5.7 kW output. The efficiency is low and brings challenges to power stage thermal management.

Another approach is pushing for high switching frequency to help shrink the size of passive components. However, it causes more high frequency loss on Litz winding and magnetic material, resulting in further reduced system efficiency. There are some efforts pushing for high switching frequency for wireless EV application. For instance, [56] uses a parallel self-resonant (SR) coil structure at 6.78 MHz and reaches an even higher power density for IPT at 290.5 kW/m^2, but the power transfer is limited at 1 kW through only 19 mm air gap as shown in Fig. 47. Still, the potential for higher power is limited by the single-turn inductance of less than 1 μH.

(d) Summary

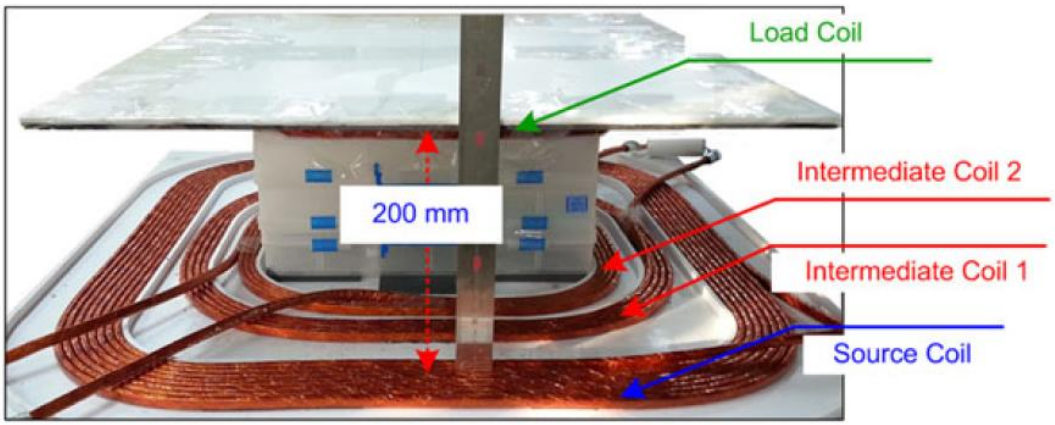


Fig. 45. Asymmetric Four-Coil Resonator without ferrite [49]

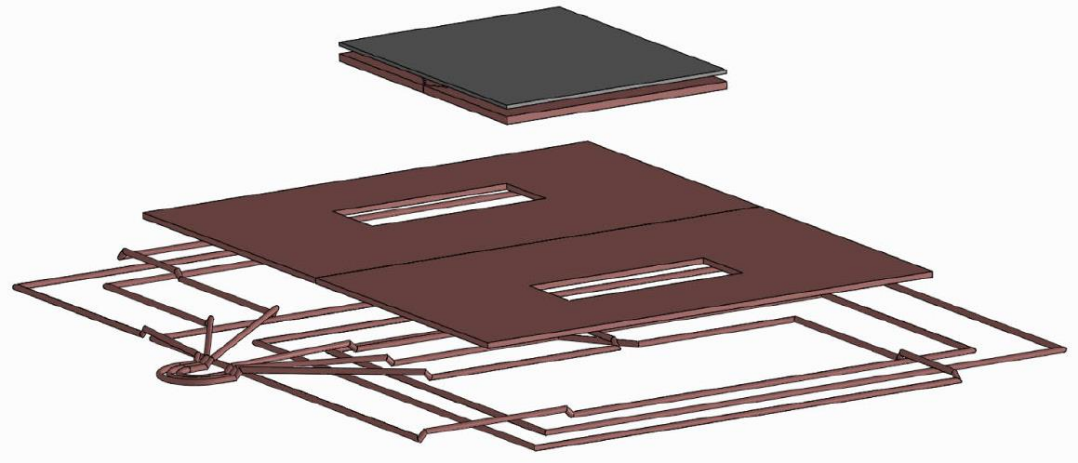


Fig. 46. Ferrite-less DD coil pad [84]

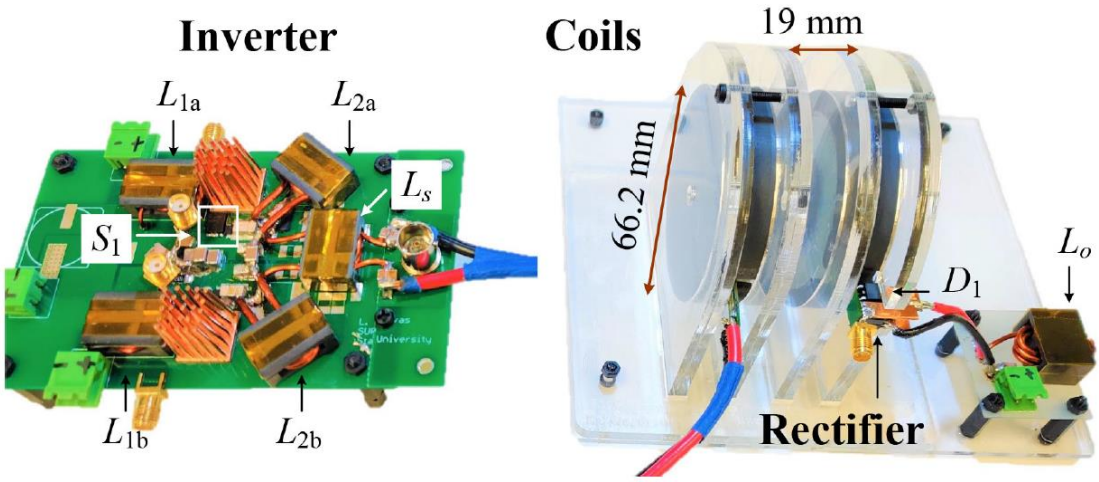


Fig. 47. 6.78 MHz, 1 kW WPT system using self-resonant coils [56]

In conclusion, in order to compensate the low coupling between couplers in WPT systems, it is natural to have larger coil with more Litz winding and ferrites to boost the coupling. However, it inevitably sacrifices the size, weight, cost of the couplers, and may deteriorate the fringing field. TABLE VII gives some of the advanced coil designs parameters. The diameter of pad usually ranges from 200 mm up to 900 mm in the current papers to increase the coupling. At the same time, because of the high power requirement and relatively low switching frequency, the quality factor of the coil is often limited.

2.2.3 Lumped Capacitors with Excessive Loss and Volume

Also, considering the associated compensation networks like capacitors, the overall size for passive components in the WPT system continue to increase. In Fig. 48 to Fig. 53, the compensation capacitors layout and system loss analysis of four designs are illustrated.

Fig. 50 shows a 50 kW WPT system from ETH running at 85 kHz, which presents an optimized overall efficiency over 95%. Still, because of the low switching frequency and large compensation capacitance, the capacitors take more than 40% of the overall loss, as depicted in Fig. 51. Accordingly, proper heat dissipation method is needed. As shown in Fig. 50, due to the high voltage requirement, five high power capacitors are connected in series. Axial cooling fans are installed at both ends of the milled aluminum heat sink for forced-air cooling. A 3D printed polycarbonate isolation duct is also made for high voltage isolation of capacitors. Besides the complexity in structure, compensation capacitors and their cooling system further increase system volume.

Another design example in shown in Fig. 52 and Fig. 53. The size of compensation capacitors is comparable to the DD coil pad, and the dielectric loss from the capacitors is the dominant loss, even larger than the ferrite and winding losses.

TABLE VII. State-of-the-art coil parameters for EV

Team name	f_{sw} (Hz)	Power (kW)	Coil area (mm^2)	Air gap (mm)	Inductance (μH)	Inductance (μH)	Couplers weight (kg)	Ferrites dimension (mm)
					Pri.	Sec.		
ETH	100k	5	210^2 (circle)	52	122	70.3	2.3x2	210^2 (circle)
ETH	85k	50	410x760	160	71.6	71.6	24.6x2	630 mm I-cores x 5
ORNL	23.5k	12	640x640	162	108	108	NA	640x640
KAIST	90k	3.3	800x800	200	186	123	NA	None
NTU	100k	2.1	300^2 (circle)	80	234	120	NA	None
HEVO	85k	25	600x900	210	60	60	NA	NA



Fig. 48. Lumped capacitor array in 25 kW, 88 kHz system [51]

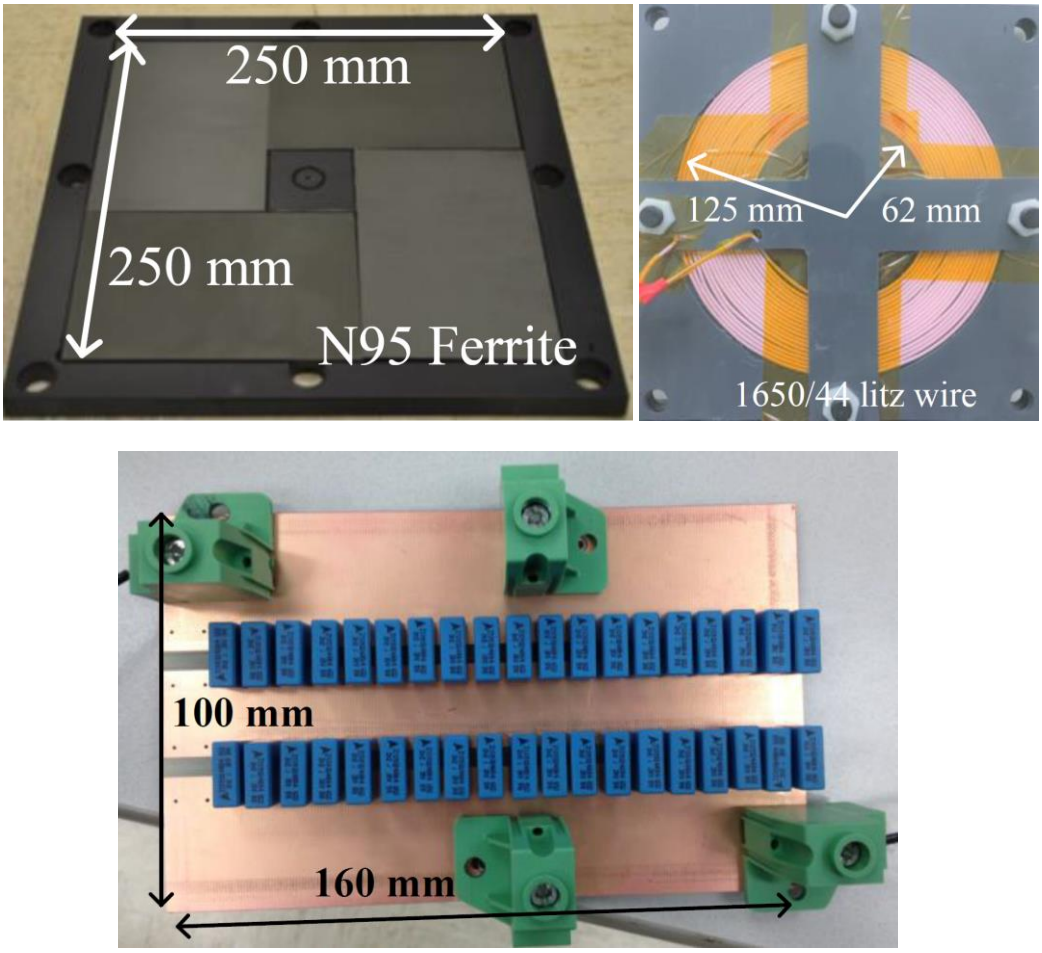


Fig. 49. Lumped capacitor array in 3.3 kW, 100 kHz system [31]

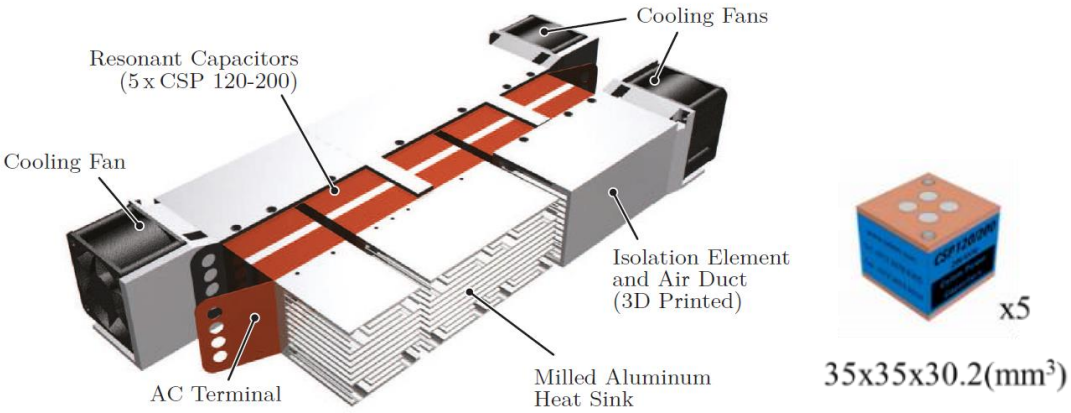


Fig. 50. Lumped capacitor module with associated forced-air cooling system for a 50 kW, 85 kHz system [35]

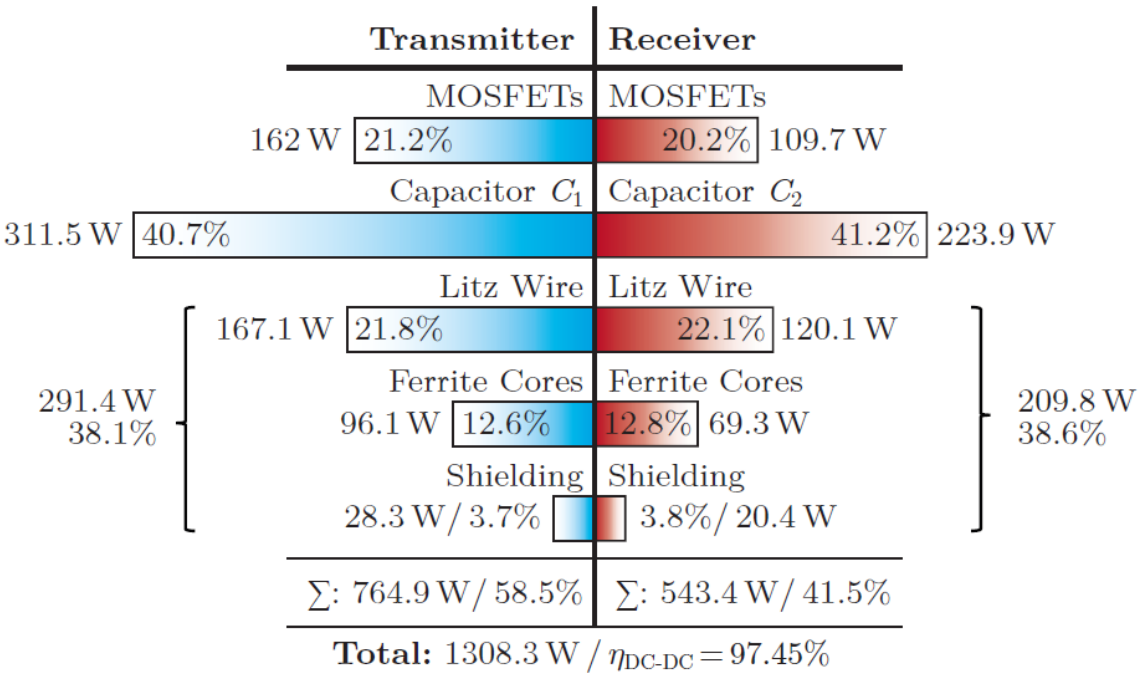


Fig. 51. Loss breakdown of a 50kW system [35]

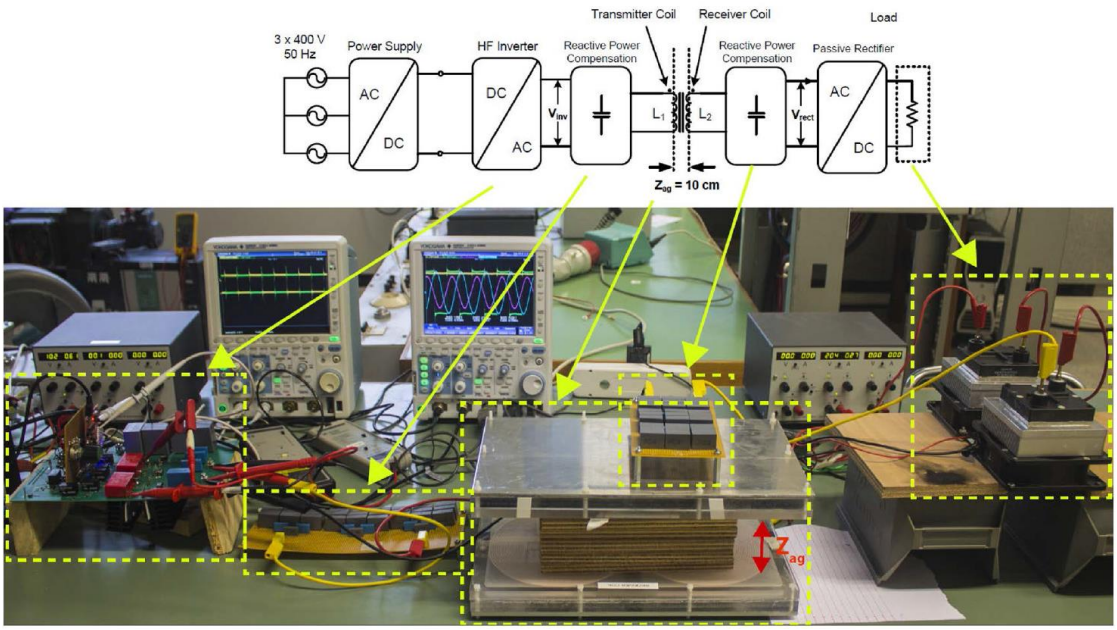


Fig. 52. System diagram of a 2.5 kW IPT system with DD coils [75]

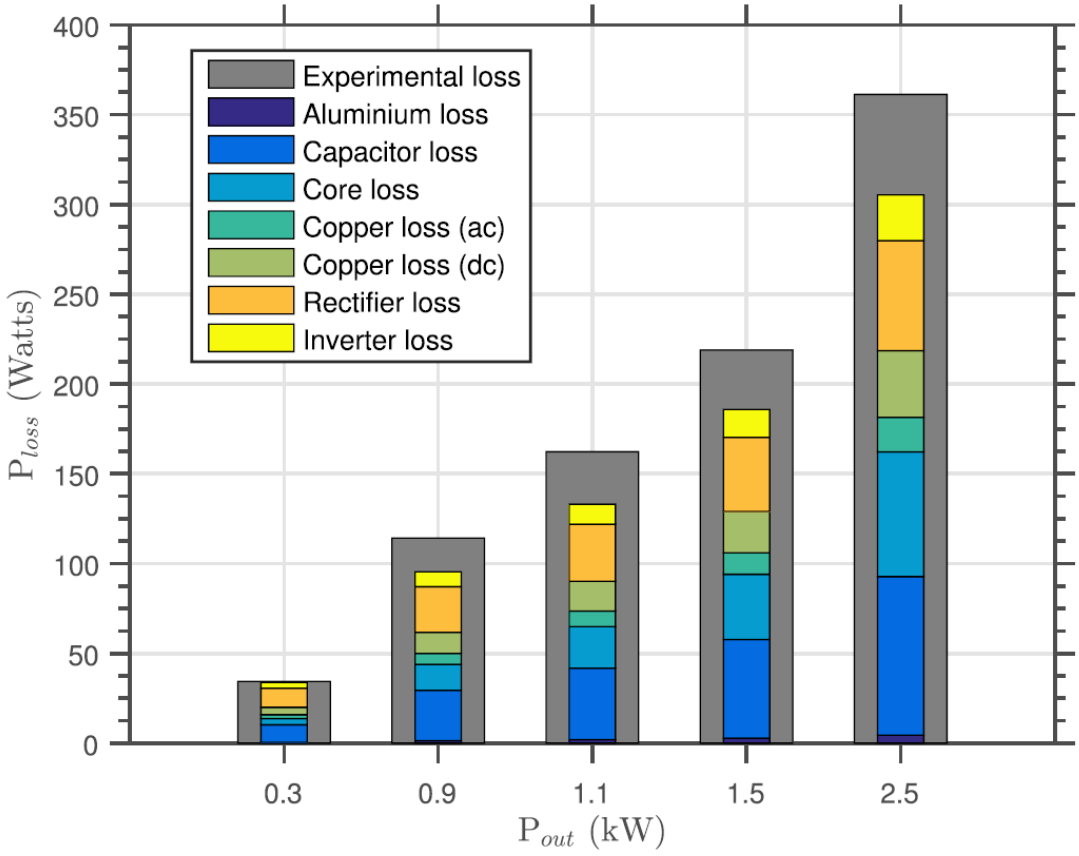


Fig. 53. Loss breakdown of a 2.5 kW system [75]

Given the facts above, if higher frequency design is possible for the WPT system, smaller capacitance is required for the compensation capacitors in IPT systems. At even higher frequency in MHz, the parasitic capacitance originated from windings could be substituted as the compensation. No lumped capacitor is needed anymore, and the thermal stress on capacitors is greatly relieved due to the distributed capacitance on copper windings.

2.3 Summary

Given the challenges, it is obvious that the EV WPT charger system performance is directly related to the coil design. Frequencies ranging from several kilohertz to hundreds of kilohertz have been adopted for many IPT EV charger prototypes from both industrial and academic designs, but high frequency design is seldom discussed in detail.

Based on the reviewed results from the previous section, higher frequency design could be beneficial for several aspects. By pushing the switching frequency higher, the quality factor of coils can be improved for a higher system efficiency. Lower coupling can be tolerated at higher frequency, making a compact coupler design with less Litz windings and ferrites possible. Since smaller external capacitors are needed at higher resonant frequency, the overall volume of passive component is smaller and system power density can be further increased. Also, at MHz frequency, self-resonant coils can be employed with no external capacitor needed anymore. The fringing magnetic field at a given horizontal distance to the coil will decrease compared with large coil at kHz range, which could potentially relieve the burden of shielding components. Of course, there are two major challenges for high frequency high power WPT system, including high frequency inverter

design and high *Q* coil design. Considering the recent development of GaN based switches which are capable of high switching speed, the main obstacle that remains is to have a more advanced coil design that can maintain a high quality factor at high frequency.

CHAPTER 3. PROPOSED MULTI-LAYER NON-UNIFORM SELF-RESONANT COIL STRUCTURE

3.1 Candidate Structures Suitable for High Frequency Coil Design

In this section, winding materials and coil structure are discussed separately based on the review results to help identify the potential candidates for a high frequency, high quality factor coil design.

3.1.1 Winding Structure: Litz Wire vs Copper Foil

For any alternating current conducted through the wire, the associated time-varying magnetic field will self-induce an electric field inside the conductor. It generates a current which counteracts the original excitation current in the center of conductor. The resulting redistributed current density is described by the skin depth,

$$\delta = \sqrt{\frac{\rho_c}{\pi \mu_0 f}} \tag{11}$$

which defines as the distance from the outer boundary to where the current density falls to $1/e$ of the maximum [85]. The μ_0 is the magnetic constant, ρ_c is the resistivity of the conductor, and f is the frequency of current. The non-uniform current distribution causes extra loss on the conductor and is termed as skin effect loss (including DC losses). Similarly, the time-varying magnetic field could also induce eddy current in adjacent conductor, and such loss is called proximity effect loss. Litz wire consists of multiple individually insulated strands, and each strand is manufactured to be thinner than the skin depth. In this way, the overall conducting area is used more efficiently, relieving the skin effect loss. At the same time, the strands are twisted in such way that each strand shares

the equal occupation of each position in the wire bundle, and proximity effect loss among strands can be strongly reduced.

However, there are certain limitations on using litz for high frequency application. The thinnest strand diameter is limited, as shown in Fig. 55. Considering its relatively expensive price for Litz wire with high gauge number for strand, it is not feasible for strand diameters below 50 μm. In addition, its porosity structure impedes a good thermal conduction between strands, which requires much more design effort for heat dissipation. To avoid undesired tradeoff between loss and cost, it is seldom used at MHz range.

Another type of winding structure is made of copper foil with thickness in dozens of micrometers. Compared with the Litz wire, it can be manufactured with much reduced price without complicated stranded structure. However, the disadvantages include the increased winding capacitance and the risk of an orthogonal flux. When the foil conductor is exposed to a flux orthogonal to the foil plane, the current will be concentrated at the ends of the foil. In Fig. 56, when the copper foil is not enclosed by any magnetic material, there exists orthogonal flux on the foil plane, making the current density not constant along the width. Comparing with the solid wire of same total cross-section area, the winding loss of foil conductor increases substantially. To substitute the expensive litz wire with foil conductors, the winding and flux distribution should be designed carefully.

Foil conductors are advantageous over the Litz wire when designing at MHz frequency range for a self-resonant coil. With the much large surface area, a large parasitic capacitance can be generated between foil plates as the compensation networks, which helps improve the system power density.

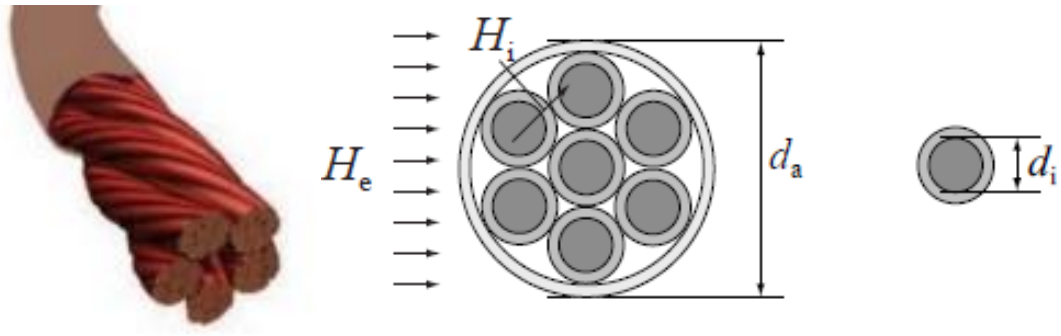


Fig. 54. Litz wire structure

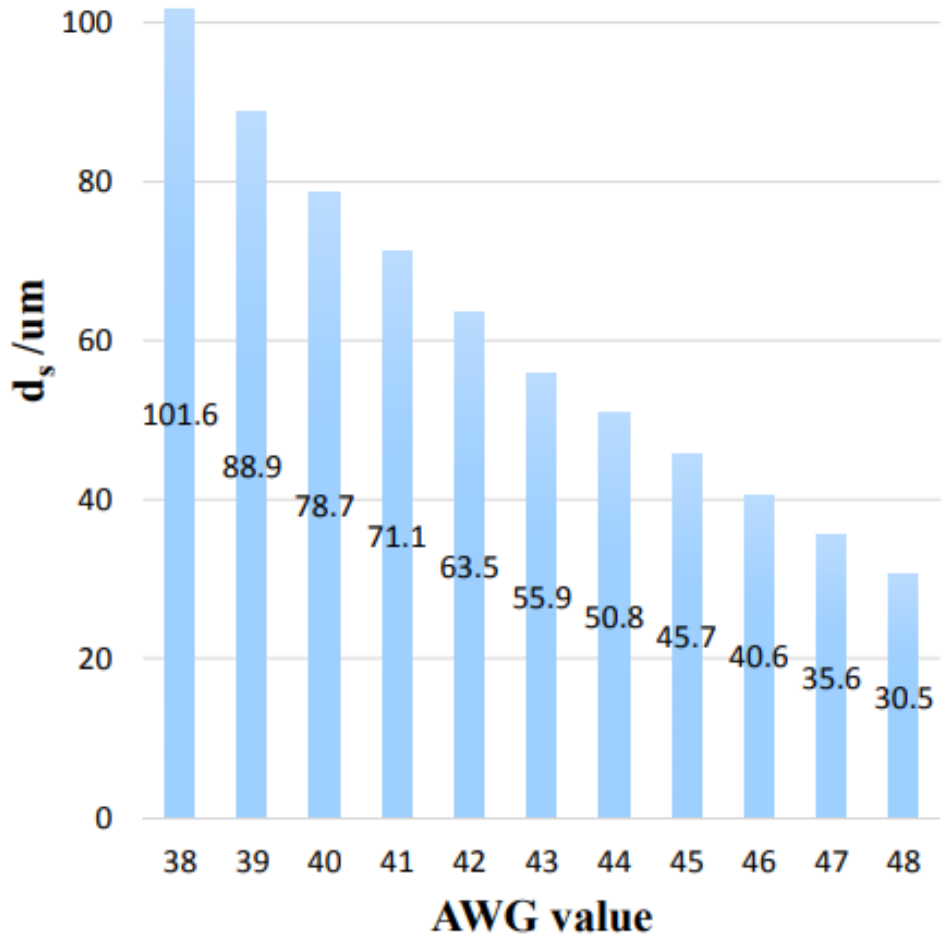


Fig. 55. Diameter of different AWG value for Litz wire

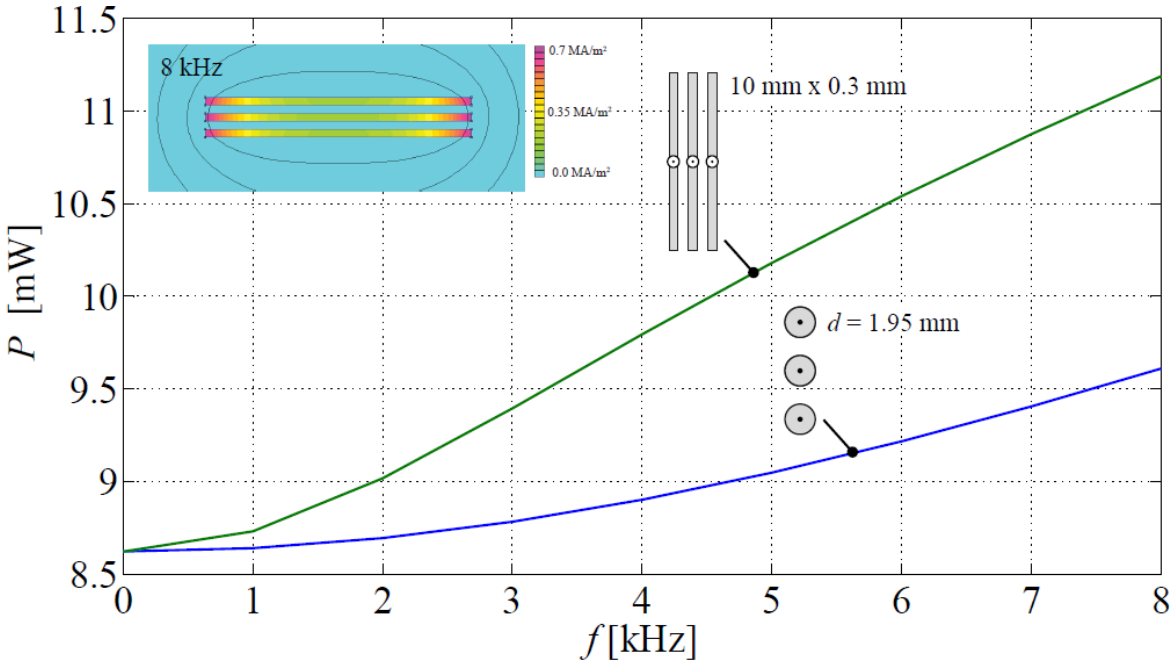


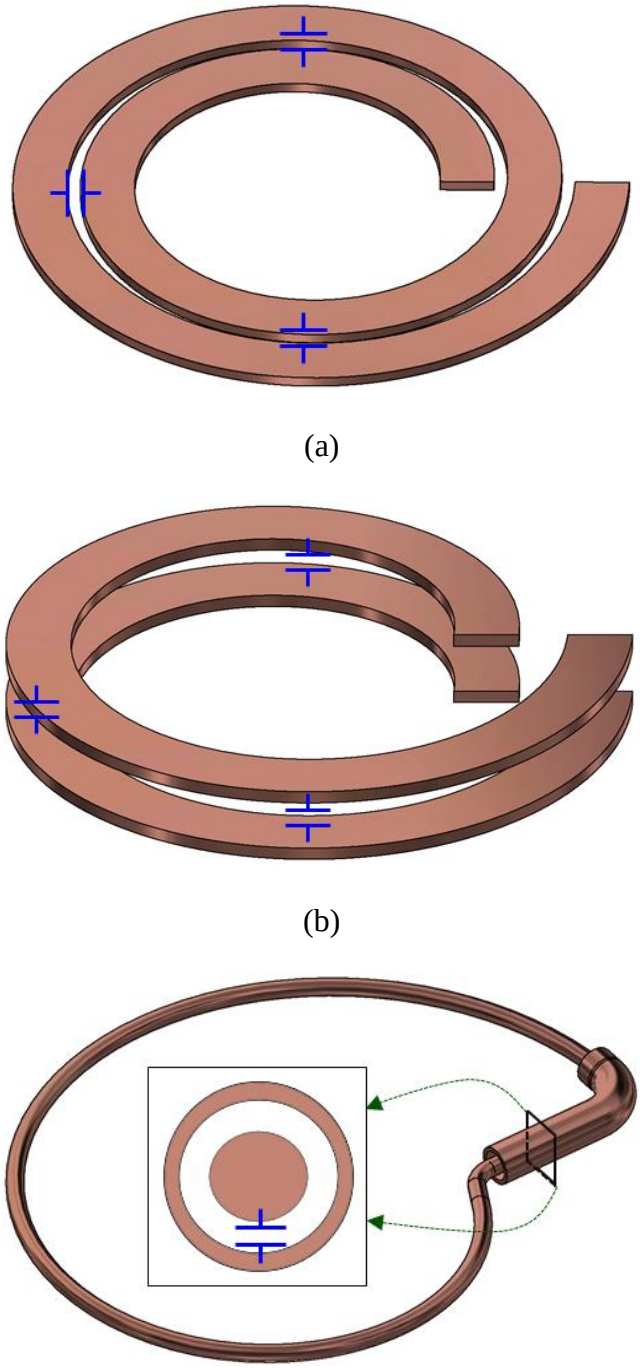
Fig. 56. High eddy current loss in foil conductor with orthogonal flux [85]

3.1.2 Review on Self-resonant Coil Structure

Coil design plays a critical role for any high efficiency, high power density, low cost, and robust WPT system. Among many WPT coil structures, the self-resonant (SR) coil has many advantages for MHz-range applications.

Based on the parasitic capacitance used for resonance, SR coils are classified into several types, including parasitic capacitance from adjacent turns [86]-[87], from parallel-plate-shaped coils [88]-[92], and from other coaxial capacitors on the turn itself with complex structures [93]. The concept diagram based on different forms of capacitance generation is shown in Fig. 57. Alternatively, SR coils are classified as series or parallel resonant types based on the *L*-*C* connection in their equivalent circuits.

The coil in [86] uses an open bifilar coil consisting of two conductors wound in parallel. As shown in Fig. 58, the terminals *b* and *c* are kept open, and series self-resonance is formed by the parasitic capacitance between two adjacent solenoid windings. The structure size is inevitably large, and extra isolation space will be needed for any high voltage application. To purposely increase the amount of generated parasitic capacitance, coils made of thin foil copper are applied in [87]-[92] instead of round wire. The coil of [87] has series-connected copper layers at both the top and bottom of a PCB inductor. Together with the parasitic capacitance between adjacent turns, PCB windings form a parallel resonant network as shown in Fig. 59. Capacitance is formed between the overlapped copper plate areas in [88]-[92]. The single-turn structure of [88] in Fig. 60 results in a low inductance value which may result in large secondary side current for a certain power rating. Three types of series resonant SR coils using copper plate capacitance, with different number of layers, are presented in [89]-[91]. In [89] multiple layers are paralleled with good current



(a)

(b)

(c)

Fig. 57. SR coil classification based on the capacitance generation source (a) adjacent turns (b) parallel plates (c) coaxial capacitance on turns

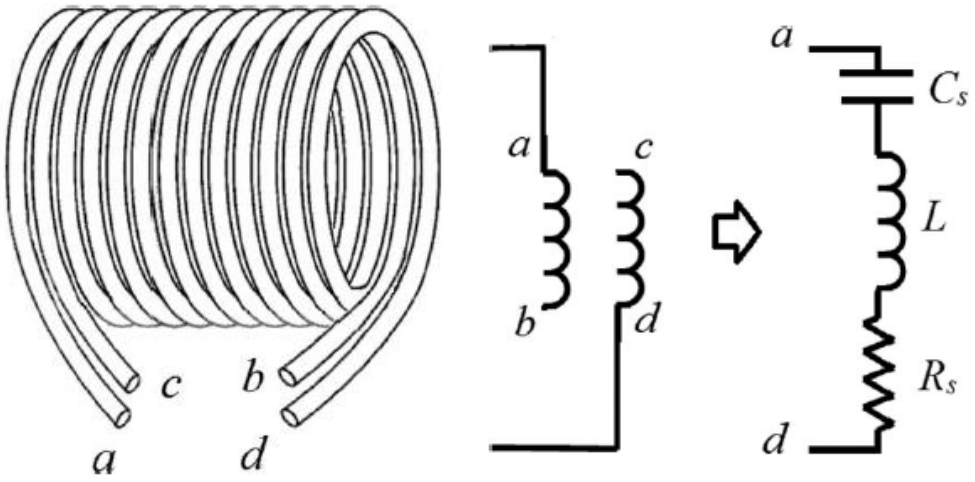


Fig. 58. Open bifilar coil with two conductors wound in parallel [86]

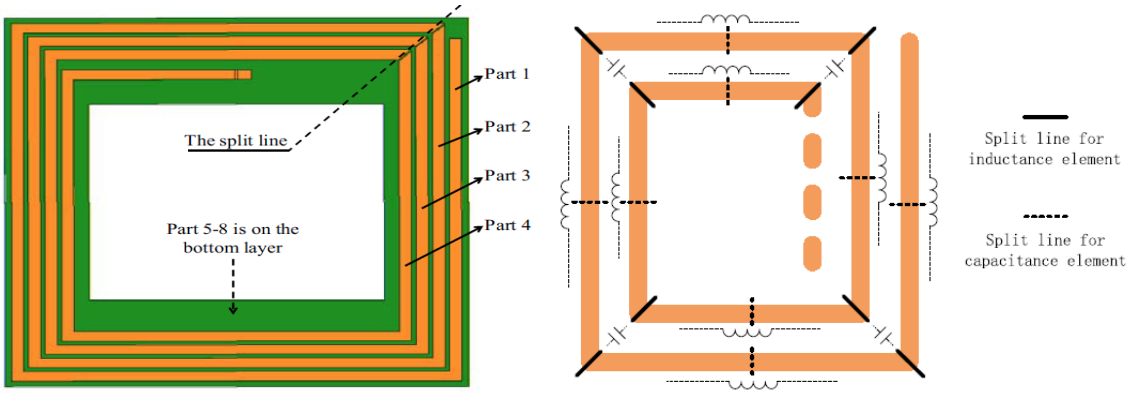


Fig. 59. PCB windings with parasitic capacitance between adjacent turns [87]

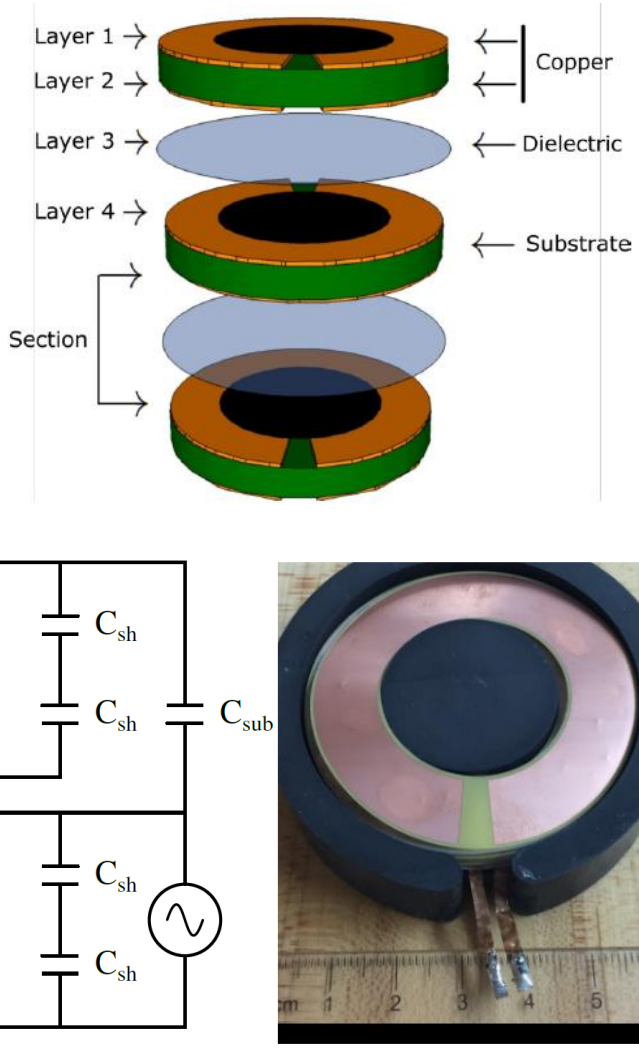


Fig. 60. Multi-layer C-shape coil self-resonant coil with copper foil [88]

sharing, which is superior to the case in [90]. However, the designed inductance in [90] is much larger due to the multi-turn spiral structure in Fig. 62. [91] is only designed in a CMOS process for less than 1 W output and the coil structure is shown in Fig. 63. Reference [92] increases the number of PCB winding layers to further increase the parasitic capacitance between layers, and the resulting multi-layer PCB boards in Fig. 64 has a much-reduced resonant frequency at 100 kHz to accommodate easy power stage design. The achieved quality factor of the coil is low, and the system efficiency is only 65% at 67 W output. In addition to utilizing the parasitic capacitance between the winding turns, [93] creates the capacitance by adding a hollow cylinder around the winding to form coaxial-like capacitor. The structure is complicated, with even larger footprint than a typical solenoid as shown in Fig. 65.

Of all the self-resonant coils in [86]-[93], only the structure in [88] reaches 1 kW output. Fig. 60 presents its structure, where the capacitance is formed between the overlapped copper plate areas. Multiple sections are stacked together, each of which is two C-shaped copper conductors with opposing orientation that are separated by a low-loss dielectric material circular plate. Within each section, current in a C-shape conductor must flow through a pair of overlapping capacitors due to non-overlapping area, forming a parallel self-resonant circuit. Since all sections are stacked up closely, strong inductive coupling exists in each section, and the source current will be shared among all the sections, which creates the total equivalent capacitance in parallel. To avoid any high dielectric loss between sections, the two adjacent C-shape copper layers are oriented with the same direction to make sure no strong electric field will be generated, as shown in layer 1 and layer 2 in Fig. 60. To increase the current capability, hundreds of layers are paralleled

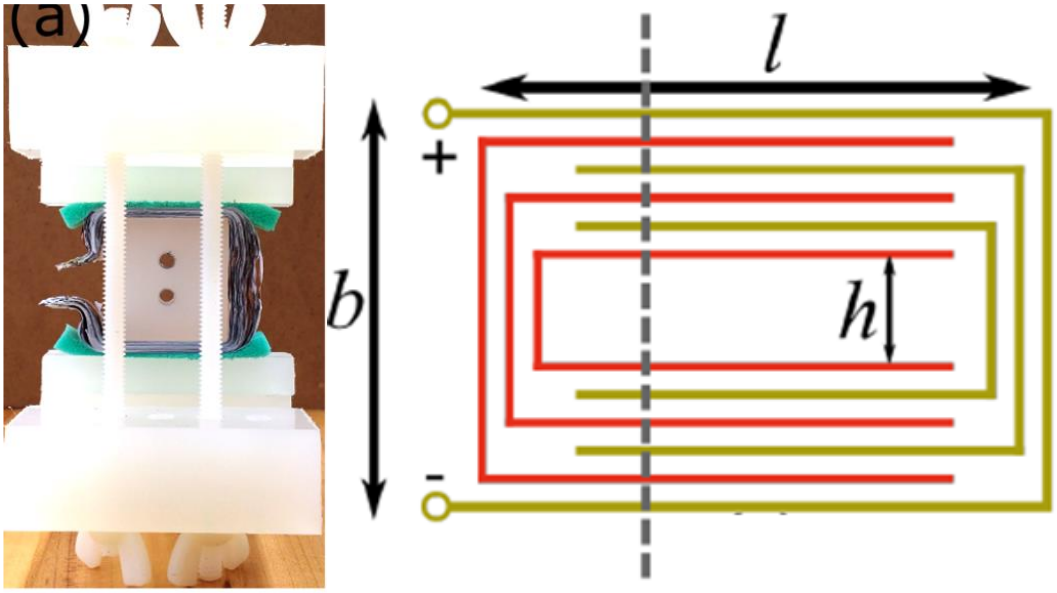


Fig. 61. Multi-layer series-resonator with copper foil [89]

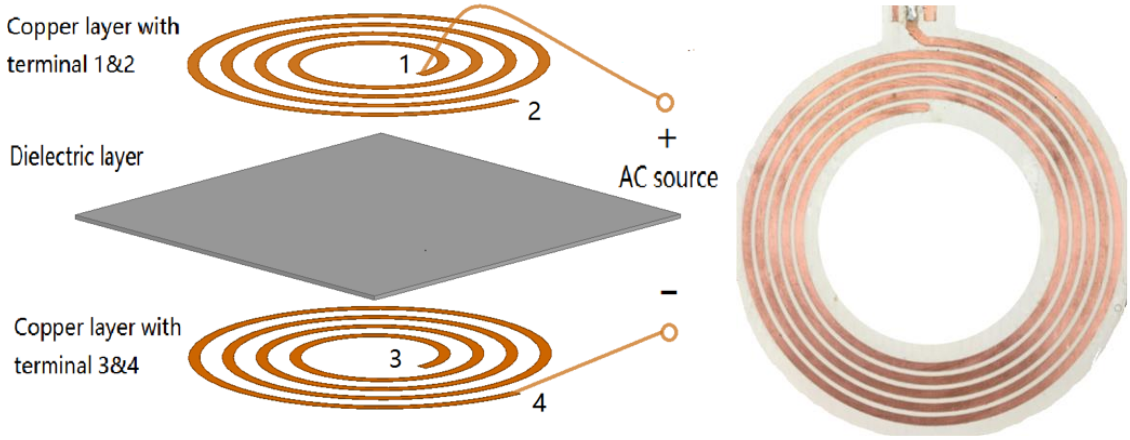


Fig. 62. Two-layer multi-turn series self-resonant coil [90]

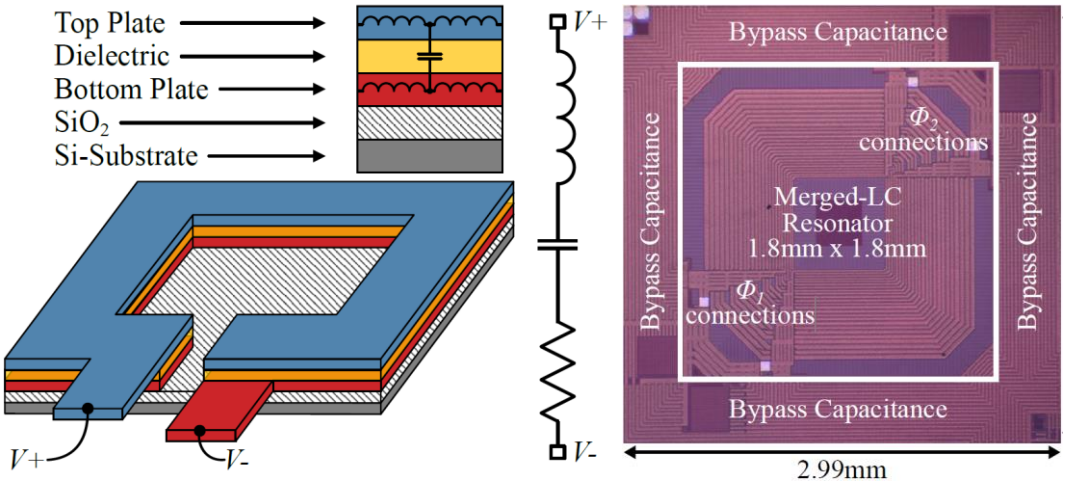


Fig. 63. Single-turn LC resonator for CMOS process [91]

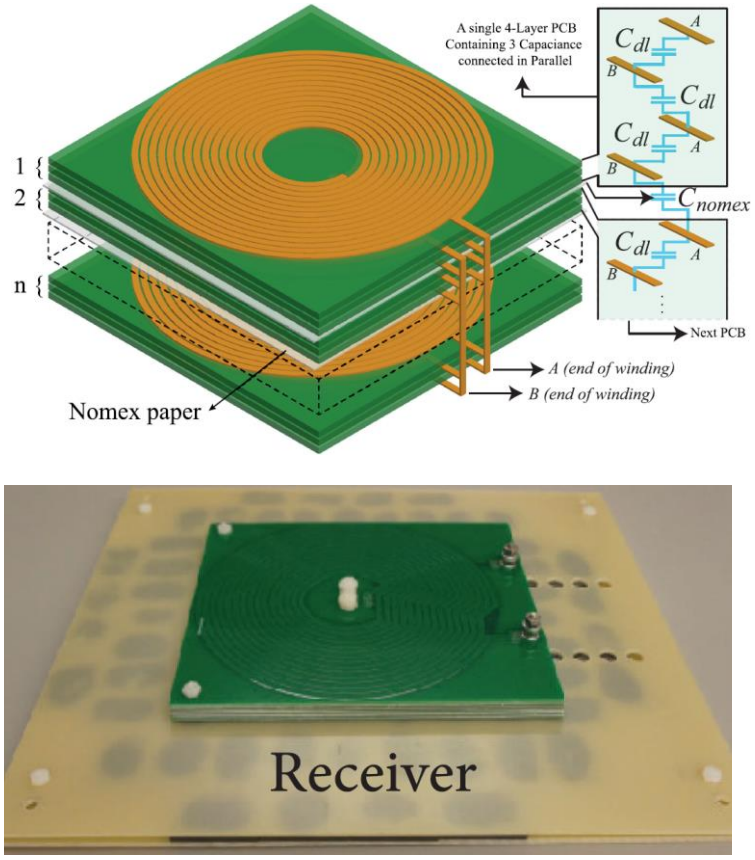


Fig. 64. Parallel connected multilayer PCB coils [92]

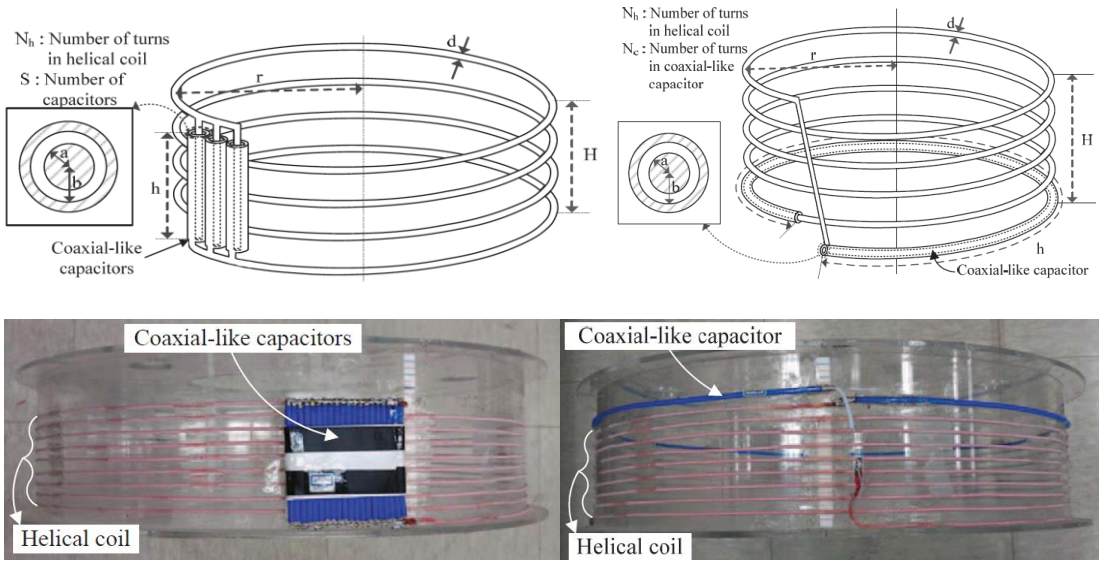


Fig. 65. Self-resonant coil with coaxial-like capacitors arranged vertically/horizontally with the helical coil [93]

together to share the current. Note that a ferrite core is placed directly adjacent to the windings in order to enforce perfectly paralleled flux to the foil layers.

Of all the self-resonant coils in [86]-[93], only the structure in [88] reaches 1 kW output. Fig. 60 presents its structure, where the capacitance is formed between the overlapped copper plate areas. Multiple sections are stacked together, each of which is two C-shaped copper conductors with opposing orientation that are separated by a low-loss dielectric material circular plate. Within each section, current in a C-shape conductor must flow through a pair of overlapping capacitors due to non-overlapping area, forming a parallel self-resonant circuit. Since all sections are stacked up closely, strong inductive coupling exists in each section, and the source current will be shared among all the sections, which creates the total equivalent capacitance in parallel. To avoid any high dielectric loss between sections, the two adjacent C-shape copper layers are oriented with the same direction to make sure no strong electric field will be generated, as shown in layer 1 and layer 2 in Fig. 60. To increase the current capability, hundreds of layers are paralleled together to share the current. Note that a ferrite core is placed directly adjacent to the windings in order to enforce perfectly paralleled flux to the foil layers.

However, the magnetic core has finite permeability, and there always will be an air gap between the magnetic core and the foil winding. At MHz range, the permeability will also deteriorate. In addition, the potential for higher power is limited by the single-turn inductance at nH level. Low inductance value, for example 167 nH inductance in [88], results in large driving current for a certain high power rating, which will decrease system efficiency and is not applicable for high switching frequency semiconductor devices. Also, to avoid short circuit and to drive the parallel resonant coils, one series L-C filter and one

choke inductor are required at the inverter side and rectifier side, respectively.

The critical specifications for the reviewed SR coils have been summarized in TABLE VIII, including their achieved inductance, capacitance, quality factor, resonant frequency, coil diameter, resonant type, and power delivery test.

Considering the practical facts above, there is no reported SR coil demonstration for high power EV charging in the reviewed literature due to the limited achievable inductance and quality factor at MHz.

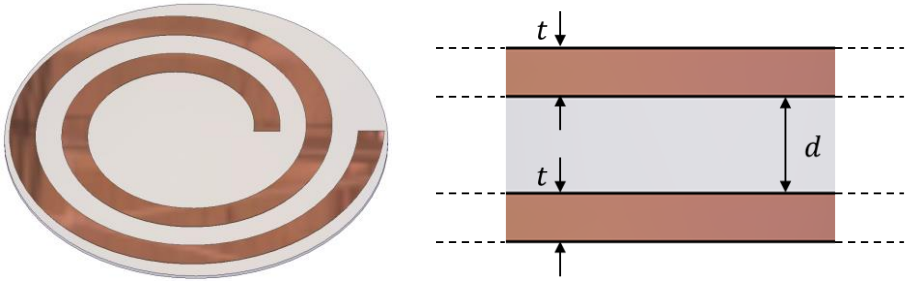
3.2 Benchmark Two-Layer SR Coil

Based on the multi-turn spiral SR coil structure in [90], a multi-layer non-uniform SR coil with series resonance is proposed in this chapter, improving the quality factor by distributing the source current among multiple layers while maintaining a multi-turn structure for large inductance. The proposed structure can be implemented with varying size and number of turns, making it applicable in WPT systems for consumer electronics and electric vehicles. Compared to the conventional SR coil designs, it has the advantages of high inductance, high quality factor, and exhibits a series *L*-*C* resonant characteristic.

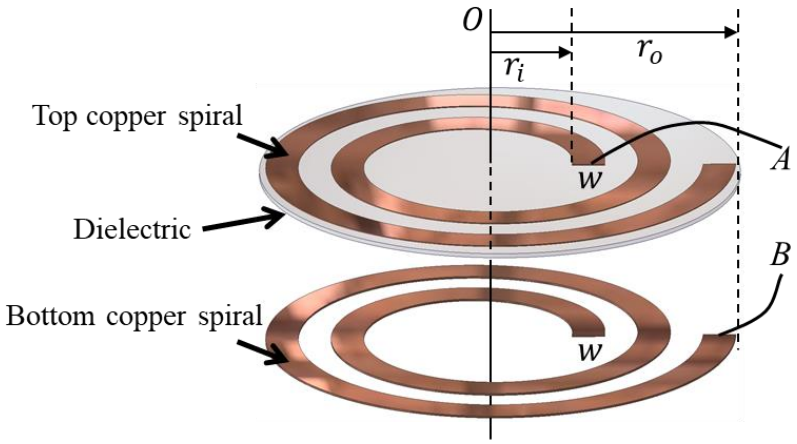
The coil structure and copper trace dimensions of the benchmark two-layer SR coil are shown in Fig. 66. The top layer and the bottom layer consist of two planar copper spirals with identical width, *w*, and trace length, l_0. The two spirals are separated by a dielectric material of thickness *d*. A parallel plate capacitor is formed between the overlapped areas of the copper traces on the top and bottom layers. The structure forms a series *L*-*C* resonant network between terminals *A* and *B*. When biased by an external ac source, current flows

TABLE VIII. State-of-the-art coil specifications

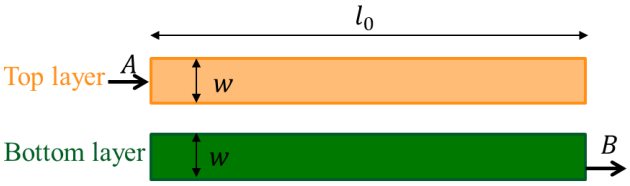
	L [μH]	*C* [nF]	*Q*	*f* [MHz]	*D* [mm]	Series/Parallel resonant	*P* [W]
UST	68.7	0.171	557	1.41	502	P	NA
UST	80.8	0.158	583	1.37	502	P	NA
UTPR	30	1.32	33	0.802	150	S	NA
THU	NA	NA	412	4.03	300	P	150
Stanford	0.167	3.32	708	6.78	66	P	1000
Dartmouth	0.138	2.54	835	8.51	46	P	NA
Dartmouth	0.131	3.24	838	7.73	46	S	NA
UTK	4.49	0.185	134	5.52	100	S	10
Dartmouth	0.008	1.7	2.7	47.5	1.8	S	0.47
Coventry	129	20	NA	0.1	230	P	67



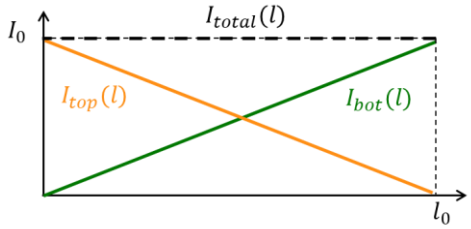
(a) (b)



(c)



(d)



(e)

Fig. 66. Two-layer SR coil structure (a) 3D view (b) side view (c) exploded 3D view (d) top view of unfurled copper traces for top and bottom layers (e) current distribution along each copper trace

through the length of the spiral, gradually transferring between layers in the form of displacement current distributed over the length of the trace.

Due to the uniform copper trace width, the capacitance per unit length is constant over the length of the spiral. Thus, the current in the top spiral trace decreases linearly along its length as it transfers to the bottom spiral trace. Consequently, current on the bottom layer will be increasing at the same rate. At any point along the length of the spiral, the sum of the currents in two layers is equal to the source current I_0, as shown in Fig. 66(e).

As in a conventional spiral coil, the copper resistance can be reduced, thereby increasing the quality factor of the coil, by increasing the copper width *w*. However, for this two-layer coil structure, the trace width also determines the interlayer resonant capacitance, causing a reduction in resonant frequency as the trace width is increased. The maximum copper width is also limited by the coil diameter and number of turns needed to achieve a designed inductance value. As shown in Fig. 67, any increase in copper width will shift the coil resonant frequency, and the maximum copper width is limited with given coil pad size.

Therefore, the achievable quality factor for a two-layer coil is inherently restricted by its self-resonant structure since the available copper trace area for each layer is always limited.

3.3 Multi-layer Non-uniform SR Coil

To increase the copper area while maintaining a designed resonant frequency, a multi-layer non-uniform SR coil is proposed. The structure of a three-layer case is shown in Fig. 68. Three layers of copper spiral traces are stacked vertically, with two equal-thickness layers of dielectric material sandwiched between. Similar to the two-layer case, the current

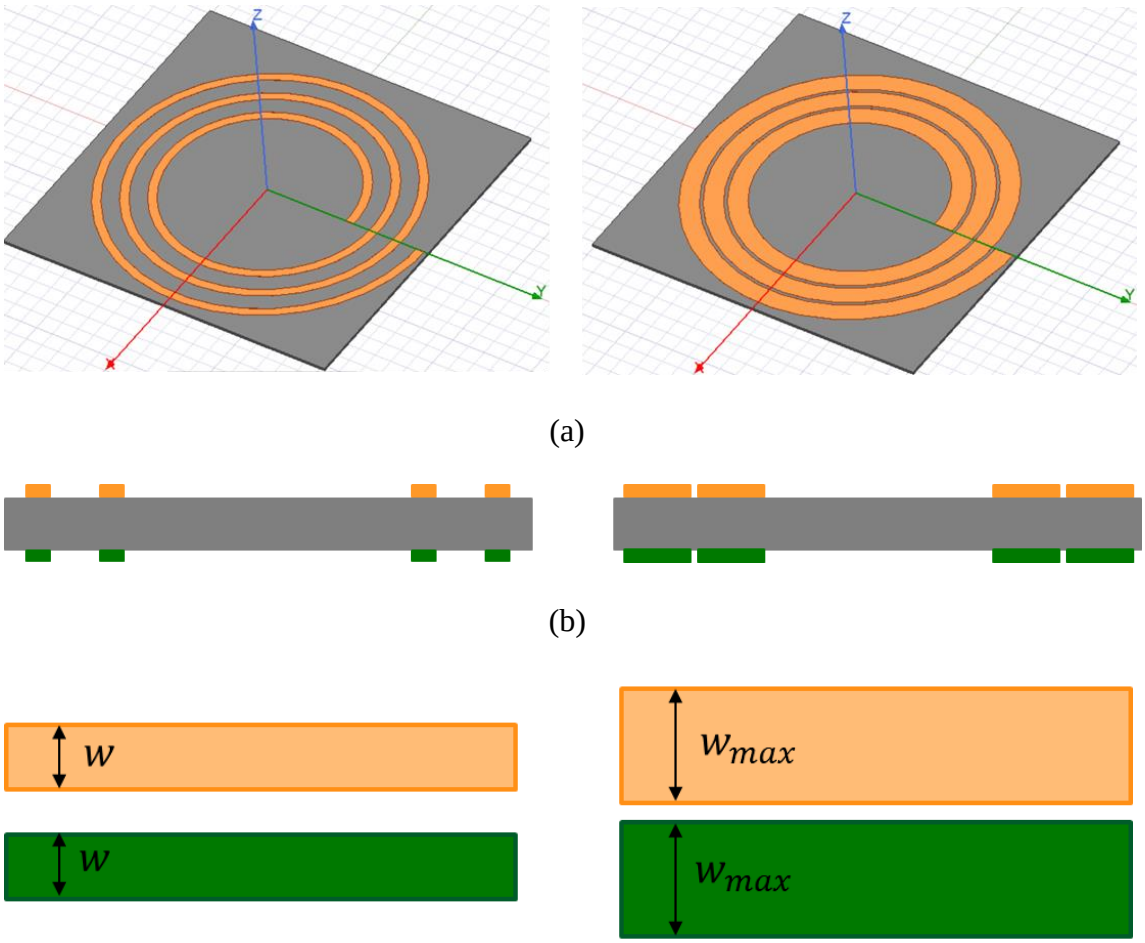


Fig. 67. Two cases of two-layer SR coil comparison with smaller copper width on the left and maximum copper width on the right: (a) 3D view; (b) side view; (c) top view of unfurled copper traces for top and bottom layers

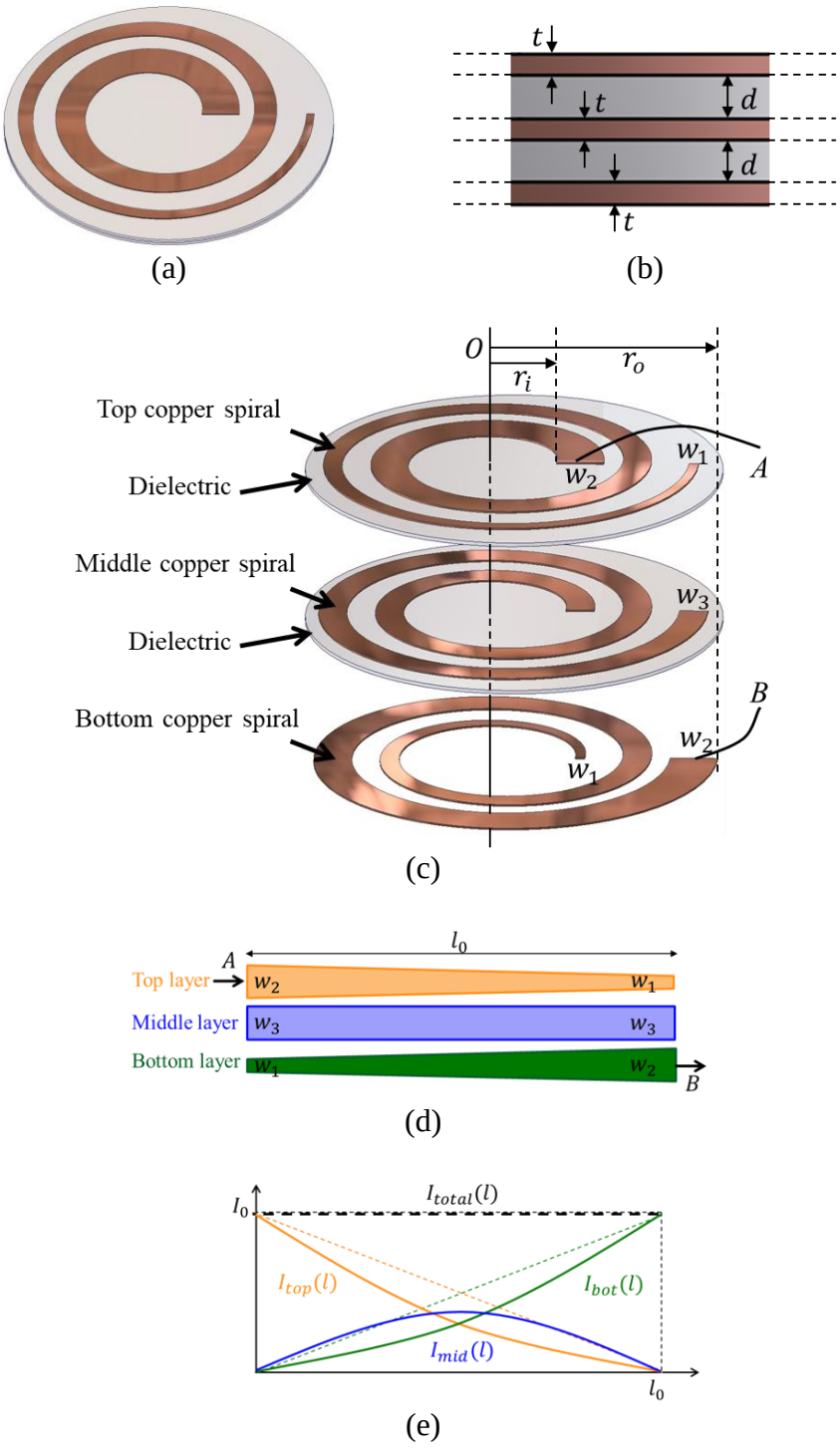


Fig. 68. Three-layer non-uniform SR coil structure: (a) 3D view; (b) side view; (c) exploded 3D view; (d) top view of unfurled copper traces for top, middle, and bottom layers; (e) current distribution along each copper trace

will flow from terminal *A* on the top layer, to the terminal *B* on the bottom layer. However, as the current flows from terminal *A* to terminal *B*, it must gradually transition through both dielectric layers in series. Together with the inductance from the spiral coils, the three-layer coil still works as a series *L*-*C* resonant network.

The total current I_0 is now distributed over three layers of copper, allowing lower current density in the conductor and improved quality factor. To control the current density of each layer, the geometry of the traces is manipulated to have non-uniform width. As shown in Fig. 68(d), the width of the top layer is linearly decreased from w_2 to w_1, while the bottom layer width is linearly increased from w_1 to w_2. The width of the middle layer is a constant, w_3. Due to the non-uniform copper width, the capacitance per unit length formed between adjacent copper layers varies along the trace length l_0. This variable capacitance is used to control the impedance and thereby the current distribution between the three layers.

The current distribution achieved by the coil geometry of Fig. 68(d) is given in Fig. 68(e). The top layer current decreases exponentially along the spiral length, while the bottom layer current increases symmetrically. At any point in the spiral, the sum of the current in all three layers is constant. Varying the width profile of any trace will modify the current distribution. In the design of Fig. 68, the largest current among the three layers always flows in the copper trace with widest width, resulting in reduced current density and conduction loss.

3.4 Lumped Element Model Simulation

LTspice simulations are used to verify the relationship between the capacitance and

current distribution. The three-layer non-uniform coil is modeled using a lumped element model shown in Fig. 69 for a design resonant frequency of 1 MHz with L = 20 μH, C = 1.27 nF. The spiral coil is divided into five segments, one per turn, for a design with a number of turns $N = 5$ and $L = N \cdot L_u$. Twelve capacitors model the per-turn interlayer capacitance with value varying from $0.5C_u$ to C_u representing the varying overlapped trace area. The total equivalent capacitance is,

$$C = \frac{1}{2}(1 + 0.9 + 0.8 + 0.7 + 0.6 + 0.5)C_u \tag{12}$$

The total impedance seen at the terminals is given in Fig. 70(a), verifying a series *L*-*C* characteristic behavior and resonance at 1 MHz as predicted. Fig. 70(b) shows the current in the lumped capacitors between the top and middle layer, and Fig. 70(c) shows the current in each segment of the middle layer. The current magnitude in each of the capacitors is exactly proportional to the capacitance value. Asymmetric capacitance between any two vertically-connected capacitors results in a current difference that flows through the middle layer. At any point in the model, the sum of currents in the three vertically-aligned inductances is equal to I_0.

A special case occurs when all three layers have uniform copper width, as illustrated in Fig. 71. In this case, the currents in any two vertically-connected capacitors in Fig. 69 are equal, leaving zero current in the middle copper layer.

The current distribution of this uniform copper width three-layer coil has been simulated in Fig. 73 with the lumped element model in Fig. 72. And to have the same resonant frequency at 1 MHz as before,

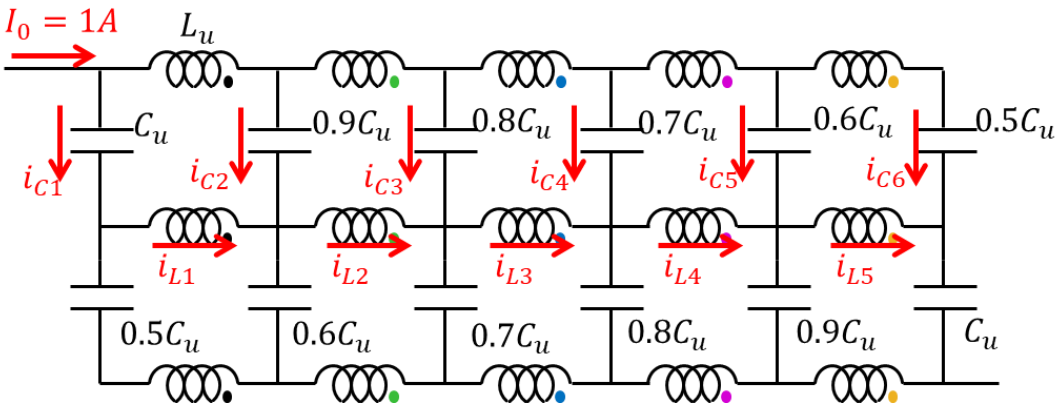
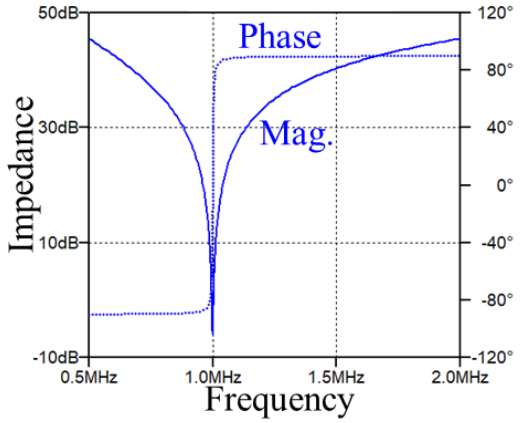
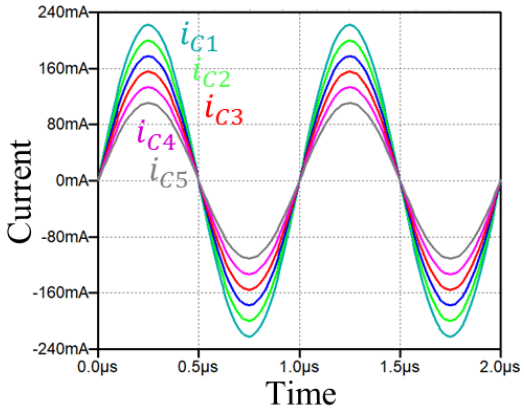


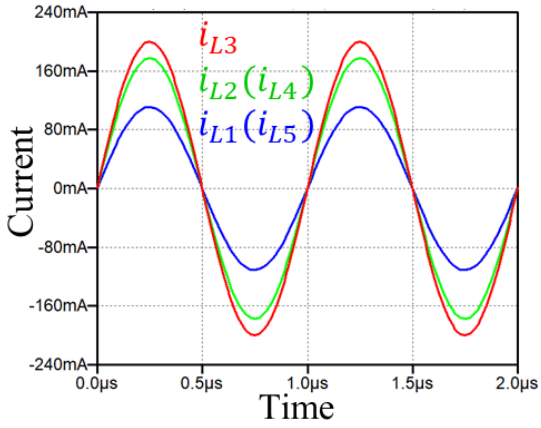
Fig. 69. Lumped element model for three-layer non-uniform SR coil



(a)



(b)



(c)

Fig. 70. LTspice simulation (a) impedance plot (b) current waveforms at distributed capacitors (c) current waveforms in the middle layer distributed inductors

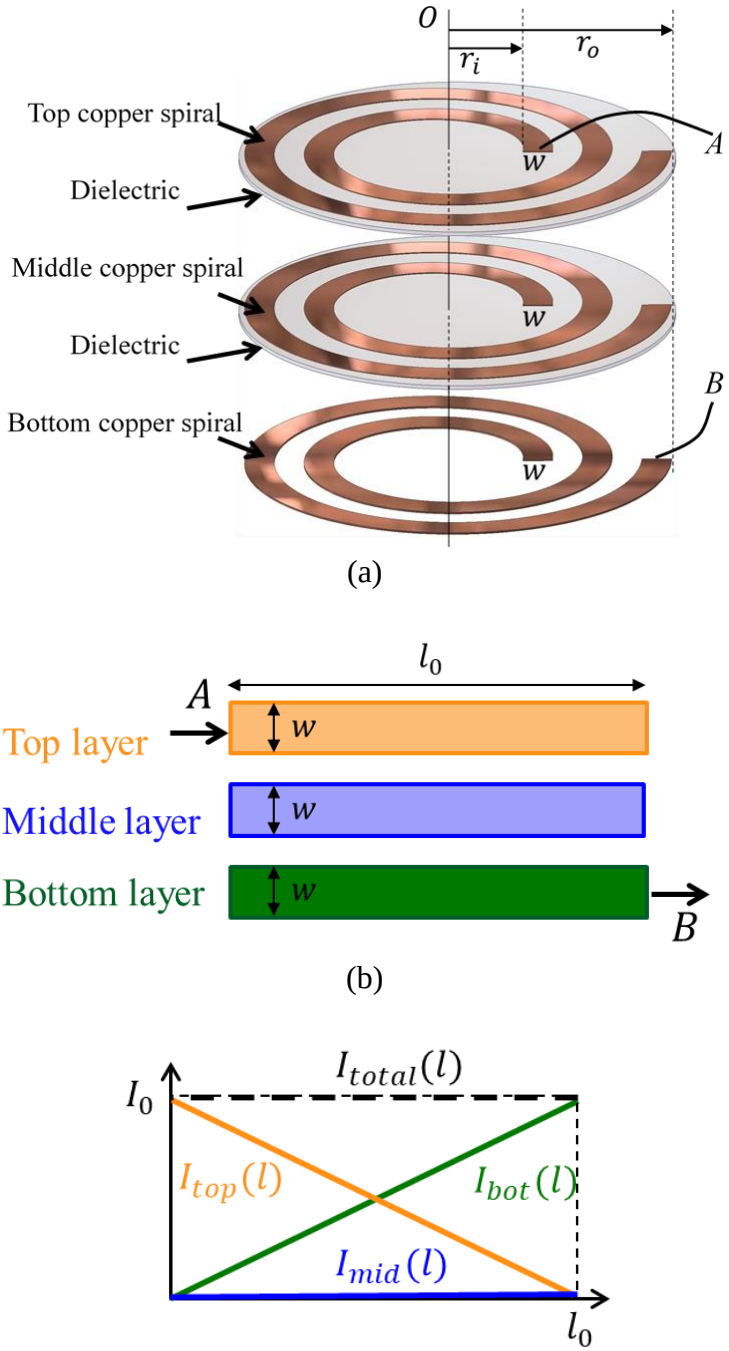


Fig. 71. Three-layer SR coil structure with uniform copper width: (a) exploded 3D view; (b) top view of unfurled copper traces for top, middle, and bottom layers; (c) current distribution along each copper trace

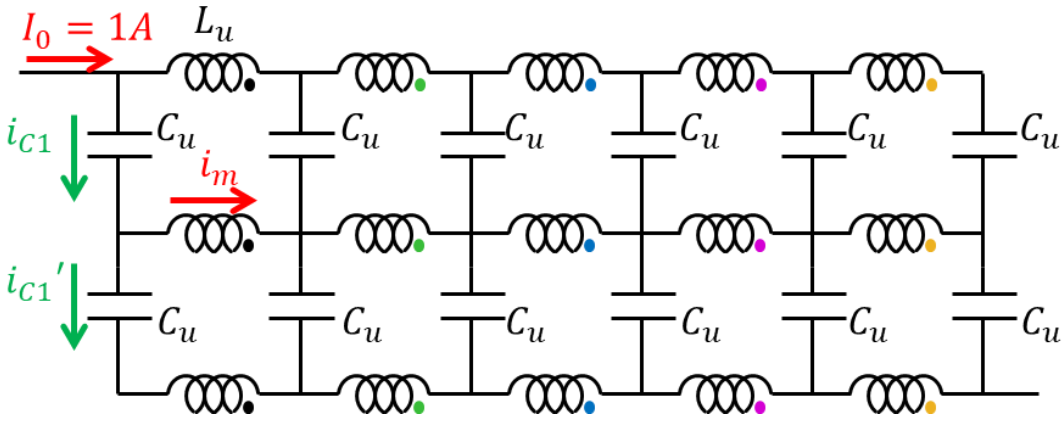


Fig. 72. Lumped element model for three-layer uniform SR coil

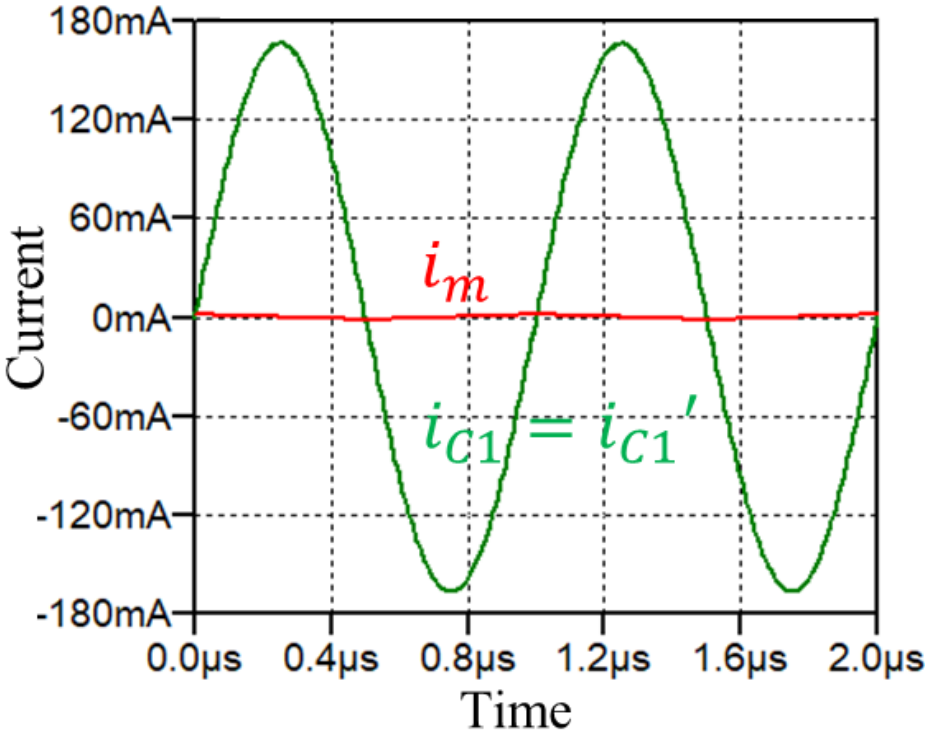


Fig. 73. LTspice simulation waveforms for three-layer uniform SR coil

$$C_u = \frac{C}{N+1} \times 2 = \frac{C}{3} \tag{13}$$

With the identical current $i_{C1} = i_{C1}$', the lumped inductors in the circuit model have no current flowing through.

This case does not fully take advantage of the three-layer structure but is instead similar to the conventional two-layer case, with significantly changed fringing electric field distribution in the dielectrics. This case will be compared in detail in the next chapter with the non-uniform copper width case after the coil *LC* modeling process.

3.4 Summary

In this chapter, possible SR coil candidates suitable for high frequency operation have been investigated. Different resonant structures are evaluated, and their key specifications are summarized. Of all SR coil candidates, they can either achieve high quality factor, high inductance, or compact structure, but none has successfully demonstrated the capability of high power delivery for EV application.

Inspired by the benchmark multi-turn two-layer SR coil made of copper foil with uniform width, this chapter proposed a multi-turn multi-layer SR coil made of copper foil with non-uniform width. Leveraging the varying copper width, current is shared among multiple copper layers, leading to a lower coil equivalent ESR and higher quality factor. The concept has been examined and validated by the lumped element model analysis and circuit simulation.

To have better understanding of its structure, the proposed coil is modeled in the next chapter, giving design guidance for high inductance, high quality factor target under certain

resonant frequency and coil geometry constraints.

CHAPTER 4. THREE-LAYER NON-UNIFORM SELF-RESONANT COIL MODELING AND DESIGN OPTIMIZATION

4.1 Inductance Modeling

The inductance of a single-layer, multi-turn spiral coil is given by [95]

$$L = \mu N^2 r_{avg}\left(\ln\frac{2.46}{r_{diff}} + 0.2{r_{diff}}^2\right) \tag{14}$$

where μ is the magnetic permeability and

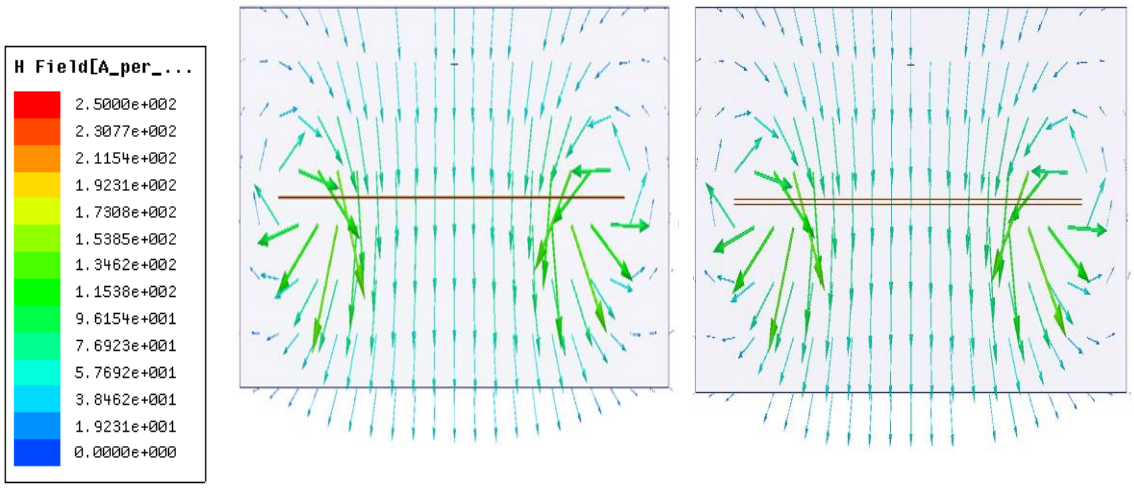
$$r_{avg} = \frac{r_o + r_{in}}{2} \tag{15}$$

$$r_{diff} = \frac{r_o - r_{in}}{r_o + r_{in}} \tag{16}$$

As was reported for the two-layer case, the inductance of the multi-layer spiral coil is well-approximated by the same empirical equation as long as the coil thickness is much smaller than its copper width [90]. Because of the multi-layer spiral structure, there is a vertical component to the current, but the vertical current flow is distributed over the entire surface area of the coil, whereas the circumferential current distributes only over the cross-sectional winding area. Therefore, the magnetic field resulting from the vertical component is relatively minor, and the component inductance is well-approximated by the field resulting from the circumferential flow, as shown in Fig. 74.

4.2 Capacitance Modeling

In the three-layer structure, the capacitance is generated by the parallel plate structure between adjacent copper layers. With unequal copper width, both the overlap area and the



(a) (b)

Fig. 74. H field distribution comparison of size radius and copper width (a) single layer spiral coil (b) multi-layer spiral coil [90]

fringing effect will contribute to the total capacitance value. The capacitance per unit length from overlapped area is,

$$C_0 = \varepsilon_0 \varepsilon_r \frac{w_0}{d} \tag{17}$$

where ε_r is the relative dielectric permittivity, w_0 is the overlapped copper width between the two layers, and d is the dielectric thickness, as depicted in Fig. 75.

The capacitance caused by the fringing field between two copper plates is more difficult to model, and there are many papers discussing the potential approaches of modeling. Reference [96] and [90] apply an analytic approximation with some empirical simplifications, but the range of validity is limited. Both Langton and Lin use conformal transformations to form a uniform field problem around the paralleled plates [97][98].

Compared to other methods, GM in [99] gives the most accurate result by using potential-theoretic method to describe the E field in the form of Fourier series expansion. Based on Fourier series expansion, the electric field is

$$\phi(x, y) = \sum_{n=1}^{\infty} A_n \sin(k_n y) e^{-k_n x} \tag{18}$$

A_n and k_n are constants determined by the boundary conditions for electric potential around the parallel plate. A symmetric boundary condition is assumed for simplification,

$$f(\xi) = \begin{cases} F_1(\xi): & -T \le \xi \le -d - t \\ -v_0: & -d - t \le \xi \le -d \\ \dfrac{v_0}{d}\xi: & -d \le \xi \le d \\ v_0: & d \le \xi \le d + t \\ F_2(\xi): & d + t \le \xi \le T \end{cases} \tag{19}$$

where $F_1(\xi)$ and $F_2(\xi)$ can be defined as either exponentially or linearly decreasing functions. The period is selected as $T = 1.4(d+t)$ based on trial-and-error process to find a

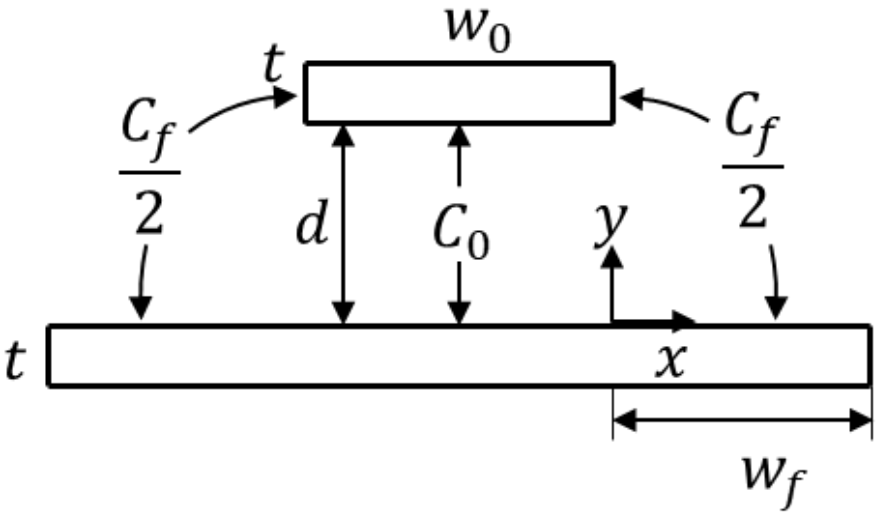


Fig. 75. Parallel plate capacitor with unequal width

proper boundary condition to precisely model the electric field, where *t* is the copper thickness.

A linear boundary condition is applied here:

$$F_1(x) = -v_0 \frac{(T+x)}{(T-d-t)} \tag{20}$$

$$F_2(x) = v_0 \frac{(T-x)}{(T-d-t)} \tag{21}$$

Under these boundary conditions, the Fourier series coefficients are

$$A_n = \frac{1}{T}\sum_{-T}^{T} f(\xi)\sin(k_n\xi)d\xi \tag{22}$$

$$k_n = \frac{n\pi}{T} \tag{23}$$

With the electric potential, the electric field is derived as,

$$E = -\nabla\phi \tag{24}$$

$$E = \sum_{n=1}^{\infty}[A_n k_n sin(k_n y)e^{-k_n x}\hat{x} - A_n k_n cos(k_n y)e^{-k_n x}\hat{y}] \tag{25}$$

For isotropic dielectric materials, the electric displacement field is

$$D = \varepsilon E \tag{26}$$

and at the conductor-dielectric boundary, the normal component of electric displacement field *D* has the same magnitude of surface charge density with opposite sign,

$$\rho_s = -D \tag{27}$$

Accordingly, the total electric charge is integrated along the surface,

$$Q = \sum_{n=1}^{\infty}\int_s \rho_{rs}dS = \sum_{n=1}^{\infty}\varepsilon_0\varepsilon_r A_n\left(1 - e^{-k_n(w_f+d)}\right) \tag{28}$$

and fringing field capacitance is

$$C_f = \frac{Q}{v_0} = 2\sum_{n=1}^{\infty} \varepsilon_0 \varepsilon_r \frac{A_n}{v_o}\left(1 - e^{-k_n(w_f+d)}\right) \tag{29}$$

where w_f is half of the width difference of two copper plates, and v_o is electric potential difference between two plates. The capacitances calculated in (17) and (29) together give the total capacitance per unit length,

$$C_{tot} = C_0 + C_f \tag{30}$$

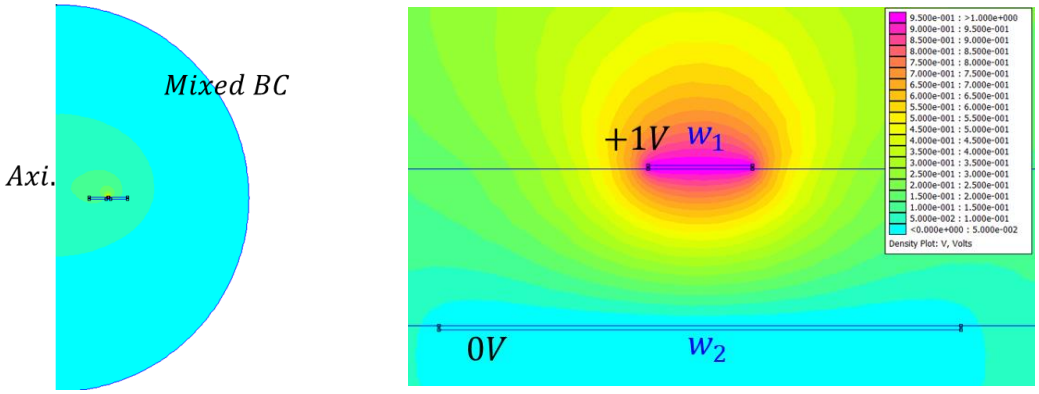
FEMM [100] is used to perform two-dimensional finite element analysis (FEA) to verify the effectiveness of different modeling approaches. The simulation setup of a parallel plate capacitor is shown in Fig. 76 and corresponding results are plotted in Fig. 77.

Keeping one plate width w_2 = 5 mm and changing the other, w_1, in the range of 1-5 mm, the fringing capacitance is dominant when the width ratio between two plates is large. Of all the modeling methods, GM gives the most accurate result for the fringing capacitance and is adopted, with less than 5% error when w_1>0.5 mm.

4.3 3D HFSS Simulation for Coil Current Distribution

A three-dimensional electromagnetic field simulation in HFSS is used to further validate the proposed structure and the *L*-*C* modeling result. TABLE IX gives the coil parameters for the simulation.

Based on the proposed capacitance model, the current distribution of designed coil example can be derived. The copper width for top layer, middle layer, and top layer (w_t, w_m and w_b) are defined as follows along the copper spiral trace,



(a) (b)

Fig. 76. Simulation setup in FEMM (a) boundary setup (b) parallel plate capacitor with voltage excitation

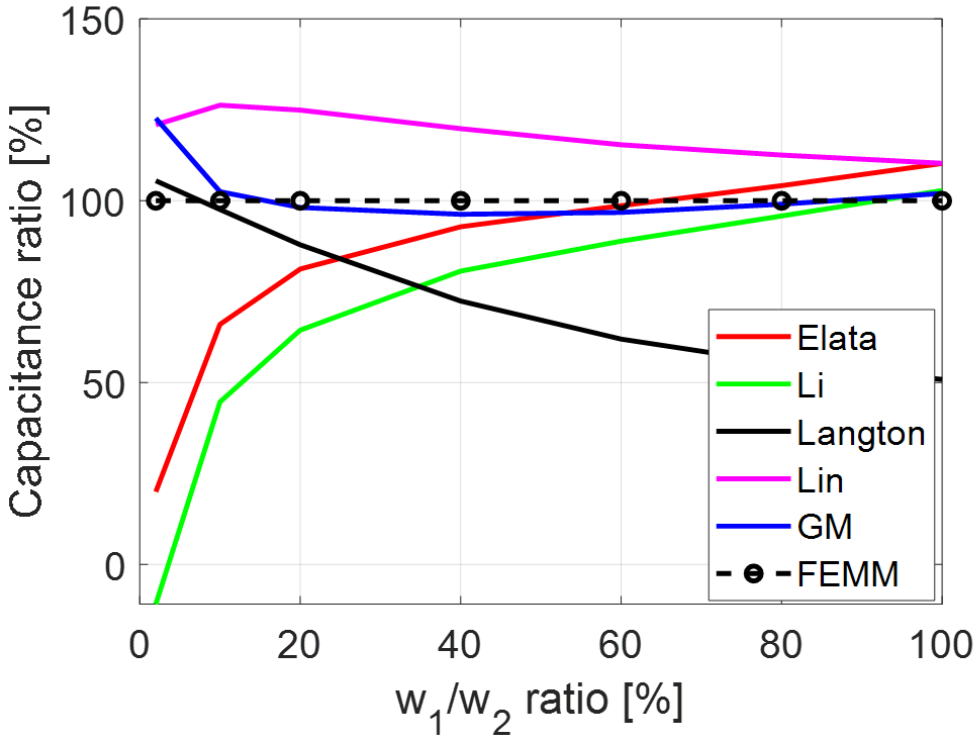


Fig. 77. Total capacitance ratio vs. copper width ratio, compared with FEMM simulation

TABLE IX. Coil Geometry Details for HFSS Simulation

Inductance L [μH]	6
Capacitance C [pF]	92
Resonant frequency f_0 [MHz]	6.78
Outer radius r_o [mm]	100
Inner radius r_i [mm]	61.93
Copper thickness t [oz]	1
Total dielectric thickness $2d$ [mm]	3.048
Turns N	5
w_1 [mm]	0.1
w_2 [mm]	4.9
w_3 [mm]	4.9

$$w_t(l) = w_1 - \frac{w_1 - w_2}{l_0}(l_0 - l) \tag{31}$$

$$w_m(l) = w_3 \tag{32}$$

$$w_b(l) = w_2 - \frac{w_2 - w_1}{l_0}(l_0 - l) \tag{33}$$

where the copper spiral total length at any layer is,

$$l_0 = \pi N(r_i + r_o) \tag{34}$$

With given copper width, the generated capacitance between any two adjacent layers is calculated with the proposed capacitance model,

$$C_{t-m}(l) = f(w_t(l), w_m(l)) \tag{35}$$

$$C_{m-b}(l) = f(w_m(l), w_b(l)) \tag{36}$$

Then, the current distribution in three layers is calculated based on the integral of capacitance along the trace. Essentially, the current transfer ratio is directly proportional to the capacitance value at a given position on the trace.

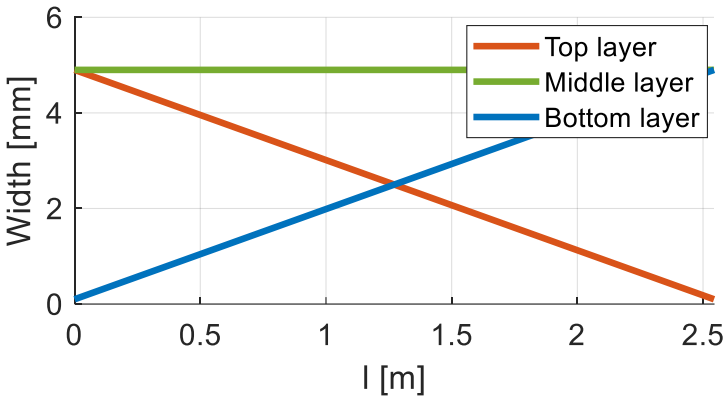
$$i_t(l) = I_0(1 - \frac{\int_0^l C_{t-m}(l)dl}{\int_0^{l_0} C_{t-m}(l)dl}) \tag{37}$$

$$i_m(l) = I_0 - i_t(l) - i_b(l) \tag{38}$$

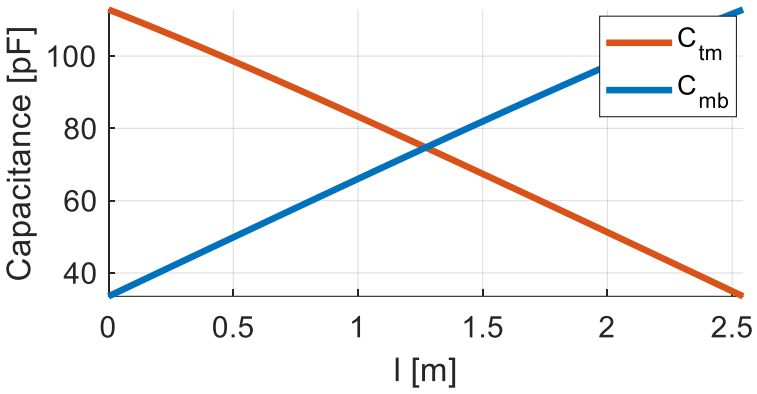
$$i_b(l) = I_0 \frac{\int_0^l C_{m-b}(l)dl}{\int_0^{l_0} C_{m-b}(l)dl} \tag{39}$$

The modeled copper width, capacitance, and current distribution along the copper trace for the coil design example are plotted in Fig. 78.

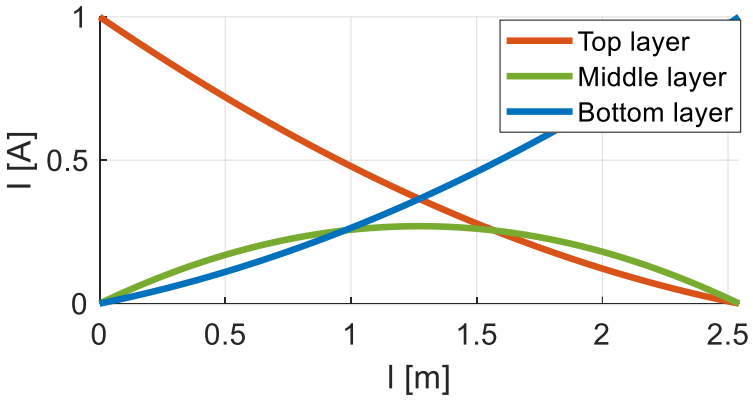
Fig. 79(a)-(b) provides the simulation model in HFSS, and Fig. 79(c) shows the current density of the three layers. Starting from the innermost turn on the top layer, the current is gradually transferred to the middle and bottom layers. The current density on the middle



(a)



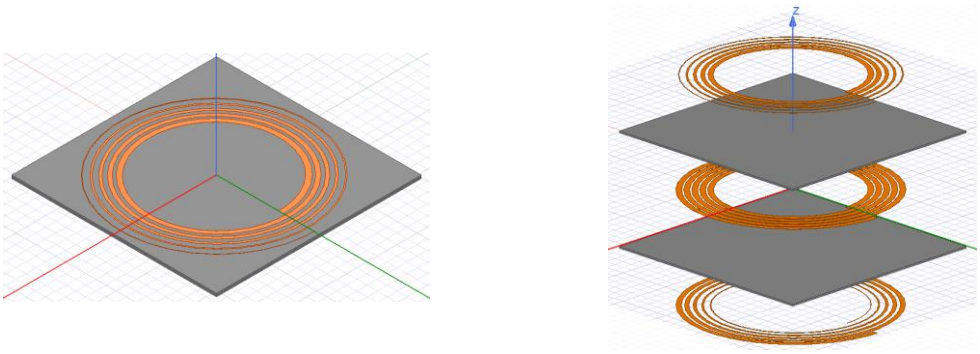
(b)



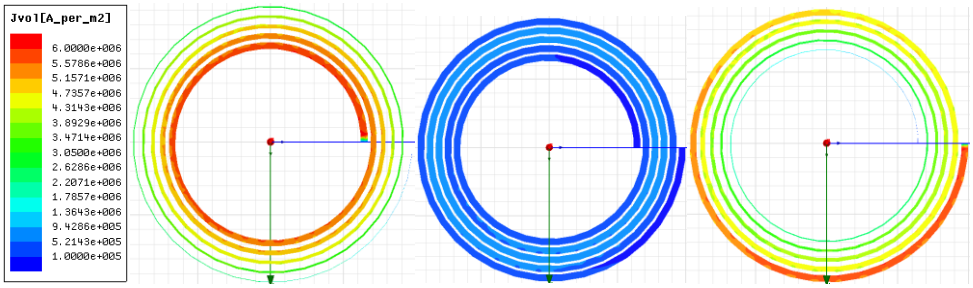
(c)

Fig. 78. Coil design example L = 6 µH, f_0 = 6.78 MHz (a) copper width (b) capacitance

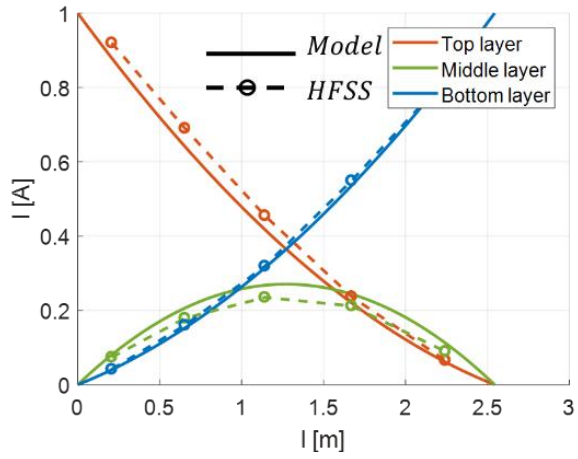
(c) current distribution



(a) (b)



(c)



(d)

Fig. 79. (a) HFSS model for coil (b) Exploded view of HFSS model (c) HFSS simulation for current density on three layers, top (left), middle (middle), and bottom (right) (d) Current distribution comparison based on model and HFSS simulation

layer reaches its peak value at the spiral trace midpoint, then drops to zero slowly, as expected from both analysis and lumped-element simulation. Fig. 79(d) gives a detailed comparison between the modeled and simulated current distribution. The current magnitude is integrated over the copper spiral intersection surface at selected points along the copper trace,

$$I_i = \iint (J_{vol} \cdot \vec{n}) ds \tag{40}$$

The model has good agreement with the modeling result within 10% error on average for all layers.

4.4 Effect of Fringing Capacitance in Three-layer Coil Design

The three-layer self-resonant coil gains additional benefit over a two-layer design due to the impact of the fringing capacitance, especially when the distance between copper layers is comparable to the dielectric material thickness in between.

Fig. 80 shows the ratio of fringing capacitance C_f to the total capacitance C_{tot} for varying dielectric thickness d in a parallel plate capacitor of equal width. When the width of the plates w is small and the distance d between them is large, the fringing field dominates the overall capacitance.

To better understand the impact from fringing capacitance, Fig. 81 compares the electric fields of a segment of two-layer and three-layer coils. The total dielectric thickness d and width w are identical for both cases. Neglecting fringing fields, the capacitance of both structures is the same.

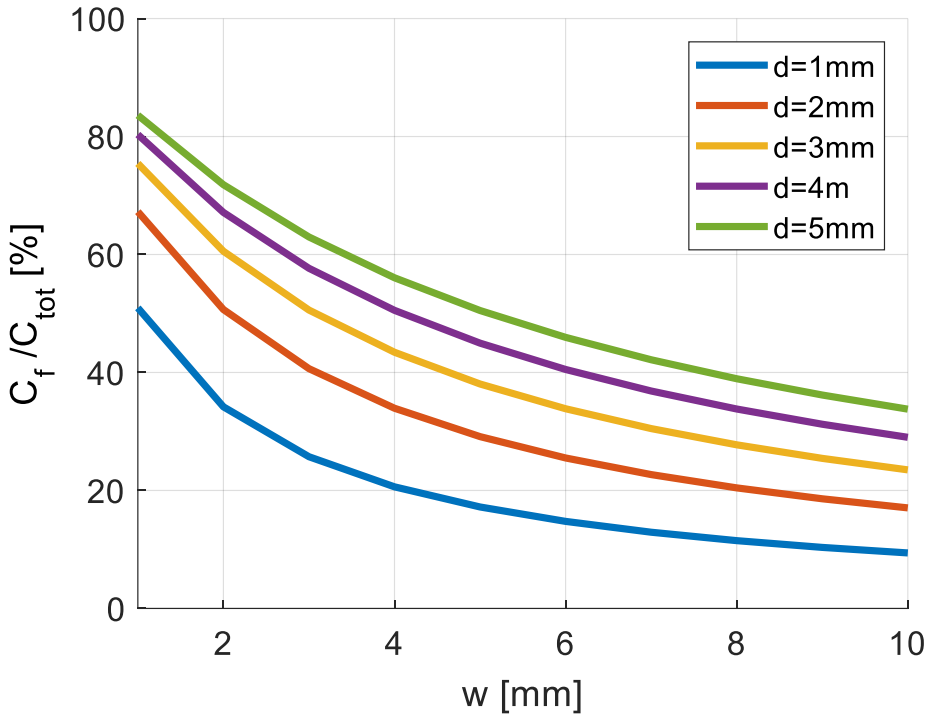
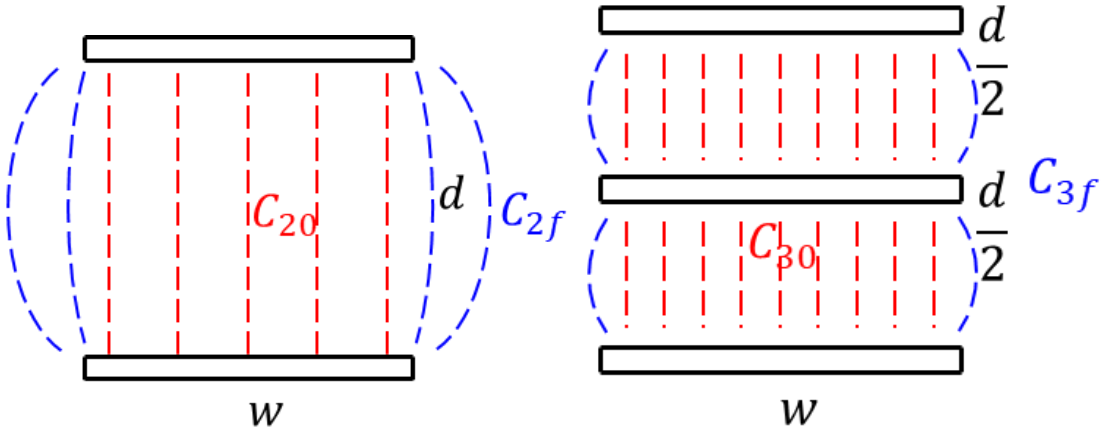


Fig. 80. Fringing capacitance to total capacitance ratio with different dielectric thickness for a parallel plate capacitor



(a) (b)

Fig. 81. Electric field of (a) two-layer capacitor; (b) three-layer capacitor

$$C_{20} = C_{30} \tag{41}$$

However, when fringing is considered, the three-layer structure exhibits a smaller capacitance due to the lower fringing field contributed by the smaller plate-to-plate distance.

$$C_{2f} > C_{3f} \tag{42}$$

$$C_2 = C_{20} + C_{2f} > C_3 = C_{30} + C_{3f} \tag{43}$$

In other words, if both structures are designed for the same target capacitance, wider plates will be needed in the three-layer structure.

This effect is detailed in Fig. 82 by examining the numerical capacitances C_2 and C_3 from the two structures of Fig. 81 when total thickness d is 3 mm. The closer distance between parallel plates in the three-layer case gives better confinement of the fringing field, making the total capacitance C_3 smaller than C_2. Fig. 82 also shows the ratio of trace widths required in the 3-layer and 2-layer cases to achieve the same target capacitance. For example, when the copper width w = 3 mm, the copper width of the three-layer case needs to be increased by 52% such that $C_3 = C_2$. This increase results in further conduction loss reduction in addition to the current sharing effect in the three-layer non-uniform SR coil. The benefit of the confined fringing field in a multi-layer coil is further quantified by quality factor comparison for optimized coil geometries later in this chapter.

4.5 FEMM Based Design Optimization for the Proposed Three-layer Coil

Based on the *L*-*C* modeling, the design of both inductance and capacitance values are coupled by the geometry of the coil and the properties of the dielectric material. The coil

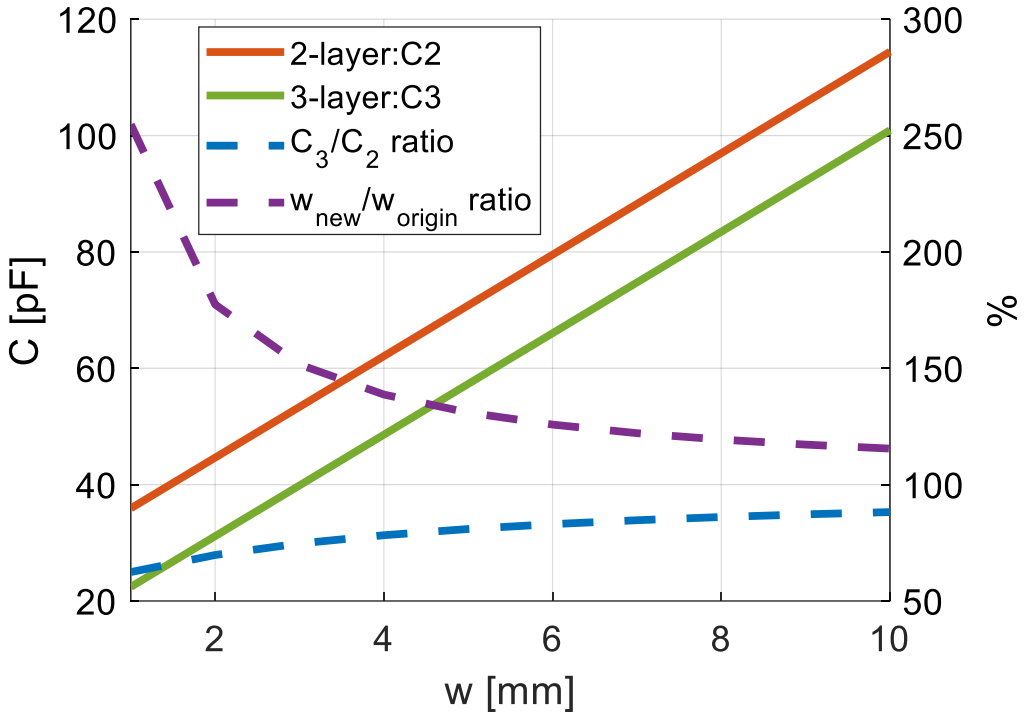


Fig. 82. Capacitance and copper width comparison of two-layer and three-layer coils

inner radius r_i, outer radius r_o and number of turns N determine the inductance value and also constrain the available trace width which determines the total capacitance.

With a fixed coil size, there is a single coil geometry which will exhibit the highest quality factor for any achievable pair of inductance and capacitance values of the self-resonant coil. Between these designs, selection of the optimal (L,C) pair requires consideration of the power stages and overall converter operation, which will be addressed in Chapter 5. Initially, the coil design space is narrowed by considering only the optimal quality factor designs for any (L,C) pair in this chapter.

To find coil designs with optimal quality factor, the coil resonant frequency f_0, inductance L, capacitance C, inner radius r_i, number of turns N, copper trace width w_1, w_2, and w_3, and dielectric material thickness d are swept to generate all feasible coil designs. The coil design flow chart in shown in Fig. 83. In the sweeping process, the number of turns N is always pre-selected as the minimum number based on the inductance L requirement, since any larger N results in larger copper trace length and will unnecessarily increase the coil loss significantly. For each possible geometry combination, the coil total ESR R is calculated and compared to locate the optimal design with minimum R, or equivalently, largest Q.

The dielectric ESR R_c is determined by the loss tangent D_g of the dielectric material,

$$R_C = \frac{D_g}{2\pi f_0 C} \tag{44}$$

As for the R_{skin} and R_{prox} from the copper traces, FEMM is used to perform two-dimensional finite element analysis (FEA) for a fast simulation of copper loss. Using the magnetostatic solver, the currents in each turn of every layer of the coil are assigned as

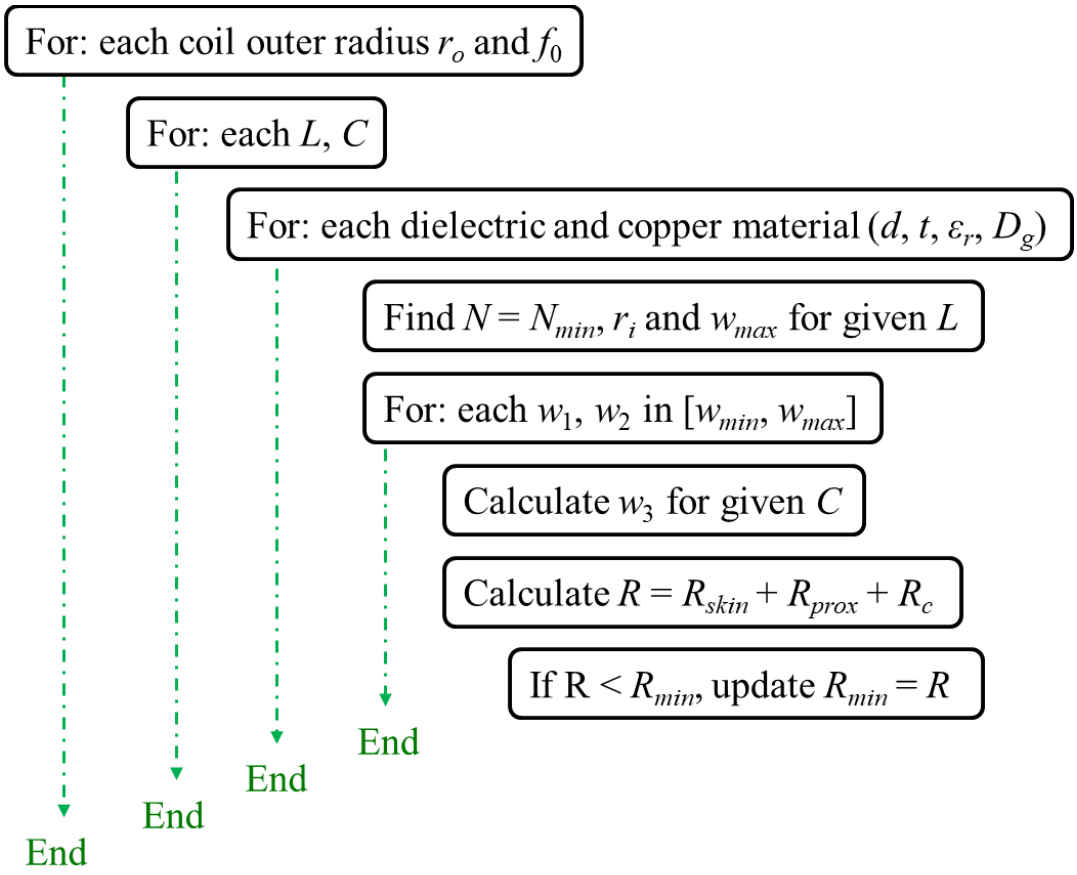
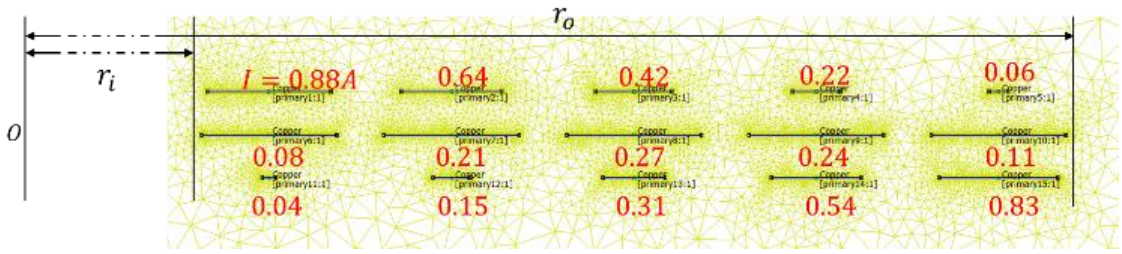


Fig. 83. Design flow chart for coil geometry

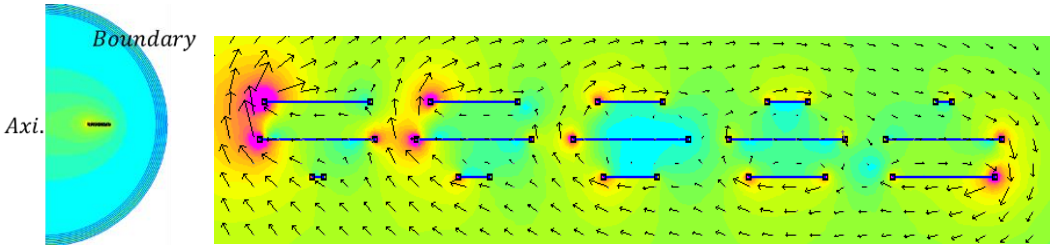
individual sources. The coil is modeled as axisymmetric. One setup example is shown in Fig. 84. Between the coil inner radius r_i and outer radius r_o, an $N = 5$ turns, three-layer coil is excited with discrete current values. From the innermost turn on the top copper layer, the current is decreasing continuously and transferred into the outermost turn on the bottom copper layer through the middle layer, as an approximate representation the real current distribution in the three-dimensional structure.

Note that the electric field between parallel copper plates cannot be simulated simultaneously with the magnetic field in FEMM. Accordingly, any current redistribution within the copper region caused by the electric field is neglected here. Still, the prototype coil experimental measurements later will prove that FEMM simulation provides a fast and accurate tool to demonstrate the benefit of the three-layer structure over the two-layer case. The resulting simulated quality factor Q, including the calculated dielectric loss of three-layer coil, is shown Fig. 85. For each inductance value, the coil geometry is optimized by the sweeping process in Fig. 83 for the highest quality factor Q. The dielectric material properties align with the ROGERS Teflon laminates RO3003 [101], with relative dielectric constant $\varepsilon_r = 3$, maximum thickness $d = 1.52$mm, loss tangent $D_k = 0.001$, and copper thickness $t = 1$ oz. The minimum inner radius r_i is fixed at one third of the outer radius r_o. In this design example, the coil outer radius $r_o = 200$ mm with resonant frequency $f_0 = 6.78$ MHz.

With the increasing inductance value along the x-axis, the inner radius needs to be increased when N is fixed. When $L = 4$ μH, the inner radius needs to be larger than 176.9 mm and is close enough to the outer radius such that no design is available to fulfill the inductance requirement. As a result, N is increased from 2 to 3, allowing r_i to drop to 116.0



(a)



(b)

Fig. 84. Two-dimensional FEMM simulation example (a) current setup (b) H field distribution

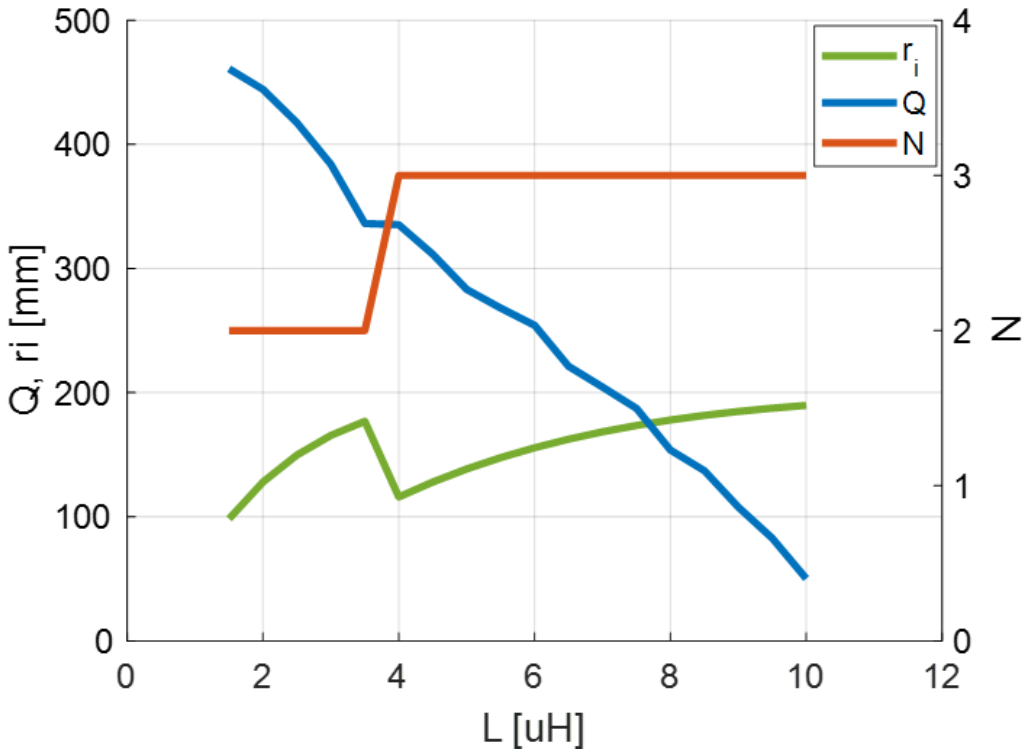


Fig. 85. Sweeping result of three-layer coil with r_o = 200 mm, f_0 = 6.78 MHz

mm and more space is available for copper traces between the inner and outer radius. The three design point geometries are compared in Fig. 86.

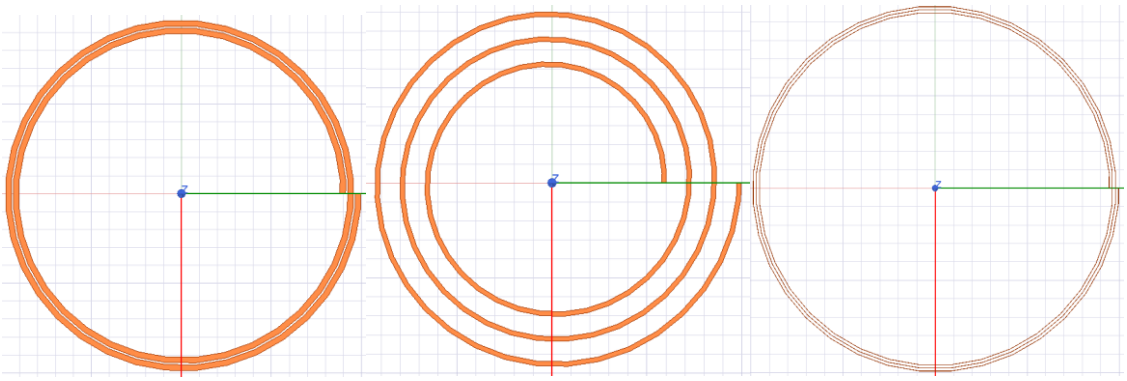
When N jumps again to 4 at $L > 10$ μH, the total copper trace length is so large such that it needs very small copper width ($w \leq 0.1$ mm) to satisfy the capacitance value requirement, which lead to impractical fabrication requirements. In the design iteration, it means that a larger dielectric thickness is needed to allow wider copper width for a given L-C design point.

A design comparison between the two-layer and three-layer coil is given in Fig. 88. The maximum dielectric thickness for the 2-layer case is 3.04 mm for a fair comparison with 3-layer cases. A third case of a three-layer coil with uniform copper width $w_1 = w_2 = w_3$, is also included as shown in Fig. 87.

The uniform width case represents solely the advantage of diminished fringing electric field compared to the two-layer case as discussed previously. The trace width ratio between the 2-layer and 3-layer, uniform width, designs is shown by the dashed line.

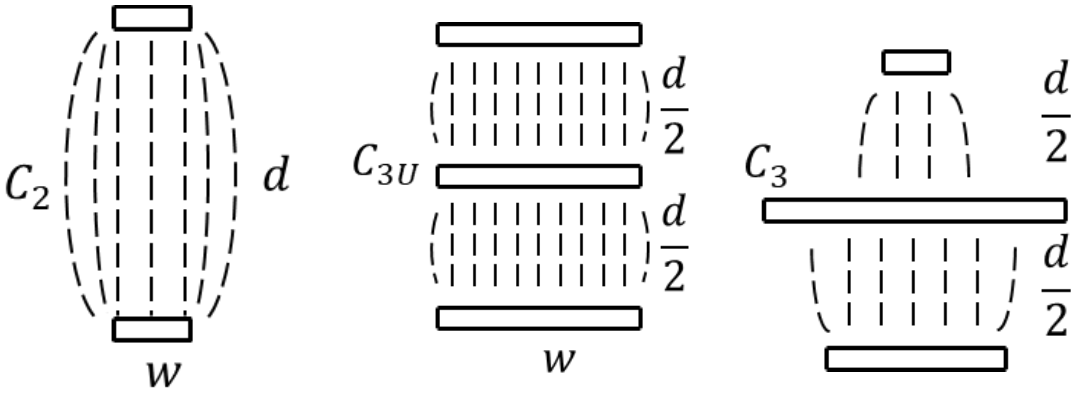
Note that the available design range for the 2-layer coil is much shorter than 3-layers and stops at 5.5 μH due to limited maximum dielectric thickness at 3.04 mm. At that point, the coil copper width r_i=196.1 mm, and w is only 0.36 mm. As depicted in Fig. 89, any further increase in inductance would require an increase in number of turns, which greatly increase the total length of the copper trace. To maintain the capacitance value as desired, the copper width required is reduced from 0.36 mm to the unattainable 0.023 mm.

Clearly the fringing field effect partially accounts for the quality factor improvement in the 3-layer non-uniform case in most of the sweeping range, especially with larger



(a) (b) (c)

Fig. 86. Three-layer non-uniform coil design cases (a) L = 3.5 µH, N = 2, r_i = 176.9 mm (b) L = 4 µH, N = 3, r_i = 116.0 mm (c) L = 10 µH, N = 3, r_i = 189.7 mm



(a) (b) (c)

Fig. 87. Geometry illustration of different coil structure: (a) 2-layer; (b) 3-layer uniform copper width; (c) 3-layer non-uniform copper width

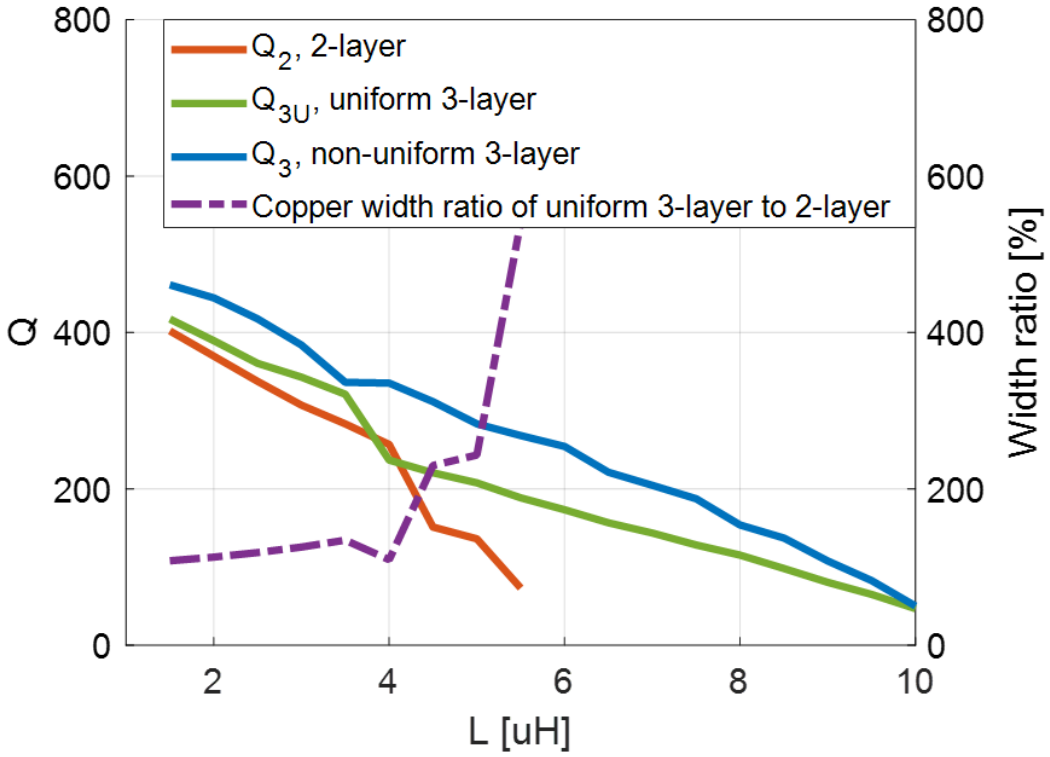
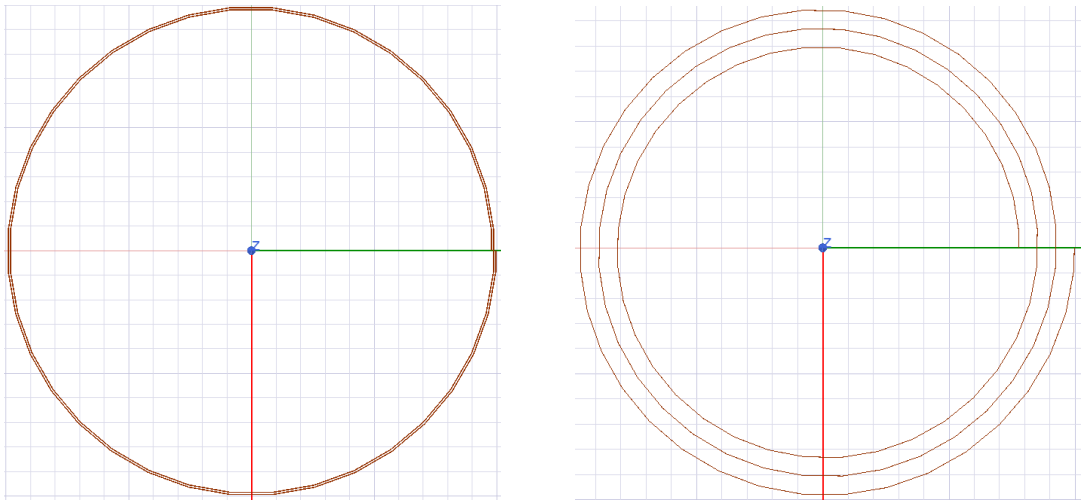


Fig. 88. Quality factor comparison for two-layer, three-layer with uniform copper width, and three-layer with non-uniform copper width coils. r_o = 200 mm, f_0 = 6.78 MHz



(a) (b)

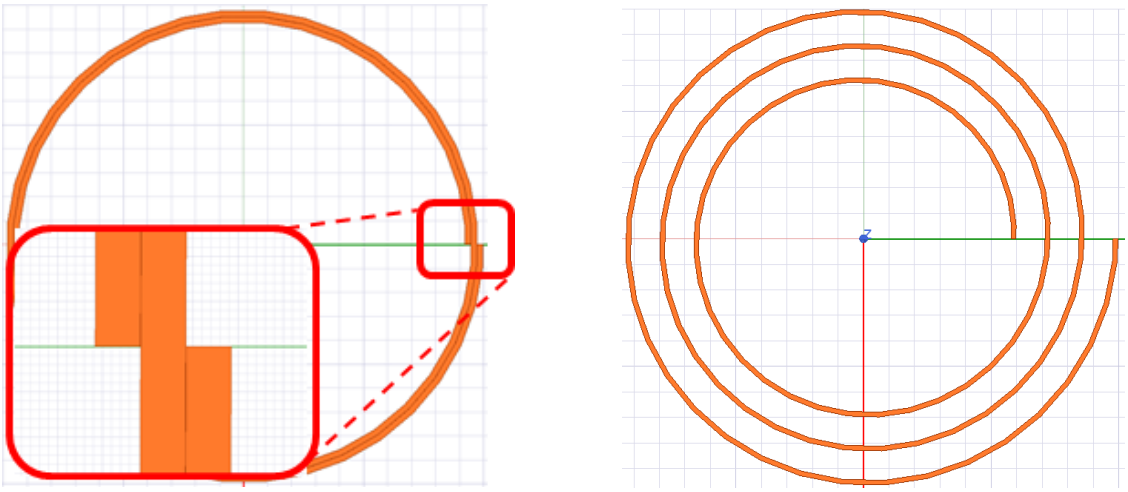
Fig. 89. Two-layer coil design cases (a) L = 5.5 µH, N = 2, r_i = 196.1 mm, w = 0.36 mm (b) L = 6 µH, N = 3, r_i = 155.6 mm, w = 0.023 mm

inductance value. Note that one exception occurs when L = 4 μH. Due to the fact that N = 3 for the uniform 3-layer case and N = 2 for the 2-layer case at this point, the 3-layer has much longer total copper trace length than the 2-layer case, resulting in a comparable copper width and slightly lower quality factor. Fig. 90 compares the two designs for the same inductance for uniform 3-layer coil. With smaller N = 2, wider copper width is available for higher quality factor than the 2-layer coil. However, the gap between adjacent turns is only 0.1 mm, which is not feasible for practical design. Further increasing the total dielectric thickness of 3.04 mm could help eliminate such exceptions.

A more detailed comparison of designs from Fig. 88 is provided in TABLE X to show the effect of copper width on the generated capacitance from different coil structures.

The targeted inductance is 5.5 μH and capacitance is 100.2 pF. For the 2-layer case, the copper width is limited to a very small value due to the relatively high fringing electric field, leading to a quality factor less than 100. The 3-layer with uniform copper width case reduces the fringing effect, and much wider copper with is allowed resulting in 1.58 times higher quality factor. Combining the advantages from both better-controlled fringing capacitance and current sharing among three layers, the non-uniform copper width case gives an additional 42% increase in quality factor over the uniform width case.

Fig. 91 gives the coil design results for the two-layer coil and the three-layer non-uniform coil with different outer radius. The quality factor is largely increased for the three-layer coil. At larger radius and inductance, the advantage is more significant. Note that for any coil structure, the largest, 200 mm radius is only advantageous in the range of smaller inductance, or equivalently larger capacitance. For example, for L > 10 μH, the three-layer coil has the highest Q for the smallest, 50 mm radius. When the desired capacitance is small

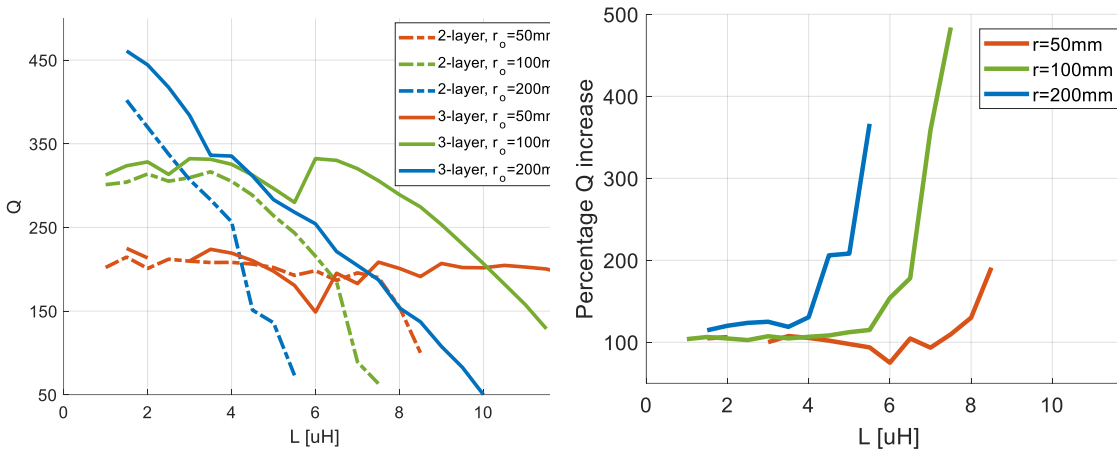


(a) (b)

Fig. 90. Three-layer uniform coil design cases L = 4 µH, d = 1.5 mm (a) N = 2, r_i = 184.9 mm, w = 5.0 mm, gap = 0.1 mm (b) N = 3, r_i = 116.0 mm, w = 3.7 mm, gap = 2.3 mm

TABLE X. Multi-layer Coil Design Case Comparison

	2-layer	**3-layer uniform width**	**3-layer non-uniform width**
Capacitance [pF]	100.2	100.2	100.2
w_1 [mm]	0.36	1.94	0.1
w_2 [mm]	0.36	1.94	4.38
w_3 [mm]	NA	1.94	2.47
Q	73.2	188.5	268.2
Q improvement		158%	42%



(a) (b)

Fig. 91. (a) Quality factor comparison for two-layer and three-layer coil with different coil radius, f_0 = 6.78 MHz (b) percentage increase of quality factor from 2-layer to 3-layer, with different coil radius

at high inductance, the copper width of the 200 mm radius case is much smaller than the 50 mm radius case due to the limited maximum dielectric thickness, leading to an insufficient utilization of coil pad surface area.

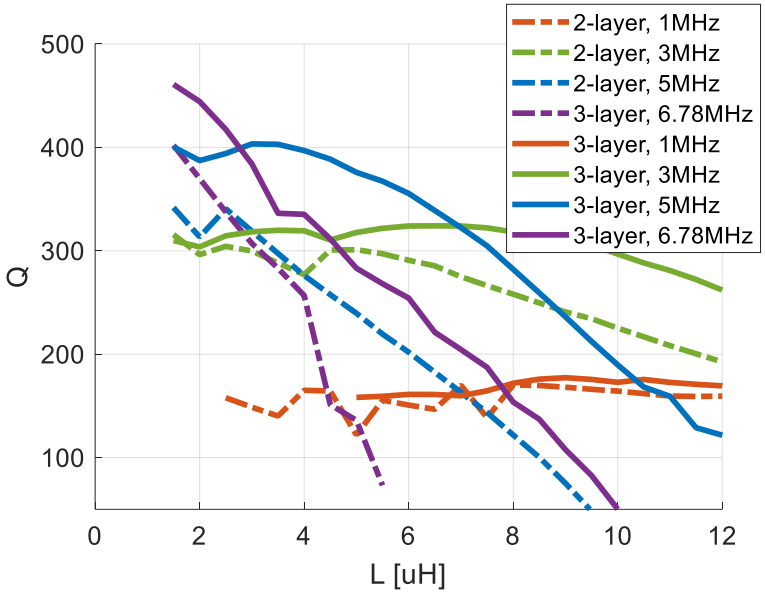
At 200 mm coil radius, similar trend is applied for different frequencies. In Fig. 92, higher frequency enables a much higher quality factor improvement comparing to the 2-layer case, especially at lower inductance range. Although the coil equivalent ESR is also increasing with higher frequency, the coil quality factor is improved as long as the increment in frequency is larger than the increment in coil ESR.

The complete 3-layer non-uniform coil design result is given in Fig. 93, with coil outer radius r_o = 200 mm and resonant frequency ranging from 1 MHz to 7 MHz. The laminate specs are d = 0.13-1.5 mm, $\underline{D_q}$=0.001, ε_r = 3, t = 2 oz. For fabrication consideration, w_{min} = 0.1 mm, gap_{min} = 1 mm. Coil inner radius is limited with $ri_{min} = r_o/3$.

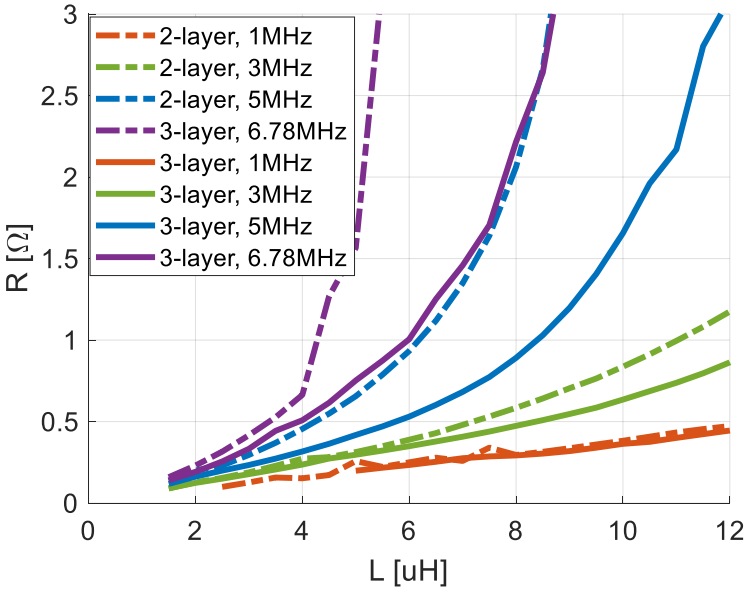
This plot contains the optimal coil design for a range of coil inductances from 0.5 µH to 20 µH. The highest quality factor coils with $Q > 500$ occur with very small inductance and high frequency. These designs do not necessarily guarantee the highest system efficiency; instead, the coil design in Fig. 93 is combined with a system-level design optimization including power stages to determine the best overall system design in the next chapter.

4.6 Summary

In this chapter, based on the magnetic and electric field analysis, both inductance and capacitance models of the three-layer non-uniform SR coil are proposed, and they are verified by the current distribution comparison in the HFSS 3D simulation. The



(a)



(b)

Fig. 92. (a) Quality factor comparison for two-layer and three-layer coil with different frequencies, r_o = 200 mm (b) Coil ESR comparison for two-layer and three-layer coil, with different frequencies

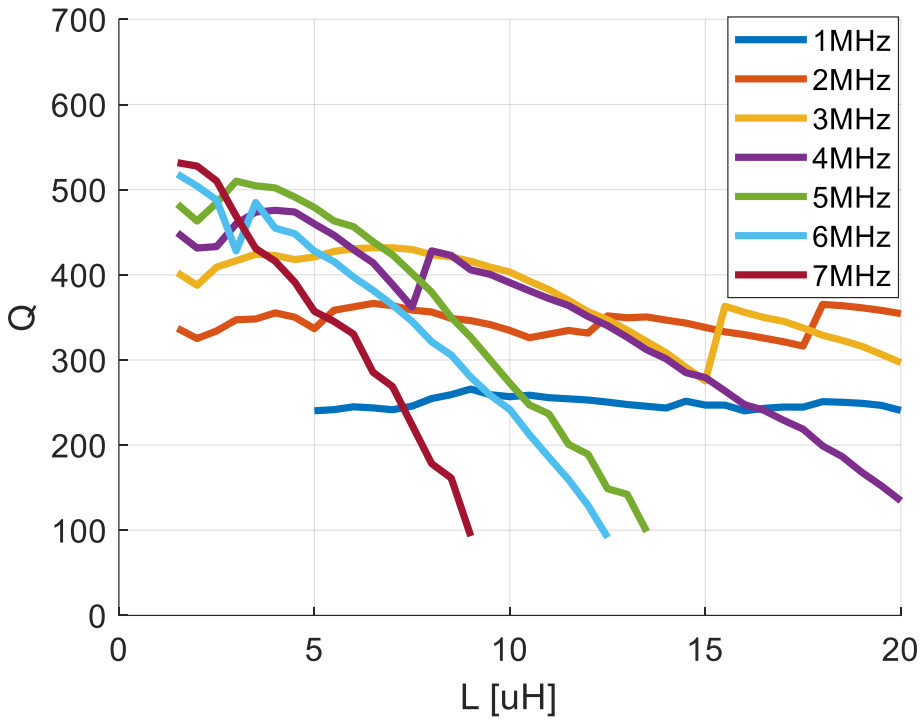


Fig. 93. Coil quality factor comparison with different frequency, r_o = 200 mm

significance of better-confined fringing electric field in the three-layer coil has been studied, showing its contribution on wider copper width design with higher coil quality factor than the conventional two-layer SR coil.

A coil design optimization scheme is proposed in this chapter, allowing design space sweeping for highest quality factor design aided by the FEMM 2D fast simulation for copper loss. Three coil structures, including the two-layer coil, the three-layer coil with uniform width, and the three-layer coil with non-uniform width, have been optimized and compared in detail. With both advantages of smaller fringing capacitance from the three-layer structure and better current sharing from the non-uniform copper width, the three-layer SR coil with non-uniform copper width gives highest quality factor, especially with large coil size and high resonant frequency. The design result proves that the high quality factor SR coil design is achievable at MHz frequency. Still, the optimized coil design result needs to be integrated with the system-level design for best system performance, as will be discussed in the next chapter.

CHAPTER 5. WIRELESS CHARGING SYSTEM DESIGN PROCESS

5.1 System Design

The integrated system design flow chart is shown in Fig. 94. For a given system power rating P_o and output voltage V_{2DC}, the system efficiency is calculated as both the transmitter and receiver coil designs are swept across all locally-optimal designs from the previous chapter. Note that the coupling coefficient k between two coils is also a strong factor affecting the system operating point, which is determined by the coil geometries and distance between them. In Fig. 94, k is calculated based on the geometries of two coils for a fixed coil-to-coil distance. Switching frequency f_s is also tuned, and maximum efficiency is calculated for each L_1 and L_2 pair.

In this section, the power stage loss models are based on GaN Systems GS66516T 650 V GaN transistors and CREE C4D08120E 1200 V SiC Schottky diodes implementing the high frequency inverter and rectifier, respectively. In the system modeling process, coil waveforms are approximated by their fundamental frequency component. Junction capacitance of both GaN transistors and diode bridge are accurately modeled during the high frequency transient, as discussed in [102]-[103]. The system diagram is given in Fig. 95. The coils are designed with radius up to r_o = 200 mm and an air gap of 100 mm. Input and output voltages are allowed to vary but constrained below voltage ratings of the selected GaN FET (Field Effect Transistor) and diode. Complete system design specifications are summarized in TABLE XI.

For a 6.6 kW GaN inverter with MHz switching frequency, the zero-voltage-switching (ZVS) condition should always be maintained within the wide load range to avoid any hard

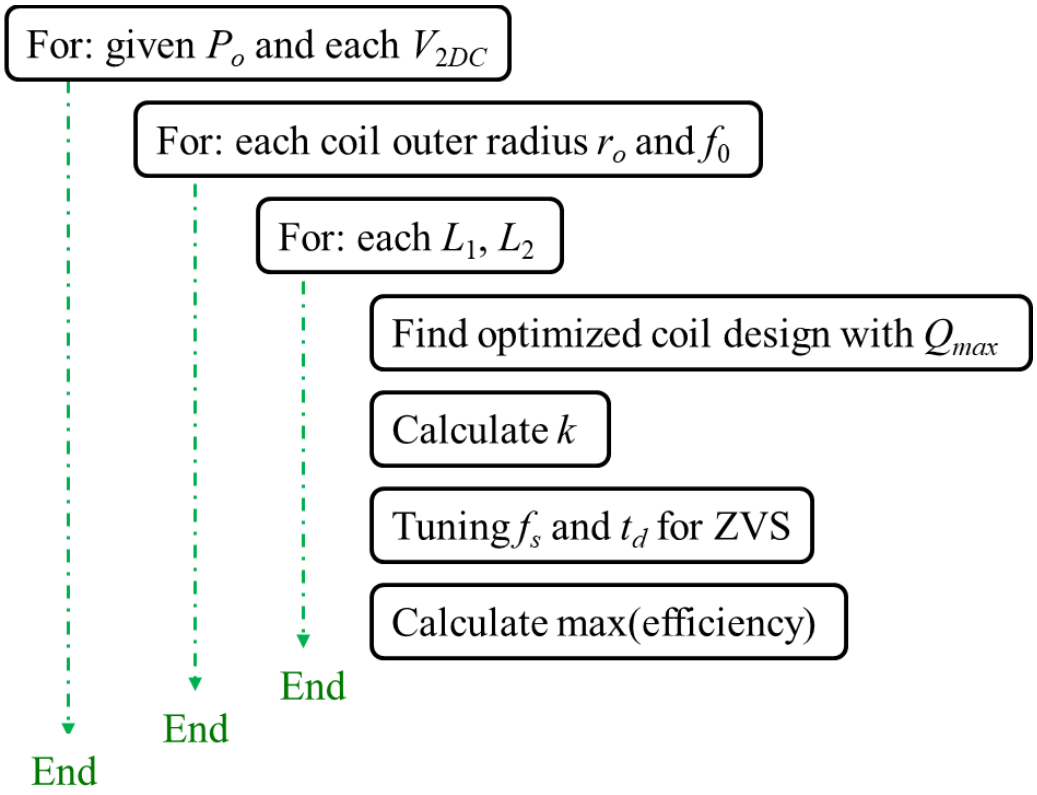


Fig. 94. Design flow chart for WPT system

TABLE XI. System Design Specifications

Output power P_o [kW]	6.6	Coil radius r_o [mm]	200
Maximum input voltage V_{1DC} [V]	500	Maximum output voltage V_{2DC} [V]	800
Airgap [mm]	100	Gate driver voltage [V]	6

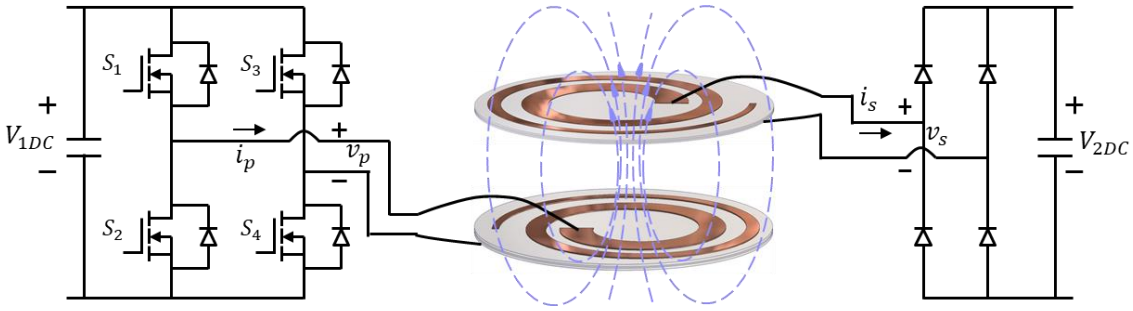


Fig. 95. Proposed WPT system diagram with two SR coils

switching. As shown in Fig. 96, proper tuning of the switching frequency f_s around the coil resonant frequency f_0 gives a positive phase shift t_0 between the zero-crossing of the inverter output voltage and current. The green shaded area is the total charge $2Q_{oss}$ required during the dead-time to achieve full ZVS of one phase leg. For the completion of ZVS, time intervals t_{d1} and t_{d2} need to fulfill,

$$Q_{oss} = \int_{\frac{T_s}{2}-t_0-t_{d1}}^{\frac{T_s}{2}-t_0} \sqrt{2} I_p \, sin(\omega_s t) dt \tag{45}$$

$$Q_{oss} = \int_{\frac{T_s}{2}-t_0}^{\frac{T_s}{2}-t_0+t_{d2}} \sqrt{2} I_p \, sin(\omega_s t) dt \tag{46}$$

where I_p is the RMS value of i_p, and the switching dead-time t_d is selected such that

$$t_{d1} + t_{d2} \leq t_d \leq t_{d1} + t_0 \tag{47}$$

The lower boundary of dead-time t_{d1} + t_{d2} is determined by the total charge $2Q_{oss}$, and the upper boundary t_{d1} + t_0 prevents any re-charging of C_{oss} that may occur if the dead-time does not complete before the polarity of i_p reverses direction. In the system optimization process, t_d is selected as the average value of the two boundaries to have some margins at both ends.

In the following section, converter losses are modeled in detail to facilitate system-level optimization.

5.2 System Loss Model

5.2.1 GaN Conduction Loss

The conduction loss when the transistor is on is,

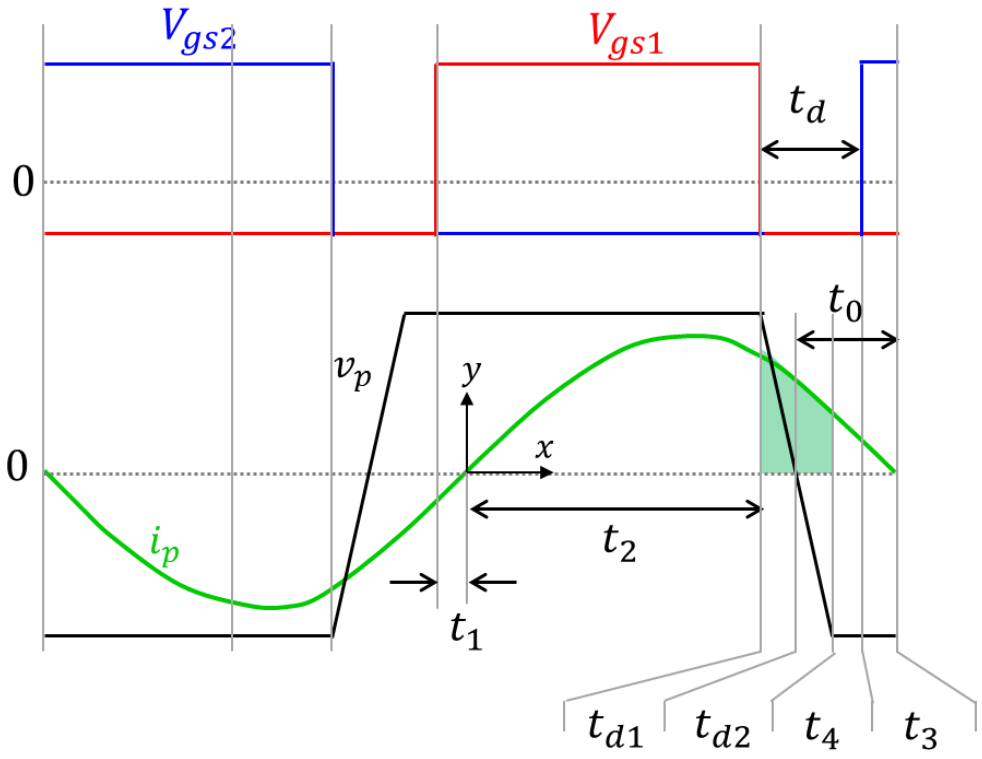


Fig. 96. Waveforms for inverter gate signals V_{gs1}, V_{gs2}, and inverter switching node voltage v_p, current i_p within one switching cycle

$$P_{con+} = 4\frac{1}{T_s}\int_{-t_1}^{t_2} i_p^2 R_{ds} dt = 4f_s I_p^2 \left[t_2 - \frac{\sin(2\omega_s t_2)}{2\omega_s} + t_1 - \frac{\sin(2\omega_s t_1)}{2\omega_s}\right] R_{ds} \quad (48)$$

The reverse conduction time, t_4, should be minimized especially when applying a large negative off-state gate voltage. The reverse conduction loss is

$$P_{rev} = 4\frac{1}{T_s}\int_{\frac{T_s}{2}-t_0+t_{d2}}^{\frac{T_s}{2}-t_0+t_{d2}+t_4} (v_{0rev} + R_{rev} i_p) i_p dt \quad (49)$$

$$\begin{aligned} P_{rev} = 4\Bigg\{ & v_{0rev}\left(-\frac{\sqrt{2}I_p}{2\pi}\right)\{cos[\omega_s(t_3+t_4)] - cos(\omega_s t_3)\} \\ & + f_s I_p^2 \left\{t_4 - \frac{sin[2\omega_s(t_3+t_4)]}{2\omega_s} + \frac{sin(2\omega_s t_3)}{2\omega_s}\right\} R_{rev}\Bigg\} \end{aligned} \quad (50)$$

where R_{ds} is the conducting resistance during on-time and R_{rev} is the reverse conduction resistance. v_{0rev} is the forward voltage when reverse conducting, and it depends on the gate voltage selected for off-states. For example, when -3 V is selected instead of 0 V, the v_{0rev} will be largely increased from 1.6 V to 4.6 V for GS66516T. Adding (21) and (23) together gives the total conduction loss.

5.2.2 GaN Turn-off Loss

The residual turn-off loss with ZVS fulfilled is estimated by the difference between the hard switching energy E_{off} and the energy stored in C_{oss} from device datasheet [104].

$$P_{off} = 4f_s(E_{off} - E_{oss}) \quad (51)$$

$$E_{off} = \int_0^{t_{off}} v_{ds} i_{ds} dt \quad (52)$$

$$E_{oss} = f(V_{ds}) \quad (53)$$

The voltage-dependent C_{oss} energy can be looked up from the E_{oss} curve in the datasheet,

but the E_{off} needs to be evaluated based on specific circuit parameters. A half bridge double pulse test circuit in LTspice, shown in Fig. 97, is used as the test bench to measure E_{off} under different switching voltage and current [105]. Parameters including switching frequency, junction temperature, gate voltage, gate resistance, and parasitics in the gate loop and power loop are assigned to match the PCB design since they have strong impact on the switching characteristics.

With given switching voltage and current, E_{off} is calculated by the integration of switching node voltage and device current. The detailed circuit parameters like L_{ds} and L_{gate} are found after the design of PCB, as introduced in detail in the next chapter. One simulation result is demonstrated in Fig. 98. With V_{dc} = 502 V, and I_{off} = 17.9 A, the switching energy during hard-switching turn-off is 23.5 μJ.

5.2.3 C_{oss} Hysteresis Loss

It has been reported that there is net charge difference in one charging and discharging cycle for the GaN power devices as plotted in Fig. 99 [106]. This hysteresis loss is exponentially increasing with dV/dt, and comparable to the conduction loss when the device is operating at MHz range.

To quantify the hysteresis loss, different modeling methods have been proposed, and a number of GaN transistors have been tested in the literature. The equation used in [106][107] has the form of Steinmetz equation to give a curve-fitting of the loss dependence on voltage and frequency under sinusoidal excitation, with the tested results shown in TABLE XII [106].

$$E_{DISS} = kf^{\alpha}V^{\beta} \tag{54}$$

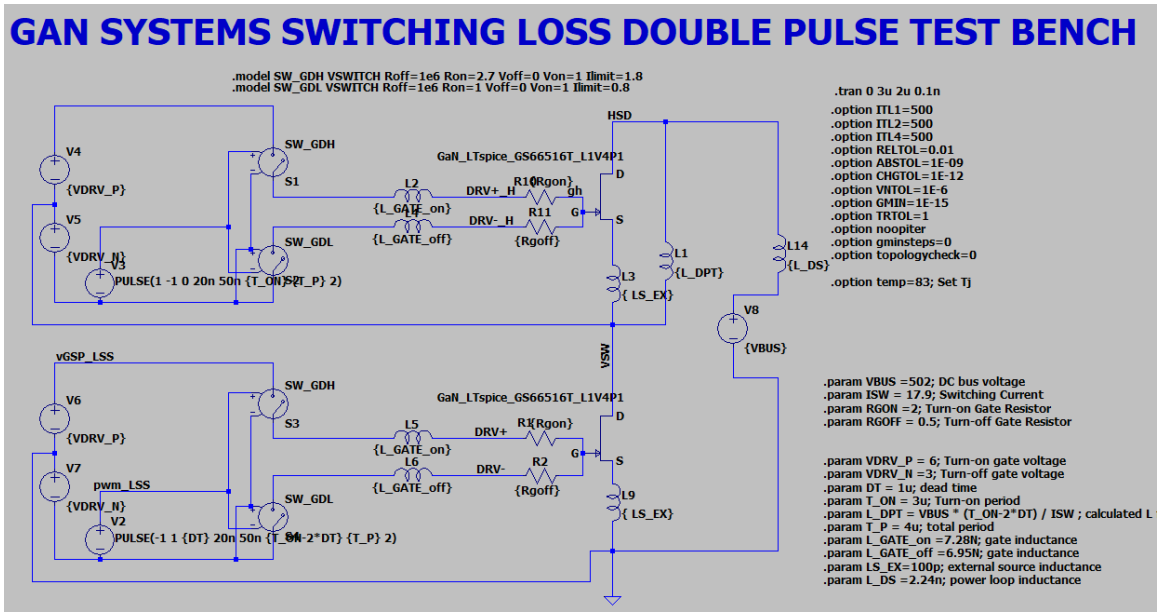


Fig. 97. Double pulse test simulation circuit [105]

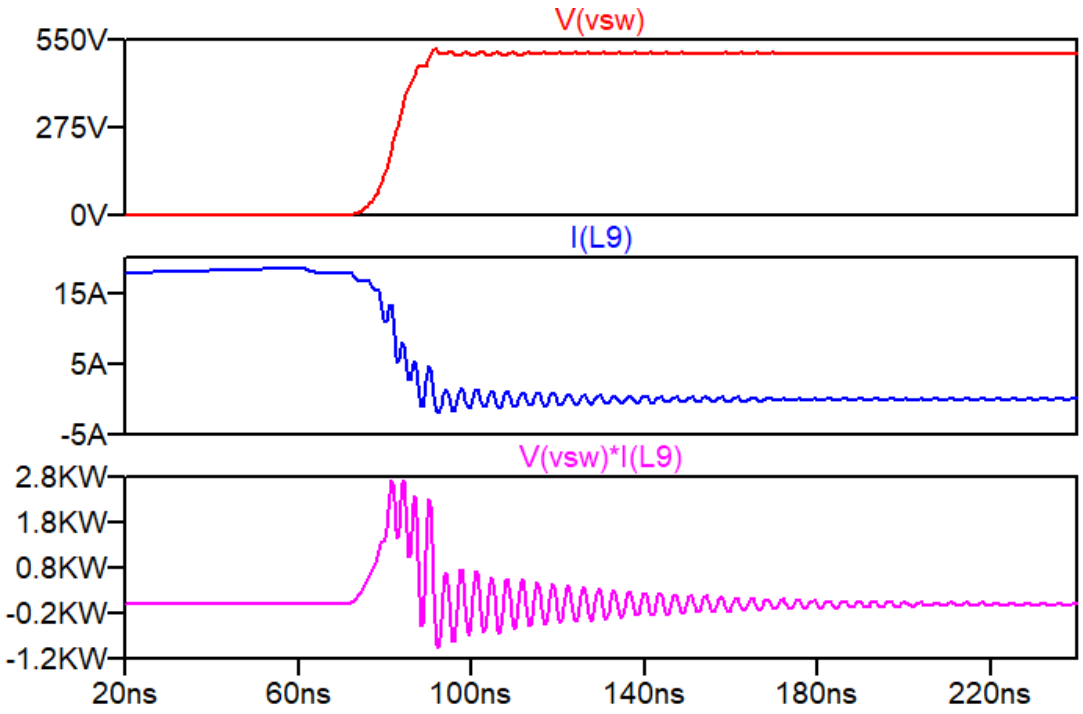


Fig. 98. Double pulse test simulation result for E_{off}

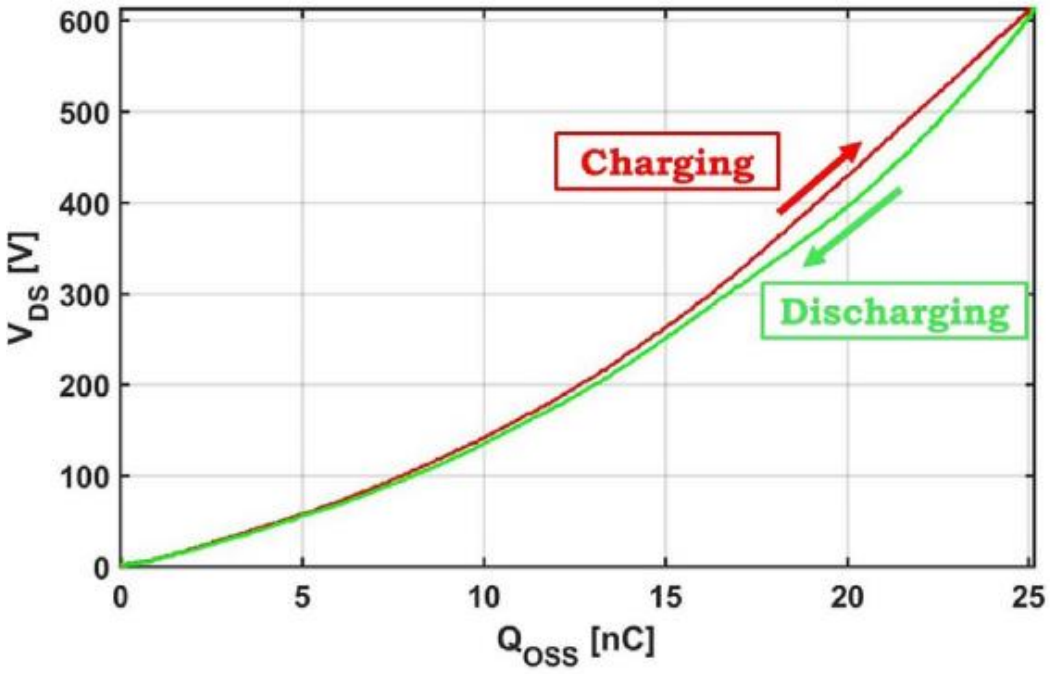


Fig. 99. C_{oss} hysteresis loss in V_{dc} vs Q_{oss} curve [106]

TABLE XII. Steinmetz Parameters in GaN Devices [106]

Device	k [μJ/(V $\cdot$ Hz)]	α	β
GS66504B	$2.84 \cdot 10^{-10}$	0.6	1.70
PGA26E19BA	$1.96 \cdot 10^{-9}$	0.5	1.76
TPH3202LS, V $<$ 300 V	$1.78 \cdot 10^{-11}$	0.8	1.46
TPH3202LS, V $\geq$ 300 V	$8.72 \cdot 10^{-18}$	0.8	4.01

However, the sinusoidal excitation has the lowest dV/dt for a given frequency and peak voltage, and the C_{oss} loss would be underestimated in a voltage source inverter. For different voltage excitation waveforms shown in Fig. 100, the measured losses per cycle are plotted in Fig. 101 under different dV/dt transient slew rates. The normalized dV/dt is used to eliminate the voltage swing under different excitations and have a fair comparison on dV/dt dependence for power devices,

$$\left(\frac{dV}{dt}\right)_{NORM} = \left(\frac{dV}{dt}\right)_{MEAS}\left(\frac{V_{DS}}{V_{DS,MAX}}\right)^{\beta} \tag{55}$$

To have a relatively accurate calculation for the hysteresis loss, C_{oss} related loss P_{coss} is approximated based on the test data for GaN Systems GS66504B transistors in Fig. 101 with square excitation. The normalized dV/dt is calculated based on system inverter waveform, and energy loss per cycle E_{DISS} is found in Fig. 101. Based on the assumption that the loss scales linearly with the output energy storage of the device within a device family, the E_{DISS} for GS66516T is linearly-scaled by the device C_{oss} ratio between GS66516T and GS66504B. The final hysteresis loss for GS66516T is,

$$P_{coss} = 4f_s E_{DISS} \tag{56}$$

It should be noted that all the modeling approaches above only provide an estimated result for the C_{oss} related loss. Many factors including device package size, package structure (top or bottom cooling), temperature, and excitation waveform are not considered.

5.2.3 Other Losses

The diode bridge conduction loss and coil conduction loss are,

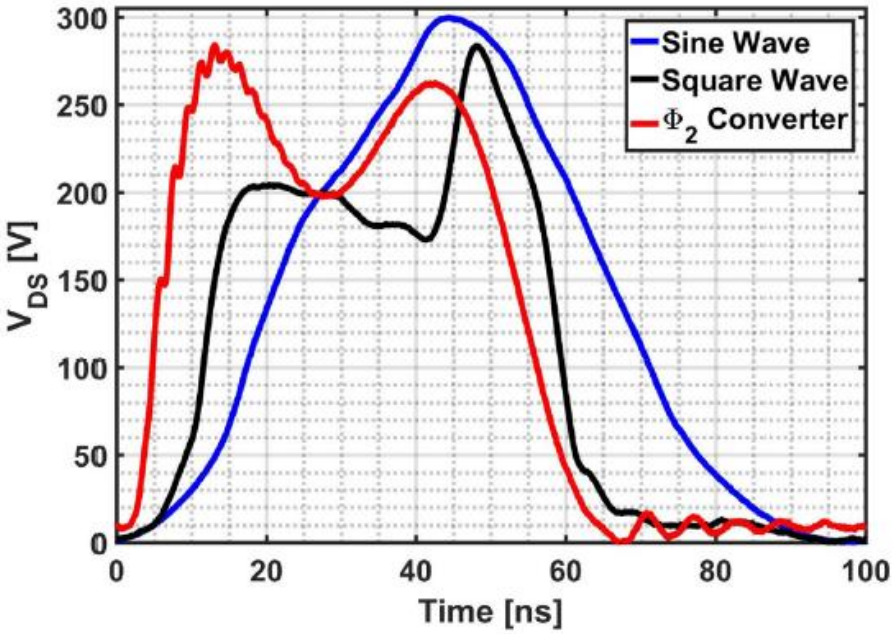


Fig. 100. Sine wave, square wave, and Φ_2 converter excitations at 10 MHz [106]

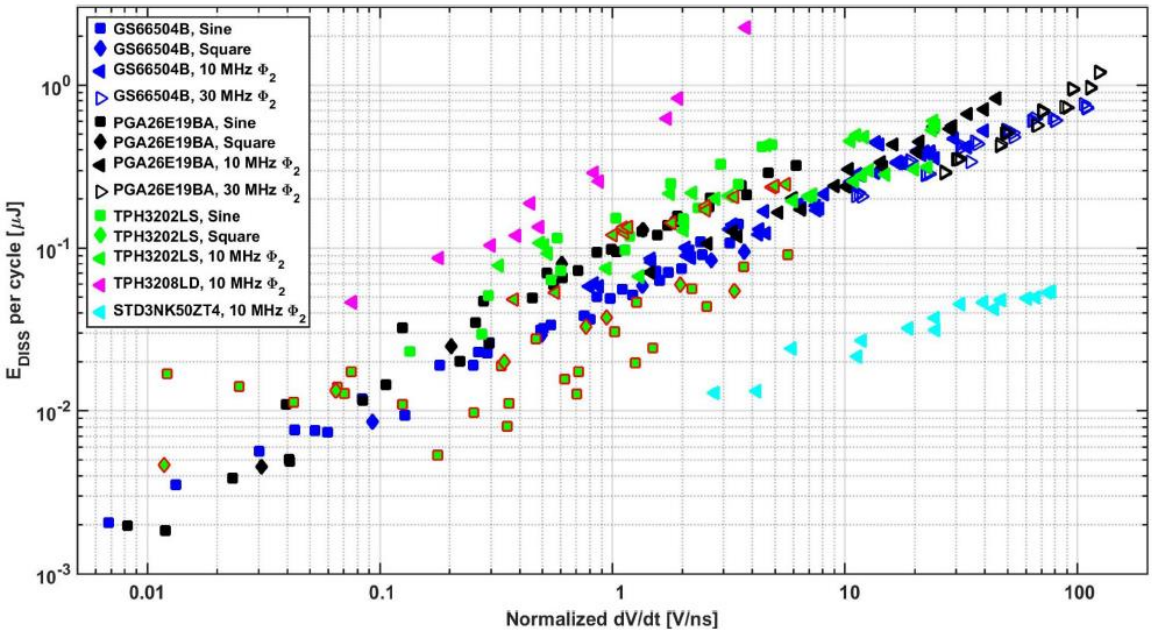


Fig. 101. Hysteresis loss per cycle vs. normalized dV/dt for GaN power devices [106]

$$P_D = 4\left(v_0 I_{davg} + I_{drms}^2 R_d\right) = 4\left(v_0 \frac{\sqrt{2} I_s}{\pi} + \frac{I_s^2}{2} R_d\right) \quad (57)$$

$$P_{coil} = I_p^2 R_1 + I_s^2 R_2 \quad (58)$$

where I_s is the RMS value of i_s, v_0 is the diode forward voltage, R_d is the diode resistance during conduction.

The final system efficiency is,

$$\eta = \frac{P_o}{P_o + P_{con+} + P_{rev} + P_{off} + P_{coss} + P_D + P_{coil}} \quad (59)$$

5.3 System Efficiency Contour and Analysis

After the optimizations both at the coil level and system level, the projected system efficiency is shown in Fig. 102 for different coil resonant frequencies. The target power rating is 6.6 kW and coil radius is 200 mm. The peak modeled efficiency point is achieved around f_0 = 3 MHz when V_{2DC} = 700 V. This design point is further expanded into the efficiency contours in Fig. 103, where the inductance values of primary side and secondary coil, L_1 and L_2 are used as variables.

With different combinations of L_1 and L_2, the coil quality factor from Fig. 93 strongly impacts the system efficiency. The high quality factor, low inductance coil designs have degraded the system performance due to excessive peak currents on the primary side as plotted in Fig. 104.

The right side of Fig. 103 contains a blank area where designs were eliminated due to exceeding the 650 V voltage rating of GaN devices, which is also shown in the system

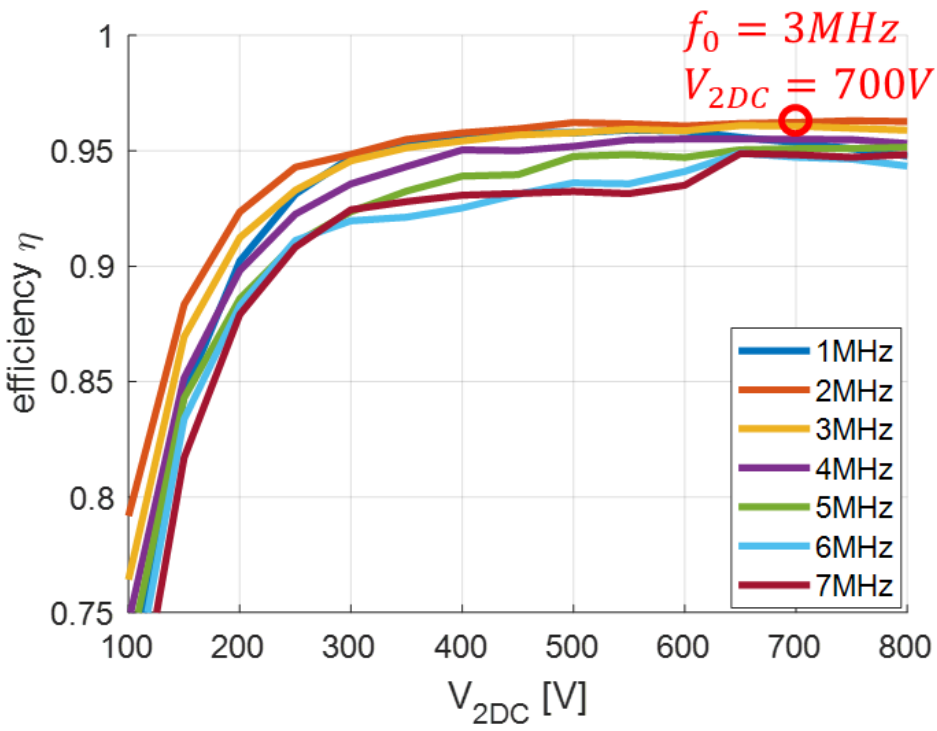


Fig. 102. Efficiency comparison with coil resonant frequency f_0 and load voltage V_{2DC}

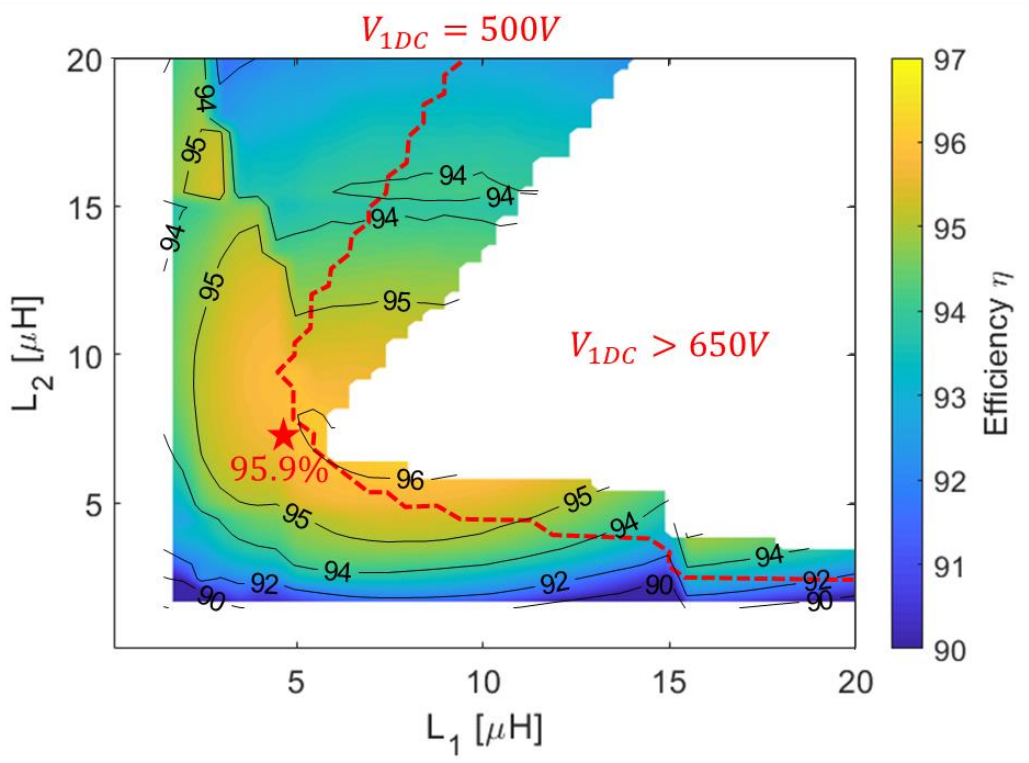


Fig. 103. System efficiency contour, V_{2DC} = 700 V, f_0 = 3 MHz

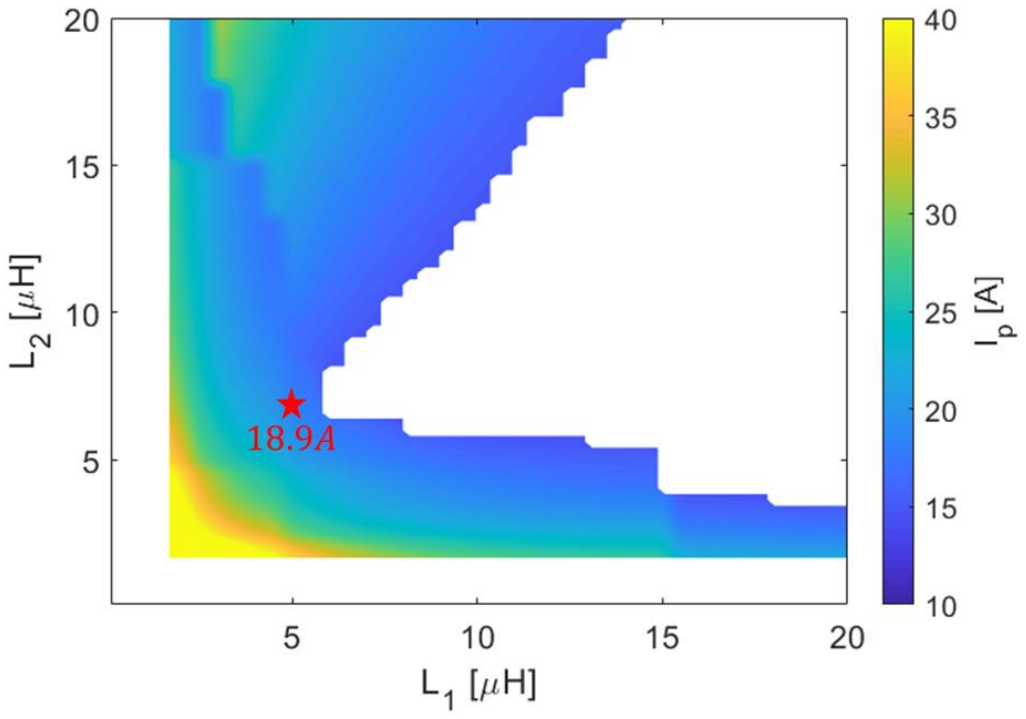


Fig. 104. System primary side coil current i_p contour, V_{2DC} = 700 V, f_0 = 3 MHz

input voltage contour in Fig. 105. Given a 150 V voltage margin, the highest efficiency design below the 500 V input voltage safety limit achieves 95.9% efficiency as marked. The coil inductances are L_1 = 5 μH and L_2 = 6.5 μH, with predicted quality factor of 421 and 432 with 3 MHz resonant frequency, respectively. The final system at full power operates at input voltage V_{1DC} = 451 V, output voltage V_{2DC} = 700 V, and a switching frequency f_s = 3 MHz based on the optimization result.

To evaluate the thermal stress on the high frequency switching GaN devices, the total loss in the GaN devices is plotted in Fig. 106. Note that the total loss for four GaNFETs is close to 100 W, or 25 W per device, at the selected system design point. To mitigate the heating at such high power for the devices, a forced-air cooling solution with air duct and heatsink is designed and implemented, as illustrated in the following experimental verification in Chapter 6. The total coil loss contour is also shown in Fig. 107, which is almost comparable to the GaN related loss. The loss from the diode bridge rectifier is relatively low considering the high system output DC voltage.

The optimized system parameters are summarized in TABLE XIII, and the simulated system waveforms are shown in Fig. 109 with ZVS achieved at full power.

5.4 Summary

This chapter focuses on the system-level optimization with the design result of the proposed three-layer non-uniform SR coil in Chapter 4. To quantify the optimal design point for highest system efficiency, a design flow chart is adopted to define the design space and process. High frequency effects related to device parasitic capacitance are

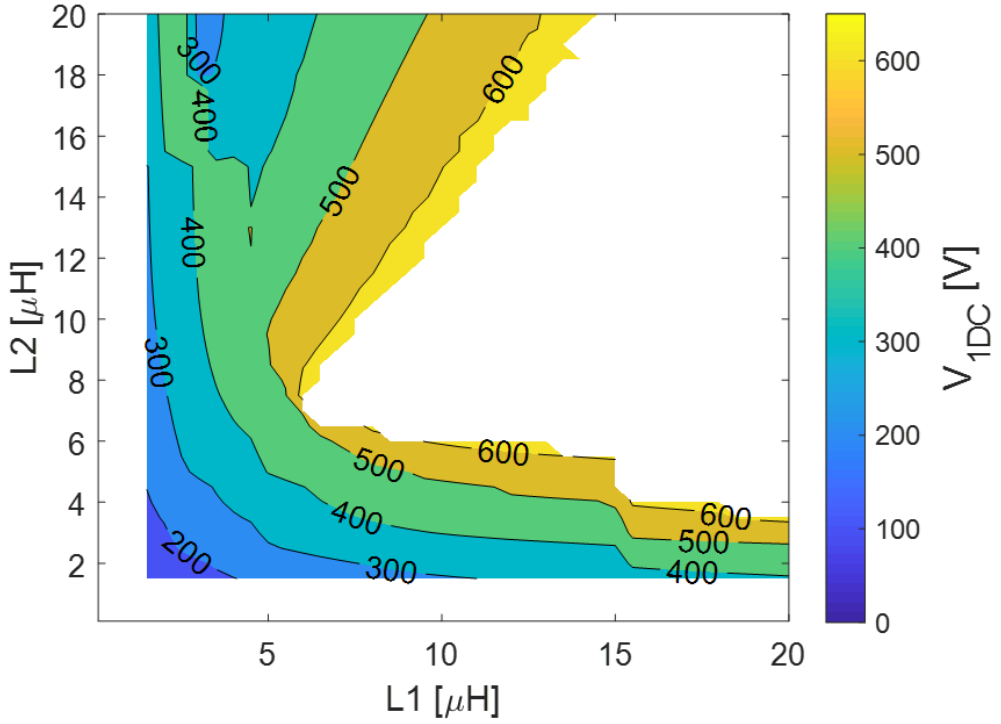


Fig. 105. System input voltage V_{1DC} contour, V_{2DC} = 700 V, f_0 = 3 MHz

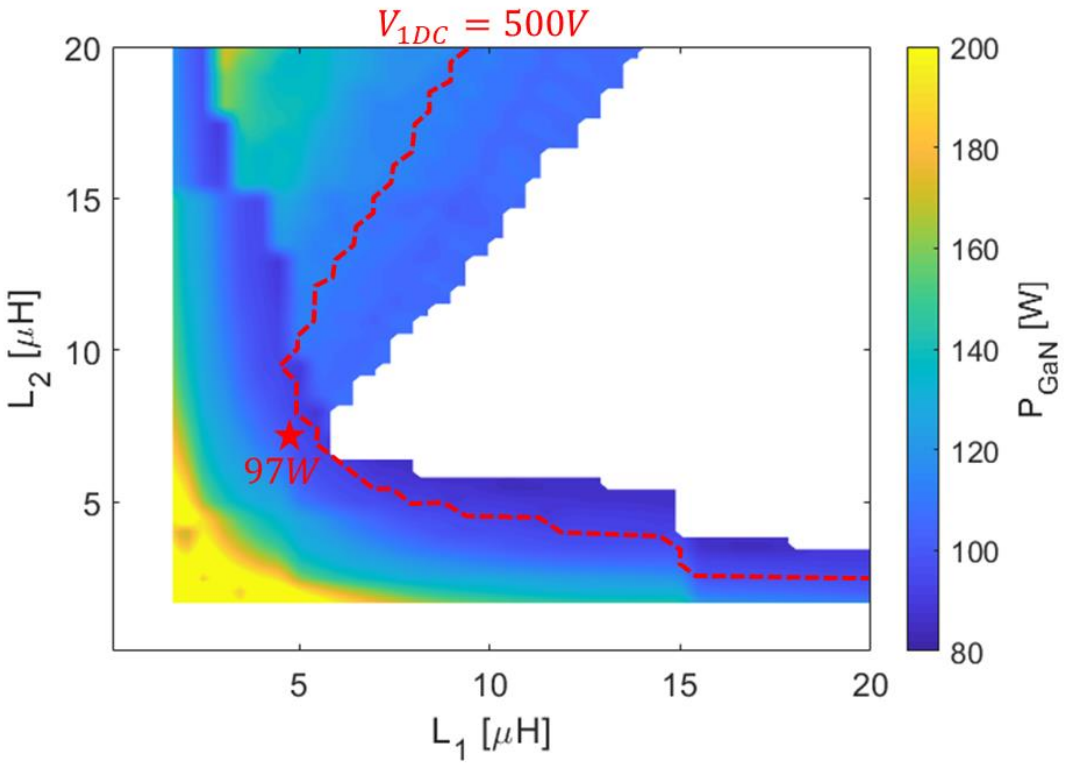


Fig. 106. GaN total loss contour, V_{2DC} = 700 V, f_0 = 3 MHz

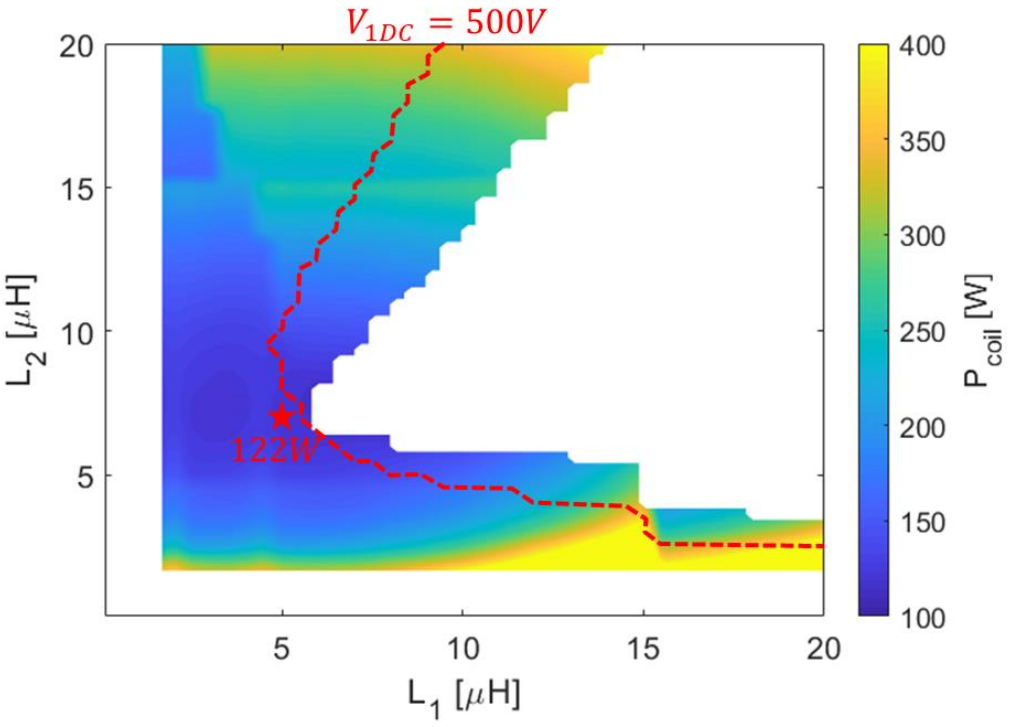


Fig. 107. Coil total loss contour, V_{2DC} = 700 V, f_0 = 3 MHz

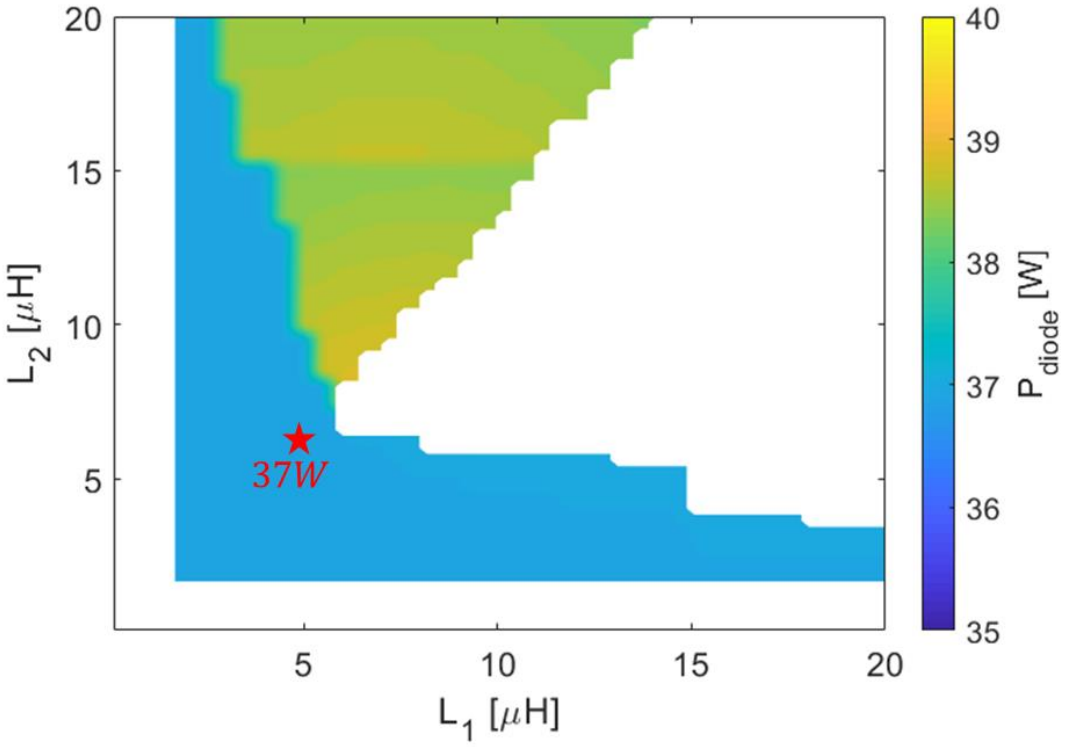


Fig. 108. Diode bridge rectifier loss contour, V_{2DC} = 700 V, f_0 = 3 MHz

TABLE XIII. Optimized System Parameters

Coil parameters			
L_1 [µH]	5	L_2 [µH]	6.5
Q_1	421	Q_2	432
Power stage parameters			
V_{1DC} [V]	451	V_{2DC} [V]	700
I_p [A]	18.9	I_s [A]	12.1
f_s [MHz]	3	η [%]	95.9

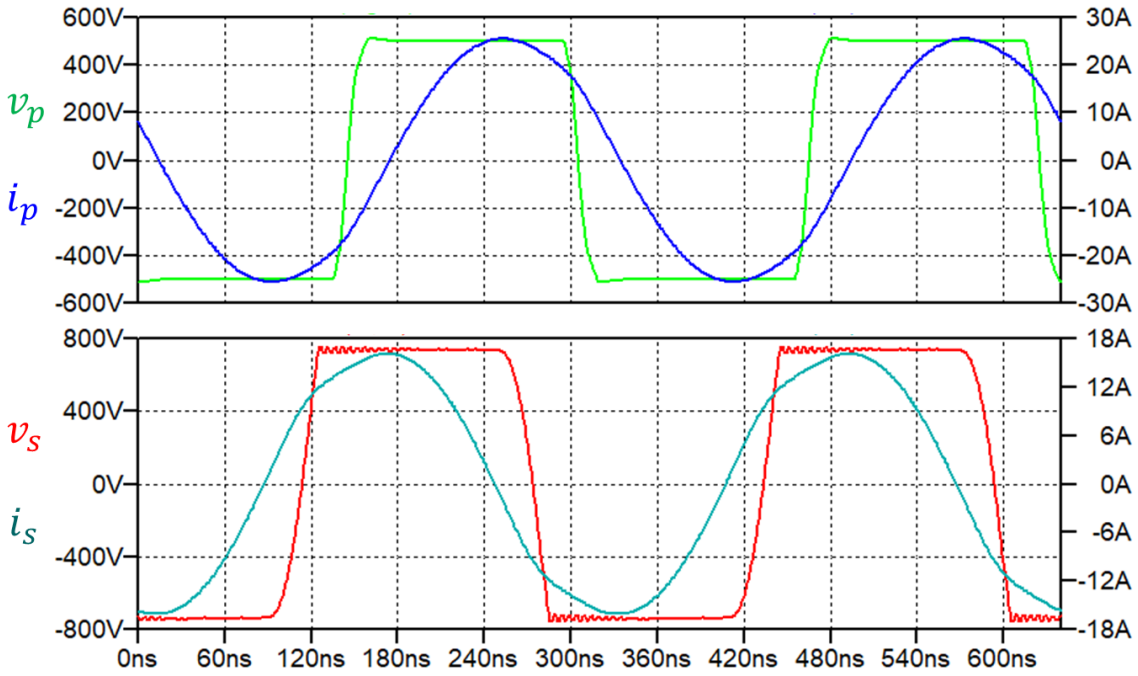


Fig. 109. Simulated inverter output voltage v_p current i_p, and rectifier input voltage v_s current i_s at 6.6 kW output

considered, and design constraints like ZVS condition for GaN transistors and voltage stress on devices are included in the design process. To have an accurate system loss model, GaN transistor related loss mechanisms are detailed, including the conduction loss, turn-off loss, and C_{oss} hysteresis loss.

Based the optimization result, a 3 MHz WPT system is designed for 6.6 kW power output and 95.9% overall efficiency. The primary and secondary coil inductances are selected as 5 μH and 6.5 μH, respectively. Contours for system operating conditions are analyzed, giving in-depth understanding of the optimization process, which also confirms the fact that highest quality factor design for coil does not necessarily guarantee the highest system efficiency. The total loss on GaN transistors at full power is close to 100 W and comparable to the loss on coils, which needs special attention for thermal management and will be discussed in the next chapter.

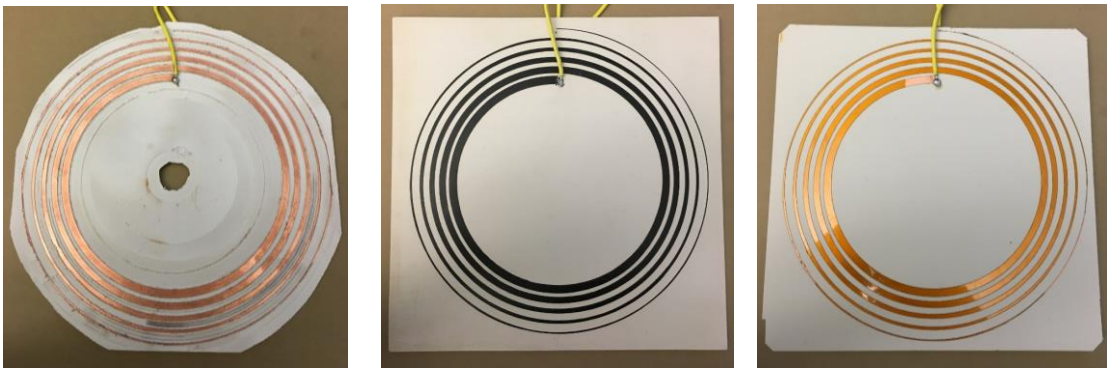
CHAPTER 6. THREE-LAYER COIL FABRICATION AND SYSTEM EXPERIMENTAL RESULT

6.1 Coil Fabrication Process and Characterization

6.1.1 Coil Fabrication Process

With the system operating point determined, two three-layer non-uniform SR coils have been fabricated with RO3003 laminates. The transmitter coil has inner radius r_i = 79.5 mm, N = 4 turns, and copper trace widths w_1 = 14.0 mm, w_2 = 19.8 mm, and w_3 = 18.0 mm. For the receiver coil, r_i = 106.7 mm, N = 4, w_1 = 6.3 mm, w_2 = 17.0 mm, and w_3 = 13.6 mm. A t = 2 oz layer of copper cladding on the dielectric is used to form the spiral traces.

Different fabrication methods have been tested first on a scaled-down r_o = 100 mm coil, as shown in Fig. 110. The first method involves only mechanical milling and drilling on the copper cladding of the laminates and no chemical exposure is needed. However, with only 2 oz copper thickness, it is hard to keep an absolute horizontal position of the laminates during the fabrication. In fact, the mechanical stress on the laminates when milling will cause strain in material and lead to an even worse horizontal placement. The fabricated coil spiral edge is ragged, and the process is time-consuming for larger coils. The other two methods use liquid acid solution to etch the spiral patten, with the difference on how to coat the spiral trace. As shown in Fig. 110(b), one method applies paint to cover the whole surface and uses laser to vaporize paint from the unwanted copper area for acid etching. The laser vaporization process is time-consuming considering the micrometer level laser width. Also, to remove the paint from the spiral trace after etching, chemical paint remover is required, which may degrade the laminate's dielectric properties and cause increased coil resistance. Instead of paint, the final method uses film tape for copper



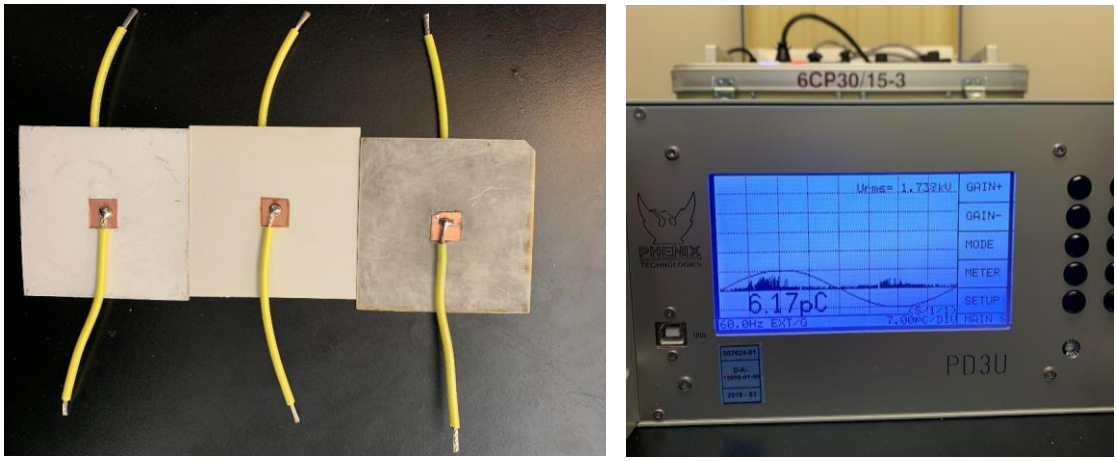
(a) (b) (c)

Fig. 110. Coil fabrication methods (a) CNC milling (b) paint + laser etching (c) tape + laser cutting

protection, and only the spiral outline needed to be cut instead of the area. Although the taping process requires extra caution to avoid accidental air bubbles, the fabrication process is relatively fast, with smoother coil trace outlines compared to mechanical milling.

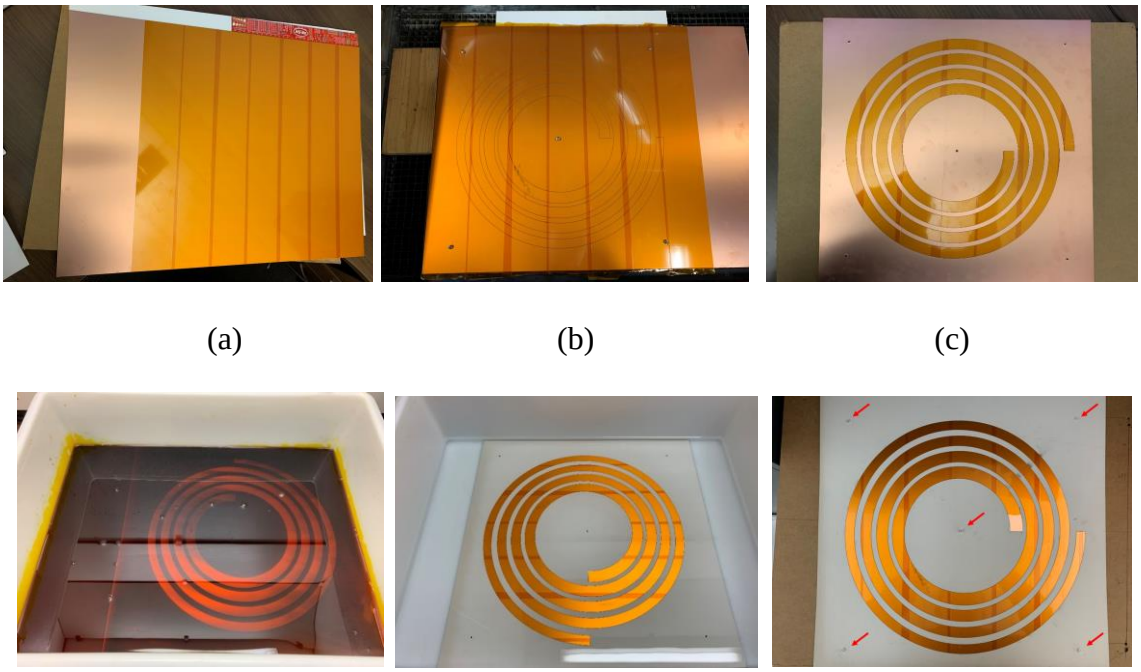
The voltage insulation capability is another concern for the coil fabrication. The dielectric laminate RO3003 is rated for 300 V/mil. To check for degradation due to chemical exposure, a Phenix 6CP30/15-3 AC dielectric test set is used for dielectric strength measurement. For the three fabrication methods mentioned above, partial discharge is measured with increasing sinusoidal voltage excitation as shown in Fig. 111. The fabricated sample with tape and laser cut passed the partial discharge test at 30 pC discharge with the highest 4.4 kV RMS voltage, which is 2 times larger than the 1.9 kV RMS voltage on coil at full power and verifies the robustness of the laminates. For the other two methods using milling or paint and laser etching, the 30 pC discharge is reached at 3 kV and 4 kV, respectively. Comparing the fabrication feasibility and associated material degradation, tape with laser cut in Fig. 110(c) is selected as preferred method for coil fabrication.

The 200 mm radius full-scale coils are fabricated using laser cutting and chemical etching with the following steps shown in Fig. 112. Polyimide film tape from 3M is first used to cover the entire copper cladding of the laminate. The tape is dimensionally stable at the high temperature, flame retardant and chemical resistant to prevent any damage on the outline of copper trace during the cutting or etching. Then, a very low power laser is used to selectively cut the outline of spirals, leaving only the spiral coil area covered to protect the copper for the acid etching. Ferric Chloride solution serves as the etching liquid and continuous agitation is applied for faster rate of reaction. After the spirals are fully etched,



(a) (b)

Fig. 111. Dielectric strength test (a) tested samples with different fabrication methods (b) test setup



(a) (b) (c)

(d) (e) (f)

Fig. 112. One three-layer coil fabrication process (a) film tape on laminates (b) laser cut for coil outlines (c) film tape removal (d) acid etching (e) water and IPT wash (f) three-layer coil matching and assembly

the coil is cleaned with isopropyl alcohol and deionized hot water, then baked for 1 hour in a 150 °C heat chamber. The three spiral patterns on top, middle, and bottom layers of a 3-layer coil are center aligned for an accurate resonant capacitance control with plastic screws. The three layers of the finished receiver coil are shown in Fig. 113.

For each coil, the 3-layer structure is held together with nylon screws. Quarter-inch thick polycarbonate sheets are applied for better clamping and half-inch polycarbonate bars are used to control the air gap between two coils. Based on the creepage requirement from UL60950, a 20 mm clearance is kept from all holes in the laminates and polycarbonate parts to any copper traces for a 2 kV RMS voltage. The minimum clearance is drawn with red outlines in Fig. 114(a), with 20 mm distance to coil outlines in white. Also, keeping the 20 mm clearance guarantees that additional dielectric loss from the polycarbonate is minimal. The dielectric loss brought by the polycarbonate is simulated in HFSS as shown in Fig. 114(b), with only 2% increase in ESR for each coil.

Fig. 115 shows the completed coils with mechanical support for testing, with 100 mm airgap between two coils.

6.1.2 Coil Characterization

TABLE XIV shows the comparison between modeled, simulated, and measured coil parameters. The model is based on analysis supplemented with 2D magnetostatic FEA using FEMM. The HFSS simulation uses 3D electromagnetic FEA to verify the resonant behavior, with impedance curve around the resonant frequency plotted in Fig. 116.

The fabricated coils have quality factor 417 and 452 on the primary and secondary, respectively, with less than 10% error from theoretical design point. Due to the impacts from both contact resistance and lead wires, the fabricated coils have slightly larger ESR

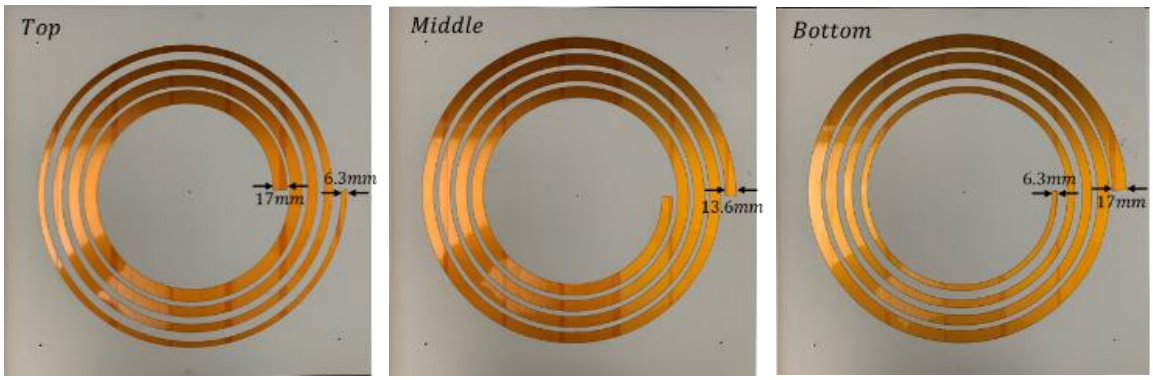
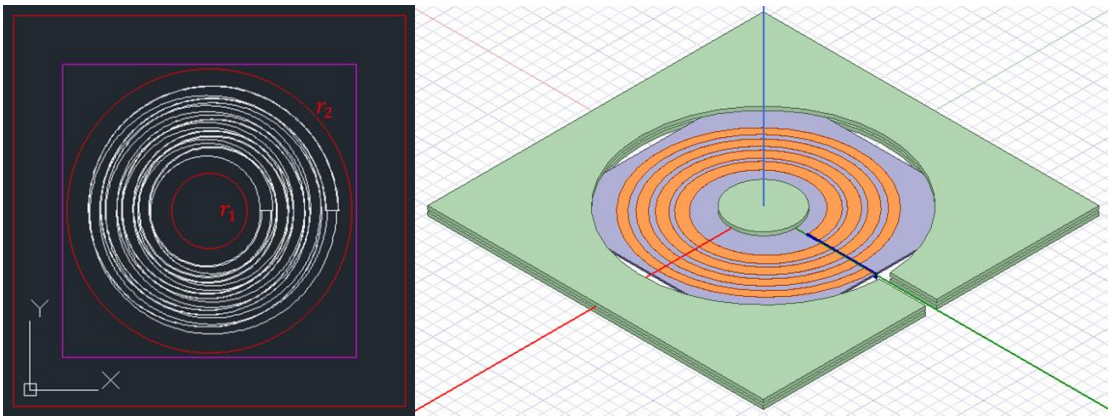


Fig. 113. Completed three copper layers for the receiver coil



(a) (b)

Fig. 114. (a) mechanical design for clamping polycarbonates (b) HFSS simulation for coil with clamping polycarbonates

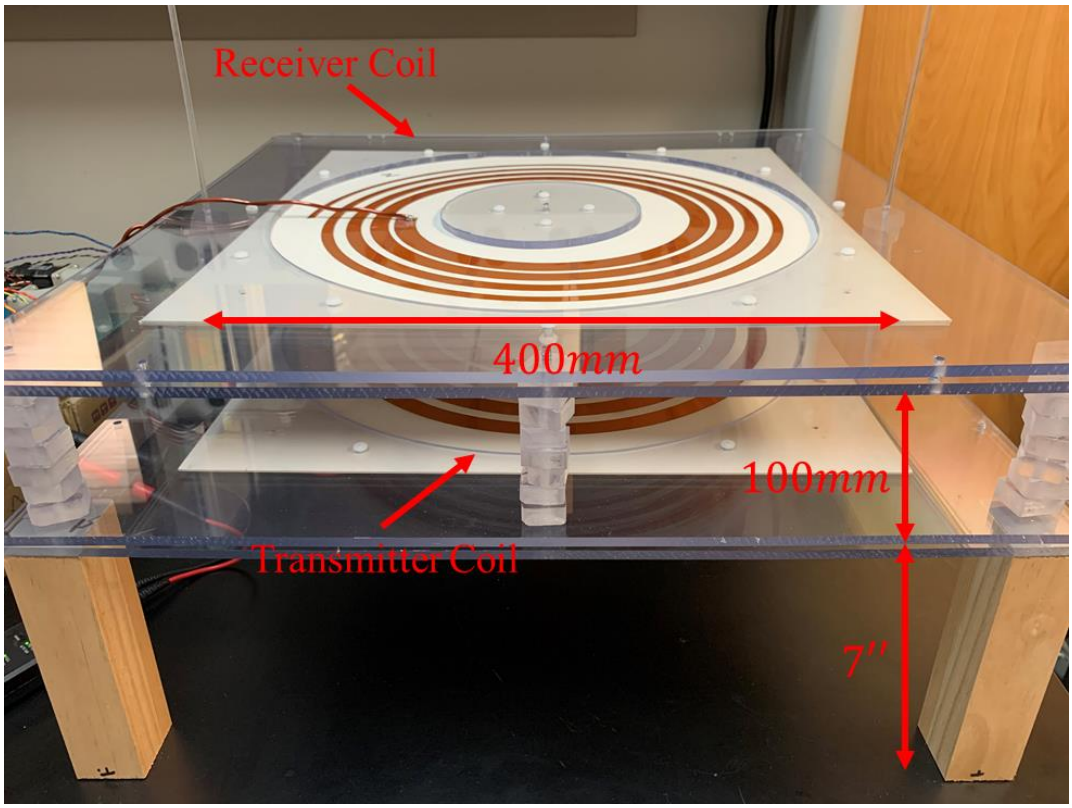
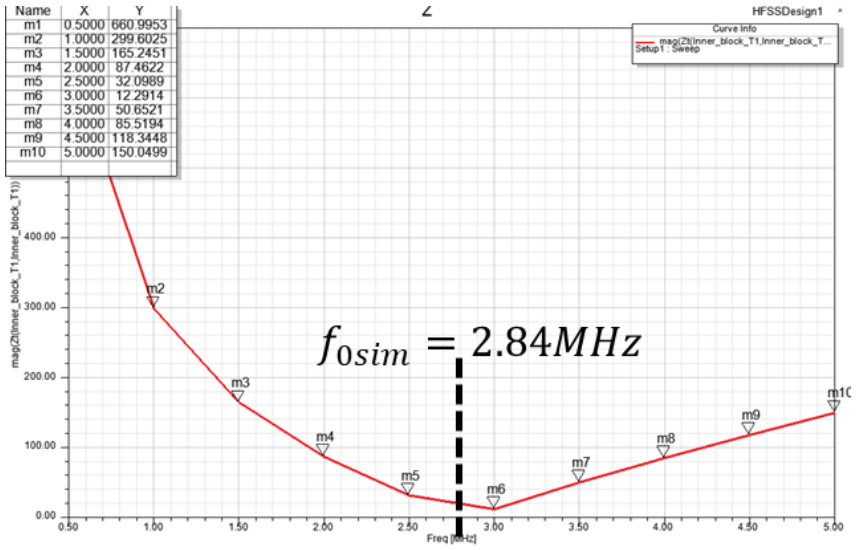
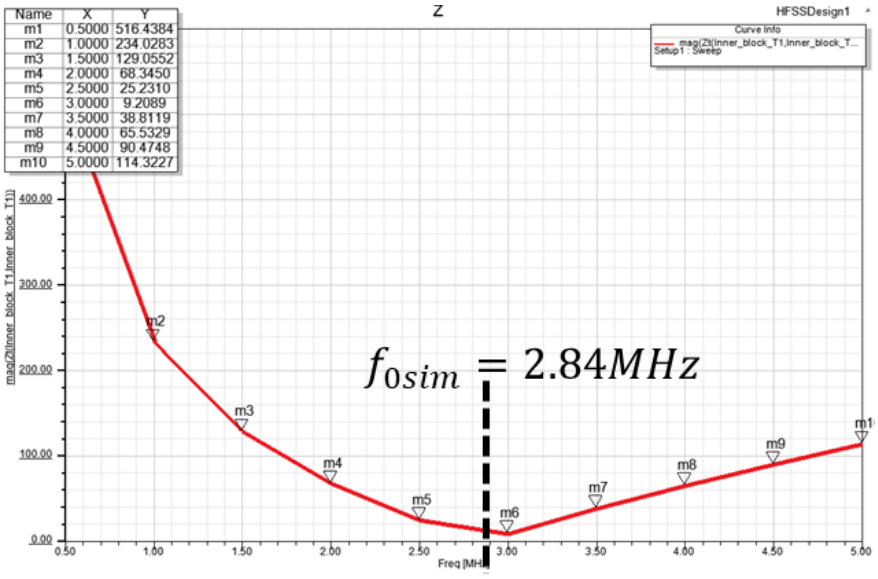


Fig. 115. Fabricated coils with mechanical setup



(a)



(b)

Fig. 116. Impedance results in HFSS simulation (a) transmitter coil (b) receiver coil

TABLE XIV. SR Coils Characterization and Comparison

	Model	**HFSS simulation**	**Impedance analyzer**
	Transmitter coil		
f_0 [MHz]	3	2.8	3
L [μH]	5	5.3	5.2
R [Ω]	0.224	0.220	0.235
Q	421	427	417
	Receiver coil		
f_0 [MHz]	3	2.8	3.21
L [μH]	6.5	6.8	6.7
R [Ω]	0.284	0.278	0.301
Q	432	435	452

compared to the modeling and HFSS simulation results.

The connecting wires between the power stages and coils also suffer from high ac loss at MHz, especially when conventional multi-strand wire is used. In Fig. 117, two connecting setups with either stranded wire or solid wire are tested with similar total length, and the measurement results are listed in TABLE XV, including comparison on ESR, inductance, and mutual inductance.

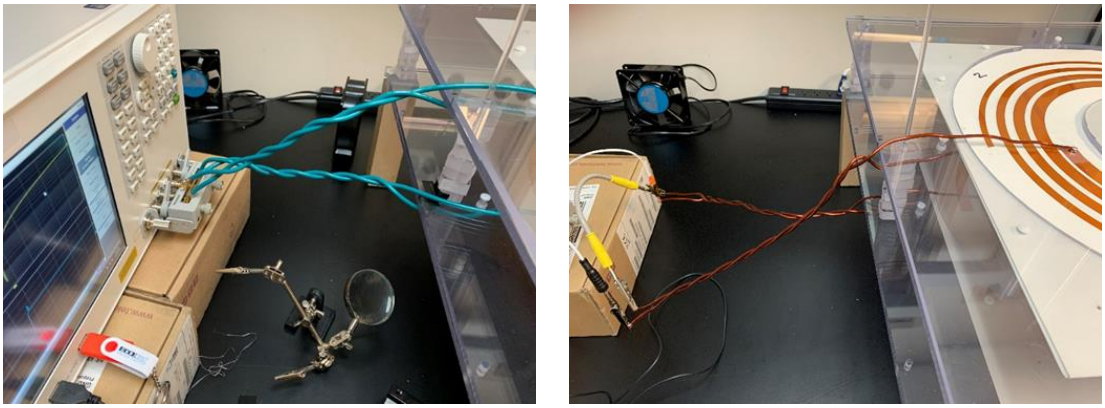
Compared to the stranded wire, the solid wire can substantially increase the quality factor of two coils which minimizes the impact from the connecting wires. In final design, MW16-C AWG 8 solid wires are used, with preferred 240 °C maximum working temperature and 3.5 kV dielectric breakdown voltage compared to 105 °C and 1 kV for stranded wires.

The designed coils have also been validated in COMSOL thermal simulation in Fig. 118, with 90 W calculated loss at transmitter coil and 45 W loss at receiver coil for a 6.6 kW system power output. The heat sources are assigned for layers separately in each coil based on the modeled current density distribution. Ambient temperature is set as 30 °C, with 10 W/m^2K heat transfer coefficient assumed for air in natural convection. The maximum temperature points reach 70 °C and 53 °C for each coil.

6.2 Hardware PCB Design

6.2.1 Gate Driver Design

Gate drivers with low-dropout regulators (LDOs) have been adopted for the PCB based on the following considerations. For the conventional bootstrap gate driver, the bootstrap

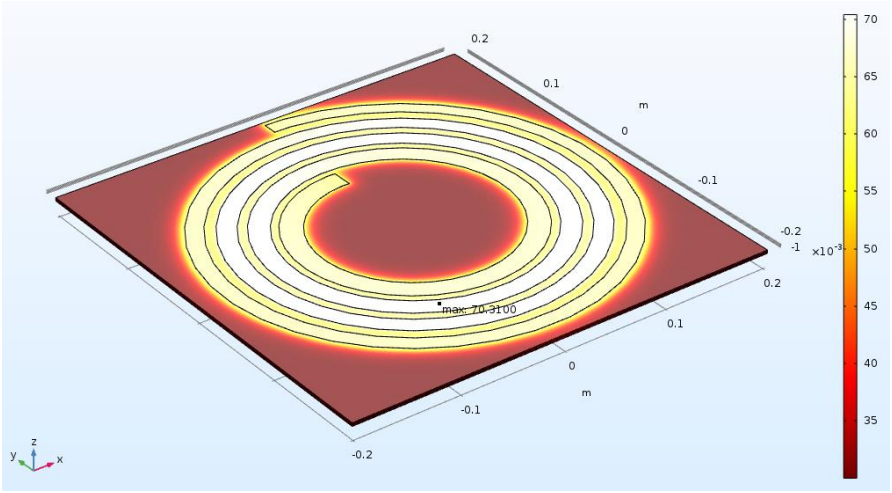


(a) (b)

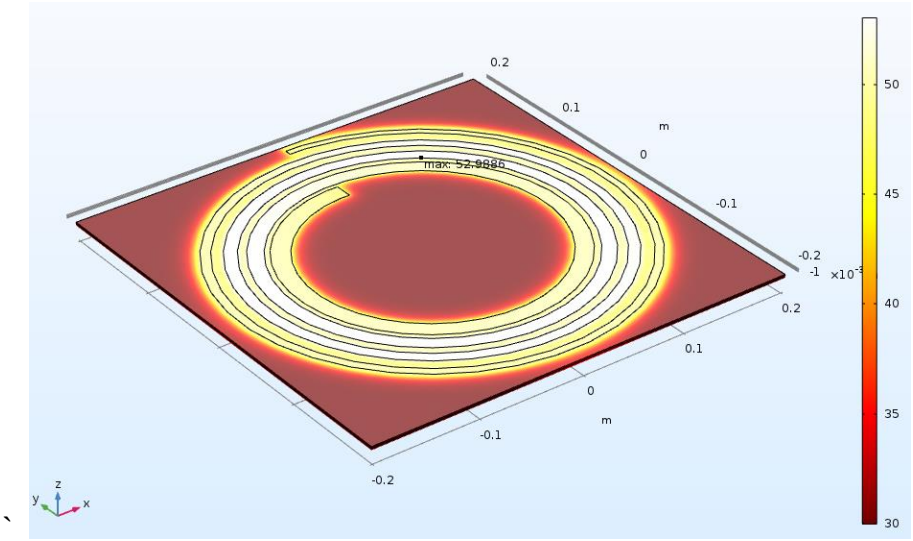
Fig. 117. Connecting wires between power stages and coils (a) stranded (b) solid

TABLE XV. SR Coils Measurements with Connecting Wires

	Coils	**Coils with stranded wires**	**Coils with solid wires**
	Transmitter coil		
f_0 [MHz]	3	2.92	2.98
L [μH]	5.2	5.59	5.62
R [Ω]	0.235	0.343	0.285
Q	417	299	382
	Receiver coil		
f_0 [MHz]	3.21	2.86	2.90
L [μH]	6.7	7.14	7.12
R [Ω]	0.301	0.395	0.312
Q	452	325	416
	Two Coils		
M [μH]	NA	1.68	1.62
k	NA	0.265	0.255



(a)



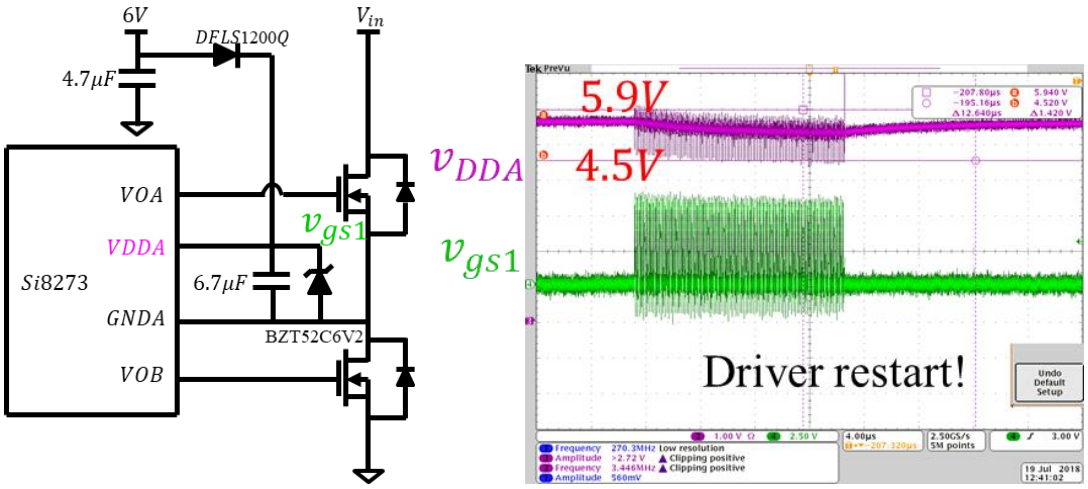
(b)

Fig. 118. Thermal simulation for coils in COMSOL

diode often cannot fulfill the requirement of MHz switching frequency and high blocking voltage. For an initial gate driver design of a 100 V input voltage, 100 W output power system in Fig. 119, for example, the bootstrap capacitor voltage V_{DDA} drops from the nominal 6 V to less than 4.9 V due to the junction capacitance and forward voltage of bootstrap diode, which continuously triggers the UVLO protection in Si8273 gate IC. In a 6.6 kW system, the blocking voltage for the bootstrap diode would be greater than 1 kV, making it even harder to stabilize the gate voltage. Considering all the factors above, isolated power supplies are used to power the devices to avoid using a high voltage diode with high junction capacitance and slow recovery time.

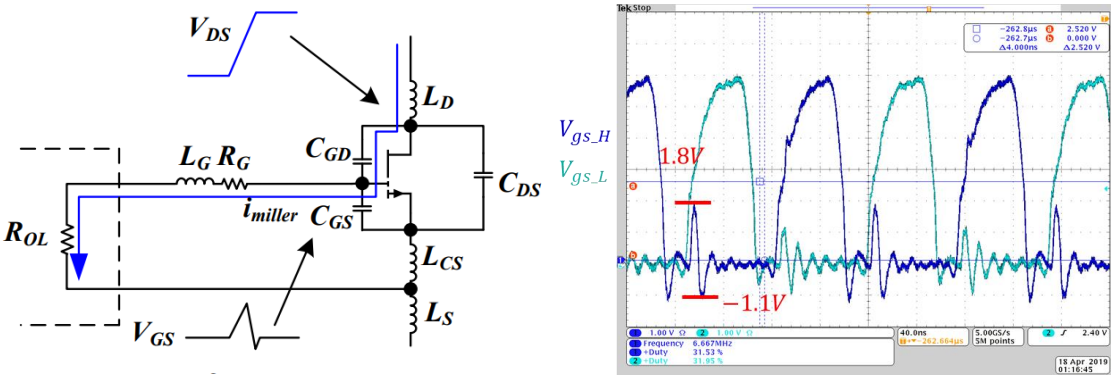
Also, to attenuate the cross-talk issue at high dV/dt at the switching node, -3 V gate voltage for turn-off should be used to avoid false turn-on and possible shoot-through. In Fig. 120, a 1.8 V voltage spike is observed when input voltage is 30 V at hard-switching condition, which is already greater than the 1.7 V threshold gate voltage for the device. Any slight non-ZVS operation at higher power could accidentally cause shoot-through.

The revised gate driver design using LDOs with +6/-3 V voltage is shown in Fig. 121, with one 9 V and one 3 V LDO. Note that a 3 V Zener diode is added at the 3 V LDO output terminals to clamp the gate voltage. As shown in Fig. 122, without the Zener diode, the voltage of 3 V LDO is shifted to 5 V in a conduction test when DC current is 25 A, which is caused by the very limited power absorption capability at output terminals of LDOs. Considering the total 9 V clamping voltage, the turn-on voltage is forced to drop from 6 V to 4 V. This phenomenon would be catastrophic during the high power test because both forward and reverse conduction loss of GaN transistors would increase significantly. In addition, to avoid excessive heating near the IC, an 8.2 Ω resistor is



(a) (b)

Fig. 119. Bootstrap gate driver (a) circuit diagram (b) oscillation in gate voltage



(a) (b)

Fig. 120. (a) Cross-talk mechanism in gate driver circuit (b) voltage spike by cross-talk, V_{in} = 30 V, f_s = 6.67 MHz

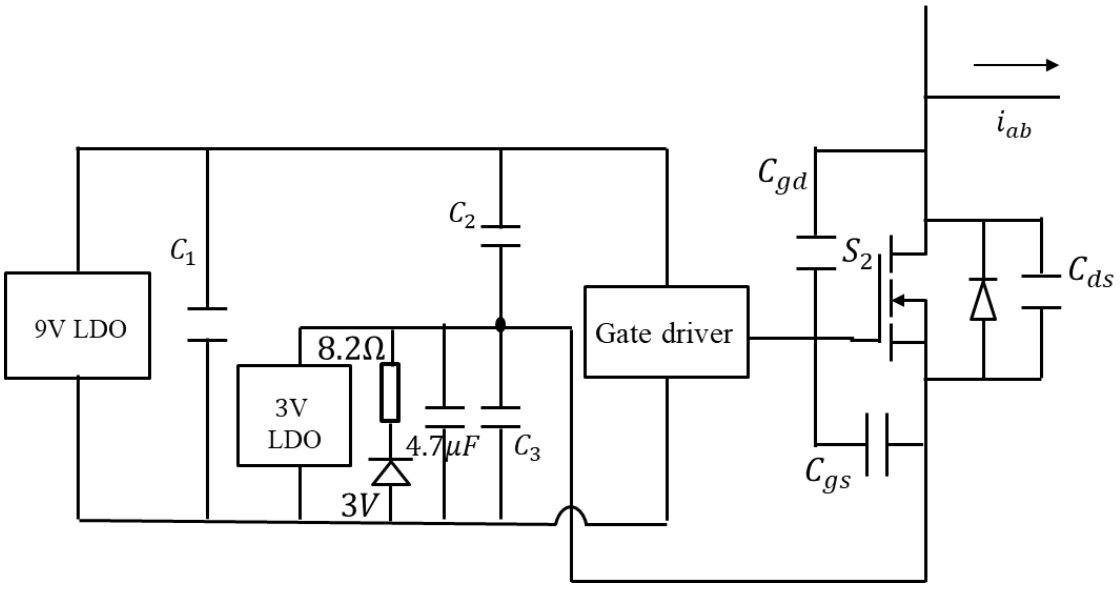
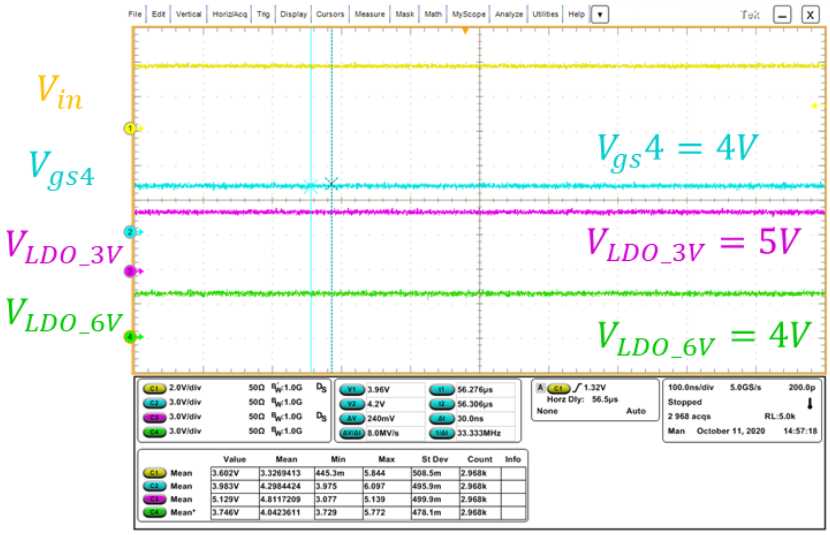
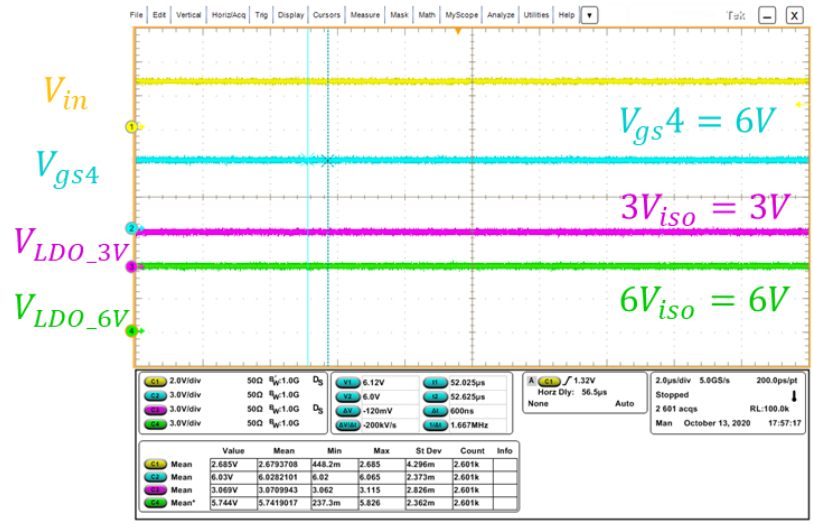


Fig. 121. Gate driver circuit design with LDOs



(a)



(b)

Fig. 122. Gate driver voltages in device forward conduction test (a) without Zener diode (b) with Zener diode

connected in series with the Zener diode.

6.2.2 PCB Parasitics

The parasitic parameters in the PCB have a direct impact on the system operating point and efficiency for a MHz converter. Their existence in the power loop and gate loop affects the quality of gate signals and may cause unexpected voltage ringing or a possible device failure. They need to be carefully designed to improve system efficiency and quantified for an accurate system loss model.

The parasitic parameters in the PCB are found by simulation in Q3D. For the PCB designed in Altium Designer, the model is exported to Q3D through SIwave conversion, including the copper trace, via, and polygon. All parameters are simulated at 3 MHz.

(a) Inductance

The power loop inductance L_{ds} is simulated in Fig. 123 with excitation defined at the device's drain and source terminal pad, with L_{ds} = 2.24 nH.

The gate driver loop inductance is found separately for turn-on and turn-off transient as shown in Fig. 124, with L_{gate_on} = 7.28 nH, L_{gate_off} = 6.95 nH.

Note that the gate loop inductance is, in fact, much larger than the power loop inductance although the footprint for the gate loop is much smaller. This is mainly caused by the large vertical distance between the device on the top layer and gate driver on the bottom layer of the PCB. Due to the large size of heatsink, the space is limited on the top layer for the gate driver IC, which is taller than the GaNFET package.

(b) Capacitance

Because of the overlapping area of copper polygon between layers of the PCB, there are parasitic capacitances that affect the operating condition of the converter as depicted in

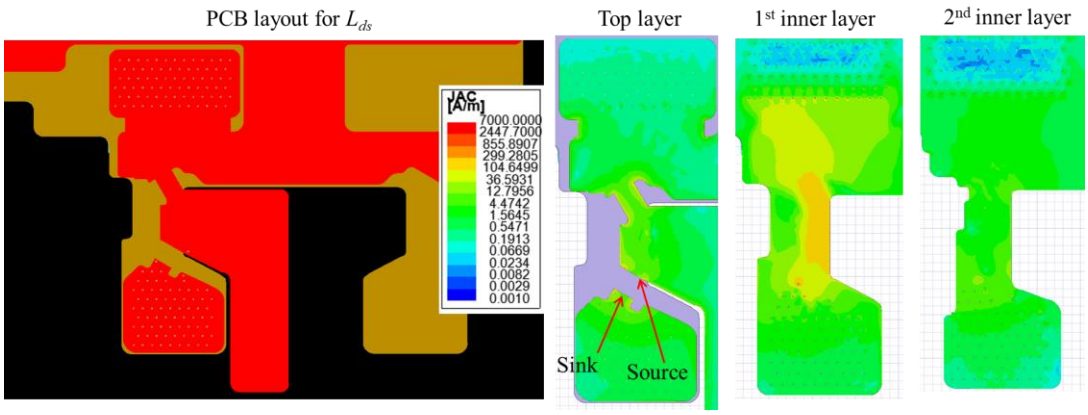


Fig. 123. PCB extraction and Q3D simulation for L_{ds}

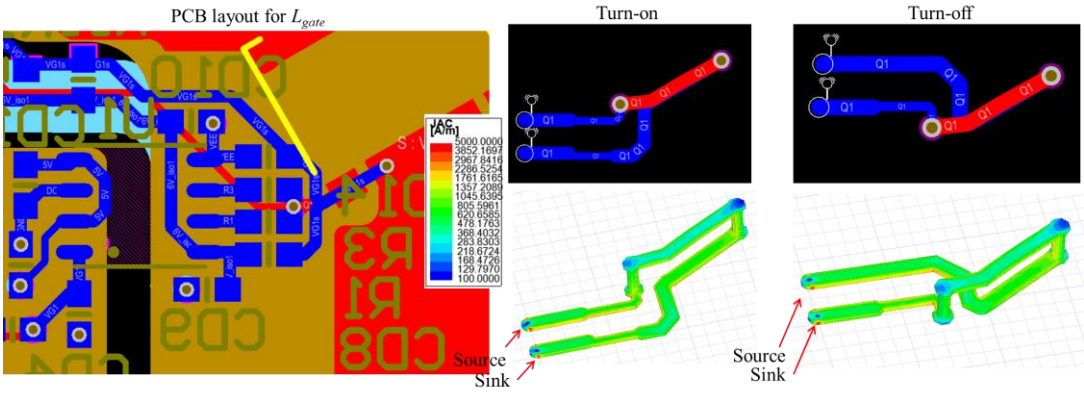


Fig. 124. PCB extraction and Q3D simulation for L_{gate}

Fig. 125. For the inverter side, the capacitance generated between the switching node to positive or negative power bus directly affects the ZVS condition for GaN devices. Any additional capacitance would require more time or higher current to fully charge or discharge the output capacitance of the devices during the ZVS transient. For the rectifier side, switching node capacitance could also increase the secondary side current magnitude and lead to a higher loss. The calculated system operating point and other calculated losses will also shift if parasitic capacitances are not included in the model.

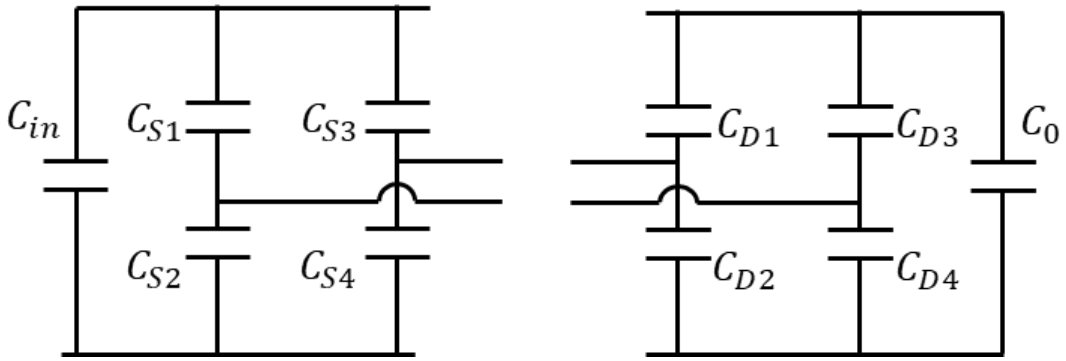
To have better reduction in parasitic capacitance, two versions of PCB have been designed and implemented as shown in Fig. 126 and Fig. 127.

TABLE XVI summarizes the measurement result of PCB capacitance. Since the parasitic capacitors are either connected in series or parallel, the measured capacitance value at any two nodes is not the actual value, and needs further conversion based on the circuit derivation for actual parasitic capacitance on PCB. Based on the calculation result, the overlapping area of copper polygon between switching node to positive or negative power bus has been intentionally reduced in the second version PCB.

The residual capacitance in PCB v2 is inevitable due to the overlapping of power loop in vertical direction and switching node terminal in horizontal direction. There is always a tradeoff between small parasitic capacitance, small power loop and gate loop, and enough copper area for switching node heat dissipation. Note that there exists a small negative value for capacitance between switching node and positive power bus caused by the measurement error brought by the large ratio between C_{in} and C_{S1}(C_{S3}), C_o and C_{D1}(C_{D3}).

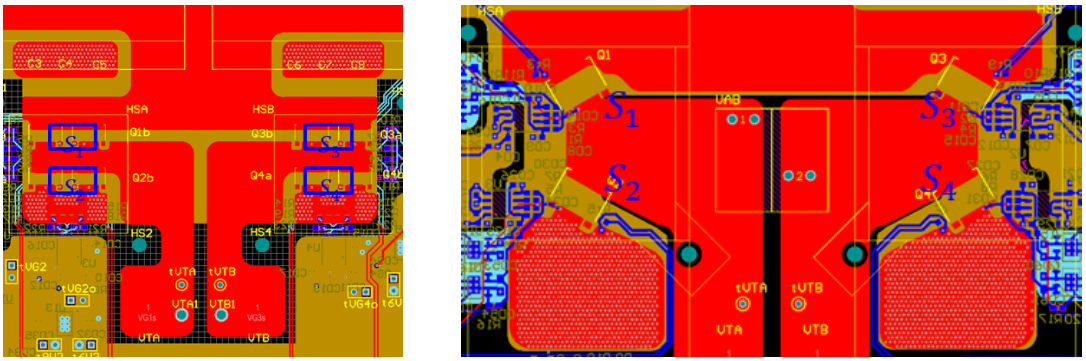
(c) Resistance

In Fig. 128 and Fig. 129, the ESR in the current loop on PCBs is simulated for both



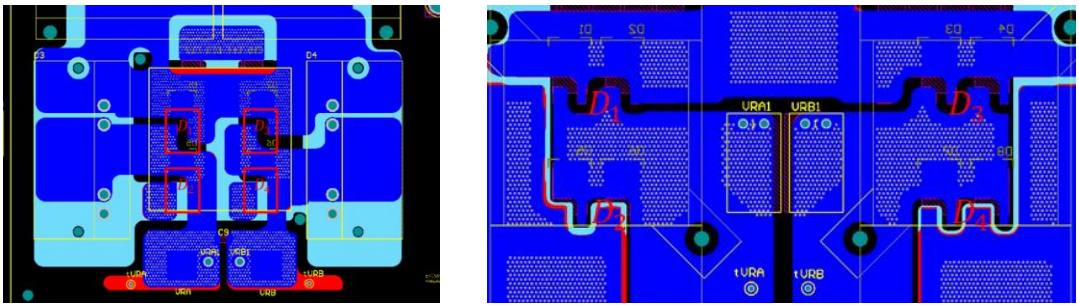
(a) (b)

Fig. 125. PCB parasitic capacitors equivalent circuit for (a) inverter and (b) rectifier



(a) (b)

Fig. 126. Inverter PCB comparison (a) first version, (b) second version



(a) (b)

Fig. 127. Rectifier PCB comparison (a) first version, (b) second version

TABLE XVI. PCB Capacitance Comparison between Two Versions of PCB

	PCB v1		PCB v2	
3 MHz	Measured terminal C	Calculated actual C	Measured terminal C	Calculated actual C
C_{S1} [pF]	184	**-0.3**	33.2	**-6.4**
C_{S2} [pF]	198	**198.3**	33.7	**40.1**
C_{S3} [pF]	188	**3.8**	32.8	**-11.6**
C_{S4} [pF]	202	**198.2**	33.4	**45.0**
C_{in} [pF]	2610	**2607**	3090	**3113**
C_{D1} [pF]	313	**-1.1**	9.48	**-4.2**
C_{D2} [pF]	351	**352.1**	9.54	**13.7**
C_{D3} [pF]	331	**1.9**	8.93	**-2.8**
C_{D4} [pF]	373	**371.1**	8.98	**11.8**
C_o [pF]	2910	**2909**	2650	**2609**

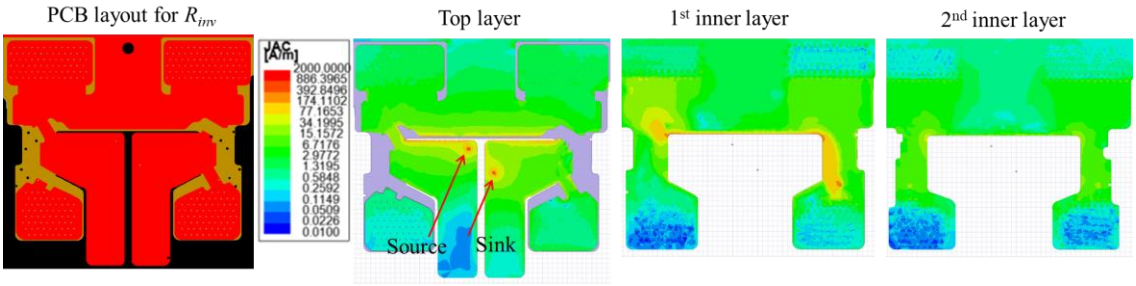


Fig. 128. PCB extraction and Q3D simulation for R_{inv}

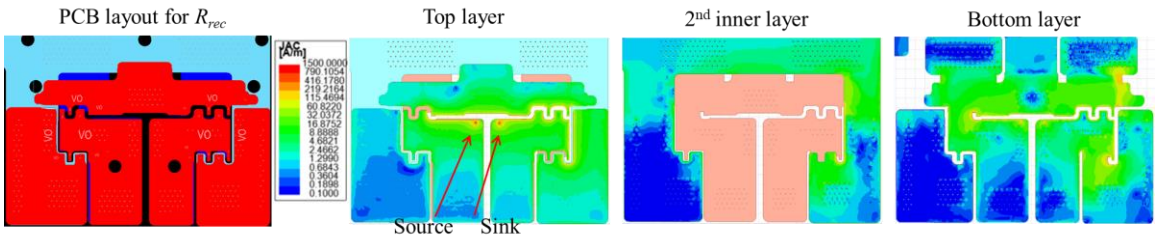


Fig. 129. PCB extraction and Q3D simulation for R_{rec}

inverter and rectifier. The resistance is measured at the switching node, with one pair of devices in diagonal position shorted. The terminals for input and output DC voltages are also shorted to form the complete current loop. R_{inv} = 14.8 mΩ, and R_{rect} = 15.2 mΩ, completing the system loss model.

6.3 Thermal Management

6.3.1 Forced-air Cooling with Heatsink and Air Duct

As discussed in Chapter 5, approximately 25 W loss per GaN transistor is expected when output power is 6.6 kW. To effectively dissipate the heat from the device and prevent thermal runaway, heatsinks with forced-air cooling are applied for both the inverter and rectifier PCB boards.

A number of candidate thermal interface materials (TIM) between the heatsink and the device package are listed in TABLE XVII from manufacturers 3M and BERGQUIST. There are generally three types of TIMs, including adhesive, gap pad, and phase change. Adhesive TIMs provide easy installation without need for constant pressure, but the thermal conductivity is often sacrificed due to the addition of adhesives into the material. Non-adhesive gap pad has the highest thermal conductivity but requires a proper mounting mechanism to keep a constant pressure between the heatsink and the PCB. The phase change material is capable of wetting the contact interface between different materials to provide most consistent thermal performance, and its thermal conductivity lies between the adhesive and gap pad TIMs. Mounting with pressure is also needed for the phase change material.

TABLE XVII. Thermal Interface Materials

Part No.	Thermal conductivity [W]	Thickness [mm]	Dielectric strength	Dielectric constant	Adhesive
8810	0.6	0.125-0.5	26 kV/mm	3.0-3.5	Yes
5571	2.0	0.75-2.0	13 kV/mm	NA	One side
5590PI	3.0	0.2	8 kV	NA	One side
5519	5.0	0.5-2.0	2 kV/mm	NA	Yes
5578H	3.5	0.5-1.0	19 kV/mm	NA	Yes
Bondply-100	0.8	0.127-0.279	30 kV/mm	NA	Yes
SIL-PAD 1500ST	1.8	0.203	3 kVac	6.1	Yes
GAP3000S30	3.0	0.254-3.175	3 kVac	7	Yes
HC5000	5.0	0.508-3.175	5 kVac	8.0	Yes
HF300P (phase change)	1.6	0.102-0.127	5 kVac	4.5	No/one side
3500S35 (gel)	3.6	NA	10 kV/mm	8.0	No

HC5000 from BERGQUIST is selected for its high thermal conductivity with natural inherent tack on both sides of the material, and the 5 kV dielectric strength also fulfills the insulation requirement. The complete list of components for the thermal management system is shown in TABLE XVIII.

The parasitic capacitance brought by the heatsink is negligible as shown in Fig. 130 if 0.5 mm thickness is selected for HC5000,

$$C_{leg} = \frac{1}{2} \times \varepsilon_0 \times 8 \times \left(\frac{8.27mm \times 5.64mm}{0.5mm} \right) = 3.3pF \tag{60}$$

To have the best utilization of air flow from fans and to guarantee a laminar flow through the fins on the heatsink, a customized air duct is designed and fabricated with a 3D printer. The printing material is FLHTAM02 from FORMLABS [108], with 238 °C heat deflection temperature at 0.45 MPa external pressure after the proper post-cure in a thermal chamber. Fig. 131 illustrates the designed air duct with assembly position on the PCB boards together with the fans. Fig. 132 gives the 3D printed air duct and final hardware assembly.

Considering the insulation requirement and to prevent metal scraping the PCB soldermask, plastic screws and nuts are used together with Loctite 2620 to prevent loosening caused by fan vibration.

6.3.2 Thermal Test Results

To validate the thermal dissipation capability of the proposed cooling system, a reverse conduction test is performed with high DC current for the inverter with -3 V gate voltage. The temperature at the surface of the heatsink is captured by the infrared thermal camera. Up to 70 °C on the heatsink, a total of over 130 W loss is dissipated from four GaN transistors as shown in Fig. 133. Note that the power loss from test is about 15% higher

TABLE XVIII. Selected Thermal Management Bill of Materials

Name	Part number	Quantity	Parameters
Heatsink	ATS-FPX035035035	4	fine-pitch straight, 35x35x35 mm^3
Thermal pad	HC5000	4	5.0 W/(m-K), 35x35x0.5 mm^3
Air duct material	FLHTAM02	4	Heat deflection temp 238 °C @0.45 MPa
Fan	GFC0412DS-TP01	4	12 W, 30.5 CFM

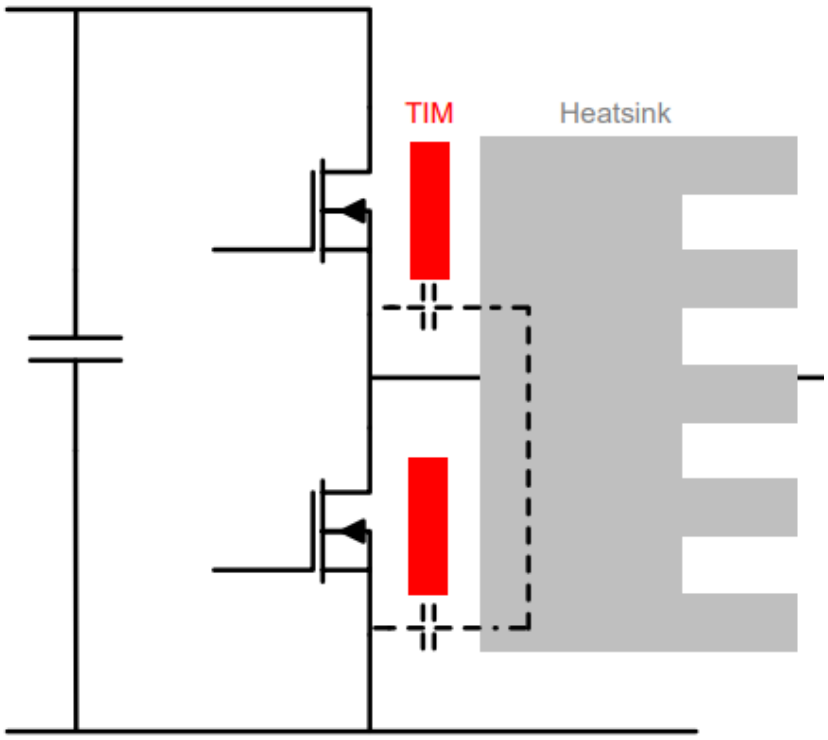


Fig. 130. Parasitic capacitance between the heatsink and device package in one phase leg

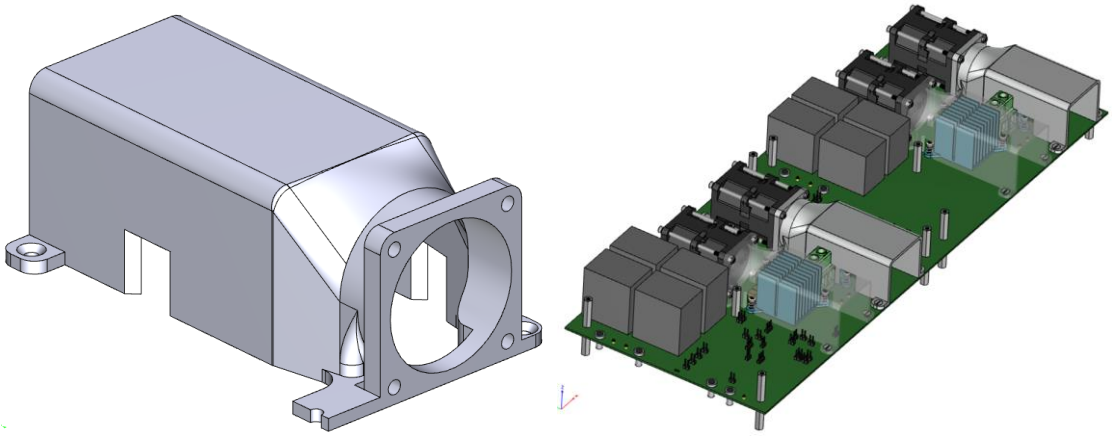


Fig. 131. 3D illustration of air duct on PCB boards

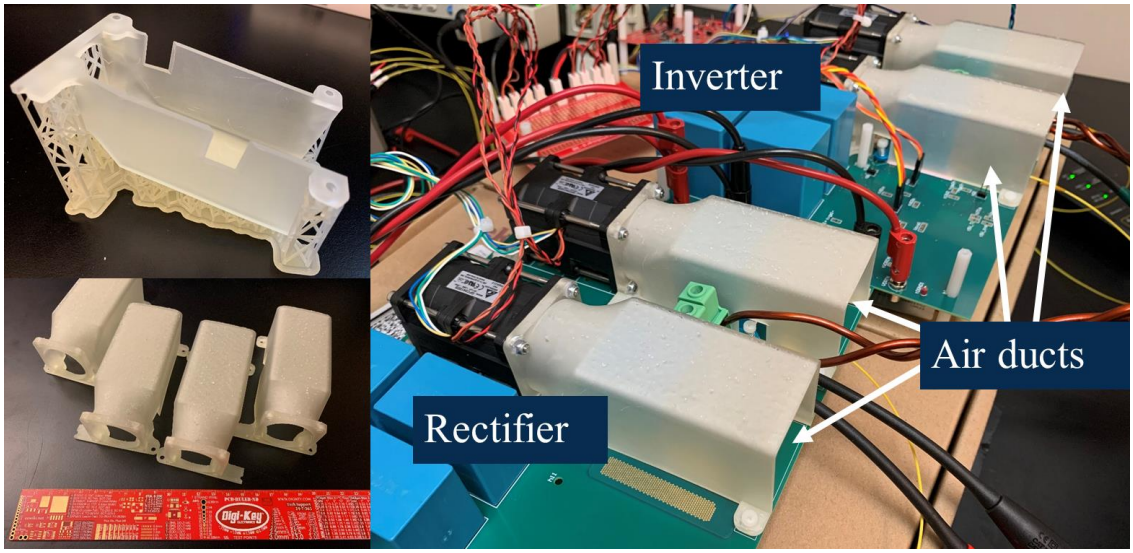
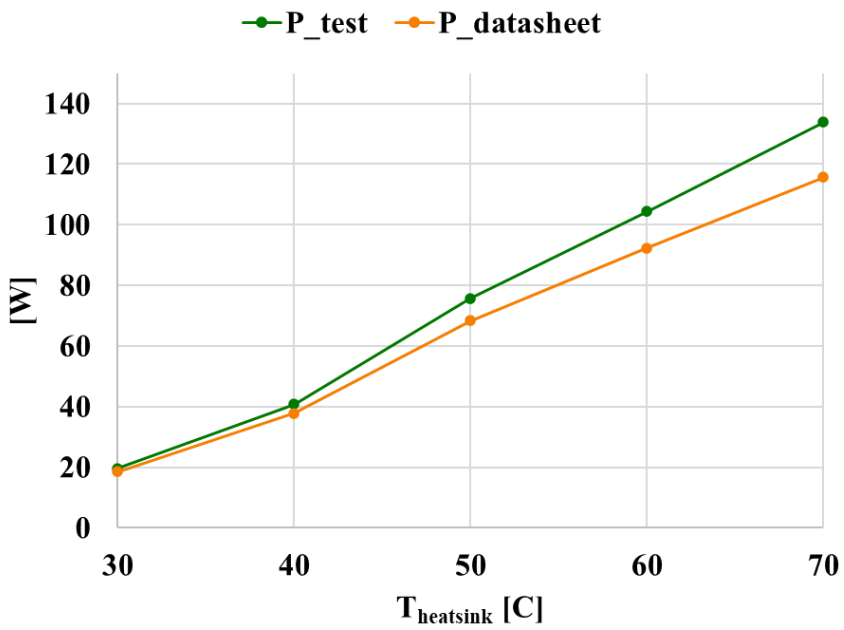
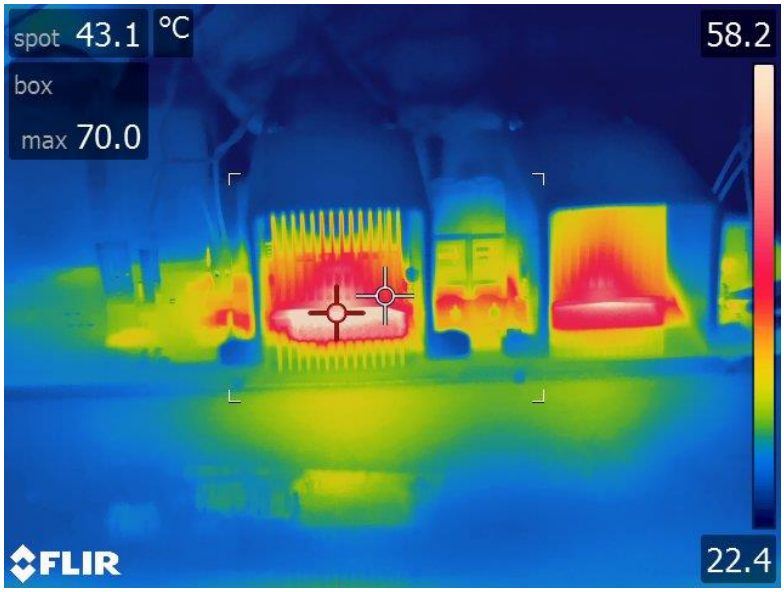


Fig. 132. 3D printed air duct installation on PCB boards



(a)



(b)

Fig. 133. Reverse conduction test result (a) total power loss vs temperature on the heatsink (b) thermal image at 70 °C

than the value from datasheet when the temperature is relatively high. There is also a 5-10 °C temperature difference between two phase legs mainly due to the difference of forward voltage in reverse conduction from transistors.

The equivalent thermal resistance circuit per phase leg is shown in Fig. 134, with the calculated thermal resistance value based on the datasheet.

$$R_{jc} = 0.27°C/W \tag{61}$$

$$R_{tim} = \frac{t}{Ak} = \frac{0.508mm}{8.27mm \times 5.64mm \times 5W/mK} = 2.18°C/W \tag{62}$$

To have a real-time overtemperature protection, a voltage divider using a thermistor is built to sense the temperature of a PCB trace in proximity to the GaN transistors. The sensed voltage fed to the DSP is shown in Fig. 135 for the four transistors compared with the captured heatsink temperature captured from the thermal camera under 24 A forward conducting current in the inverter. After calculating the equivalent thermal resistance between the heatsink and the device junction, Fig. 136 gives the relation between the junction temperature and the sensed thermistor voltage, which is monitored real-time during the system power tests to avoid any unexpected thermal runaway.

6.4 System Experimental Test Results

The system experimental setup is shown in Fig. 137. The power stage and coils are connected via solid wires with short length to minimized additional high frequency ac loss.

Operating waveforms at 6.6 kW output are given in Fig. 138, showcasing full ZVS for the GaN switches. With 80 Ω load resistance, 3.125 MHz switching frequency, and 35 ns

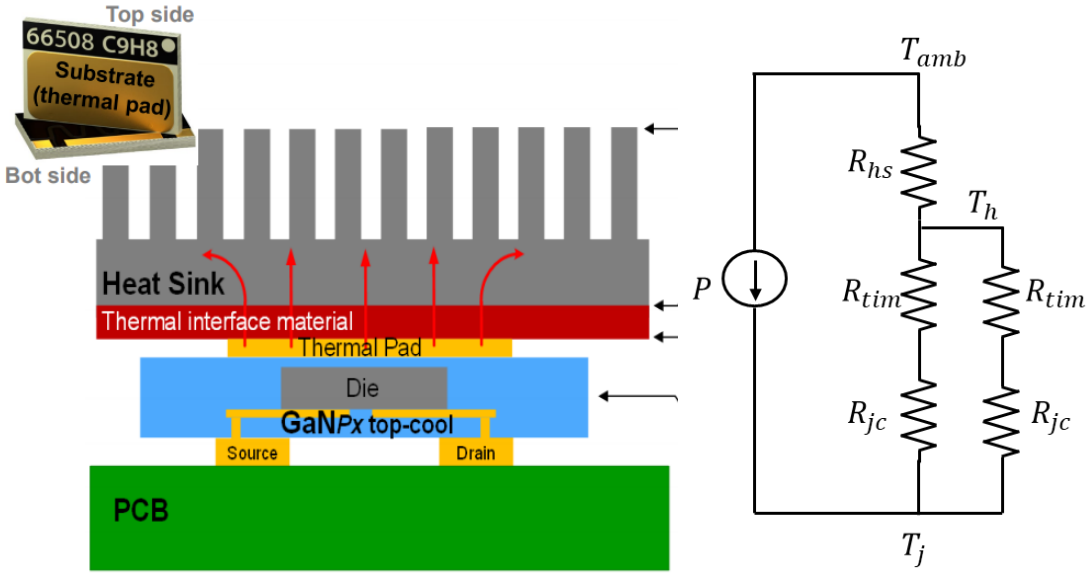


Fig. 134. (a) GaN transistor heat flow path (b) equivalent thermal resistance circuit for one phase leg with two GaN transistors

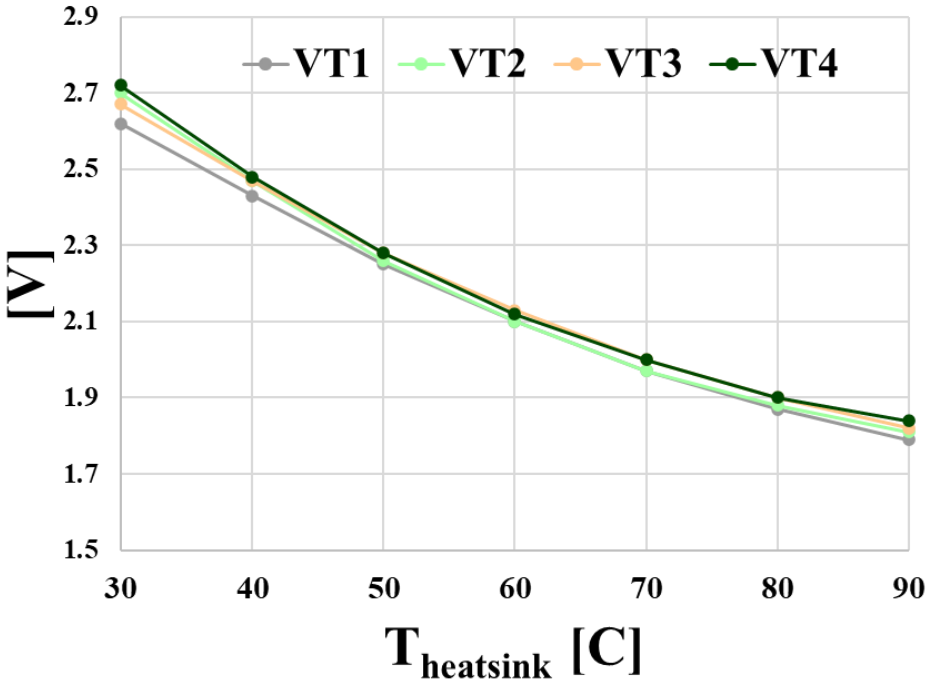


Fig. 135. Thermistor voltage vs heatsink temperature

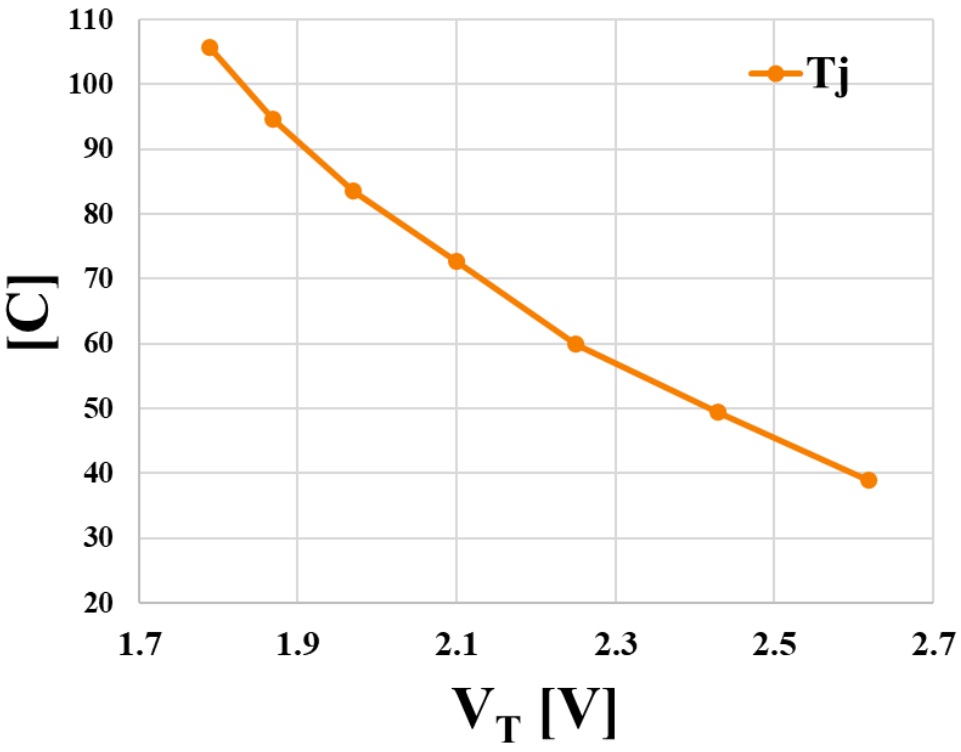


Fig. 136. Calculated GaN transistor junction temperature vs thermistor voltage fed to DSP

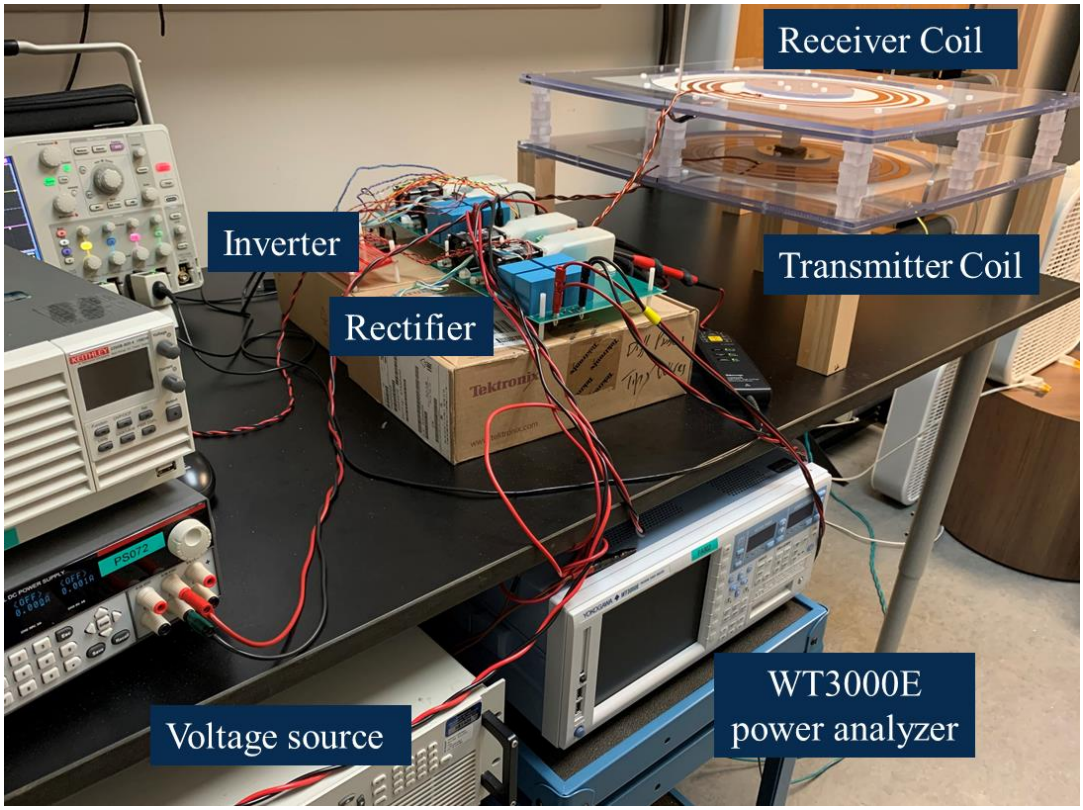


Fig. 137. System test setup with three-layer SR Coils

dead-time, the system efficiency is 95.2% measured with a Yokogawa WT3000E power analyzer. TABLE XIX compares the operating point at full power for modeling and test result with less than 5% difference.

The loss breakdown is calculated based on the tested operating condition for different output powers and is shown in Fig. 139. Note that at 6.6 kW power output, there is close to 100 W of loss in the GaN transistors which accounts for 34% of the total loss.

The varying current characteristic of the SR coil is also verified by the temperature distribution on the copper traces. As shown in Fig. 140, the decreasing temperature distribution from innermost turn to outermost turn of the transmitter coil indicates the decreasing current density in the copper trace.

The junction temperature of GaN transistors in the inverter and diodes in the rectifier is plotted in Fig. 141. The calculated results are based on the sensed voltage from the thermistor near the case of the GaN transistor. The diode case temperature is sensed by a fiber-optic thermal sensor attached to the surface of device TO-252 package. The maximum temperature of the GaN transistors at full power is well-regulated at 85 °C. Higher temperature is found for diodes due to the longer thermal transfer path from the bottom-cooled package and the heatsink on the other side of the PCB.

6.5 Summary

In this chapter, the optimized multi-layer SR coil and system designs are implemented with power tests to validate the concept of high frequency WPT system at MHz with compact and lightweight coil structure.

TABLE XIX. Operating Point Comparison for Modeling and Test Result

	Model	**Test**
Input voltage V_{1DC} [V]	502	501
Transmitter current I_p [A]	17.9	18.6
Load voltage V_{2DC} [V]	727	732
Receiver current I_s [A]	11.9	11.6

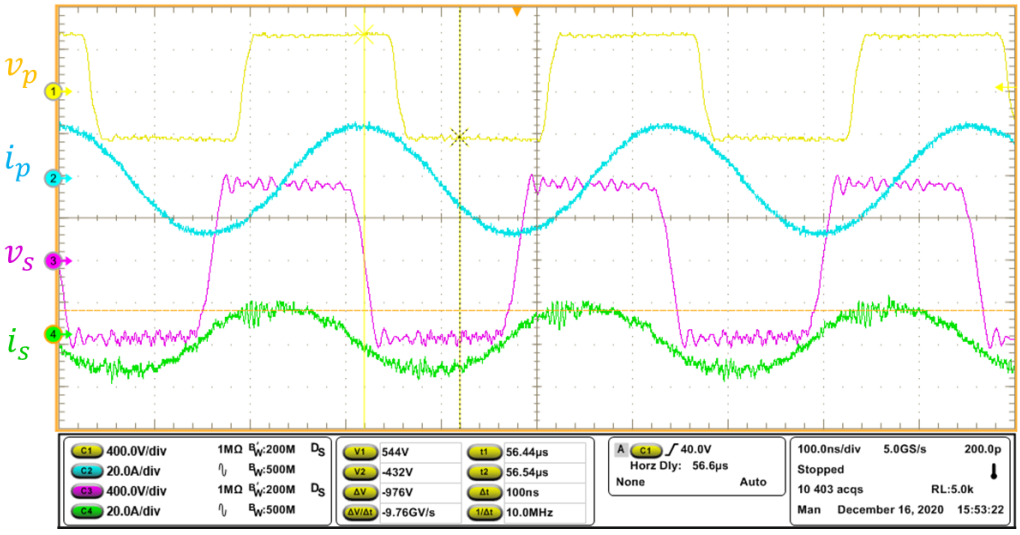


Fig. 138. Inverter output voltage v_p, current i_p, and rectifier input voltage v_s, current i_s, at 6.6 kW output

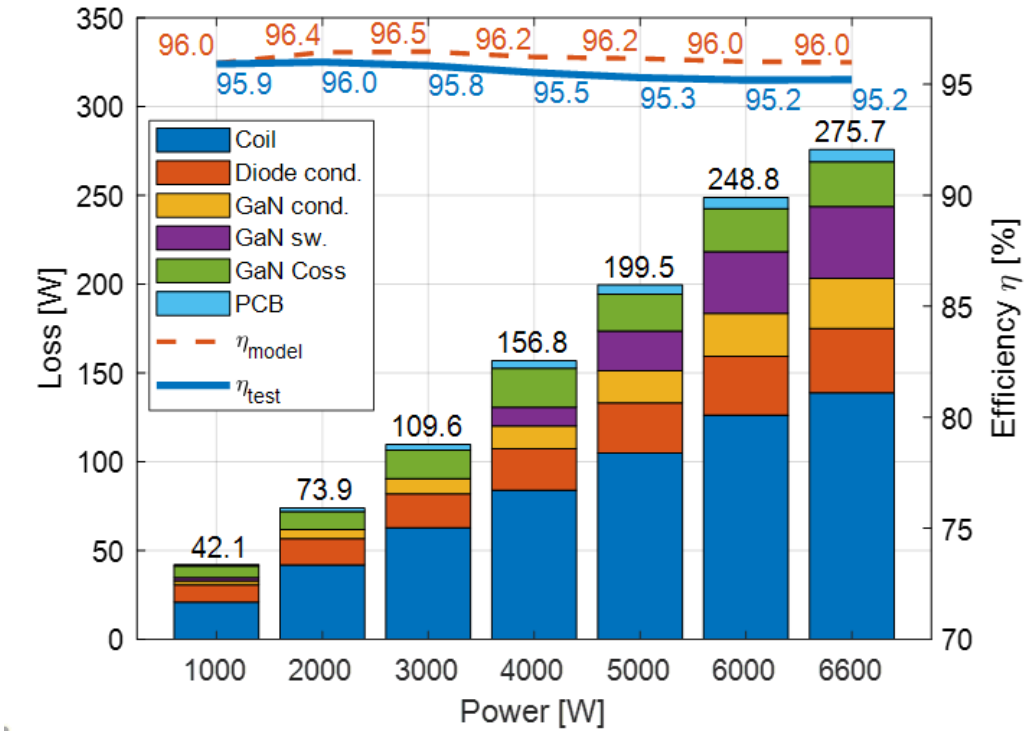


Fig. 139. System power loss breakdown for different power output

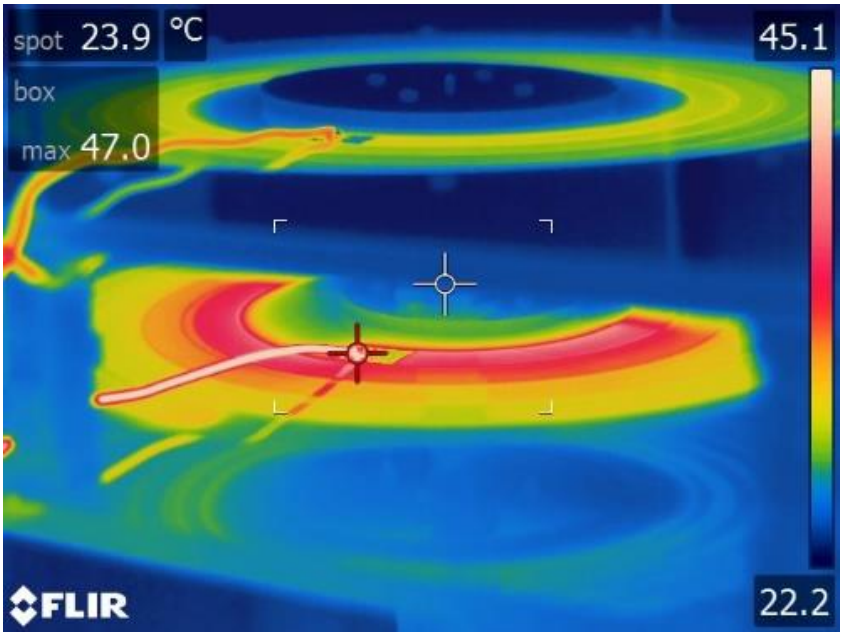


Fig. 140. Thermal image of SR coils at 4 kW output power

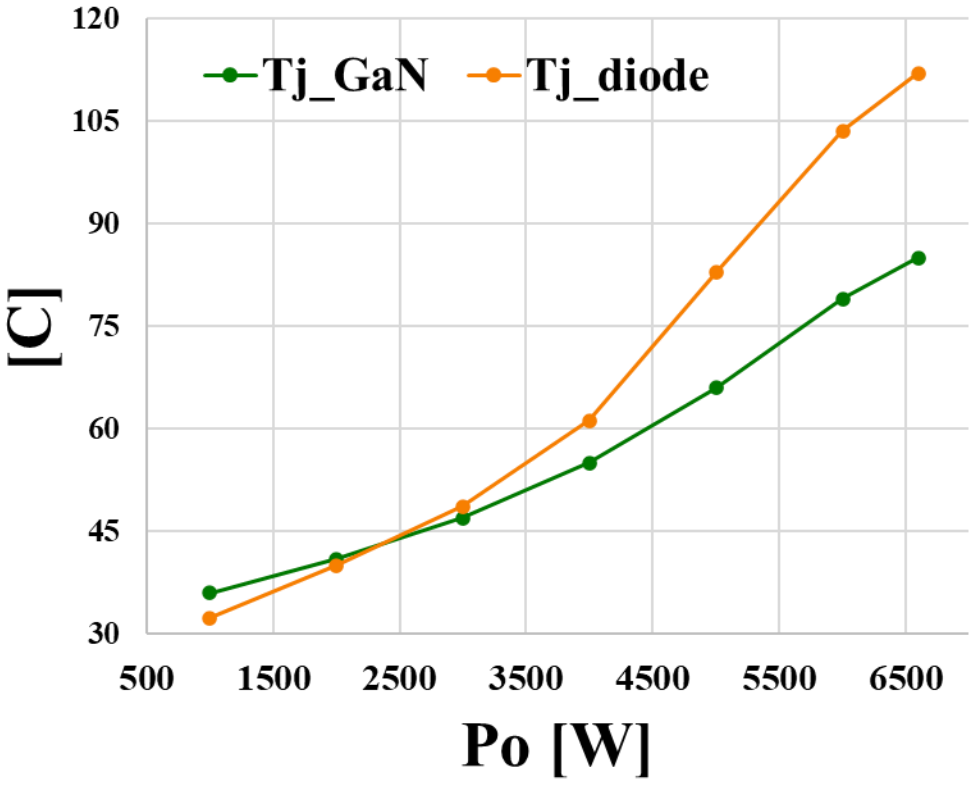


Fig. 141. Junction temperature for GaN transistors and diodes

To fabricate the designed 3 MHz SR coil, chemical etching is applied for the copper spiral on three copper layers. The fabricated coils are measured with an impedance analyzer, showing a good match with the analytical and simulation results. The laminate material is also analyzed and tested for dielectric strength and thermal dissipation, ensuring its robustness at high power operating condition.

Since the GaN transistors take high power loss at 3 MHz for 6.6 kW power output, the PCB is carefully designed, minimizing the impact of parasitics on system operation. A 3D-printed airduct is designed and fabricated to provide laminar air flow over the fins on the heatsink for maximum thermal dissipation capability. Conduction tests are conducted to verify the proposed thermal management system, achieving over 100 W power dissipation on GaN transistors with well-regulated junction temperature. The final prototype system is tested up to 6.6 kW, with 95.2% DC-DC efficiency.

CHAPTER 7. SHIELDING DESIGN OF THE PROPOSED WPT SYSTEM WITH MULTI-LAYER SELF-RESONANT COILS

When installed in an EV, any charging coils will exert high leakage magnetic field, causing excessive eddy current loss on the structural elements of the vehicle chassis like carbon steel or aluminum alloys. To avoid such high power loss on the chassis and also to attenuate stray field in surrounding areas [109]-[112], proper shielding is required for any coil, including SR coils. In this chapter, a complete shielding design solution is provided based on the proposed 3MHz multi-layer non-uniform SR coils, as shown in Fig. 142. With the existence of both ferrite and aluminum, the impact of shielding on the multi-layer SR coil is analyzed in detail. Design guidelines are provided for the ferrite geometries, and an integrated design optimization process is proposed within the WPT system. To verify the design result, a shielding structure is assembled based on the multi-layer non-uniform SR coils of Chapter 6 and tested up to 6.6 kW. This chapter validates the performance of high frequency WPT system with SR coils considering the practical shielding requirement for wireless charging deployment on EVs.

7.1 Shielding Requirement for SR Coils Deployment on EVs .

A fast 2D magnetic simulation is conducted first using FEMM to illustrate the shielding challenge when the SR coils are deployed for EV charging. Fig. 143(b) gives the magnetic field distribution for the 6.6 kW system with the proposed multi-layer SR coils. The coil radius is 200 mm with 17.9 A transmitter coil current, 11.9 A receiver coil current (100.45° leading phase of transmitter current calculated by system model in Chapter 5), 3.125 MHz frequency, and 100 mm airgap between two coils. Clearly, high fringing field exists at top and bottom of coils, which will induce high eddy current loss at any surrounding metal objects on the vehicle.

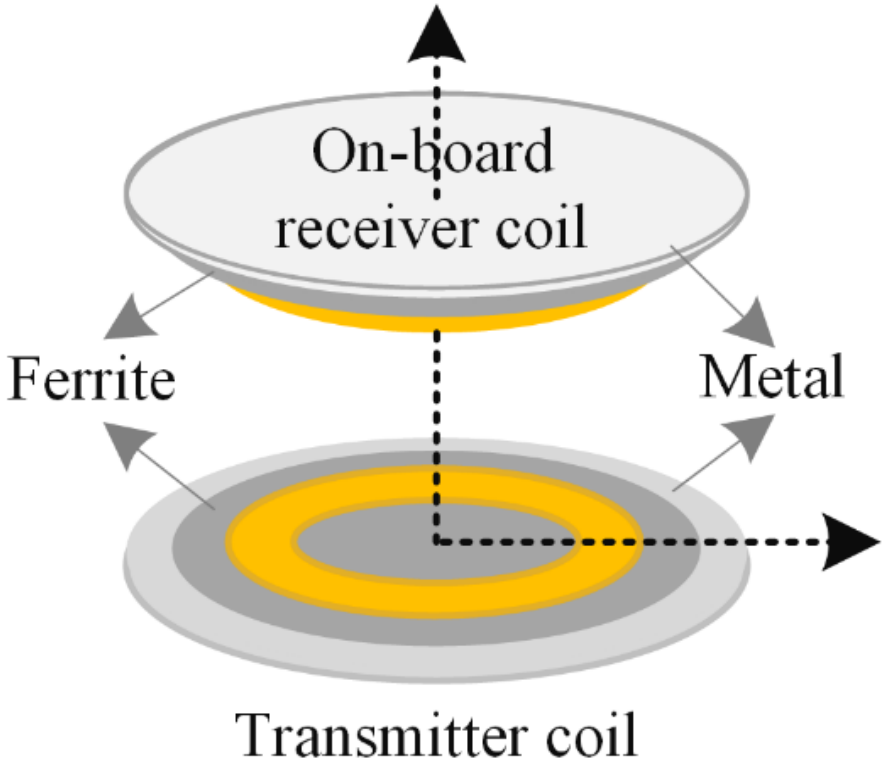
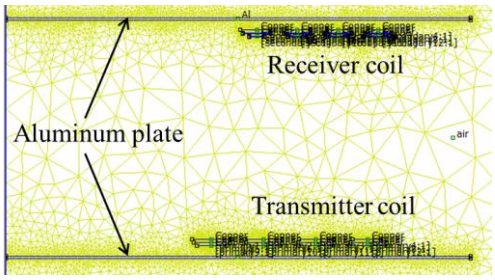
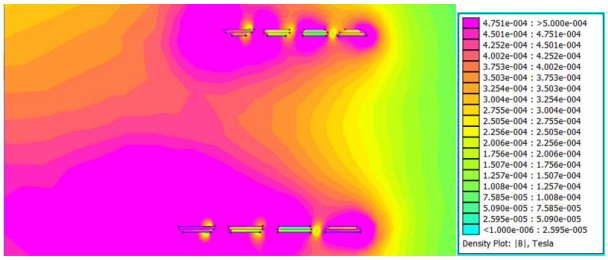


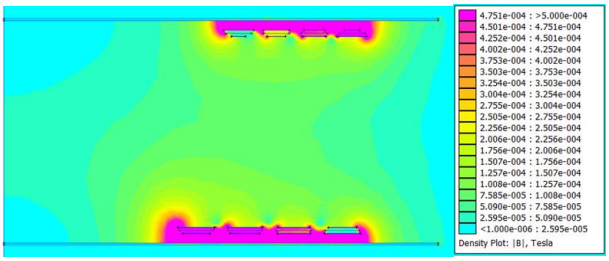
Fig. 142. Typical coil shielding structure of the WPT system for EVs



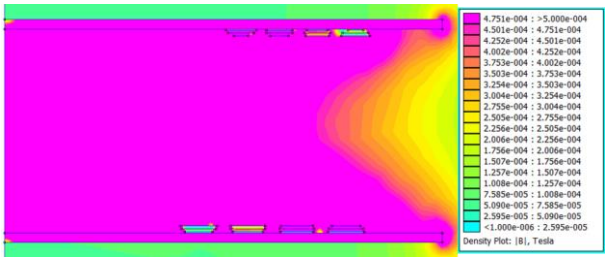
(a)



(b)



(c)



(d)

Fig. 143. FEMM based 2D magnetic field simulation for a 6.6 kW system with multi-layer SR coils (a) meshing setup in FEMM (b) magnetic field without shielding (c) magnetic field with aluminum shielding (d) magnetic field with ferrite shielding

One straightforward approach to shielding is to apply conductive metal, as shown in Fig. 143(c) where the magnetic field outside the plates is well constrained at several μT level by the field cancellation effect using 1 mm thickness, 18 in. Aluminum plates placed 5 mm away from the coils. However, the opposing magnetic field generated by the eddy current that is induced on the metal plate completely alters the field distribution around the coils, and the coil inductance and coupling are greatly impacted, leading to a significant coil-to-coil maximum efficiency drop as summarized in TABLE XX. The other approach would be using ferrite materials to channel the flux around the coil as shown in Fig. 143(d). Most of the flux outside the two coils is now contained by the ferrite cores, with a boost in both inductance and coupling coefficient. Still, the leakage magnetic field above the receiver coil is much larger compared to the aluminum shielding case, with much higher weight required for shielding.

Based on the case study above, ferrite cores and aluminum plates are needed together for shielding in a complete high frequency SR coil pad design, with ferrites to channel the flux around the coil, increasing the inductance and coupling coefficient, and aluminum plates to shield the remaining stray field and also provide the mechanical structure to mount the coil on the vehicle. In the next section, a more detailed analysis is provided, giving shielding design guidelines for optimal power density.

7.2 Shielding Design Guidelines Considering the Parasitic Capacitance with Ferrites

Compared to the conventional 85 kHz system, shielding design for high frequency SR coils faces more challenges, including the coil performance degradation caused by the parasitic parallel capacitance between winding turns, which needs to be addressed before

TABLE XX. Coil Inductance and Coupling Comparison

Shielding condition	Inductance [µH]		Quality factor @3MHz		Mutual inductance [µH]	Coupling coefficient	Coil-coil max. efficiency	Leakage field 10mm above RX [µT]	Shielding weight [kg]
	TX	RX	TX	RX					
None	5.24	6.82	426	434	1.66	0.278	98.34%	300	0
Al.	0.83	1.14	90	94	0.02	0.021	37.01%	0.02	0.9
Fe.	10.5	13.5	539	595	4.98	0.418	99.16%	73	7.7

deploying the SR coils on EVs. There are multiple studies for WPT shielding design using ferrites and metal plates [113]-[115], yet no work has been proposed to study the shielding impact on SR coils in the current literature.

For the proposed high frequency SR coils, parallel resonance introduced by the shielding material needs to be considered during the design process for its impact on the coil properties. The electric potential is simulated between two adjacent turns of the coil as shown in Fig. 144. Below the coil, DMR51W ferrite material [116] and an Al plate are used for shielding. To tune the parasitic capacitance, PTFE is selected as the airgap filler material between the coil and ferrites, which is low-cost and available for a wide range of thicknesses. It has 2.1 dielectric constant and 0.0003 dielectric loss tangent.

Between the two adjacent copper traces, there are four parasitic capacitances which are connected in series: C_1 and C_2 formed between the Aluminum plate and copper trace on the left, C_3 and C_4 formed between the Aluminum plate and copper trace on the right. The total equivalent capacitance is,

$$C_{eq} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}} \tag{63}$$

Note that C_1 and C_4 are much smaller than C_2 and C_3, if the thickness of PTFE and DMR51W are comparable. This is caused by the very high dielectric constant for DMR51W close to 40000 at MHz range (dielectric constant = 38700 @ 3MHz) [117]. In other words, the total equivalent capacitance is dominated by the capacitance contributed by the PTFE layer.

With the varying thickness of the PTFE as shown in Fig. 145, the equivalent capacitance between two coil turns can be tuned accordingly. If the PTFE layer is too thick, although

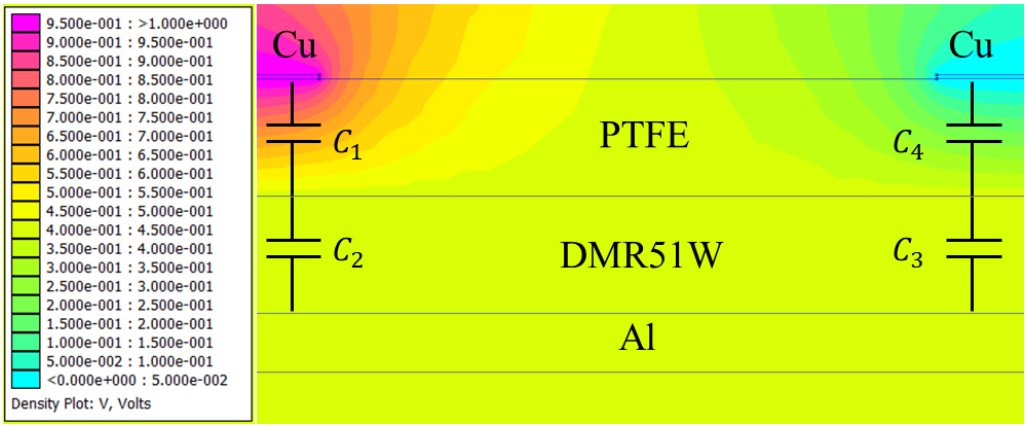


Fig. 144. FEMM based 2D electrostatic simulation for the coil with shielding

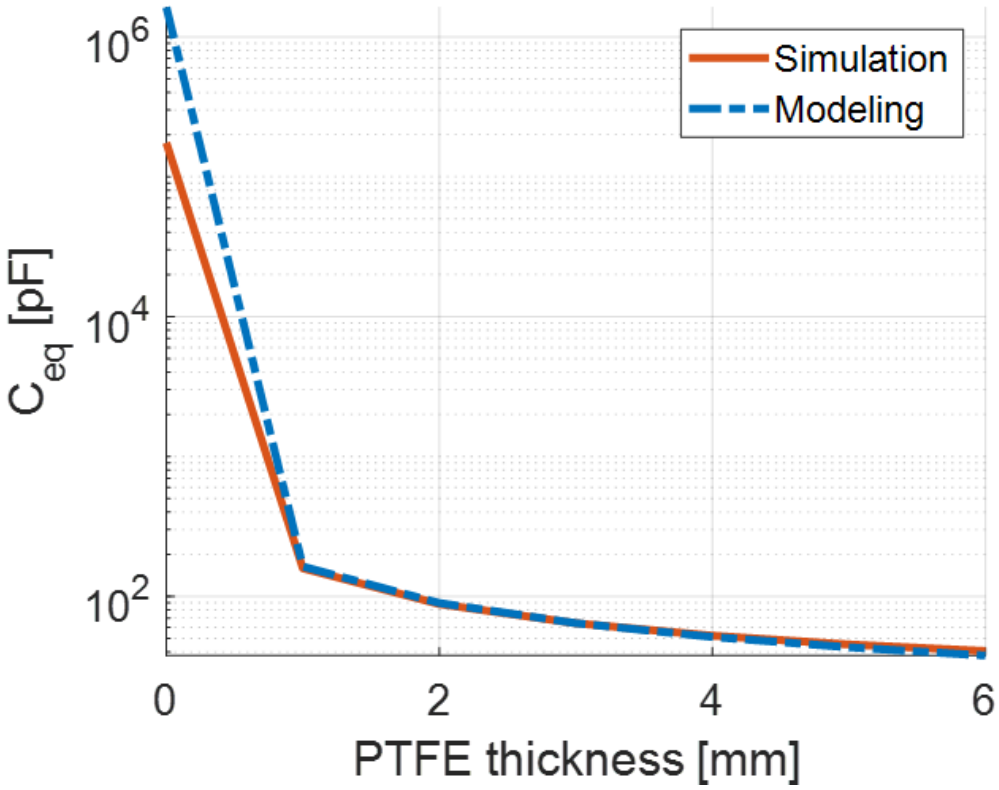


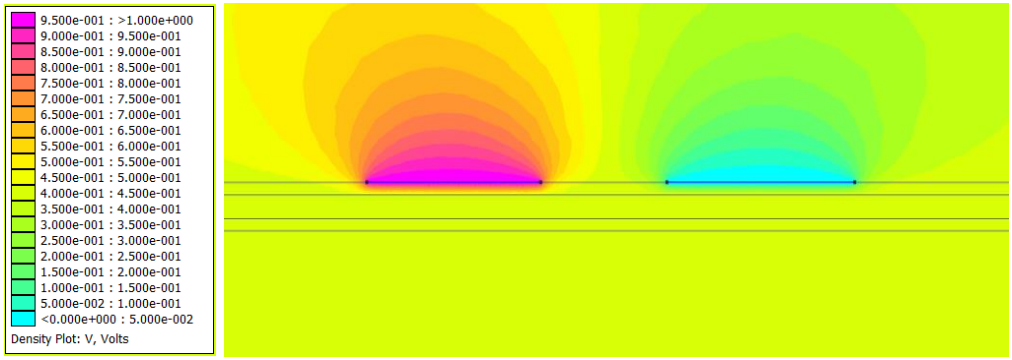
Fig. 145. Equivalent capacitance between two adjacent coil turns

the value of the equivalent capacitance drops to several pF and the impact of the parallel resonance can be ignored, the power density of the coil is largely sacrificed considering the increased weight and size of PTFE layer.

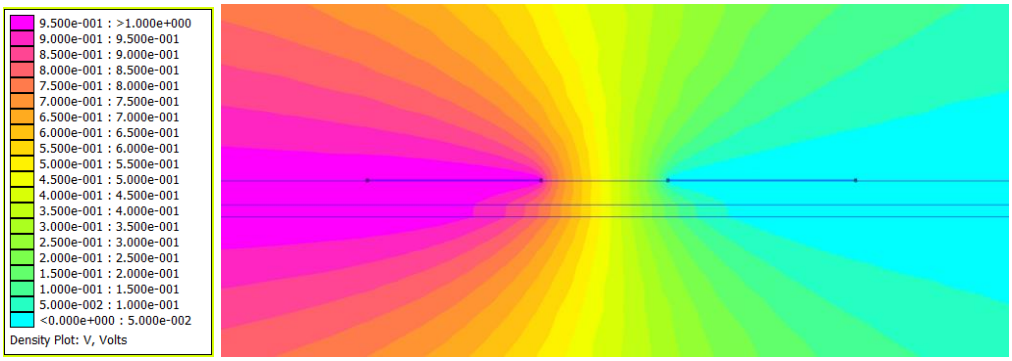
On the other hand, if the PTFE layer is designed to be too thin, the power density of the coil pad is improved, but there will be high equivalent parallel capacitance, leading to a lower frequency parallel resonant frequency and negative impact on the coil performance. Note that when the thickness of PTFE layer is zero (no PTFE layer exists), the pattern of electric potential changes completely as shown in Fig. 146(b) due to the conductivity of the ferrites. Unlike the parallel-plate capacitor case in Fig. 146(a), now the electric potential drops directly between the two adjacent copper traces horizontally, and much higher equivalent capacitance is generated. As a result, a minimum airgap is always needed for insulation between the ferrites and copper traces.

To help better understanding the impact of the parallel resonance on the coil performance, a lumped element model for the three-layer SR coil with the parallel parasitic capacitance is shown in Fig. 147. One capacitor is used to simulate the impact from PTFE and ferrites, and corresponding coil impedance is shown in Fig. 148. With higher parasitic capacitance, the parallel resonant frequency decreases, leading to a higher resonant current within the coil as shown in Fig. 149 due to the closer distance to the parallel resonant peak, which will increase the equivalent ESR for the whole coil. In addition, with larger parasitic capacitance, the series resonant frequency also decreases because of a larger equivalent inductance.

To verify the analysis of the coil model in the lumped element model mentioned above and provide quantitative results of the change of resonant frequency and ESR, a 3D



(a)



(b)

Fig. 146. Electric potential plot comparison (a) PTFE thickness = 1mm (b) no PTFE layer

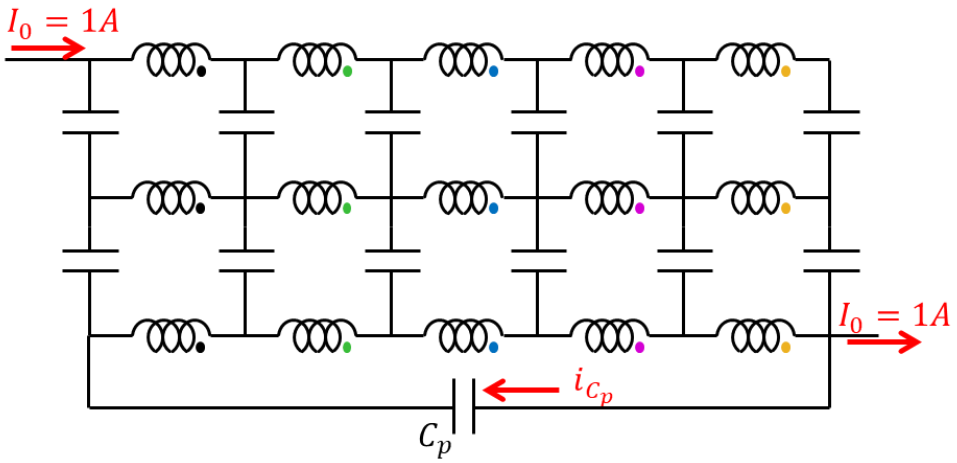


Fig. 147. Lumped element model for three-layer non-uniform SR coil with parallel parasitic capacitance

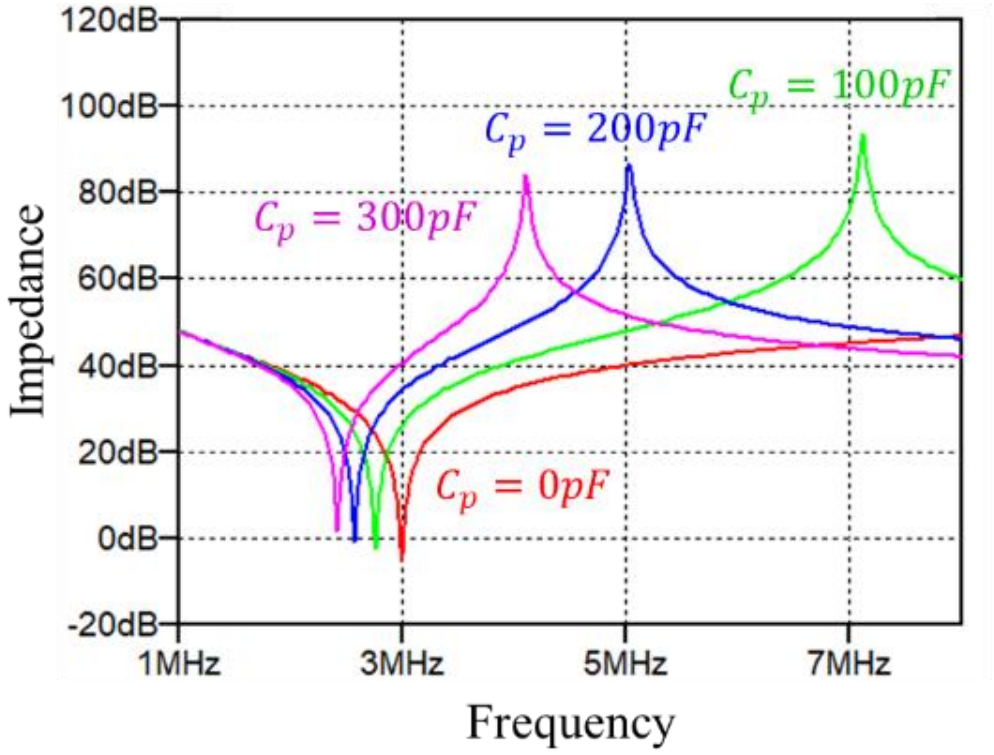


Fig. 148. Coil impedance with varying equivalent capacitance as a function of frequency

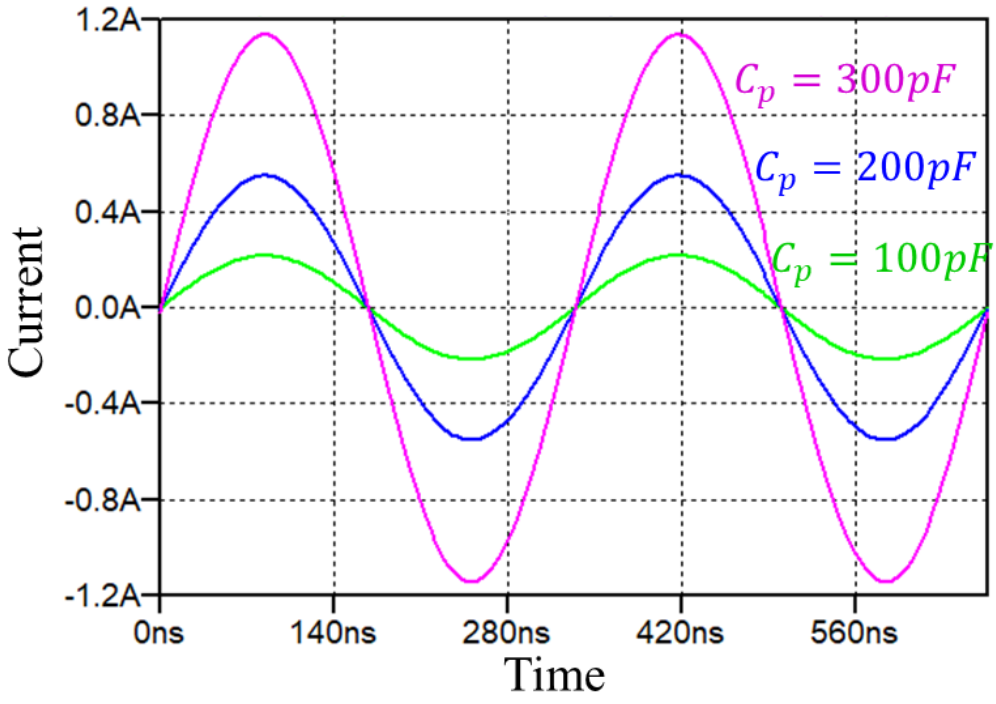


Fig. 149. Parallel capacitance current with varying equivalent capacitance at 3 MHz

electromagnetic simulation is performed. Fig. 150 and Fig. 151 give the HFSS simulation results of the coil impedance and ESR, respectively with varying PTFE thickness. The coil parameters are the same as the coil structure from Chapter 6, with 5 μH inductance 3 MHz resonant frequency.

With the increasing PTFE thickness, the parasitic capacitance caused by the shielding continues to decrease, leading to a higher parallel resonant frequency and lower coil ESR, which verifies the analysis of the lumped element model. The simulation results with different PTFE thickness are summarized in TABLE XXI.

With larger parasitic capacitance, both coil ESR and equivalent inductance are increased. In order to quantitatively evaluate the shielding impact on the coil quality factor, and to facilitate the best trade-off between the electrical performance and the power density, the shielding structure should be optimized together with the system design based on the 3D FEA simulation results, as explained in the next section.

7.3 Systematic Shielding Geometry Optimization

Since the shielding design will strongly impact the trade-off between system efficiency and power density, a system-level design optimization procedure is proposed to locate the optimal design of the shielding geometry, as summarized in Fig. 152. To relieve the calculation burden from 3D electromagnetic simulation, 2D FEMM based fast simulation is first used to calculate the inductance and coupling coefficient of the coils under the influence of the shielding, while 3D HFSS based electromagnetic simulation is used to calculate the coil ESR considering the impact from the parallel parasitic capacitance and

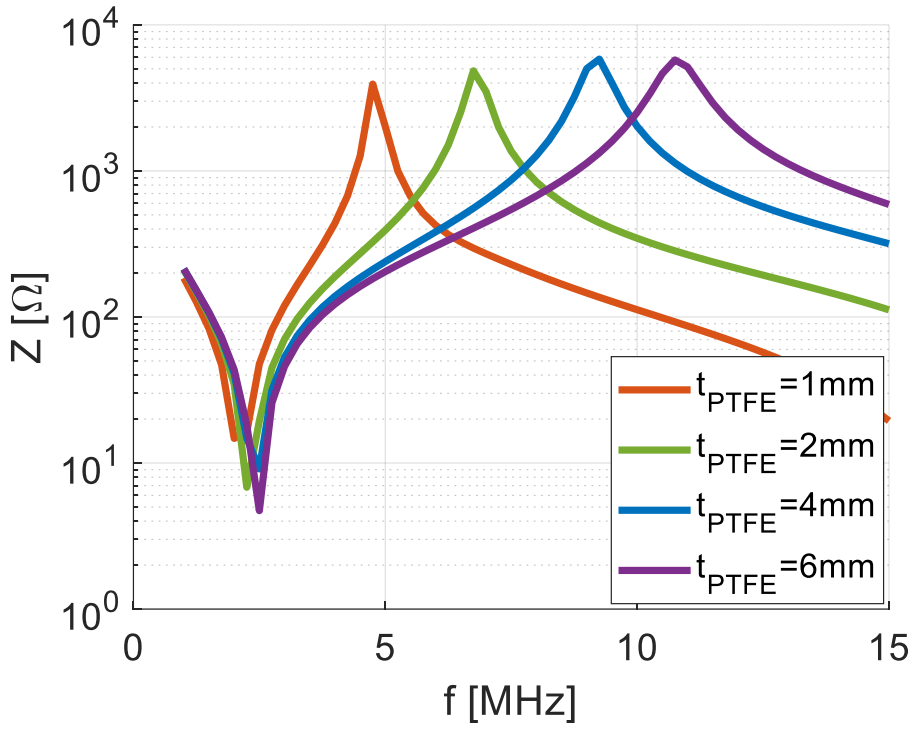


Fig. 150. Coil impedance plot with varying PTFE thickness in HFSS

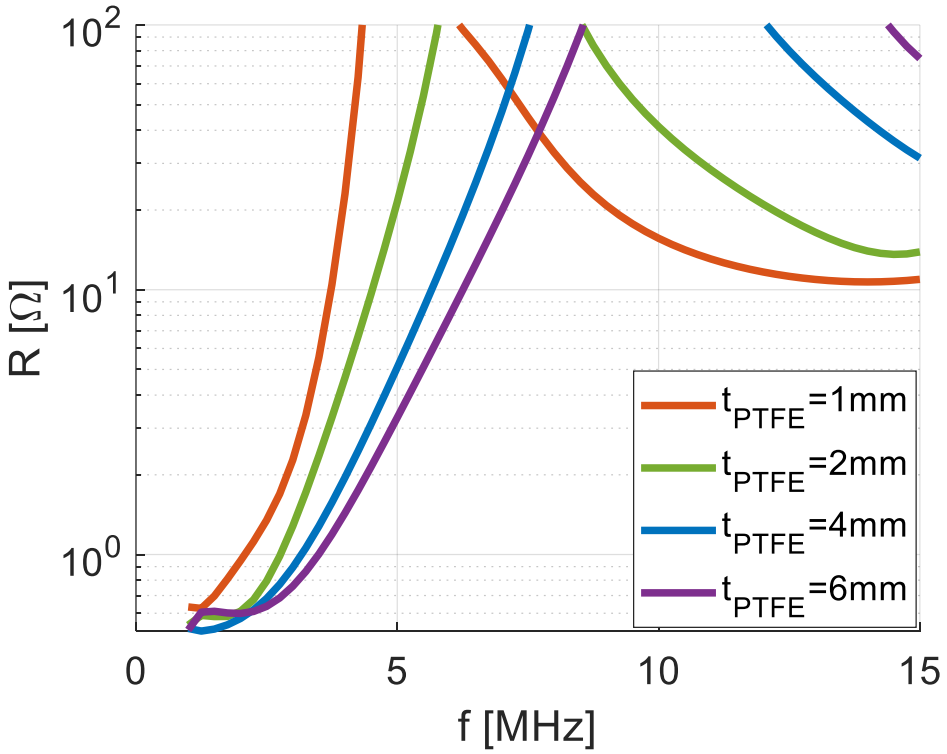


Fig. 151. Coil ESR plot with varying PTFE thickness in HFSS

TABLE XXI. Resonant Frequency and ESR of Coil with Varying PTFE thickness

PTFE thickness [mm]	1	2	4	6
Series resonant frequency [MHz]	2.12	2.31	2.40	2.45
Parallel resonant frequency [MHz]	4.89	6.85	9.18	10.82
ESR [Ω]	1.030	0.704	0.657	0.632

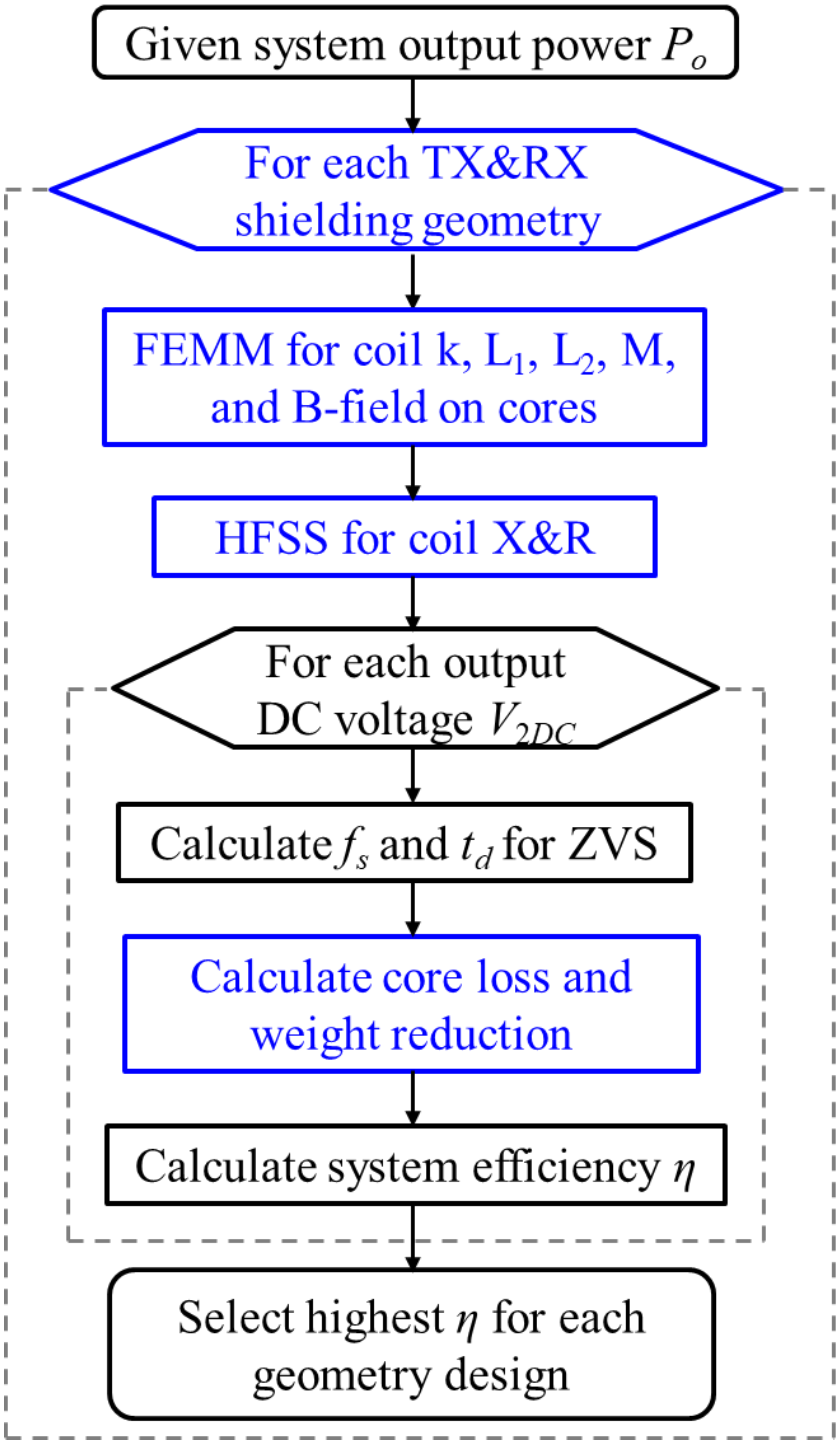


Fig. 152. Design flow for shielding optimization

the dielectric loss from ferrites, which cannot be found by 2D FEMM magnetostatic simulation. Note that the core loss of the ferrites is estimated by the magnetic field distribution captured from FEMM simulation and core loss data from the datasheet provided by the vendor as shown in Fig. 153. Together with the WPT system model proposed in the previous chapter, the highest system efficiency is calculated for each shielding geometry.

Parameters including Ferrite plate thickness [2 mm, 4 mm], Ferrite plate inner radius [25 mm, 50 mm, 75 mm], and PTFE thickness [2 mm, 4 mm, 6 mm] are swept, and corresponding HFSS simulation results are incorporated into the WPT system model to calculate the system efficiency, weight of shielding materials, and shielded coil volumetric power density. The dimension of the Al plate is 18" x 18" with 0.016" thickness. The outer radius of the Ferrite plate is selected to be the same as the coil pad at 200 mm to channel the flux from all coil traces.

Totally 324 cases of shielding design are simulated and optimized, and the sweeping result for system efficiency is shown in Fig. 155. The x-axis shows the total weight of ferrites and PTFE for two coils, and the color of the dot represents the volumetric power density based on the RX coil volume, including copper, RO3003 laminates, ferrites, and PTFE spacer. The detailed specifications of three cases on the Pareto front are summarized in TABLE XXII. Case No. 3 is selected for the prototype build considering the balance between efficiency, power density and the cost of magnetic material: for the ferrite, 2 mm thickness DMR51W with 25 mm inner radius, 200 mm outer radius is applied for both the transmitter side and receiver side; for the airgap filling material, 6 mm and 2 mm thickness

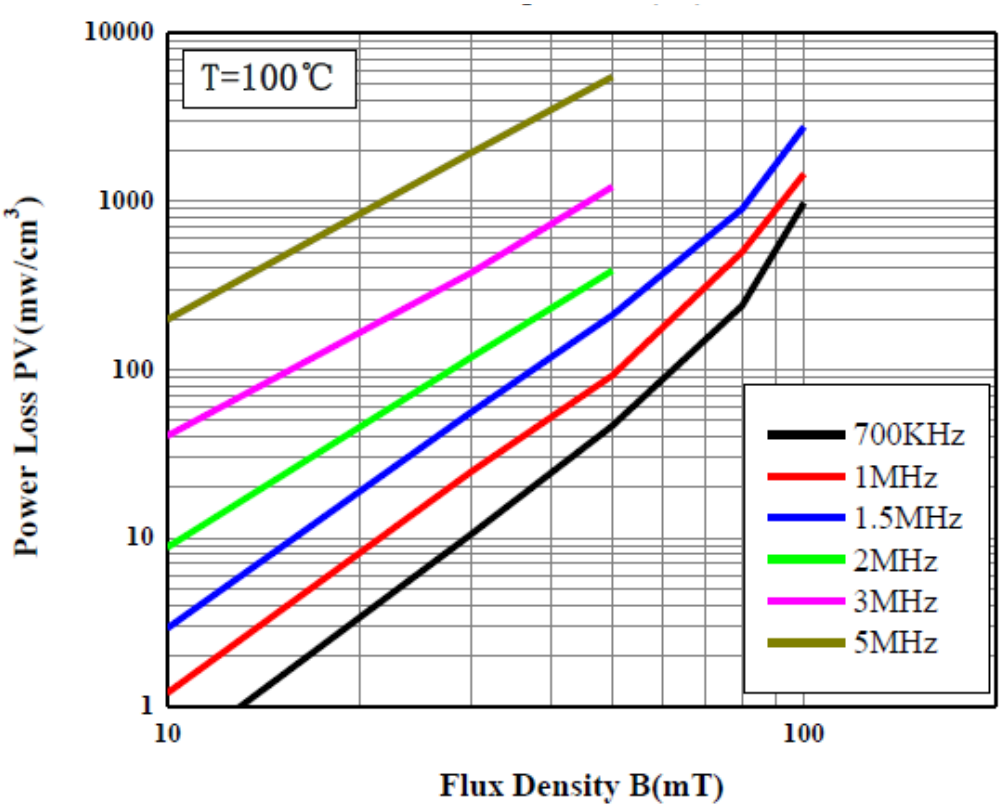
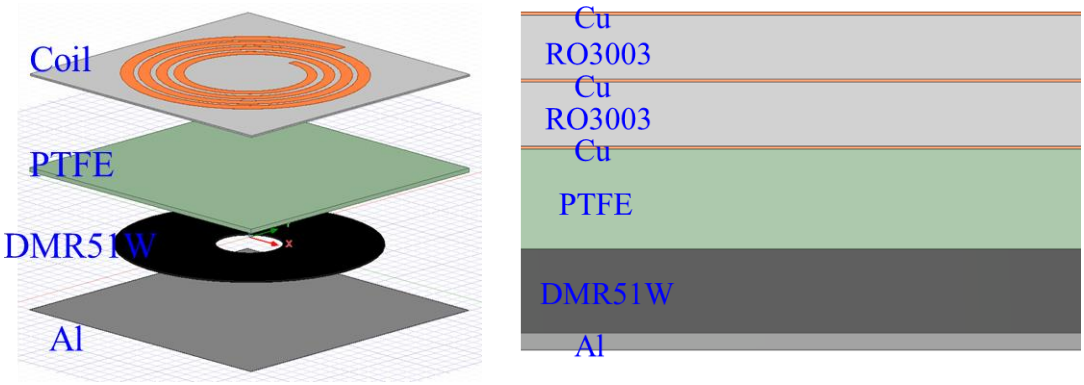


Fig. 153. Core loss datasheet for DMR51W [116]



(a) (b)

Fig. 154. Shielding structure for optimization (a) 3D overview (b) side view with stackup information

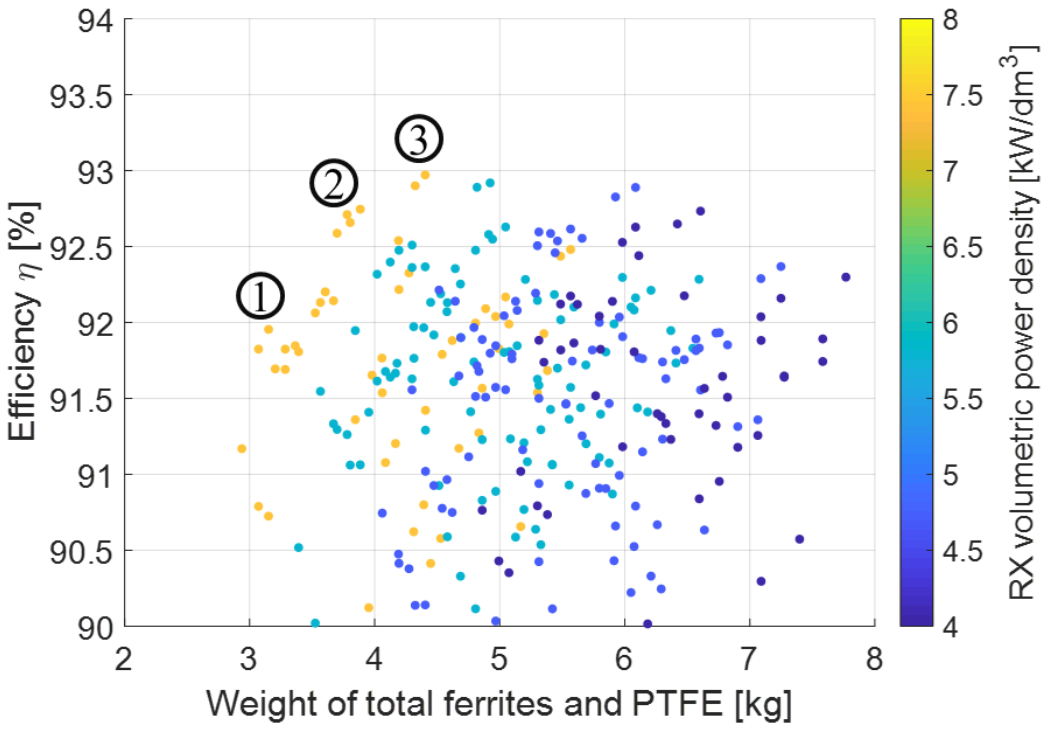


Fig. 155. Shielding design optimization result

TABLE XXII. Design parameters on cases on the Pareto Front

No.	eta [%]	W_Fe [kg]	W_PTFE [kg]	**t_Fe1 [mm]**	**t_Fe2 [mm]**	**t_PTFE1 [mm]**	**t_PTFE2 [mm]**	**r_hole1 [mm]**	**r_hole2 [mm]**
1	91.95	2.18	0.97	2	2	2	2	75	25
2	92.71	2.27	1.51	2	2	4	2	50	25
3	92.97	2.33	2.08	2	2	6	2	25	25

PTFE are applied on the transmitter side and receiver side, respectively.

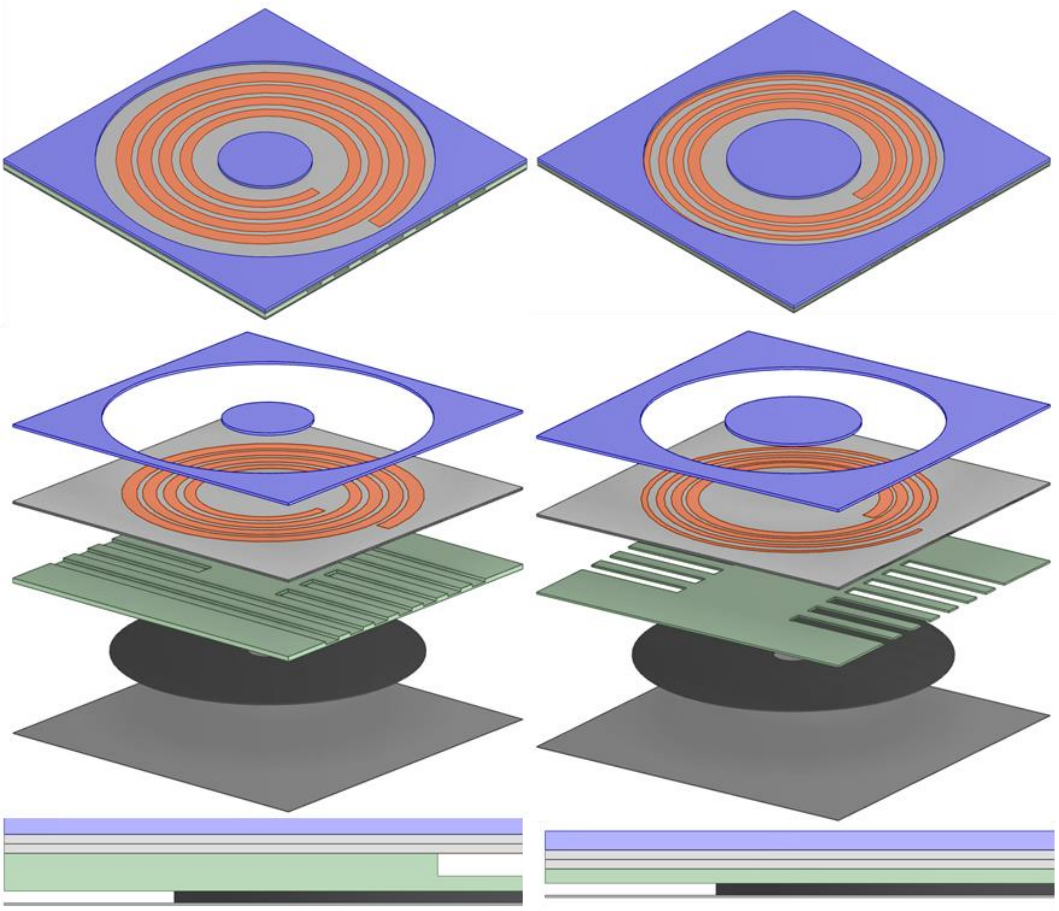
The final 3D structure of two coil pads is shown in Fig. 156 together with the exploded view and side view. For each coil, polycarbonate boards are used to clamp the coil and ferrite plate with the Aluminum back plate. Additional slots are made on the PTFE boards for the purposes of weight reduction, space for wire connection, and better air flow around the copper trace.

7.4 Shielding Hardware assembly and Experimental Verification

To validate the above design methodology, a complete WPT system with shielded SR coils is fabricated and tested. Based on the manufacturing capabilities of the vendor, 16 pie-shaped ferrite cores are fabricated and assembled to make one complete ferrite plate of a coil. Each pie-shaped core has 22.5° center angle with approximately 155.42 mm in length.

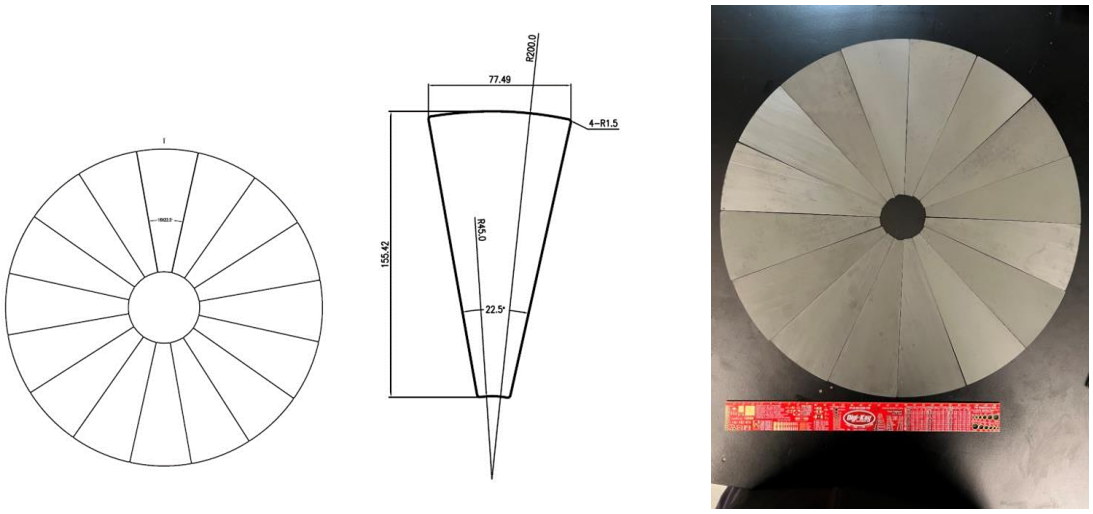
Fig. 158 gives the assembly process for the shielded coil pads for the test setup. Nylon screws are used to secure the coil pad firmly from the Al plate to the polycarbonate cover plate, with ferrite cores, coil, and PTFE spacer sandwiched in between.

For each coil, one lead wire connects to the innermost turn and passes above the outermost turn, as shown in Fig. 159(a). During the test, it is found that there will be arc flash due to the high voltage between the lead wire connected to the innermost turn and the sharp corner on the outermost turn, even when insulated with one layer of Kapton tape rated at 7 kV. To remedy the situation, multiple layers of Kapton tape are applied together with 0.5 mm thickness thermal pad in 159 (c) to leave enough clearance at the weak point.



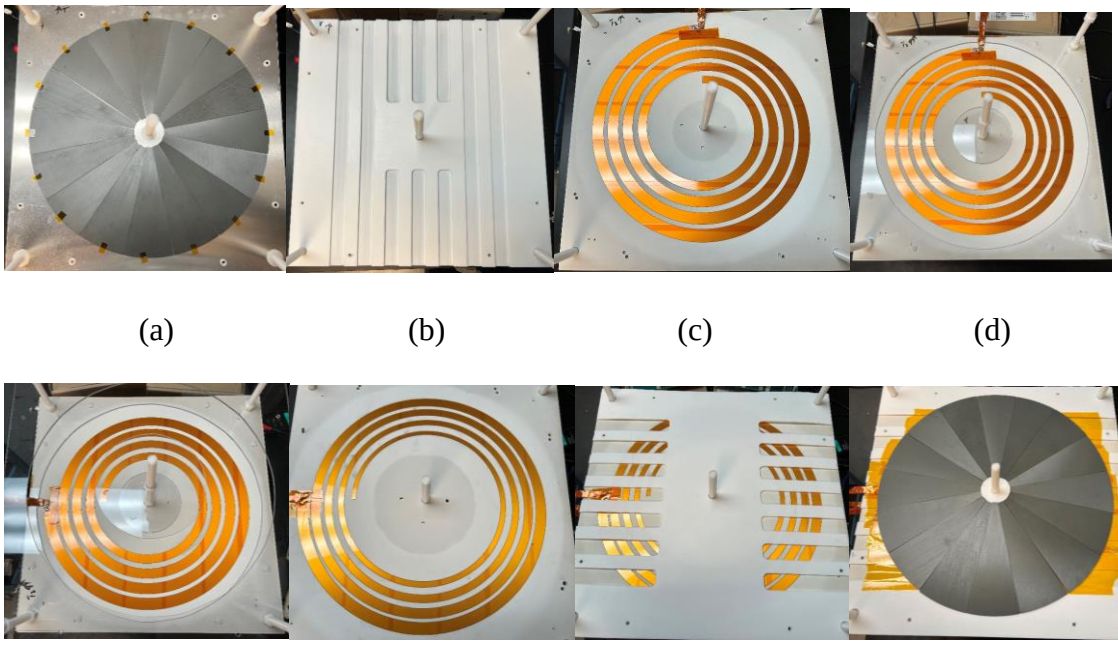
(a) (b)

Fig. 156. 3D exploded and side views of two coil pads (a) transmitter coil pad (b) receiver coil pad



(a) (b)

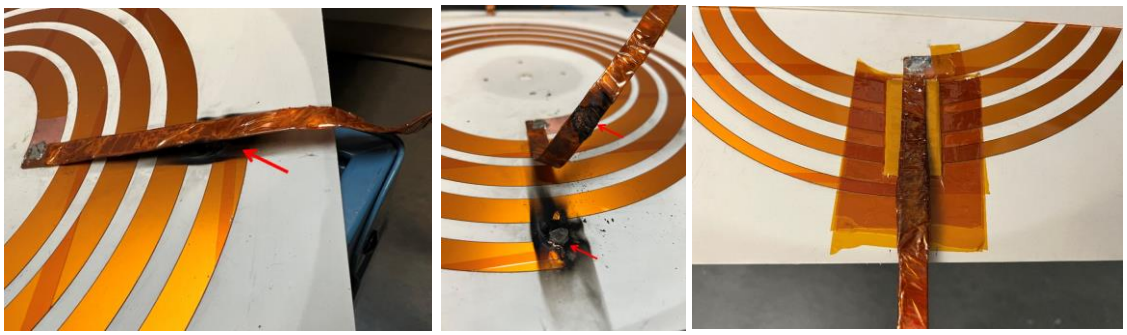
Fig. 157. DMR51W cores (a) drawing of fabrication plan (b) fabricated ferrite cores



(a) (b) (c) (d)

(e) (f) (g) (h)

Fig. 158. Shielded coil pad assembly sequence (a) TX Al+Fe (b) TX PTFE spacer (c) TX coil (d) TX polycarbonate clamps (e) RX polycarbonate clamps (f) RX coil (g) RX PTFE spacer (h) RX Fe+Al



(a) (b) (c)

Fig. 159. Insulation treatment (a) original design (b) insulation breakdown (c) updated design

Fig. 160 gives the final complete assembly for coils with shielding, with 100 mm airgap between two coil pads.

Including the PTFE spacer, the thickness of the transmitter and receiver coil pads are only 11.4 mm and 7.4 mm, respectively. The complete bill of materials for the coil pad assembly is shown in TABLE XXIII, including the Aluminum back plate and polycarbonate plate for clamping. The major weight contributor is the PTFE spacer, and only 1.2 kg ferrite plate is used for each coil. With smaller thickness of PTFE on the receiver side, the weight of receiver coil pad is 20% lighter than the transmitter side.

The characterization results of the shielded coils are summarized in TABLE XXIV. Due to the existence of the ferrites, the coil inductance has increased by about 30% compared with the original coil without shielding. In addition, compared with the tested result using an impedance analyzer, there is less than 5% error from the simulation results for parameters including series resonant frequency, inductance, capacitance, and coupling coefficient. Note that in HFSS simulation, core loss is not included and is calculated separately using the vendor's datasheet. Since core loss is nonlinear, measured coil ESR under small signal bias using an impedance analyzer is only used for fast characterization of the magnetic material, which gives relatively large error compared to the HFSS simulation result.

The hardware setup for the system is shown in Fig. 162, with 6.6 kW power test result shown in Fig. 163. At 2.439 MHz switching frequency, 40 ns deadtime, and 80 Ω load resistor, the system is tested up to 6.6 kW, with 92.3% DC-DC efficiency. The detailed tested parameter comparison in TABLE XXV confirms the validity of the optimization process in the previous section.

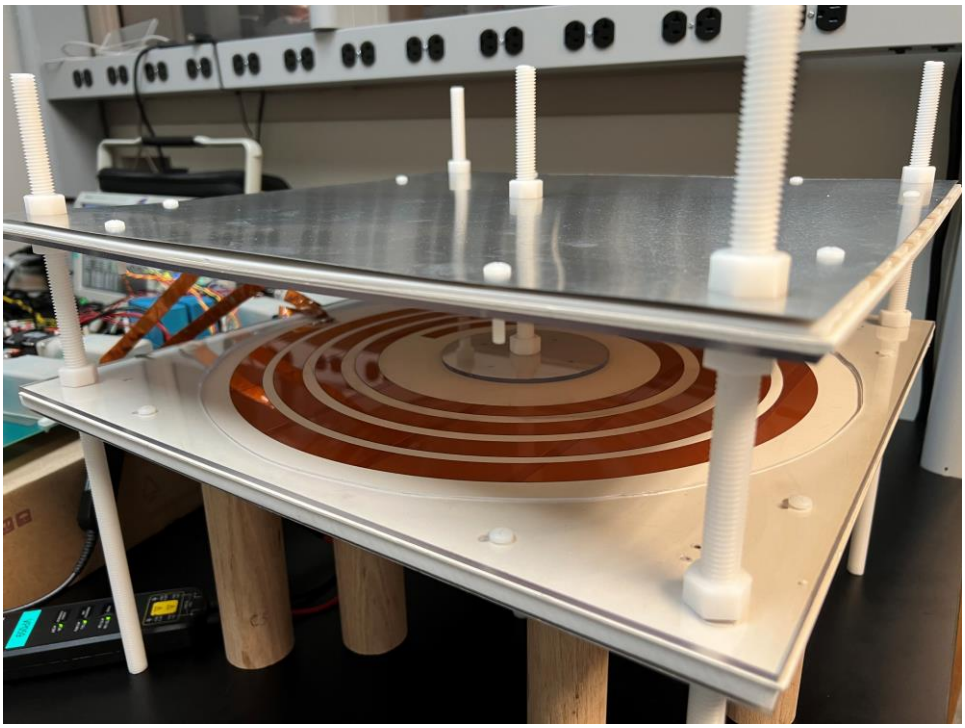
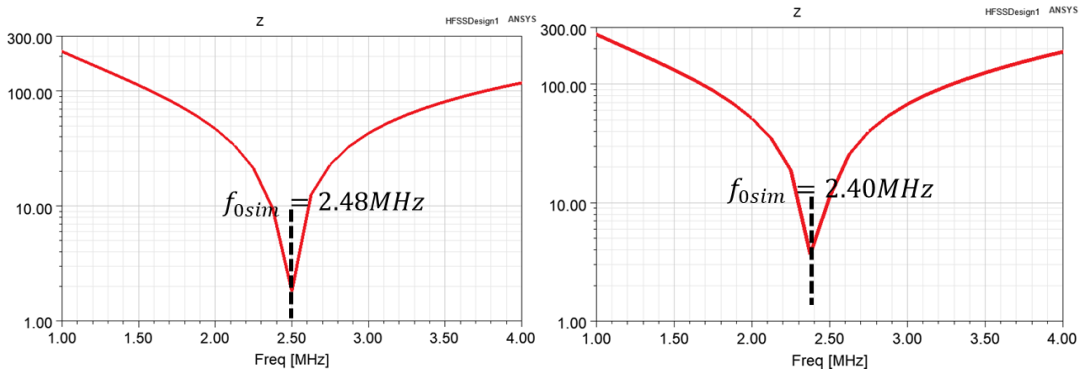


Fig. 160. Complete assembly for coils with shielding

TABLE XXIII. Shielded Coil Pads Bill of Materials

Name	Part number	Quantity	Dimension [mm]	Total weight [kg]
TX coil pad				
Coil ceramics	RO3003	2	457.2x457.2x1.5	1.317
Copper	RO3003	NA	4 turns, 2oz	0.116
Ferrite	DMR51W	16	155.42x77.49	1.163
PTFE	McMaster 8545K46	1	457.2x457.2x6.35	2.247
Aluminum	McMaster 6061	1	457.2x457.2x0.4064	0.229
Polycarbonate	McMaster 8574K53	1	457.2x457.2x3.175	0.309
RX coil pad				
Coil ceramics	RO3003	2	457.2x457.2x1.5	1.317
Copper	RO3003	NA	3-layer, 4 turns, 2oz	0.088
Ferrite	DMR51W	16	155.42x77.49	1.163
PTFE	McMaster 8545K46	1	457.2x457.2x2.381	0.856
Aluminum	McMaster 6061	1	457.2x457.2x0.4064	0.229
Polycarbonate	McMaster 8574K53	1	457.2x457.2x3.175	0.450



(a) (b)

Fig. 161. Impedance results of shielded coil in HFSS simulation (a) transmitter coil (b) receiver coil

TABLE XXIV. Shielded SR Coils Characterization and Comparison

	HFSS simulation (core loss not included)	**Impedance analyzer**
	Transmitter coil	
f_0 [MHz]	2.48	2.42
L [μH]	7.26	7.72
C [pF]	567.8	562.9
R [Ω]	0.593	0.639
	Receiver coil	
f_0 [MHz]	2.40	2.42
L [μH]	10.12	9.84
C [pF]	435.6	438.8
R [Ω]	0.957	0.878
	Two coils	
k	0.278 (FEMM)	0.272

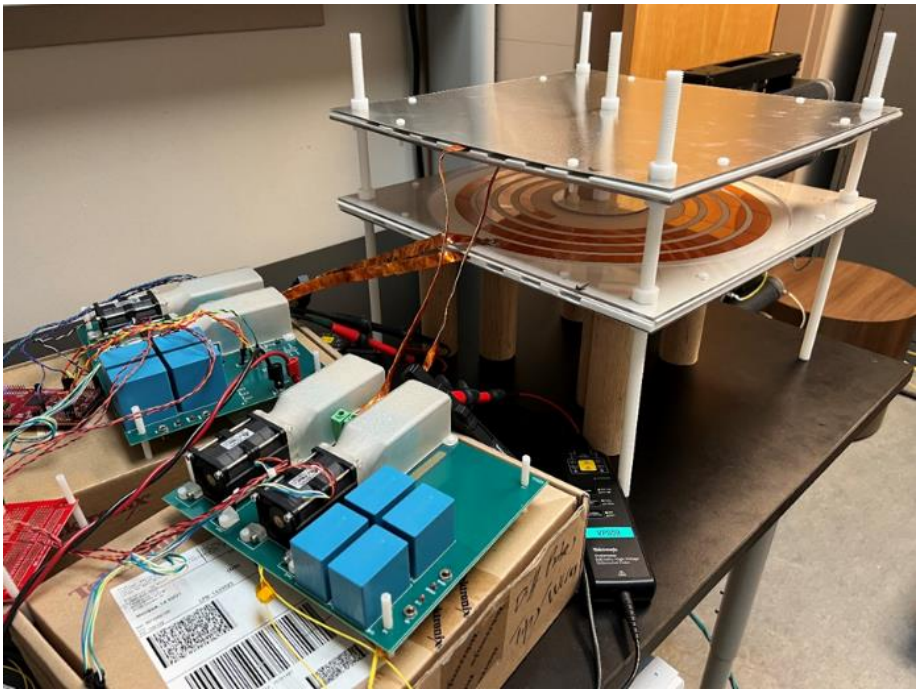


Fig. 162. WPT system with shielded SR coils

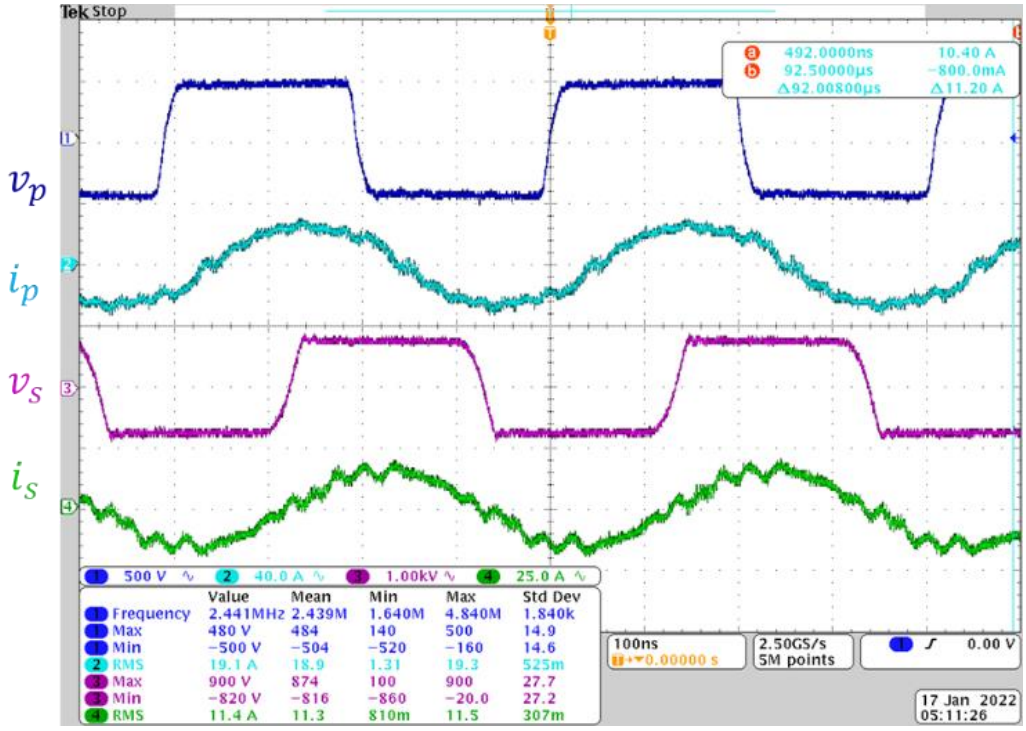


Fig. 163. 6.6 kW system power test waveforms

TABLE XXV. System Tested Result Comparison

	Input voltage V_{1DC} [V]	Transmitter current I_p [A]	Load voltage V_{2DC} [V]	Receiver current I_s [A]	Efficiency η
Model	494.7	17.8	726.6	11.5	93.1%
Test	471.8	19.1	733.6	11.4	92.3%

TABLE XXVI compares the state-of-the-art WPT system parameters with shielding considered. Compared to other systems, the proposed WPT system with SR coils achieves much higher power density at 3.2 kW/kg and 7.1 kW/dm^3 based on the weight and volume of coil windings and ferrites. The power density drops to 2.6 kW/kg when the weight of PTFE is included. Even with the mechanical components including Aluminum back plate and polycarbonate clamping considered, the final power density based on the complete receiver coil pad still reaches 1.61 kW/kg and 4.8 kW/dm^3.

7.5 Summary

This chapter provides a complete design solution for 6.6 kW WPT system based on the proposed SR coils with shielding considered. The high frequency parasitic capacitance introduced by the shielding material is considered, and a shielding geometry optimization method is proposed. Using ferrite for shielding and a PTFE spacer, the total thickness of coils are only 11.4 mm and 7.4 mm for the transmitter and receiver, respectively. The system is validated with fabricated SR coils, achieving 92.3% DC-DC efficiency and 7.1 kW/dm^3 volumetric power density. This chapter demonstrates the first 6.6-kW WPT system for EV charging using compact self-resonant coils at MHz with practical shielding implementation.

TABLE XXVI. State-of-the-art WPT system comparison with shielding

Institute	Year	Shielding	Backplate	f [kHz]	DC-DC efficiency	Power [kW]	L [μH] pri./sec.	C [nF] pri./sec.	Relative air gap, $d/\sqrt{A}$	Compensation type	Gravimetric power density [kW/kg][a]		Volumetric power density [kW/dm3][a]	
											TX	RX	TX	RX
WiTricity	2011	Ferrite	Al	145	90-93% (AC-DC)	3.3	--	--	0.38	--	0.26[b]	0.26[b]	0.35[b]	0.35[b]
ETH	2016	Ferrite	Cu + POM	85	95.8%	50	71.6/71.6	54.1/54.1	0.29	Series *L-C*	2.0[b]	2.0[b]	2.7[b]	2.7[b]
UA	2019	Ferrite	Al + Cu	100	92.1% (TX-DC)	7	196.6/198.2	--	0.28	Series *L-C*	--	--	2.4	2.4
UOA	2019	Ferrite	Al	85	91.2%	5.7	67.5/4.11	--	0.37	Parallel *L-C*	0.24	1.0	0.62	3.6
UOA	2019	No ferrite	Winding	85	89%	5.7	22.2/4.06	--	0.28	Parallel *L-C*	0.41	1.0	0.32	3.6
UOA	2021	Ferrite	Winding	85	91%	4.7	43.2/4.08	--	0.37	Parallel *L-C*	0.36	0.82	0.29	3.0
NCEPU	2022	Ferrite	Al (RX only)	85	95% (coil-coil)	3	415.3/427.3	8.45/8.21	0.29	Series *L-C*	--	--	0.20	0.20
VW	2022	Ferrite	Al	86.5	95.6%	6.6	--	--	0.34	Series *L-C*	0.77	0.77	1.73	1.73
UTK	2022	Ferrite	Al	2439	92.3%	6.6	7.7/9.8	0.56/0.44	0.28	Self-resonance[c]	3.2	3.2	4.6	7.1

a. Power densities are calculated based on the weight and volume of coil windings and ferrites
b. Final assembly of coil pad with all passive components ate included for weight and volume calculation
c. No lumped compensation capacitor is needed in prototype

CHAPTER 8. GENERALIZED *N*-LAYER SELF-RESONANT COIL ANALYSIS AND OPTIMIZATION

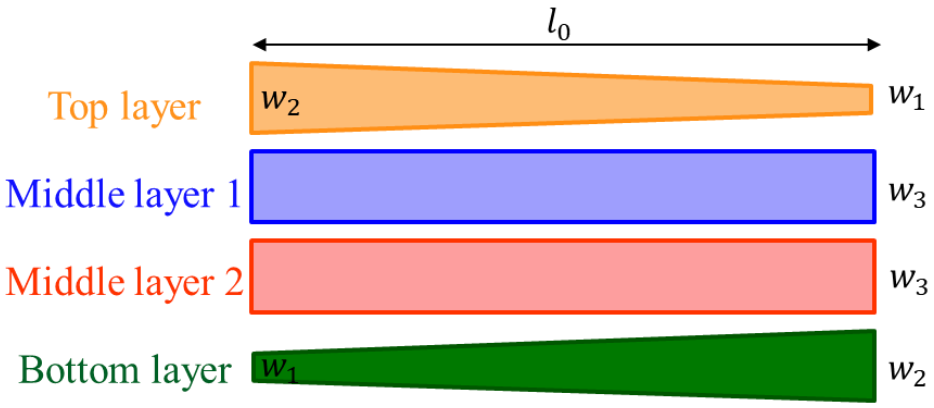
In this chapter, *N*-layer SR coil structures are analyzed to investigate the theoretical limit for the quality factor improvement. Both the advantages of fringing capacitance from multi-layer structure and current sharing from non-uniform copper width have been explored in a more generalized matter. Together with other possible structures, a design guideline is provided to conclude the advantages and disadvantages of each coil structure.

8.1 Four-layer Non-uniform SR Coil

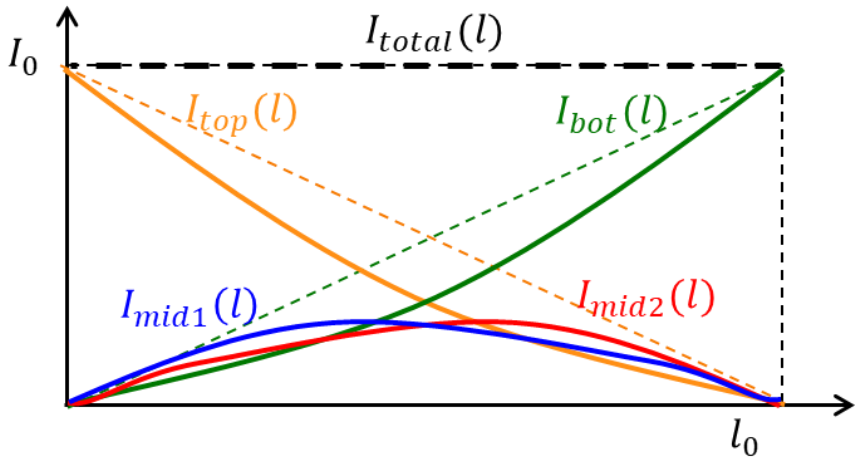
The proposed three-layer non-uniform SR coil can be extended to have more than three layers. With more middle layers, it is possible for the total current to be shared in a more distributed way. As shown in Fig. 164, for a four-layer case, the current in the original middle layer is now shared between two middle layers.

Using the similar design optimization method in Chapter 4, the optimized coil quality factor with different resonant frequencies is shown in Fig. 165, for both 3-layer and 4-layer non-uniform SR coils.

With higher frequency, there will be a wider range of high quality factor 4-layer coils, especially at high inductance. To explain the reason for the improvement, TABLE XXVII lists the coil geometries for two example cases. At 1 MHz 7 μH, better current sharing is achieved for the 4-layer coil due to the large copper width ratio between w_2 and w_1. The current is more evenly distributed among the 4 layers of copper trace as shown in Fig. 166, which outweighs the slightly reduced copper width, leading to a higher quality factor of



(a)



(b)

Fig. 164. Four-layer non-uniform SR coil structure (a) top view of unfurled copper traces for top, middle 1, middle 2 and bottom layers (b) current distribution along each copper trace

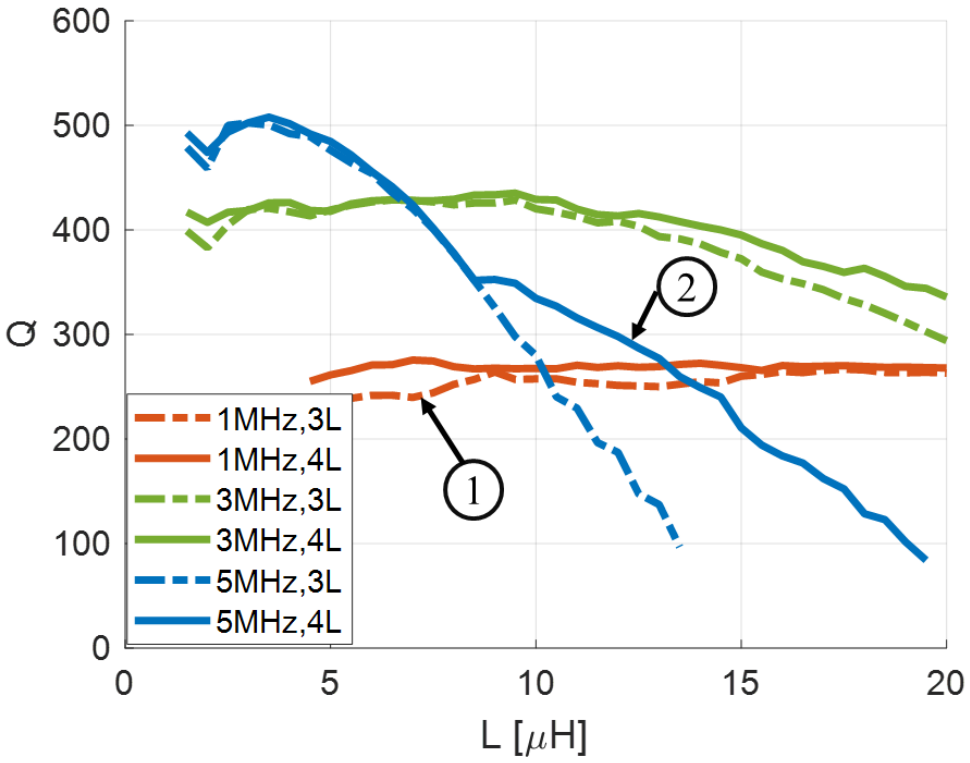


Fig. 165. 3-layer vs. 4-layer quality factor comparison

TABLE XXVII. 3-layer vs. 4-layer Design Case Comparison

Case point	Coil type	Dielectric thickness d [mm]	Copper width w_1 [mm]	Copper width w_2 [mm]	Copper width w_3 [mm]	Middle layer current I_m [%]	Quality factor Q
1 MHz 7 μH	3-L	0.127x2	2.5	14.7	13.6	34.2	240
	4-L	0.085x3	0.1	14.7	13.5	24.4x2	276
5 MHz 12.5 μH	3-L	1.5x2	0.1	0.6	0.6	6.6	149
	4-L	1x3	0.1	2.0	1.1	5.6x2	287

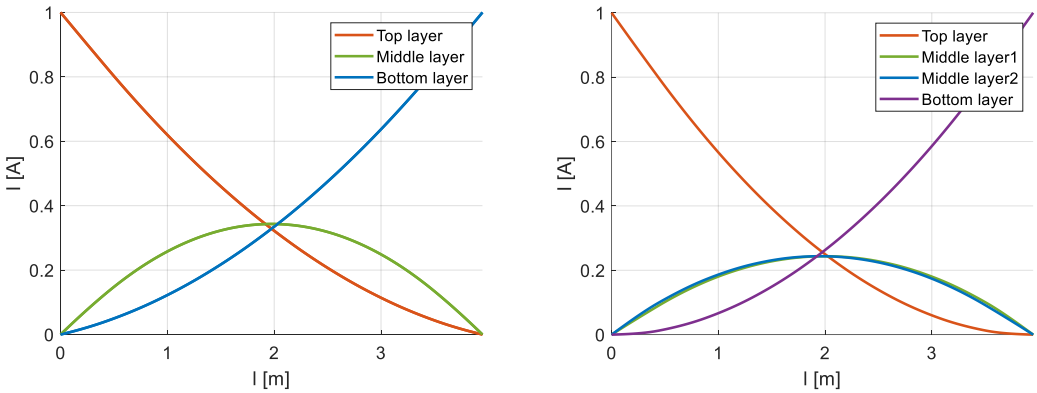


Fig. 166. 3-layer vs. 4-layer current sharing comparison, 1 MHz, 7 µH

276.

At 5 MHz, the advantage of 4-layer is more dominant at high inductance, not because of the current sharing but wider copper width due to the fringing effect. At 5 MHz 12.5 μH, for example, there is a minor increase in the middle layer current because of the relatively small copper trace as shown in Fig. 167. However, the copper trace width is still greatly increased compared to the 3-layer case considering the better-confined fringing electric field among the 4 layer of copper traces.

Compared with the 3-layer coil, adding more layers has very limited impact on current sharing improvement, which is largely cancelled out by the increased high frequency loss. At higher frequency, however, there is certain benefit of more layers, but mainly due to the wider copper width, which is determined by the capacitance requirement for resonance with given coil size and thickness.

8.2 Three-layer Truncated SR Coil with Unequal Length

In the previous section, using non-uniform copper trace sacrifices the copper width to improve the current sharing. To aggressively push more current into the middle layer, the length of copper trace can be manipulated alternatively instead of the copper trace width.

Fig. 168 gives a copper trace structure that can have current sharing even with three uniform width layers. Instead of the equal trace length of all layers, the top and bottom layers are truncated such that more current will be transferred via the middle layer. Unlike a three-layer uniform copper width coil with equal length l_0, now the current is shared in the overlapping region of three layers. In addition, no small copper traces are needed for

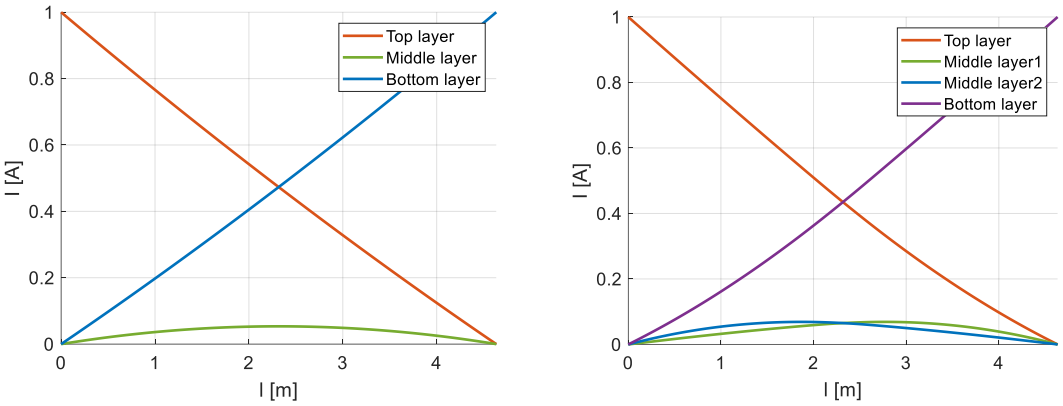
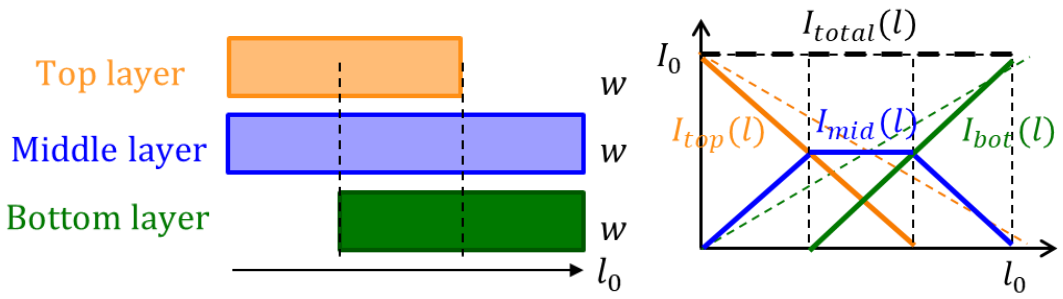


Fig. 167. 3-layer vs. 4-layer current sharing comparison, 5 MHz, 12.5 μH



(a) (b)

Fig. 168. Three-layer truncated SR coil with unequal length (a) top view of unfurled copper traces for top, middle, and bottom layers (b) current distribution along each copper trace

capacitance control, allowing better utilization of coil area. Shorter spiral length also permits wider copper width for given desired capacitance.

Fig. 169 gives the quality factor comparison for 3-layer non-uniform, 4-layer non-uniform, and 3-layer truncated coils. Compared to the non-uniform SR coils with equal copper trace length, 3-layer truncated coil has an even higher quality factor with large inductance at 5 MHz.

The copper width comparison in Fig. 170 explains the reason for the improvement. With less trace overlap between different layers, now a wider copper trace is needed to fulfill the designed resonant capacitance requirement.

In addition to the wider copper trace, the contribution of current sharing is examined by Fig. 171. N_{op}, the overlapped number of turns on top and bottom layers, is plotted together with N, the number of turns on the middle layer for a 3-layer truncated coil at different frequencies. At low frequency, N_{op} is larger than zero, indicating that the quality factor improvement is contributed by both the wider copper trace and better current sharing. At high frequency, however, there is basically no overlapped copper traces between the top and bottom layers. Accordingly, the significant quality factor improvement at 5 MHz is only caused by the much wider copper trace in the truncated coil structure.

8.3 *N*-layer Uniform SR Coil Utilizing the Fringing Effect

In addition to truncated coil, an alternative way of increasing copper width to increase the number of copper spiral layers. For a given target capacitance, more layers mean that the fringing electric field between any two adjacent layers is better confined, and the

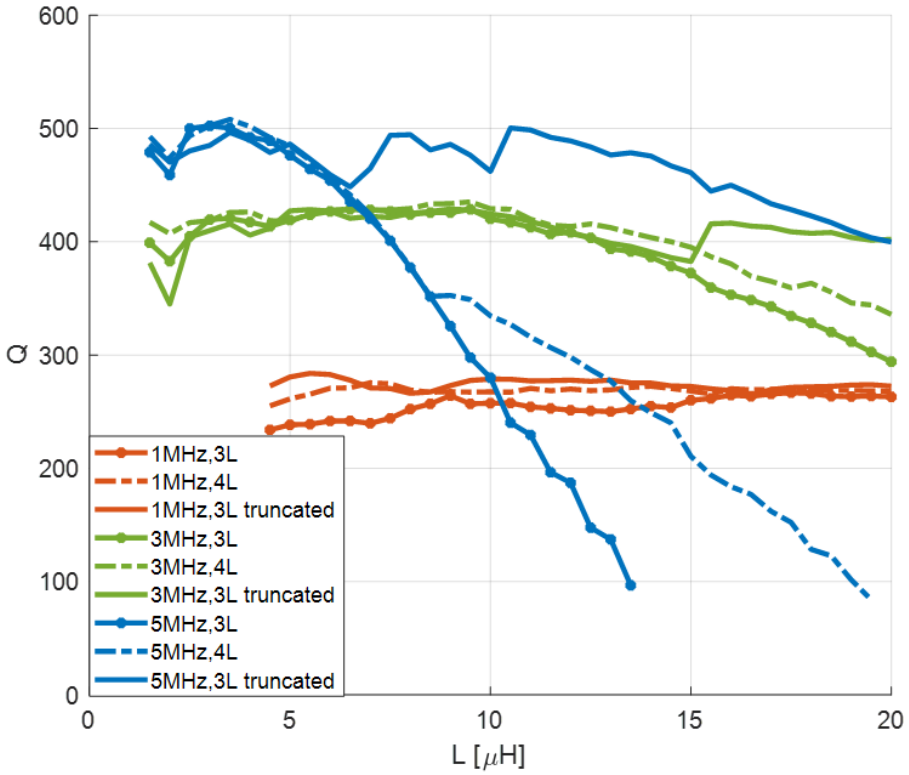


Fig. 169. 3-layer, 4-layer, and 3-layer truncated SR coils quality factor comparison

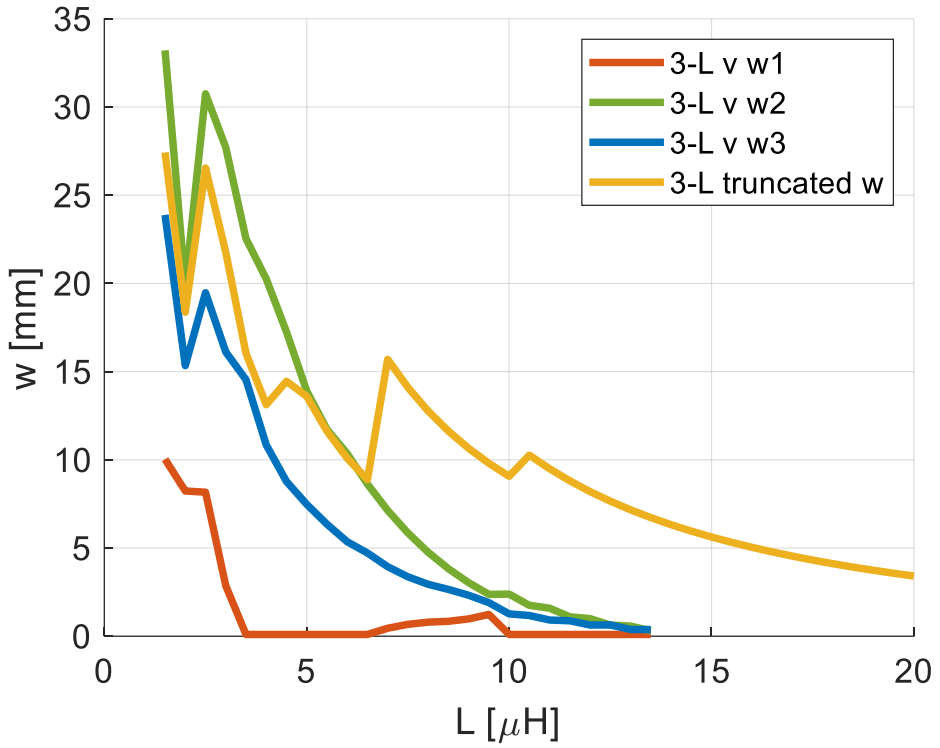


Fig. 170. 3-layer and 3-layer truncated SR coils copper trace width comparison

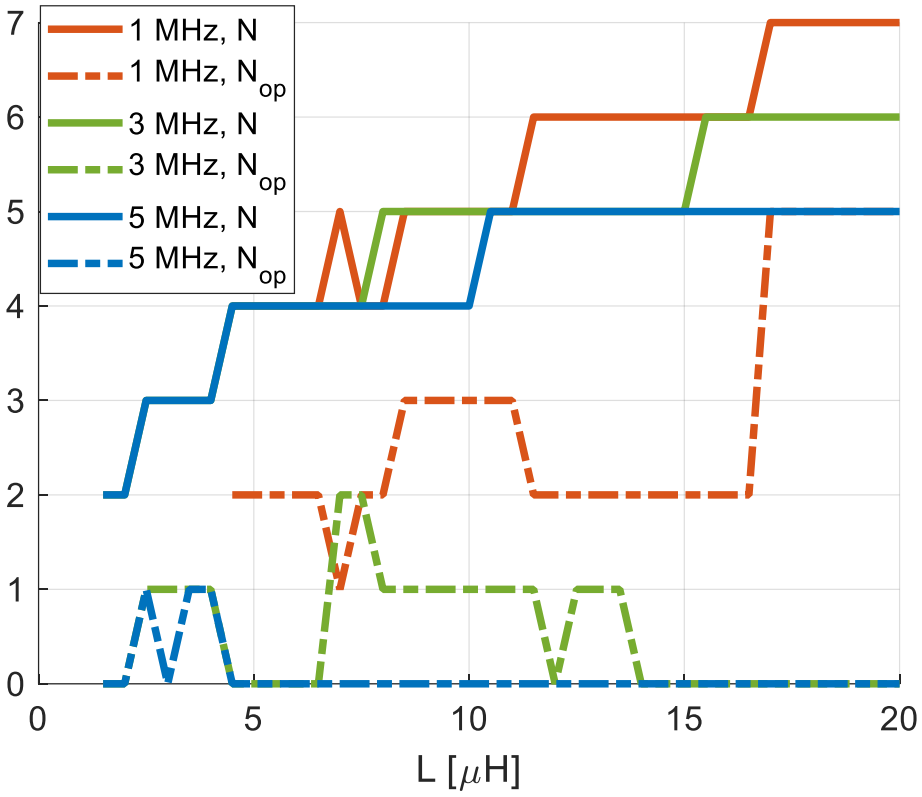


Fig. 171. Number of turns comparison for 3-layer truncated coil

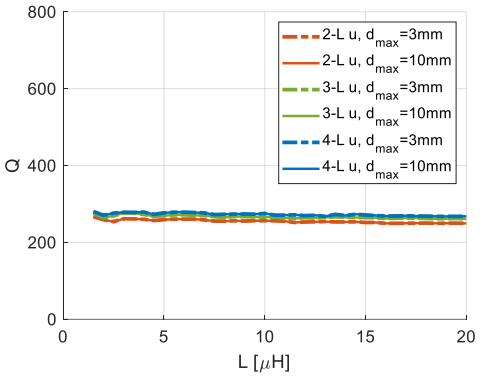
capacitance generated will be reduced. Accordingly, the copper width can be increased for each layer. Fig. 172 compares the quality factor of 2-layer, 3-layer, and 4-layer uniform SR coil with different total allowed dielectric thickness. For a given total allowed dielectric thickness d_{max}, more copper layer is advantageous when the capacitance is small, and copper width can be wider due to the fringing effect especially at 5 MHz.

To show the limiting factor for quality factor and to explore the role of total allowed coil thickness, a 2-layer uniform coil is used as an example in Fig. 173 to show the possible quality factor increase by allowing higher dielectric thickness. At 1 MHz, there is no difference in quality factor, since the required dielectric thickness is well below the limit as shown in Fig. 174(a). On the contrary, at 5 MHz, the quality factor will continue to increase with the increasing inductance. However, one should note that, as shown in Fig. 174 (c), at this time the required total dielectric thickness is extremely high to accommodate wider copper traces on each layer, which is not feasible at all for practical coil design.

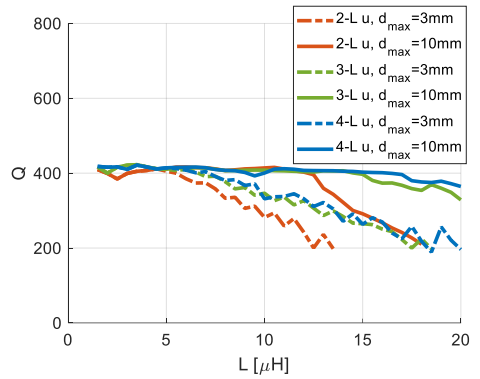
In other words, increasing the number of layers to have higher quality factor is only feasible at high frequency and high inductance. Extremely high quality factor is possible, but at the sacrifice of the coil pad thickness and corresponding power density.

8.4 Multi-layer SR Coil Comparison and Summary

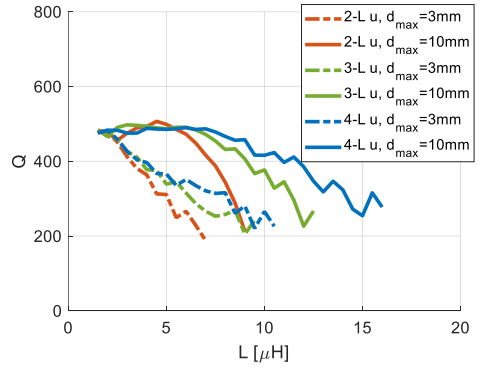
In Fig. 175, different types of multi-layer SR coil structures are compared in terms of the optimized quality factor at different resonant frequencies, including 2-layer uniform, 3-layer uniform, 4-layer uniform, 3-layer non-uniform, 4-layer non-uniform, and 3-layer truncated SR coils. For a fair comparison, the same total allowed coil thickness is set as 3 mm with 200 mm coil pad radius for all structures.



(a)

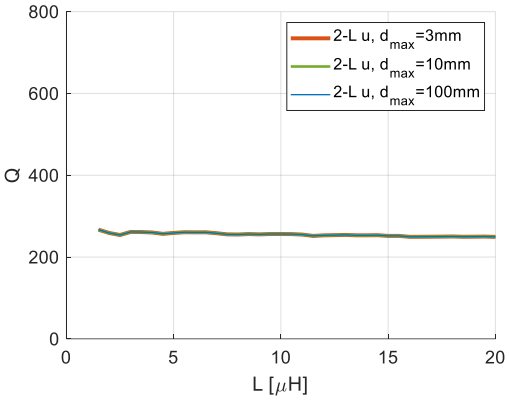


(b)

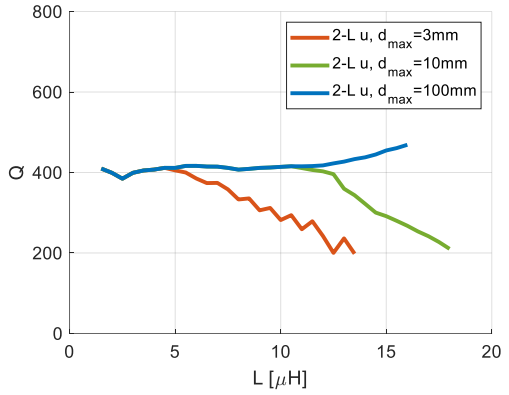


(c)

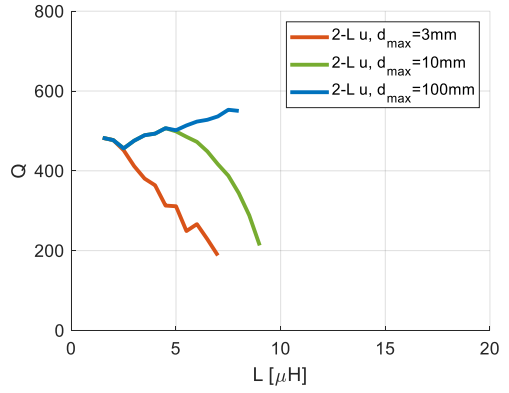
Fig. 172. 2-layer, 3-layer, and 4-layer uniform coil quality factor comparison with different total allowed dielectric thickness (a) 1 MHz (b) 3 MHz (c) 5 MHz



(a)

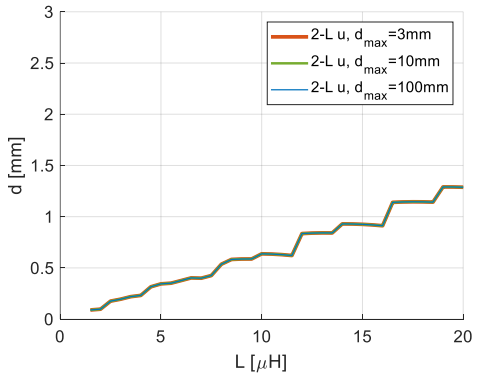


(b)

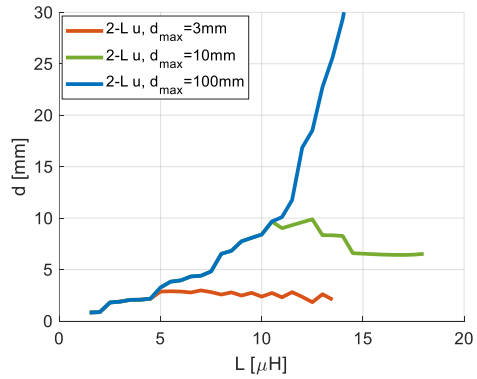


(c)

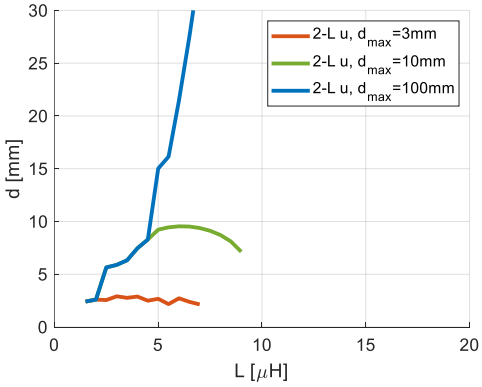
Fig. 173. 2-layer uniform coil quality factor comparison with different total allowed dielectric thickness (a) 1 MHz (b) 3 MHz (c) 5 MHz



(a)

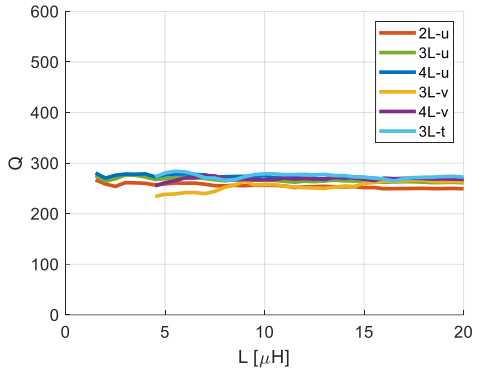


(b)

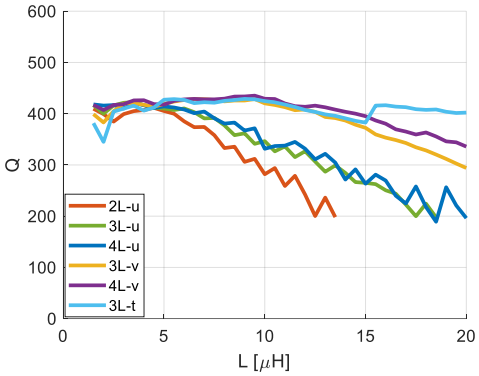


(c)

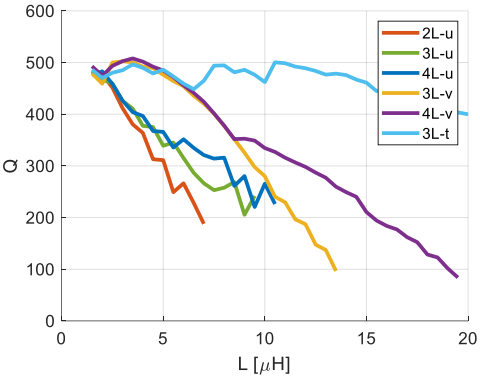
Fig. 174. 2-layer uniform coil total dielectric thickness comparison with different total allowed dielectric thickness (a) 1 MHz (b) 3 MHz (c) 5 MHz



(a)



(b)



(c)

Fig. 175. Quality factor comparison for proposed different types of multi-layer SR coil structure (a) 1 MHz (b) 3 MHz (c) 5 MHz

Multi-layer uniform SR coils take advantage of the better confined fringing electric field, and further increasing the number of layers will continue to improve the quality factor, though with diminishing returns considering the increasing manufacture complexity and limited total allowed dielectric thickness.

Multi-layer non-uniform SR coils enjoy the advantages of both better confined fringing electric field and better current sharing compared to uniform SR coils. The copper trace with varying width allows more-evenly distributed current and wider copper traces in the higher current density areas of the coil. As a result, the quality factor is further improved.

Truncated SR coils give an alternative method to manipulate the current distribution using spiral length instead of the width. Though the current sharing effect is not improved much compared to the non-uniform SR coils, the truncated spiral length allows much wider copper width for quality factor improvement, especially at high frequency, high inductance region where coil area is not fully utilized.

Some major conclusions are summarized below for the coil structure selection for the 6.6 kW wireless charger with 200 mm radius and 3 mm maximum thickness:

(a). For relatively low frequency WPT system design at 1-3 MHz, multi-layer non-uniform and truncated SR coil structures give less than 10% improvement on the coil quality factor, and 2-layer or 3-layer SR coil with uniform copper width is preferred for the simplicity of the structure.

(b). For relative high frequency WPT system design above 5 MHz, the 3-layer truncated SR coil gives the optimal quality factor since it can fully utilize the coil pad area for copper width.

(c). For any frequency in between, both non-uniform and truncated coil structures give

higher quality factor than the uniform SR coils in most of the inductance range. The optimal coil structure and optimal system frequency needs to be determined by incorporating into the system model to identify the maximum system efficiency point.

To improve the power delivery capability using proposed SR coil structure, higher inductance and low frequency design is preferred since the current power limiting factor is the thermal stress on the GaN-based high frequency inverter. As a result, both inductance and capacitance generated in the SR coil need to be increased, which will lead to a larger coil size and thinner dielectric laminate. In addition, the truncated SR coil is not preferred, and 2-layer SR coil gives the highest capacitance generation due to the large trace overlapping area compared to the truncated case and high fringing capacitance compared to the multi-layer non-uniform case. Aa a result, for future higher power wireless charging, SR coils with uniform copper width are preferred, and how to design for better current sharing is the key for quality factor improvement. Dielectric materials with small thickness, low loss, and high dielectric strength are also critical for the system efficiency.

CHAPTER 9. CONCLUSIONS AND FUTURE WORK

9.1 Work Summary

In this dissertation, high frequency WPT system for EV charging has been investigated systematically, and a MHz WPT system with self-resonant coil has been proposed and validated with compact design.

WPT system maximum coil-to-coil efficiency is determined by the coupling coefficient and quality factor of coils. Although coupling coefficient is mainly constrained by the airgap distance between transmitter coil and receiver coil, the quality factor can be increased with higher frequency if the resistance of coil is well-regulated. A coil with smaller footprint is possible since less coupled inductance is needed for the same power delivery capability. To cancel the reactive power in the loop and reduce the power loss, compensation networks are often required for the coils, and higher resonant frequency is also beneficial for a smaller compensation capacitance.

Self-resonant structures are suitable for high frequency coil design in WPT systems for low cost and easy implementation at MHz compared to Litz wire. The utilization of parasitic capacitance as the compensation makes the coil structure more compact. In this dissertation, different structures of SR coil have been evaluated, and a multi-layer non-uniform SR coil is proposed. The current is gradually transferred and shared among all copper layers, substantially decreasing the equivalent ESR of the coil. The inductance generated from the spiral coil resonates with the interlayer capacitance, forming a series self-resonant structure. Compared to other SR coils in the literature, the proposed multi-layer structure provides a solution for coil design in WPT system with characteristics of

large inductance and high power transfer capability.

The inductance and capacitance models of the proposed SR coil have been established, with verification in 2D FEMM and 3D HFSS simulations. Due to the relatively large distance between copper layers compared to the thickness of dielectric material in between, the fringing capacitance plays a critical role in coil ESR reduction in addition to the current sharing among layers. With more copper layers, the fringing electric field is better-confined between adjacent layers, and larger copper area is needed for each layer to have sufficient parasitic capacitance. Equivalently, a higher quality factor design is available. Through detailed geometry modeling aided with FEMM simulation, three coil structures, including conventional two-layer, three-layer with uniform copper trace width, and three-layer with non-uniform copper trace width, are optimized and compared under different inductance value, coil size, and resonant frequency. Optimization results show that three-layer non-uniform structure gives highest quality factor for its better current sharing and utilization of fringing capacitance.

The WPT power stages including inverter and rectifier have been designed together with the optimization results for proposed multi-layer coil. A detailed system loss model is proposed, quantifying the conduction, switching, and C_{oss} related hysteresis losses in power stages. Dynamics brought by the output capacitance of GaN transistors and SiC diodes are also considered, achieving ZVS for all GaN transistors. The proposed system design flow chart gives the design guidance to select system operating point and corresponding coil design for a 6.6 kW power output system.

The concept of high frequency WPT system with proposed SR coil is validated with fabricated 200 mm radius coil prototype, with 3 mm dielectric thickness and only 2 oz

copper thickness. Different fabrication methods have been tested and optimized, and coils are manufactured with laser cutting and acid etching. There is a good alignment between the results from model, simulation and measurement on coil, with a tested quality factor exceeding 450 at 3 MHz resonant frequency. The robustness of finished coils is also verified, including the dielectric strength of laminate material and the thermal dissipation of the completed coil. After the fabrication, the transmitter coil and receiver coil are clamped and supported with a polycarbonate structure, with designs on the creepage clearance and avoiding extra dielectric loss.

With high switching frequency, the negative impact of parasitic inductance and capacitance in the PCB becomes more obvious, which may jeopardize the robustness of the hardware. To prevent cross-talk and excessive voltage spikes, both gate driver loop and power loop have been carefully designed. In addition, the capacitance between PCB layers is minimized, since it will shift the system operating point, cause more dielectric loss, and may affect the completeness of ZVS during switching transient. The PCB layout is optimized and simulated in Q3D, providing quantification for an accurate system loss model. To dissipate the high switching loss in GaN transistors, heatsinks with forced air cooling are installed on PCBs, with a customized air duct to laminate the air flow for a better thermal management.

A 6.6 kW power test is performed with the proposed multi-layer coils with 100 mm airgap distance. The measured operating point matches well with the modeling and simulation results, and the system DC-DC efficiency is 95.2%, with 52.5 kW/m^2 power density. Through detailed design and optimization, this dissertation proves the concept of high frequency WPT system at kW for EV application, with high power density and high

efficiency enabled by the innovative multi-layer non-uniform SR coil structure.

For the implementation of the proposed SR coils on the vehicle, proper shielding is needed to attenuate the impact from any metal components around the coil, including the vehicle chassis which is usually made of steel or aluminum alloys. In this dissertation, ferrite cores are used together with the aluminum plate to shield the SR coil. However, compared to the conventional 85 kHz WPT systems, the parasitic capacitance caused by the shielding between the coil turns has greater impact on the coil performance due to the closer distance between the designed series-resonant frequency and parasitic parallel-resonant frequency. A system-level shielding design optimization method is proposed, with the trade-off between the system efficiency and coil pad power density. Completed coil pads including the SR coil, PTFE spacer, ferrite, aluminum plate, and clamping polycarbonate plate are fabricated and assembled. Together with the power electronics, the final WPT system with shielding achieves 92.3% DC-DC efficiency and 7.1 kW/dm^3 volumetric power density. It demonstrates the first 6.6-kW WPT system for EV charging using compact self-resonant coils at MHz with practical shielding implementation.

The concept of multi-layer non-uniform SR coils can be extended to more layers. Further increasing the number of layers with varying width will continue to improve current sharing, though with diminishing returns. The benefit of additional layers is physically bounded by the size of the coil. With more inter-layer capacitors connected in series, the width of copper layer needs to be increased accordingly to maintain a same total equivalent capacitance of the coil. In addition, the increased proximity loss among layers will eventually outweigh the benefit of current sharing as the number of layer increases. Another type of SR coil with truncated copper spiral length is also proposed. By

manipulating the copper trace length instead of the width, current sharing can be also controlled. All proposed multi-layer SR coil structures are optimized and compared with the same given coil thickness. It has been found that higher frequency design prefers the 3-layer truncated SR coil for its fully utilization of the coil surface area.

9.2 Conclusions and Research Contributions

In this work, a 6.6-kW high frequency WPT system for EV charging is demonstrated using lightweight and compact multi-layer non-uniform SR coils. Fig. 176 shows the state-of-the-art wireless EV chargers together with the proposed system in this paper. Comparing with other IPT systems, it is the first high frequency WPT system reported achieving 6.6 kW at MHz range, with the following advantages.

With the proposed multi-layer non-uniform SR coil structure, the quality factor remains above 400 at MHz range, which enables high coil-to-coil efficiency. Although the skin and proximity effects at high frequency increase the coil resistance, the coil can still maintain a relatively high quality factor due to the multi-layer structure with current sharing. High inductance can be achieved with the proposed multi-turn SR coil.

The proposed system has a compact size for passive components and no external compensation capacitors are needed with the proposed SR coil. With the saved size and cost of the compensation capacitors and associated cooling system, the system power density will be more advantageous to the state-of-the-art low frequency systems if compensation networks are included in the calculation of power density in Fig. 176.

The coils are made with lightweight and low-cost copper foils and no expensive Litz

wire is needed, which will reduce the energy loss due to the weight of receiver coil under the vehicle and the system manufacture cost in industrial applications.

For the practical implementation of the proposed SR coils, a complete shielding structure is optimized and fabricated, and the parallel resonance caused by the shielding is analyzed in detail. The final receiver coil pad with ferrites and aluminum shielding is only 7.1 mm in thickness, achieving 92.3% DC-DC efficiency and 7.1 kW/dm^3 volumetric power density.

Considering all the advantages above for the proposed system, the contributions of this work are summarized as below.

1. This work proposes a new self-resonant coil structure with high quality factor and high inductance, which is suitable for high frequency, high power WPT systems. The corresponding modeling and design method for the geometry optimization of the proposed self-resonant coil is also proposed.

2. This work validates the concept of high frequency high power wireless EV charging with the first reported design and demonstration of 6.6 kW WPT system at MHz range.

3. This work proposes a practical shielding solution with the proposed self-resonant coil, demonstrating the first 6.6-kW WPT system using compact self-resonant coils with practical shielding implementation.

4. This work summarizes and discusses different multi-layer self-resonant coil structures, providing structure selecting guidelines with in-depth analysis.

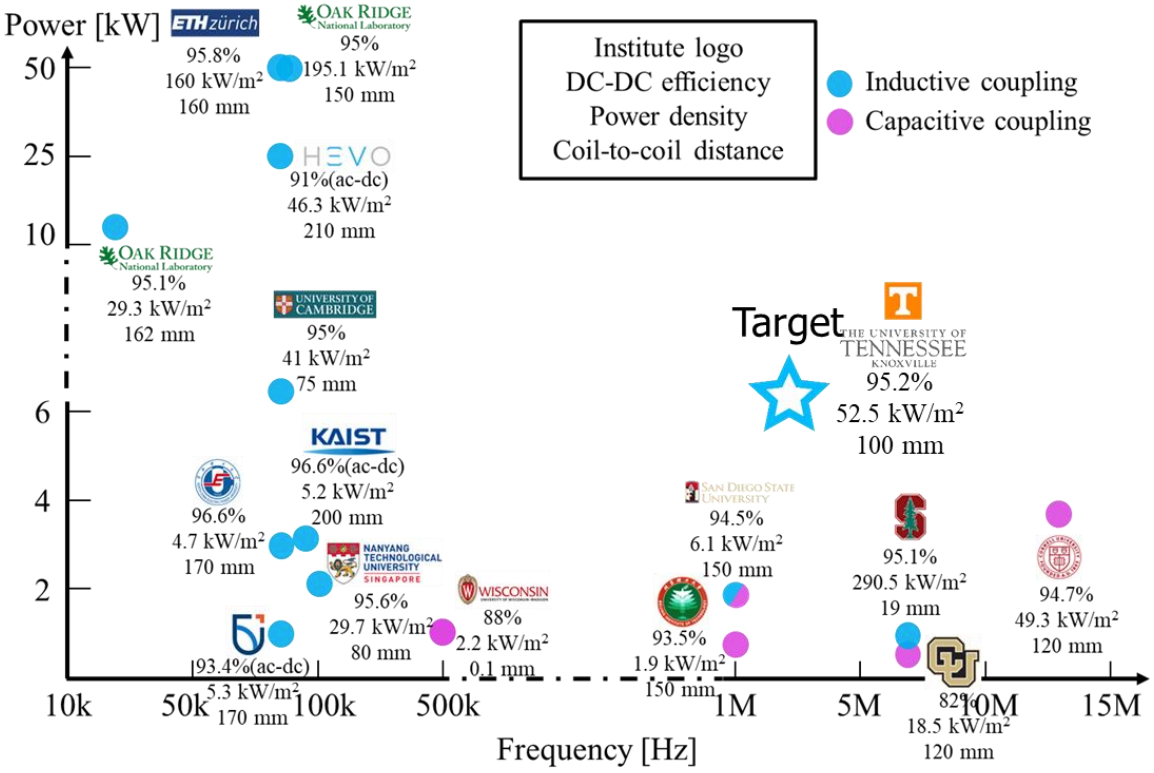


Fig. 176. State-of-the-art WPT systems for EV charging comparison

9.3 Future Work

9.3.1 Fine-tune Ferrite Geometry for Shielding

With the shielding designed for the proposed SR coils, Fig. 177 shows the magnetic flux density distribution. Clearly, most of the flux is channeled by the ferrite cores near the coil windings, and the ferrite cores at the center and the edge of coil pad is not fully utilized. Fig. 178 gives the quantitative plot for the magnetic flux density inside the ferrite cores along the coil radius.

The ferrite thickness at both ends can be reduced to have better utilization of ferrite material, but such method imposes the fabrication challenge considering the manufacturing limits. As a result, Fig. 179 gives an alternative fine-tuning plan for the shielding ferrites. Both inner edge and outer edge of the ferrite cores can be designed with saw-shape pattern to further reduce the weight while maintaining the major flux channeling capability of the ferrites. A shielded WPT system with higher power density is possible without sacrificing the system efficiency too much.

9.3.2 Synthesized WPT System Optimization with Multi-layer SR Coils

In the shielding design process, 3D electromagnetic simulations are applied to sweep for optimal shielding geometry, which is time-consuming. A possible future work would be proposing possible models for shielding impact on coil parameters including L, C, and R to relieve the computation burden for the design.

More importantly, as shown in Fig. 180, the shielding design in this dissertation in fact is optimized based on the established 3-layer non-uniform SR design at 3 MHz. With the new proposed coil modeling including the shielding impact, a synthesized system optimization process can be proposed to incorporate both coil geometry and shielding

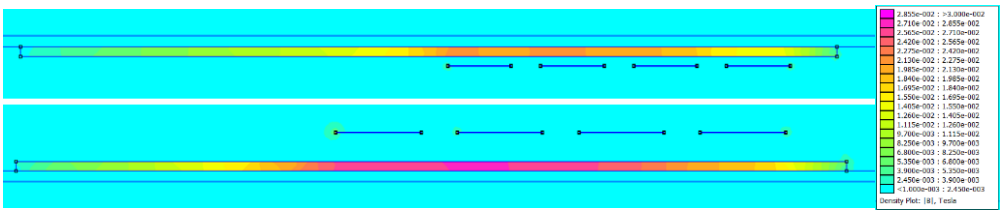


Fig. 177. Magnetic flux density for the proposed 6.6 kW system with shielding

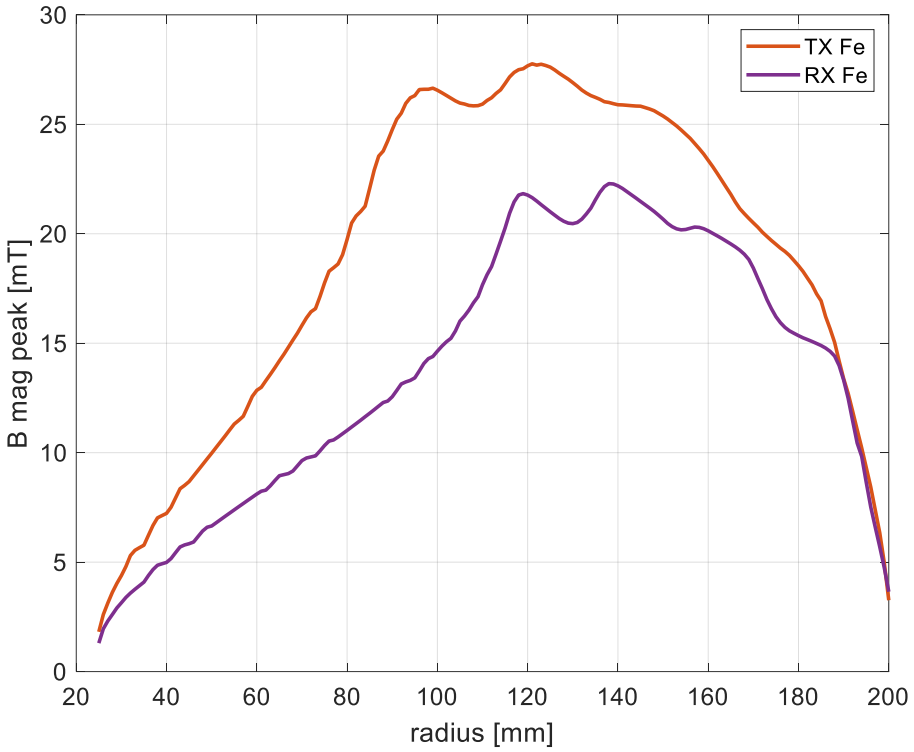


Fig. 178. Magnetic flux density magnitude inside the ferrite cores

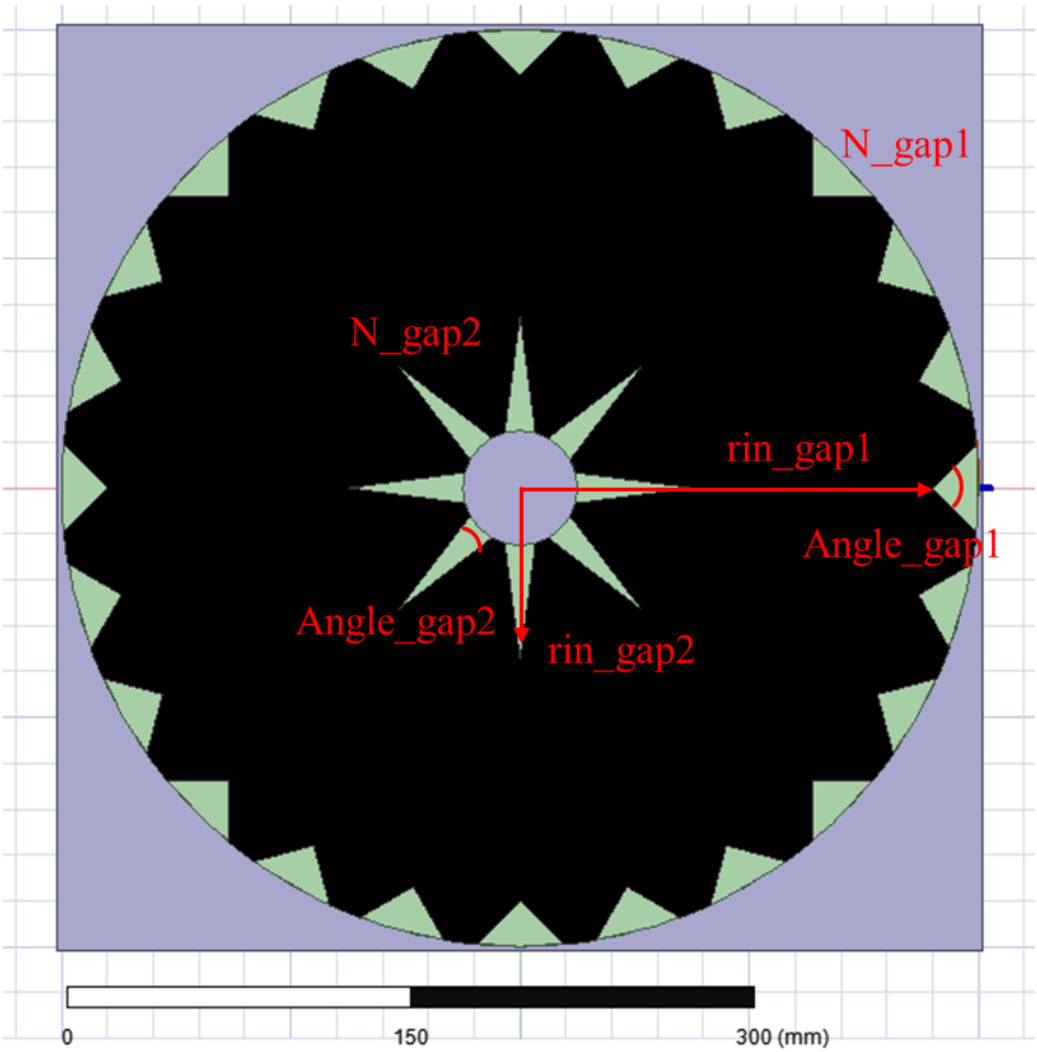
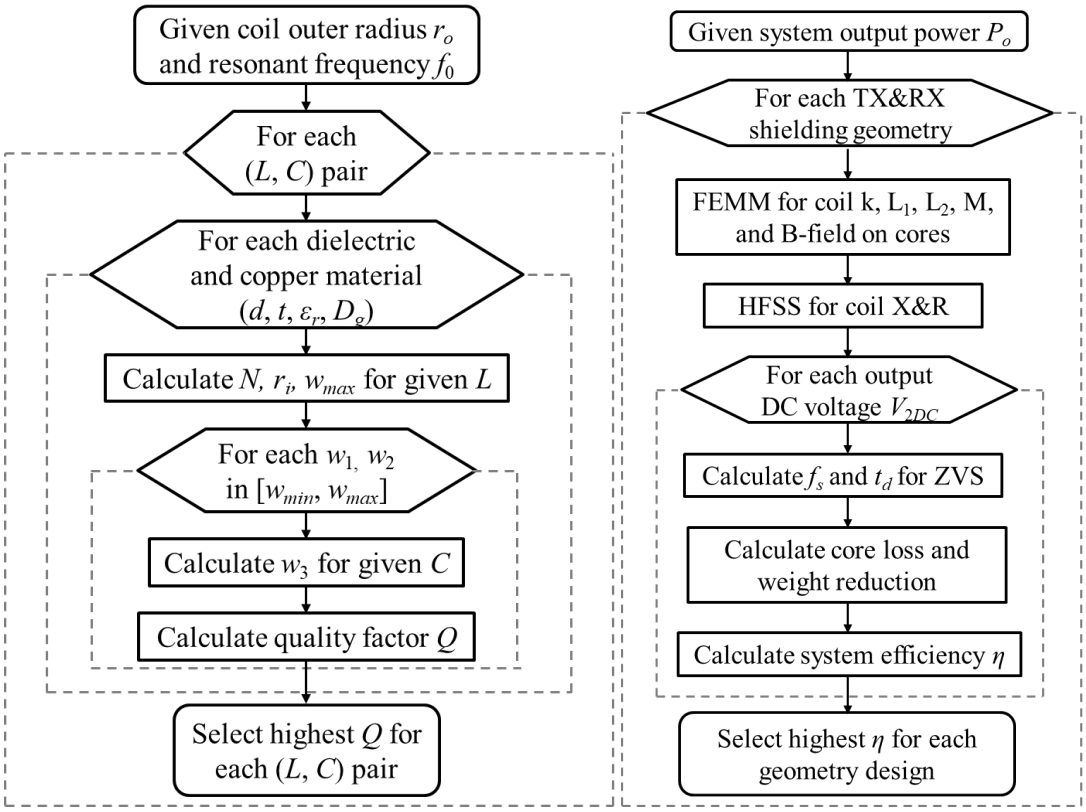


Fig. 179. Possible fine-tune plan for the shielding geometry

consideration for the optimal system performance trade-off between the efficiency and power density. Other multi-layer SR coil structure could give a better system performance from the new synthesized design flow chart.



(a) (b)

Fig. 180. Design flow chart (a) coil geometry for highest Q (b) shielding geometry for highest system efficiency

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