To the Graduate Council:

I am submitting herewith a dissertation written by M. Nance Ericson entitled "High-Temperature, High-Resolution A/D Conversion Using 2^{nd}- and 4^{th}-Order Cascaded ΣΔ Modulation in 3.3-V 0.5μm SOS-CMOS." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

James M. Rochelle
Major Professor

We have read this dissertation
and recommend its acceptance:

Charles L. Britton, Jr.

Benjamin J. Blalock

Donald W. Bouldin

Vasilios Alexiades

Accepted for the Council:

Dr. Anne Mayhew
Vice Provost and
Dean of Graduate Studies

(Original signatures are on file with official student records.)

High-Temperature, High-Resolution A/D Conversion Using 2^{nd}- and 4^{th}-Order Cascaded ΣΔ Modulation in 3.3-V 0.5μm SOS-CMOS

A Dissertation
Presented for the
Doctor of Philosophy Degree
The University of Tennessee, Knoxville

M. Nance Ericson
August 2002

Dedication

This dissertation is dedicated to my loving wife, Helen, and to my wonderful son, Stephen, who have provided much encouragement and support throughout this research.

Acknowledgements

I wish to thank Drs. Rochelle, Britton, Bouldin, Blalock, and Alexiades for their guidance as my committee. I especially want to thank my major professor, Dr. Rochelle, and colleague Dr. Britton, for their consistent encouragement and mentoring throughout my entire graduate experience. In addition, I want to thank Dr. Bobrek for his technical advice and valuable help throughout this work, and Dr. Clonts for his assistance in ASIC layout and simulation.

Many of my colleagues and friends provided support and encouragement that I want to mention: Dr. Gleason, Mike Emery, Dr. Paulus, Dr. Wintenberg, Dr. Smith, and Dr. Simpson. I also want to thank the management of the project under which much of this work was performed, specifically Dr. Roger Schultz and Tony Moore. I also thank Alex Bobrek, who wrote much of the data collection and signal processing software associated with this research.

I thank the staff at Oak Ridge National Laboratory, particularly Bill Bryan, Gary Alley, Dan McDonald, and Janet Swift for their support of my 2-year educational sabbatical that was instrumental in my decision to pursue this PhD. I also want to thank Gayle Jones and Kathy Martin for their help in preparing this document, and Norm Cooper of Mustagh Resources, Inc. and Mike Wolfe of Audio Precision, Inc. for helpful discussions.

Finally, I want to thank my parents and family for their encouragement and support.

Abstract

Sigma Delta Modulation is an oversampling technique commonly used in high-resolution analog-to-digital conversion. By employing oversampling and quantization noise shaping, the method allows very high-resolution conversion using low-resolution functional blocks. A multitude of architectural variations of this oversampled class of digitizers has been explored and reported in research literature for a wide variety of applications including seismic imaging, general low-bandwidth high-resolution instrumentation, audio conversion, and most recently high-speed communications.

Data conversion associated with seismic imaging has been recently dominated by this class of converters, though all data acquisition systems require environmental control, preventing placement of the digitizing electronics down-hole. The potential improvement in seismic imaging system performance afforded by down-hole placement of electronics is very significant. The use of sensor-localized data collection nodes will provide the optimal sensor interface, both in terms of connectivity and noise, and allow distributed parallel collection and processing of sensor signals. The use of spread spectrum communications methods for up-hole data transmission significantly increases the data integrity and potential throughput. However, in order to realize this improved system partitioning, the high-resolution data converters must be designed to meet operational specifications at elevated temperatures.

This research addresses the issue of high-resolution data conversion at elevated temperatures, with an emphasis on applicability to down-hole seismic imaging. Sigma delta modulation methods are employed and the theoretical best topology selected for imple-

mentation. Variations in target integrated circuit processes are considered and the most appropriate process for high-temperature implementation employed. A prototype sigma delta ADC was designed, fabricated, and fully characterized over temperature. The results of this research provides the first high-resolution digitizing front-end suitable for down-hole seismic imaging applications and lays the foundation for future high-temperature ADC research.

Table of Contents

List of Tables

List of Figures

CHAPTER 1

INTRODUCTION

1.1 Background

The goal of this research is to develop a high-resolution data converter suitable for the high temperature environment associated with down-hole seismic imaging. This section reviews general seismic imaging methods and associated measurement requirements, and provides an overview of the progression of commercially available instrumentation designed to address the specific needs of this field.

1.2 Seismic Imaging Methods & Instrumentation

Seismic methods employ sound waves to characterize subsurface formations in the earth's crust. Variations in geology filter the traveling acoustic waves. The variation in the traveling waves arriving at a sensor array are detected, processed, and used to determine the location and volume of oil and gas deposits. These variations are the result of reflection and refraction of the traveling wave and are observed as phase and amplitude effects. Using a number of processing algorithms, the multi-sensor data is then used to produce an image of the interrogated region. This general method is widely applied to both oil and gas exploration and oil well management, as well as other geological surveys.

In general, seismic methods can be divided into two primary categories: reflection mode and transmission mode. In reflection mode, the acoustic source and the detectors both lie in the same plane, typically placed along the surface of the ground. The sound waves from the source propagate through the medium and some portion are reflected by

subsurface features back to the detector array. Transmission mode requires that the source and detector arrays be located on opposing sides of the imaged medium. Of the two methods, reflection mode is the least invasive as both the source and detector array are typically located on the surface. However, in passing through the weathered layer twice, the acoustic waves are both low-pass filtered and significantly attenuated, resulting in received signals that are band-limited to the 8-120 Hz range. Reflection mode most commonly refers to Surface Seismic techniques (see Fig. 1.1). Transmission mode includes both Vertical Surface Propagation (VSP) and Cross-Well (CW) techniques (see Fig. 1.2). In VSP, the source is located on the surface and an array of detectors is placed in a vertical well. This approach has the advantage of only one pass through the surface or weathered layer. CW is an extension of VSP that eliminates propagation through the weather layer altogether by employing two wells, one having the source array and the other the detector array. This approach eliminates the effects of the weathered layer resulting in higher bandwidth signals (typically 8-2000 Hz). Detector arrays with readout electronics of sufficient sampling bandwidth and dynamic range can be employed for use in either transmission- or reflection-mode seismology. Other variations to these commonly used methods exist including hybrid approaches that fuse data from multiple methods.

The most demanding operational specification for digital seismic recorders is dynamic range. Due to the absorption properties of the earth, a large amount of acoustical energy has to be applied by the excitation source. Each acoustic sensor will detect both the initial direct acoustic wave along with many attenuated reflected/refracted components resulting in very demanding dynamic range requirements.

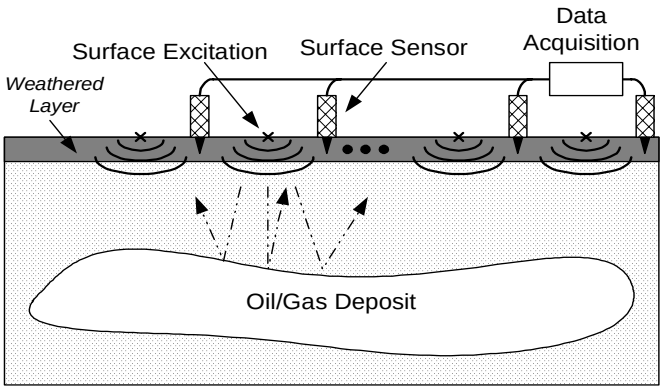


Figure 1.1 Surface seismic imaging.

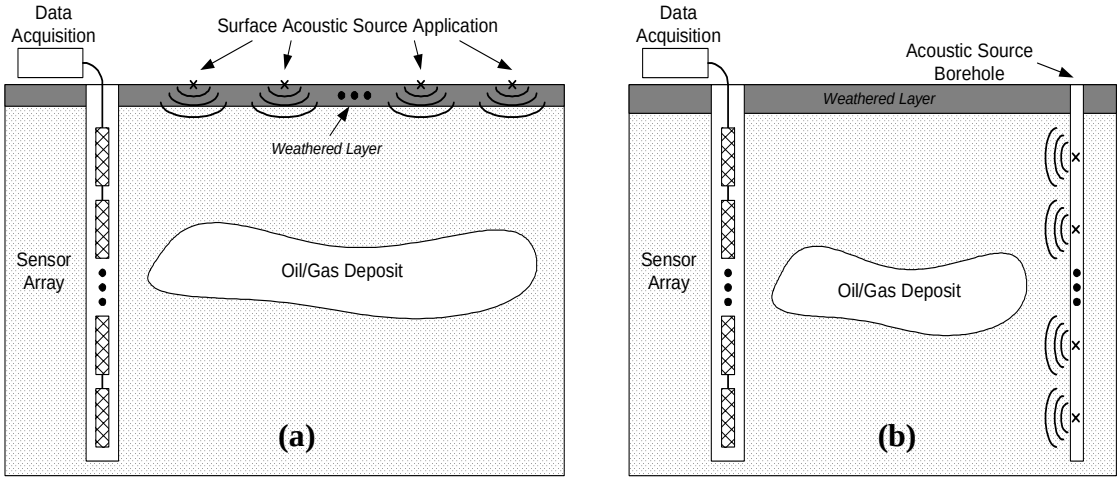


Figure 1.2 Transmission mode seismic imaging methods. (a) Vertical Seismic Profiling (VSP) and (b) Cross Well (CW).

This dynamic range is further complicated by having sensors at the surface near the sources, and sensors at distances exceeding 10,000 ft. downhole. For these reasons, sensors and readout electronics with large dynamic range (16-24 bits) are required for high resolution imaging.

Early seismic recorders stored analog signals from sensor arrays directly to magnetic tape. In the 1980s, digital seismic recorders emerged that digitized and stored the data using limited resolution analog-to-digital converters (ADCs). To increase the overall dynamic range beyond that offered by then state-of-the-art ADCs, the integer floating point (IFP) amplifier was developed [33,77,132,170,177,178,179]. IFP techniques are based on using a variable gain amplifier with binary weighted gains. At the beginning of each sampling cycle, the optimum gain for each sensor channel is determined and applied prior to digitization. The optimum gain is that which causes an ADC output code between one-half and full scale, or where the ADC most significant bit (MSB) equals 1. The output of the IFP block is then input to a moderate resolution ADC (12-16 bits). Using binary weights allows the gain code bits to be added to the ADC output code as the MSBs. Fig. 1.3 shows a block diagram for a typical IFP amplifier system. A track and hold is used to allow time for the optimum channel gain to be determined. Often two IFP channels are used for a single signal channel to allow sufficient time for gain selection and amplifier settling. The IFP channel of Fig. 1.3 has a 20-bit intrinsic dynamic range (120.4 dB).

Though IFP topologies do provide an improvement in dynamic range over fixed gain topologies, the use of switched, high-gain front-ends produce a number of complications that make practical implementation and use difficult. High performance track and hold and gain circuits are essential requiring calibration of each gain stage and separate offset

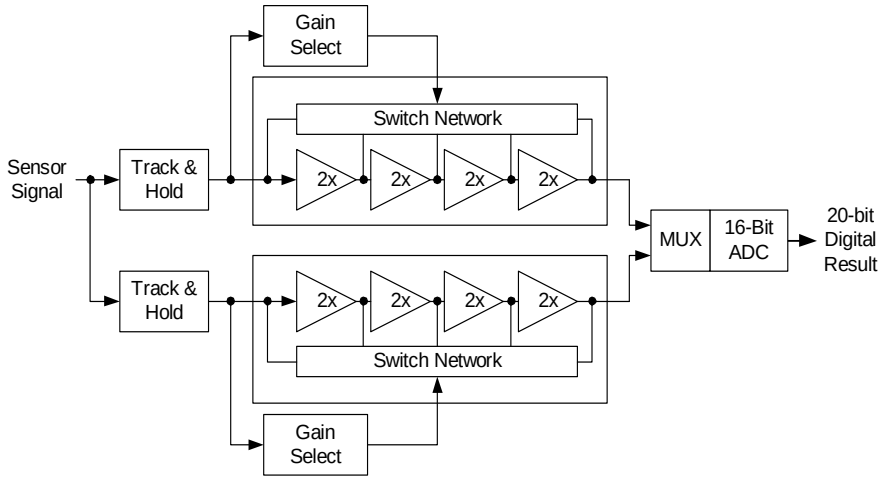


Figure 1.3 Instantaneous floating point (IFP) amplifier.

correction of both the track and hold circuits and each of the gain stages. The use of multiple variable-gain amplifiers introduce errors between different gain ranges, reducing linearity and making monotonic operation difficult - particularly over wide temperature ranges. In addition, complex control for dynamic optimal gain selection is required. Though these problems have been somewhat addressed by topological improvements, dc offset correction methods, and gain correction and calibration procedures [33,77,132,170,177,178,179], the use of IFP in digital seismic recorders came to a complete halt in the 1990s with the maturing of a new class of high-resolution, oversampling ADCs employing sigma delta modulation. However, no commercial or research literature has addressed placing the high-resolution data converters down-hole, due to extreme temperature ranges required and associated complications.

Though many commercially available ADCs indicate 24-bit resolution, the effective resolution of commercially available ADCs is as high as 22.5 bits @ 5 Hz bandwidth (or

20 bits @ 1 kHz bandwidth) [220]. The specification of 24-bit dynamic range is widely accepted in seismic systems, though a much reduced effective resolution is actually obtained. High-resolution commercially available ADCs are specified for a maximum temperature range of -40°C to 85°C with most units specified over a more limited range of 0°C to 70°C. Clearly, the temperature variations anticipated in the target application (0°C to 160°C) far exceed the specifications of any available over-sampled data converter.

The target application for this research is conventional VSP seismic systems that currently employ surface electronics and down-hole sensors at depths up to 10000 ft. Significant signal degradation associated with long distance sensor cable could be eliminated if a sensor-localized ADC were available. This would enable packetized digital data transfer and improve the fidelity of sensitive sensor signals. In addition, a system topology based on smart, sensor-localized nodes provides a number of advantages including digital data transfer, localized signal processing, increased signal channel number, and advanced monitoring and reporting functions. A block diagram of this improved system architecture is shown in Fig. 1.4 along with the conventional topology consisting of surface electronics, for comparison. However, the temperature limitations of existing commercial ADCs prohibit the design of such a system.

1.3 Overview of High-Temperature Fabrication Processes

In recent years, Silicon-On-Insulator (SOI) CMOS technology has emerged as the dominant technology for the realization of high-temperature integrated circuits. A number of research publications have demonstrated operation of SOI CMOS circuits at tempera-

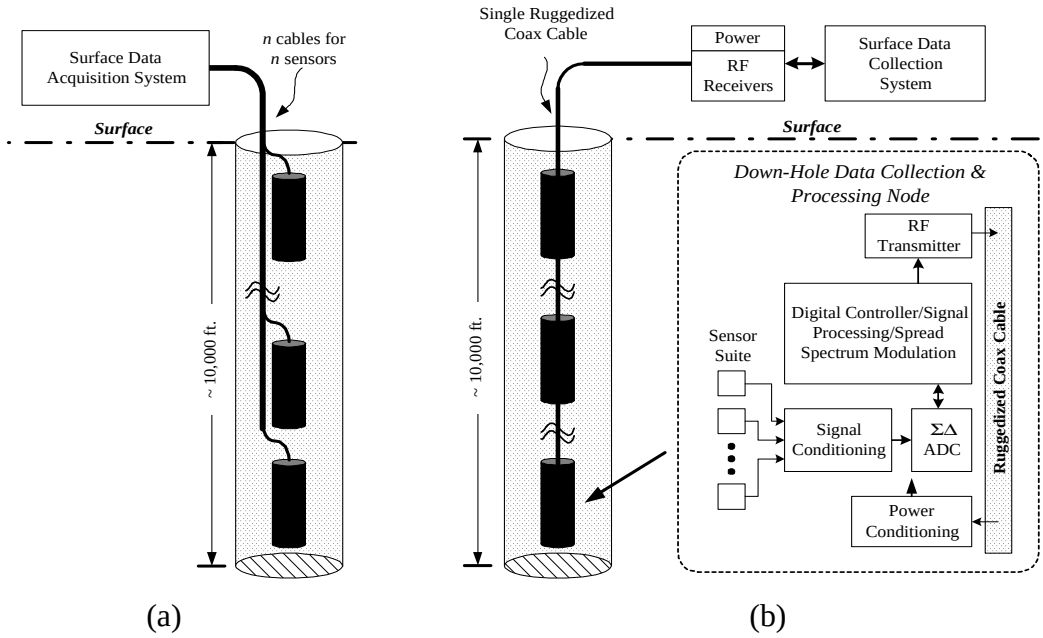


Figure 1.4 Seismic system electronics configurations. (a) Conventional surface-based system, and (b) proposed distributed system.

tures up to 300° C [38,39,48,61,65]. SOI integrated circuit fabrication technology offers many performance advantages over the industry standard bulk CMOS process technologies. Significant reduction in leakage current and substrate induced noise, and improvement in maximum operational speed and power efficiency are the most significant performance improvements of SOI over bulk CMOS. Other advantages of SOI over bulk CMOS include latch-up immunity and lower parasitic capacitances. Disadvantages of SOI as compared to bulk CMOS include higher material cost, reduced availability, higher defect density, and higher thermal resistivity resulting in increased self-heating [59,123].

SOI is a general category that is composed of two primary technologies - Separation by IMplantation of OXygen (SIMOX) and Silicon-On-Sapphire (SOS). SIMOX starts with a silicon substrate that is implanted with oxygen to form an insulator layer (buried

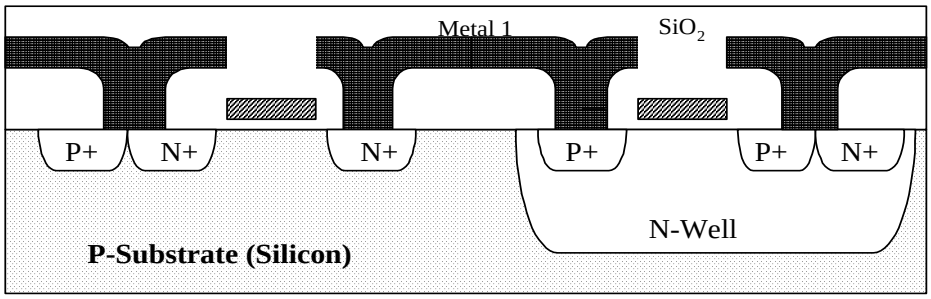
oxide layer) just under the surface. Devices are then constructed using the surface layer (as in bulk) resulting in a CMOS technology that is electrically isolated from the substrate.

SOS was first developed and used in the 1970s for applications in high radiation environments. The SOS process begins with a sapphire insulating substrate. A thin epitaxial layer of silicon is grown, and doped to form the drain, source, and channel regions of transistors. These doped areas extend to the sapphire insulator effectively eliminating significant back-gate biasing. Early application of the technology was very limited due to the high cost of fabrication and the defects associated with the silicon/oxide interface. However, recent advances in processing have made SOS a competitive technology with SIMOX and bulk CMOS.

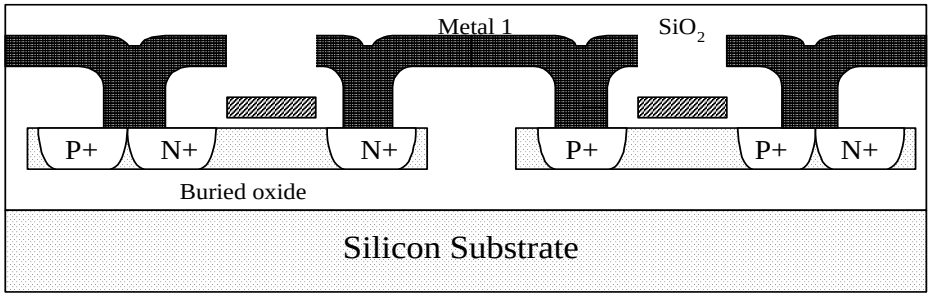
The advantages of SOS as compared to bulk is the same as those mentioned for SIMOX, namely reduced leakage currents, higher speed due to reduced parasitic capacitance, reduced substrate induced noise, and latch-up immunity. One difference is that SIMOX does have backgate biasing not present in SOS. Silicon-On-Sapphire was chosen as the fabrication technology for this research due to the availability of an SOS fabrication process through MOSIS, and the lack of backgate bias in SOS devices. Fig. 1.5 shows the primary physical differences between SIMOX, SOS, and bulk CMOS processing.

1.4 Dissertation Overview

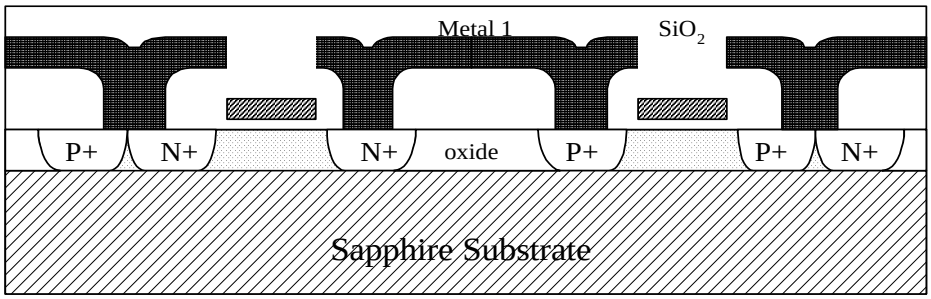
This research addresses the specific problem of high-temperature, high-resolution data conversion associated with the placement of data acquisition electronics down-hole. This goal will be realized by employing sigma delta modulation techniques, appropriate modu-



(a)



(b)



(c)

Figure 1.5 Comparison of CMOS fabrication technologies. (a) Bulk CMOS, (b) separation by implantation of oxygen SIMOX, and (c) Silicon-on-sapphire (SOS).

lator topology selection, proper fabrication process selection, and circuit design methods to maximize high-temperature performance and survivability.

This dissertation is organized into 8 chapters. Chapter 1 provides a general overview of the field of seismic imaging and summarizes the types of instrumentation historically applied to this field. The performance and environmental requirements for down-hole seismic instrumentation is reviewed emphasizing the associated difficulty of addressing the data acquisition needs of this field. In Chapter 2, the concept of analog-to-digital conversion is introduced with an emphasis on theoretical performance comparisons of Nyquist rate and oversampled data converter types ($\Sigma\Delta$). Chapter 3 provides an overview of candidate $\Sigma\Delta$ modulator architectures and compares the relative advantages and disadvantages of each topology. Having introduced the concept of $\Sigma\Delta$ modulation and associated terms, Chapter 4 provides a detailed review of the modulators published in open literature. Comparisons between single loop and cascaded architectures are made using two published performance metrics and a new performance metric introduced specifically for this research. A summary of the limited published results of modulators either fabricated in SOI/SOS CMOS or tested at elevated temperatures is presented and the specific need for this research is established. In Chapter 5, justifications for the modulator topology and associated parameters are given and the modulator design is outlined, including the design of both the circuit modules and the overall modulator. Simulation results are given where appropriate. Chapter 6 presents results of modulator circuit blocks tested from 25° C-200° C fabricated in SOS-CMOS. Comparisons to the simulations of Chapter 5 are provided when appropriate. Test results from the first 4^{th}-order modulator fabricated in SOS are presented in Chapter 7 and compared to a 2^{nd}-order modulator fabricated on

the same chip. All modulator tests are performed over a temperature range of 25°C-200°C. Details on the chip design, test methodology, test system hardware, and associated signal processing are also provided. Finally, Chapter 8 provides a conclusion of the research and identifies future directions for the furthering of this work.

CHAPTER 2

ANALOG-TO-DIGITAL CONVERTERS

An analog-to-digital converter (ADC) converts an analog signal composed of a continuum of values to a digital result. The ADC output is a digital best approximation of its input signal, with the approximation error (or quantization error) being related to the ADC resolution. ADCs can be classified as one of two types: Nyquist-rate or oversampling. Nyquist rate converters sample the input signal at approximately twice the highest frequency of the input signal using a number of different architectures including successive approximation, pipeline, algorithmic, and flash. Oversampling converters achieve improved resolution at the expense of conversion speed. Improved performance is accomplished by sampling the input signal at rates much higher than the Nyquist rate and shaping the quantization noise using single-loop low order, single-loop high order, cascaded, multi-rate, and multi-bit feedback loops, and associated combinations.

In this section, analytical expressions are developed demonstrating the advantages offered by ΣΔ modulation techniques over Nyquist rate converters.

2.1 Nyquist-Rate Converters

In an ADC, the relationship between the input voltage (V_{in}), the reference voltage (V_{ref}) and the digitized result (b0 - bn) can be represented by

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_n 2^{-n}) = V_{in} + e_q \tag{2.1}$$

where e_q represents the quantization error associated with the conversion. Thus a quantizer maps a continuum of input analog values to a discrete set of output levels. An n-bit quantizer maps an analog input range of values to 2^n discrete output levels.

A quantizer can be modeled as a linear combination of the input signal x[n] multiplied by the quantizer gain (G), and a noise source e[n] representing the quantization noise:

$$y[n] = G \cdot x[n] + e_q[n]. \tag{2.2}$$

This relationship for a midrise quantizer is illustrated in Fig. 2.1. A midrise quantizer has transition points at the midpoint of its input range.

Following the representation given by Rabii [158], the output level steps are defined as

$$\delta = \frac{\Delta}{2^n - 1} \tag{2.3}$$

where Δ is the maximum output range. Likewise, the input level steps are defined as

$$\gamma = \frac{\Gamma}{2^n} \tag{2.4}$$

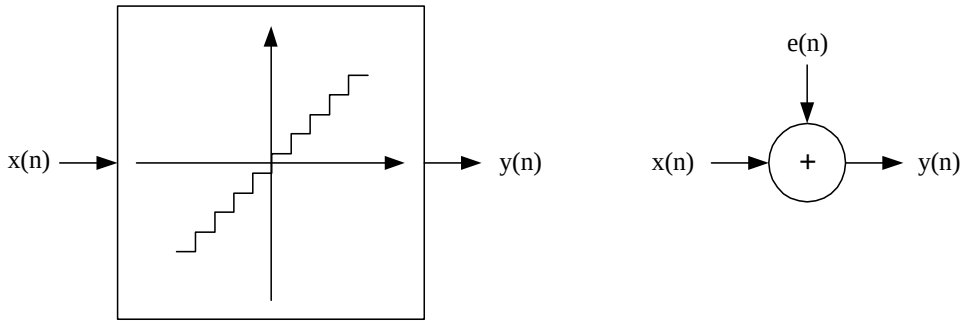


Figure 2.1 Quantizer diagrams. (a) graphical representation and (b) model including gain and quantization noise component.

where Γ is the full-scale input range. Using the notation of Eqn. 2.3 and Eqn. 2.4 the quantization characteristics for a ramp input produce a sawtooth quantization error as shown in Fig. 2.2. The linearized gain (G) of the quantizer can be expressed as

$$G = \frac{\delta}{\gamma} = \frac{\Delta(2^n)}{\Gamma(2^n - 1)}. \tag{2.5}$$

Clearly, the quantization error is nonlinear. However, a uniform white probability density assumption is valid if the following conditions are met: (a) the input signal does not exceed the input range of the quantizer, (b) the quantizer has a large number of quantization levels, (c) the input signal is active across many quantizer levels, and (d) the joint probability density of any two quantizer inputs is smooth [10,158,207,209]. Using the white noise approximation, the quantization noise probability density is shown in Fig. 2.3.

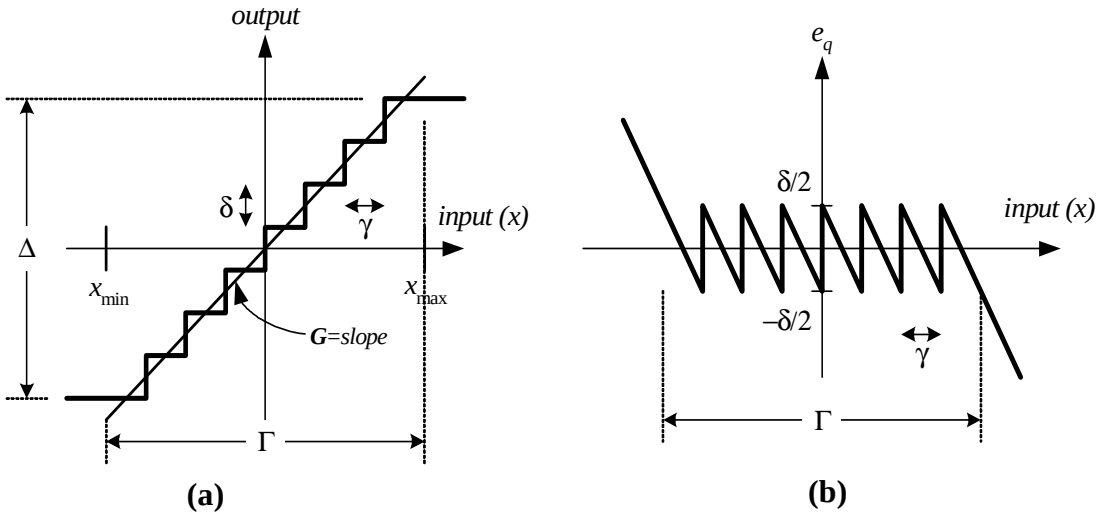


Figure 2.2 3-bit quantizer characteristics. (a) transfer function, and (b) quantization error.

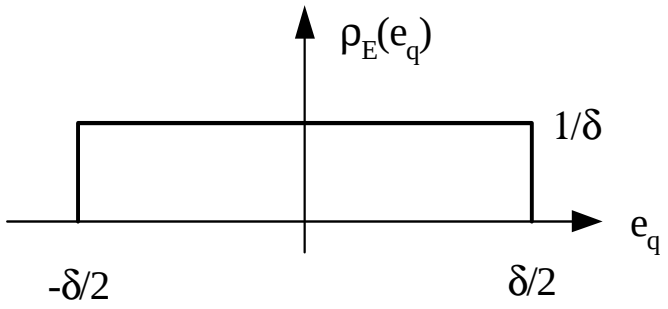


Figure 2.3 Quantization noise uniform probability density distribution.

The variance of this noise term is equal to the quantization noise power in this case and is expressed at the output as

$$\sigma_q^{\,2} = S_q = \int_{-\infty}^{\infty} e_q^{\,2} \rho_E(e_q) de_q = \frac{\delta^2}{12}. \tag{2.6}$$

In practice, one or more of the conditions listed above to justify the use of the white noise approximation are not valid. A more rigorous handling of this quantization probability density can be found in a number of contemporary publications [11,26,159]. Though inexact, use of the white noise approximation allows many useful performance metrics to be estimated and will be accepted for this work.

The primary performance metric commonly applied to ADCs and of special importance to the seismic industry is dynamic range (DR). Dynamic range is defined as the ratio of the full-scale input power to the power of the input signal when the signal-to-noise ratio is one. The signal-to-noise ratio (SNR) is measured at the output of the converter and equals the ratio of the signal power (S_s) to the quantization noise power (S_q).

Using the unity gain approximation for G, further described in later sections, the SNR of a Nyquist rate converter can be expressed as a power ratio with a sinusoidal input of amplitude A as

$$SNR = \frac{S_s}{S_q} = \frac{\frac{A^2}{2}}{\frac{\delta^2}{12}} = \frac{6A^2}{\delta^2}. \tag{2.7}$$

Alternatively, the SNR can be expressed in dB using the root mean square (rms) values of the input signal and quantization noise:

$$SNR_{dB} = 20 \cdot \log\left[\frac{V_{in_{rms}}}{V_{e_{rms}}}\right] = 20 \cdot \log\left[\frac{\frac{A}{\sqrt{2}}}{\frac{\delta}{\sqrt{12}}}\right] = 20 \cdot \log\left[\frac{2A}{\delta} \cdot \sqrt{\frac{3}{2}}\right][dB]. \tag{2.8}$$

From Eqn. 2.7, the SNR will be unity when the input signal power is $\delta^2/12G^2$. Consequently, the dynamic range can be expressed as

$$DR = \frac{\frac{(\Gamma/2)^2}{2}}{\frac{\delta^2}{12G^2}} = \frac{\frac{\gamma^2(2^{2n})}{8}}{\frac{\gamma^2}{12}} = \frac{3}{2}(2^{2n}). \tag{2.9}$$

Expressed in dB, the dynamic range of a Nyquist rate converter with a n-bit quantizer becomes

$$DR_{dB} = 1.76 + 6.02n \ . \tag{2.10}$$

Thus for a Nyquist rate converter to achieve a *DR* of 98dB (or 16 bits) requires a 16-bit quantizer. This requirement is beyond the practical achievable accuracy for untrimmed monolithic circuits [105,124] since matching of 1 part in 65536 (0.0015%) element

matching is required. As will be demonstrated, the methods employed in ΣΔ modulation allow much higher dynamic range to be obtained using low-resolution quantizers without high precision element matching.

2.2 Oversampling Converters

The previous section outlined the basic relationships between quantizer resolution, quantization noise, DR, and SNR for Nyquist-rate converters. Decreasing the quantile by increasing the quantizer resolution was shown to increase the dynamic range. However, implementation imperfections including matching errors and offsets limit the obtainable resolution of Nyquist rate converters.

Oversampling techniques were first introduced by Inose in 1962 and rely on oversampling of the input data and application of noise shaping and digital filtering functions to obtain high-resolution conversion [95]. The general topology of a ΣΔ ADC is shown in Fig. 2.4. The circuit is composed of a feedback modulator that shapes the quantization noise to reduce the noise power contribution in the signal bandwidth. Oversampling the input signal further reduces the in-band noise power. After modulation, a digital filter is used to downsample and filter the modulated signal to the Nyquist bandwidth. A summary of the signal spectral content that shows the oversampling, noise shaping, and digital filtering operations is also provided in Fig. 2.4. Oversampling and noise shaping are discussed in more detail in the remaining portions of this section.

Using the white noise approximation, oversampling alone has the effect of spreading the quantization noise power over the sampling bandwidth. Thus, a significant reduction

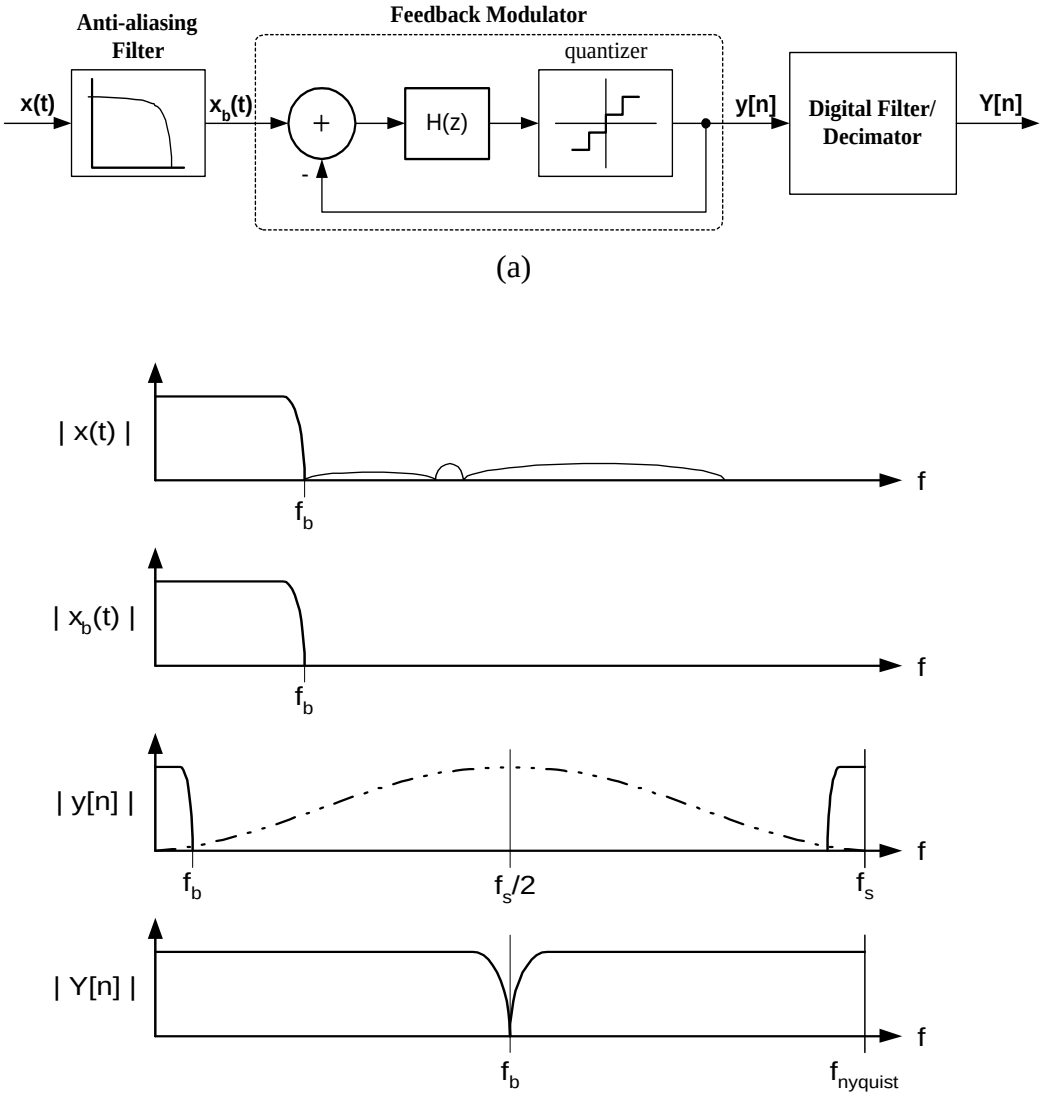


Figure 2.4 ΣΔ ADC Overview. (a) block diagram and (b) spectral content.

in the in-band quantization noise can be achieved by simply oversampling. The oversampling ratio, M, is defined as

$$M = \frac{f_s}{2f_b} = \frac{f_s}{f_n} \quad , \tag{2.11}$$

where f_s is the sampling frequency, f_b is the signal-bandwidth, and f_n is the Nyquist frequency. Oversampling the input by M and downsampling and filtering the modulator output to the signal bandwidth reduces the in-band quantization noise power by M. Incorporating oversampling, the dynamic range becomes

$$DR = \frac{S_s}{S_c / M} = \frac{3}{2} M(2^{2n}). \tag{2.12}$$

$$DR_{dB} = 10\log M + 6.02n + 1.76 \tag{2.13}$$

Though oversampling produces a significant increase in the SNR, only a modest improvement is realized that quickly reaches a limit due to the practical aspects of implementation. Oversampling improves the DR by only 3 dB for each doubling of M. Eqn. 2.13 shows that a 1-bit improvement in DR requires a 4X increase in M. A 4-bit improvement in DR requires a 256X increase in M. This exponential relationship quickly reaches a practical implementation limit due to the required sampling frequency. In addition, as the dynamic range is increased by increasing M, the linearity requirements of the quantizer must be equivalent to the overall dynamic range of the converter [158]. These complications make the improvement in dynamic range due to oversampling alone very limited and usually constrains M to 512 or less in most practical implementations.

2.3 Noise Shaping Modulators

Further improvement in the realizable dynamic range of a converter can be obtained using a feedback architecture to shape the quantization noise so that the majority of the quantization noise is moved outside the signal bandwidth. In this section, the transfer functions for a noise-shaping modulator are developed, and the effect of noise shaping on *DR* is demonstrated.

The basic transfer functions for the input signal and quantization noise of a feedback modulator are easily developed using the block diagram of a feedback system (see Fig. 2.5). Here the ADC (quantizer) is modeled as the gain, G, and additive quantization noise, $E_Q(z)$. The DAC is assumed to have the same resolution as the quantizer ADC, resulting in the addition of only implementation error, modeled as $E_D(z)$. A(z) and F(z) are discrete-time filters. For this analysis, $E_Q(z)$ and $E_D(z)$ are considered uncorrelated white noise sources. The feedback modulator is a linear, time-invariant system allowing superposition for analysis of the input signal transfer function $H_X(z)$, quantization noise transfer function $H_Q(z)$ and the DAC noise transfer function $H_D(z)$. These transfer functions are developed below.

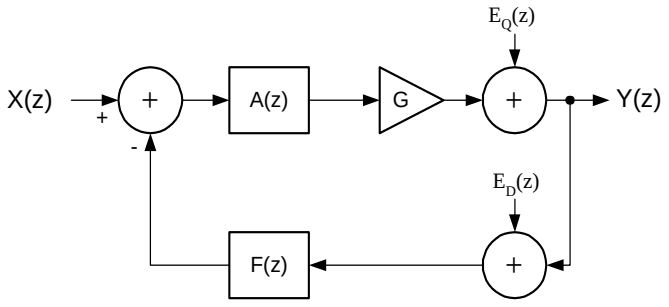


Figure 2.5 Basic feedback modulator block diagram.

$I_1(z)$ represents an intermediate node at the output of the A(z) filter block and can be defined as

$$I_1 = A(z)[X(z) - F(z)(Y(z) + E_D(z))] \ . \tag{2.14}$$

The output of the modulator becomes

$$Y(z) = (I_1 G + E_q(z)) \ . \tag{2.15}$$

Substituting [2.14] into [2.15] yields

$$Y(z) = GA(z)[X(z) - F(z)(Y(z) + E_D(z))] \tag{2.16}$$

and

$$Y(z) = X(z)\left[\frac{GA(z)}{1 + GA(z)F(z)}\right] + E_Q(z)\left[\frac{GA(z)F(z)}{1 + GA(z)F(z)}\right] + \left(-E_D(z)\left[\frac{1}{1 + GA(z)F(z)}\right]\right). \tag{2.17}$$

The individual transfer functions for the input signal, X(z), the quantization noise, $E_Q(z)$, and the DAC error, $E_D(z)$, respectively become:

$$H_X(z) = \frac{Y(z)}{X(z)} = \frac{GA(z)}{1 + GA(z)F(z)} \tag{2.18}$$

$$H_Q(z) = \frac{Y(z)}{E_Q(z)} = \frac{GA(z)F(z)}{1 + GA(z)F(z)} \tag{2.19}$$

$$H_D(z) = \frac{Y(z)}{E_D(z)} = \frac{1}{1 + GA(z)F(z)} \ . \tag{2.20}$$

For a 2^{nd}-order modulator, the desired response is

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_Q(z) - z^{-2}E_D(z) \ . \tag{2.21}$$

The desired response of the modulator is to pass the input signal and shape the quantization noise with a high-pass characteristic.

For simplification, the error associated with the DAC will be assumed zero, resulting in a modulator output in terms of the input, X(z), and the quantization noise, $E_Q(z)$:

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_Q(z) \ . \tag{2.22}$$

This requires the following solutions for $H_X(z)$ and $H_Q(z)$:

$$H_X(z) = z^{-2} \tag{2.23}$$

and

$$H_Q(z) = (1 - z^{-1})^2 \ . \tag{2.24}$$

For the general L^{th}-order modulator

$$H_X(z) = z^{-L} \tag{2.25}$$

and

$$H_Q(z) = (1 - z^{-1})^L \ . \tag{2.26}$$

To meet the required forms given by [2.25] and [2.26]

$$A(z) = \frac{z^{-L}}{(1 - z^{-1})^L} \tag{2.27}$$

and

$$F(z) = z^L[1 - (1 - z^{-1})^L] \ . \tag{2.28}$$

This assumes the gain G is unity, (unity-gain approximation). Thus the expression for A(z) is simply an L^{th}-order integrator with an L-sample delay term. F(z) must be manipulated further to obtain an easily realizable form. For example, when L=2, F(z) becomes $2z - 1$. Further manipulation produces

$$F(z) = 2z(1 - z^{-1}) + 1 \tag{2.29}$$

which is composed of two feedback terms as shown in Fig. 2.6.

Splitting A(z) into two, single order, delayed integrators allows feedback of the non-unity term between the integrators and simplifies the overall feedback function to a pair of feedback gains (see Fig. 2.7).

A generalized topology incorporating fixed gains at the inputs of the summing nodes is shown in Fig. 2.8 for the 2nd-order interpolative modulator. The associated z-domain output is given by

$$Y(z) = \frac{\left(\frac{g_1}{g_1'}\right)z^{-2}X(z) + (1-z^{-1})^2 E_{Q1}(z)}{1 + z^{-1}\left(\frac{g_2'}{g_1' g_2} - 2\right) + z^{-2}\left(2 - \frac{g_2'}{g_1' g_2}\right)} . \tag{2.30}$$

To obtain the desired modulator output given by [2.22] the following conditions must be met:

$$\frac{g_2'}{g_1' g_2} = 2, \quad \frac{g_1}{g_1'} = 1 . \tag{2.31}$$

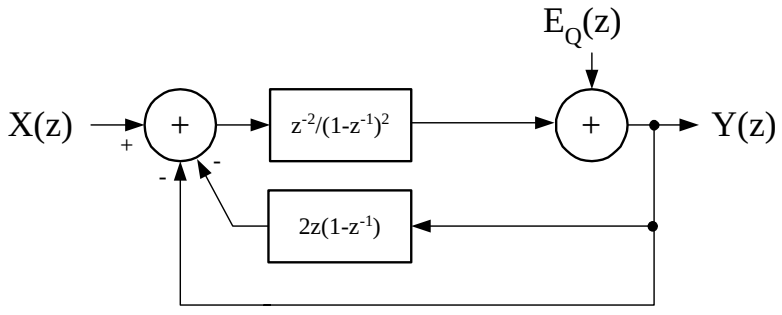


Figure 2.6 Feedback modulator architectural development (diagram 1).

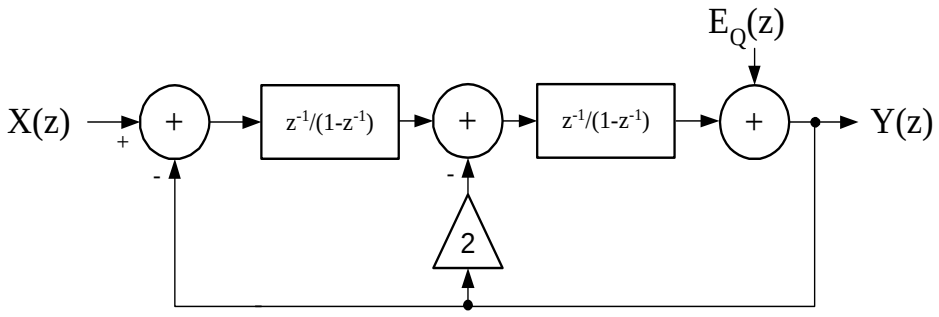


Figure 2.7 Feedback modulator architectural development (diagram 2).

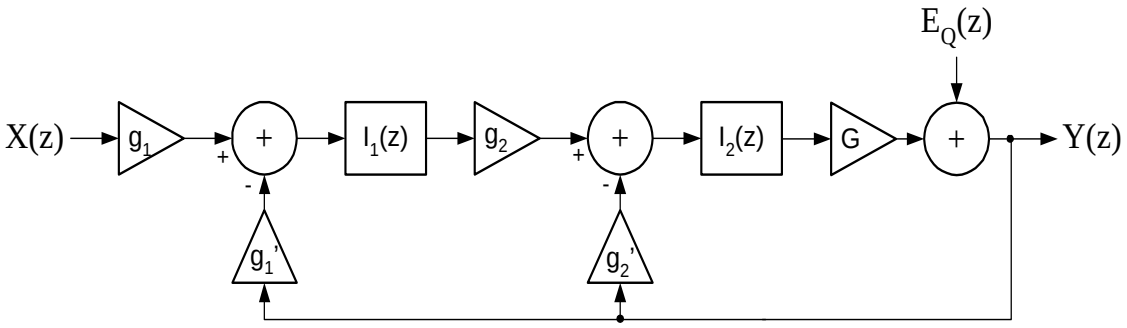


Figure 2.8 2nd-order interpolative modulator - general case.

Using the same development strategy, any order of modulator can be obtained by adding additional integrator stages and feedback paths to the interpolative architecture, resulting in the following z-domain output characteristic for an L[th]-order modulator:

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^{L}E_{Q}(z). \tag{2.32}$$

However, interpolative modulator architectures of order >= 3, are at best conditionally stable and must be implemented with caution. The following sections will address architectural selection and provide topology alternatives that allow high-order, stable, noise-shaping modulators.

The effect of noise shaping on the quantization noise is demonstrated in Fig. 2.9 and Fig. 2.10. In both graphs *f* actually represents the normalized frequency (f/f_s).

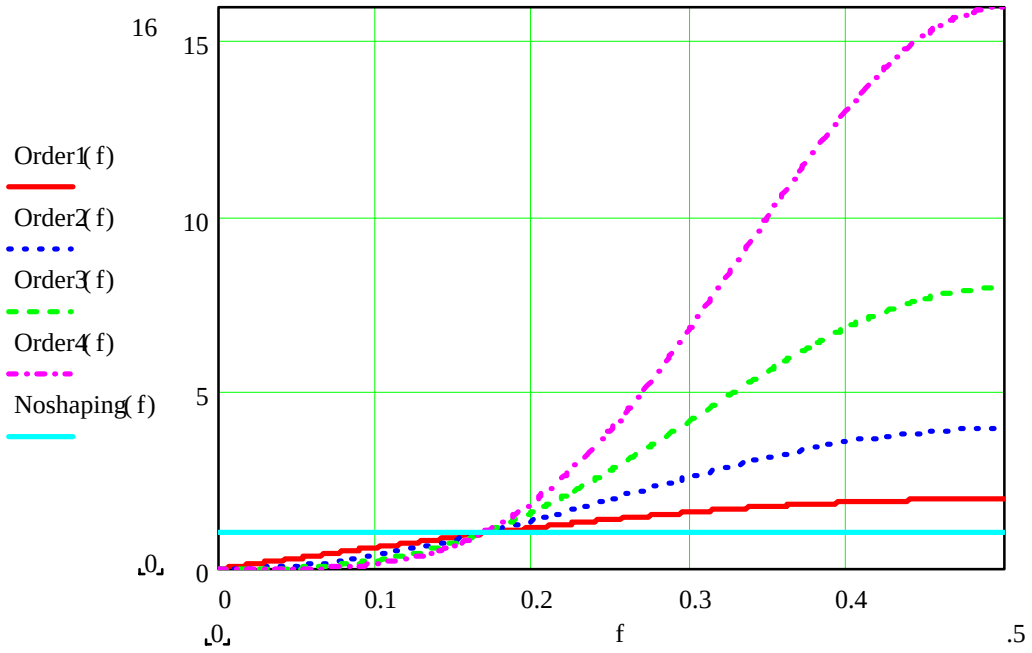


Figure 2.9 Noise shaping as a function of integrator order.

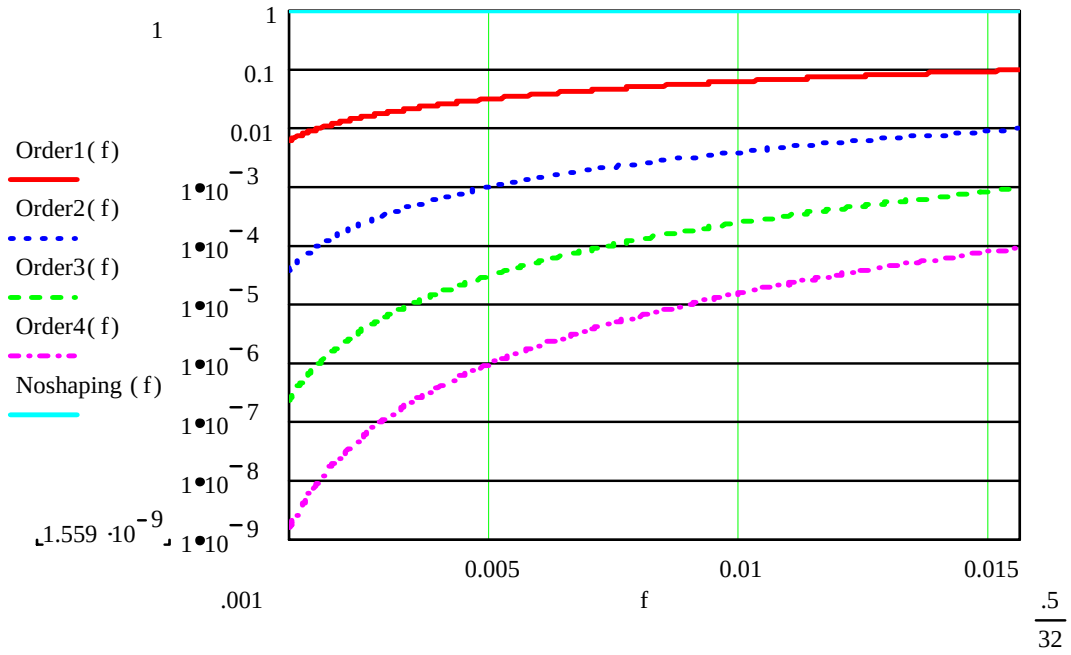


Figure 2.10 Noise shaping and integrator order (zoom view).

2.4 Multi-bit Quantizers

In addition to oversampling and noise shaping, increasing the internal quantizer resolution (n) can be used to further increase the achievable dynamic range of a ΣΔ modulator. If properly implemented, the incremental improvement in the obtainable resolution roughly tracks the increase in internal resolution. However, precise implementation of the multi-level error feedback DACs are essential to improve the performance and can significantly reduce the modulator performance if the design is not extremely linear [127]. This is the result of the DAC output being summed at the input of the loop.

2.5 Oversampling, Noise Shaping and Multi-Bit Quantization

Combining the effects of oversampling, noise shaping, and multi-bit quantization, ΣΔ modulators have been shown to provide significant increases in achievable dynamic range over Nyquist rate converters. The following expression provides the theoretically obtainable dynamic range for a ΣΔ modulator as a function of the oversampling ratio (M), noise shaping order (L), and internal quantizer resolution (n) [127]

$$DR = \frac{S_s}{S_q} = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(M^{2L+1})(2^n-1)^2. \tag{2.33}$$

Eqn. 2.33 can also be expressed in bits of resolution (B) as

$$B(bit) = \frac{1}{2}\log_2\left(\frac{(2^n-1)^2(2L+1)(M^{2L+1})}{\pi^{2L}}\right). \tag{2.34}$$

Note that these expressions can be used to calculate the theoretically obtainable resolution and do not account for practical implementation losses or the contribution of electronic noise sources which limit the achievable performance in modulator implementations. In Chapter 3 an overview of candidate modulator topologies is discussed and the associated advantages and disadvantages of the different architectures are summarized.

CHAPTER 3

SIGMA DELTA ADC ARCHITECTURES

Many different architectures have been developed for ΣΔ modulator implementation, each providing distinct advantages and disadvantages. Fig. 3.1 provides an overview of the most common modulator architectures and summarizes the primary advantages and disadvantages of each architectural family. In general, there are three primary degrees of freedom associated with the architectural selection for ΣΔ modulators: oversampling ratio (M), noise shaping order (L), and the modulator internal resolution (N), expressed in bits. Oversampling ratio is somewhat independent of the architecture. However, the noise shaping order (L) and the internal resolution (N) are intimately linked to the architecture. This section will provide an overview of the most common architectures and provide justifications for the topology targeted in this research.

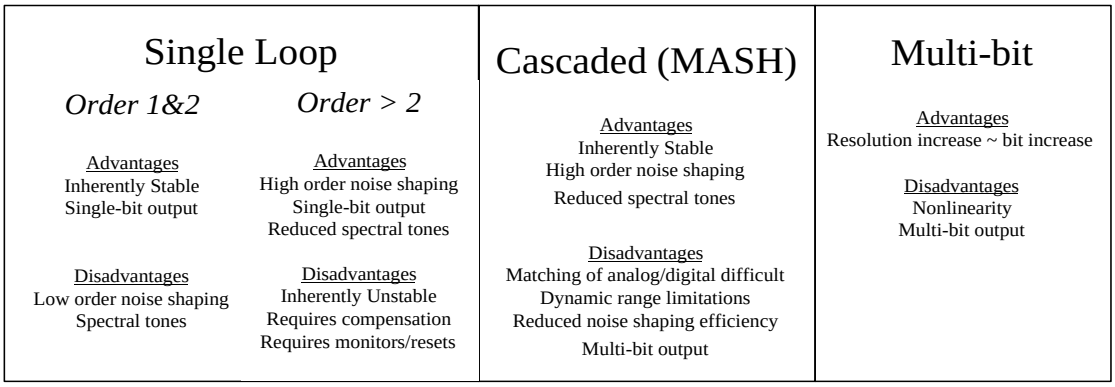


Figure 3.1 **ΣΔ modulator architectural comparison.**

3.1 Single Loop Modulators

ΣΔ modulators began with the most straight-forward architecture -- a single loop. When implemented as a loop of noise-shaping order 1 or 2, the configuration is unconditionally stable. Unconditional stability means a bounded input will produce a bounded output, regardless of initial conditions. However, low-order modulators ($L \leq 2$) provide very limited noise shaping and have been shown to produce undesired spectral tones that further reduce the obtainable effective resolution. For these reasons, higher-order loops ($L > 2$) have been developed that provide high-order noise shaping, reduce the spectral tones, and still provide a single-bit output. Minimum output data path width is desired to minimize the complexity and implementation size of the digital filter. However, single-loop topologies of order > 2 are only conditionally stable and require the addition of compensation and monitoring/reset functions to detect and provide control for recovering from an unstable state. The cascaded modulator or MASH (multi-stage noise-shaping) architecture provides a method to realize high-order modulators (>2) that are inherently stable [120]. However, this topology has several limiting characteristics including reduced input dynamic range, reduced noise-shaping order due to element mismatch, and multi-bit output. Of these, the dominant resolution-limiting characteristic is integrator gain mismatch. Precise integrator gain is required to minimize integrator leakage and to obtain high-order noise shaping functions. This requirement results from the fact that both analog and digital means are used to implement the noise-shaping function and therefore the gains must be matched very closely to obtain the desired result. Further resolution can be obtained in both single-loop and cascaded modulators by using a multi-bit comparator/DAC in the loop. This method, called multi-bit, provides a resolution increase that is approximately

equal to the increase in the internal resolution. However, multi-bit modulators have two primary disadvantages - increased modulator output data width and a high sensitivity to DAC non-linearity errors [127].

In addition to the configurations discussed in this section, a new topology called multi-rate has recently been the focus of much research and has specific applicability to high-rate data conversion associated with communications applications [32]. This topology is not particularly suitable for seismic applications since the architecture is intended to extend the dynamic range of high-bandwidth converters employing low oversampling ratios.

3.2 Cascaded Modulators

Cascaded architectures provide an alternative to interpolative structures for obtaining high-order stable noise-shaping functions. These topologies are composed of two or more cascaded interpolative or single-loop modulator stages. Each interpolative stage has a 1^{st}- or 2^{nd}-order noise-shaping function, therefore ensuring stable operation. The quantization noise from each stage is fed as the input into the following stage and each modulator output is filtered and a single output is produced as the sum of the filter outputs. Proper selection of the filter stages results in cancellation of the quantization noise of every stage but the last. The final stage quantization noise is shaped to the order of the overall modulator thus producing the desired noise-shaping order. The error cancellation filters are implemented as digital functions since the output of each of the modulator stages is a bit stream. However, as will be shown later, precise analog integrators are required to cancel the early stage quantization error and thus produce the desired overall noise shaping function.

The most simple cascaded architecture, a 1-1 cascade, is composed of 2 single-order loops (See Fig. 3.2). However, the 1-1 cascade is generally undesirable due to the low-order noise shaping efficiency, spectral tones, and increased sensitivity to gain mismatch. A more common topology that ideally provides a 4th-order noise shaping function is the 2-2 cascade shown in Fig. 3.3 [142]. The remainder of this section will develop the z-domain expressions for the 2-2 cascade modulator including the associated digital noise cancellation function.

For the 2-2 cascade modulator architecture, the output of the first 2nd-order modulator block is

$$Y_1(z) = \frac{\left(\frac{g_1}{g_1'}\right)z^{-2}X(z) + (1-z^{-1})^2 E_{Q1}(z)}{1 + z^{-1}\left(\frac{g_2'}{g_1' g_2} - 2\right) + z^{-2}\left(2 - \frac{g_2'}{g_1' g_2}\right)}. \tag{3.1}$$

Similarly, the output of the second modulator block is given by

$$Y_2(z) = \frac{\left(\frac{1}{g_3''}\right)z^{-2}X_2(z) + (1-z^{-1})^2 E_{Q2}(z)}{1 + z^{-1}\left(\frac{g_4'}{g_3'' g_4} - 2\right) + z^{-2}\left(2 - \frac{g_4'}{g_3'' g_4}\right)} \tag{3.2}$$

where

$$X_2(z) = Y_1(z)(g_3 - g_3') - g_3 E_{Q1}(z)\ . \tag{3.3}$$

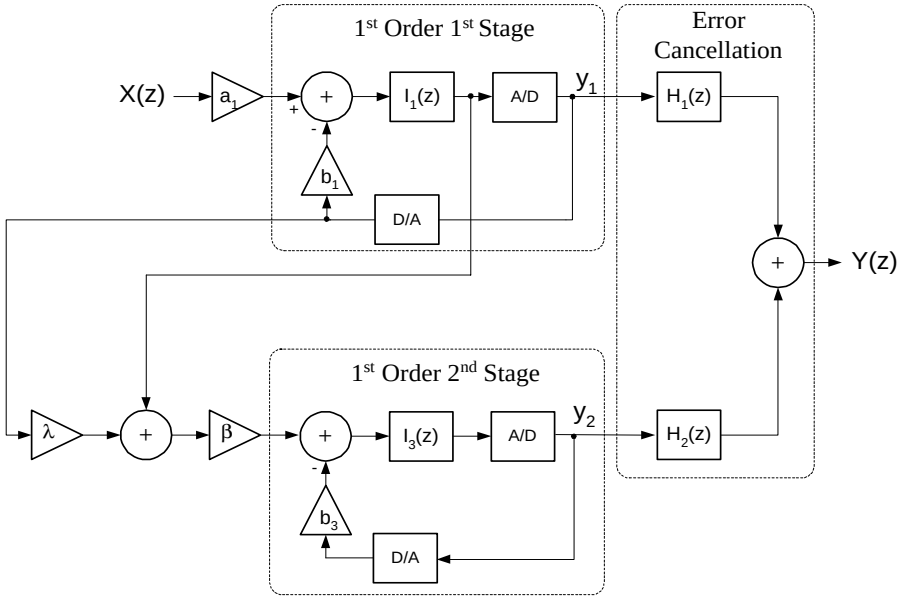


Figure 3.2 1-1 cascade modulator architecture.

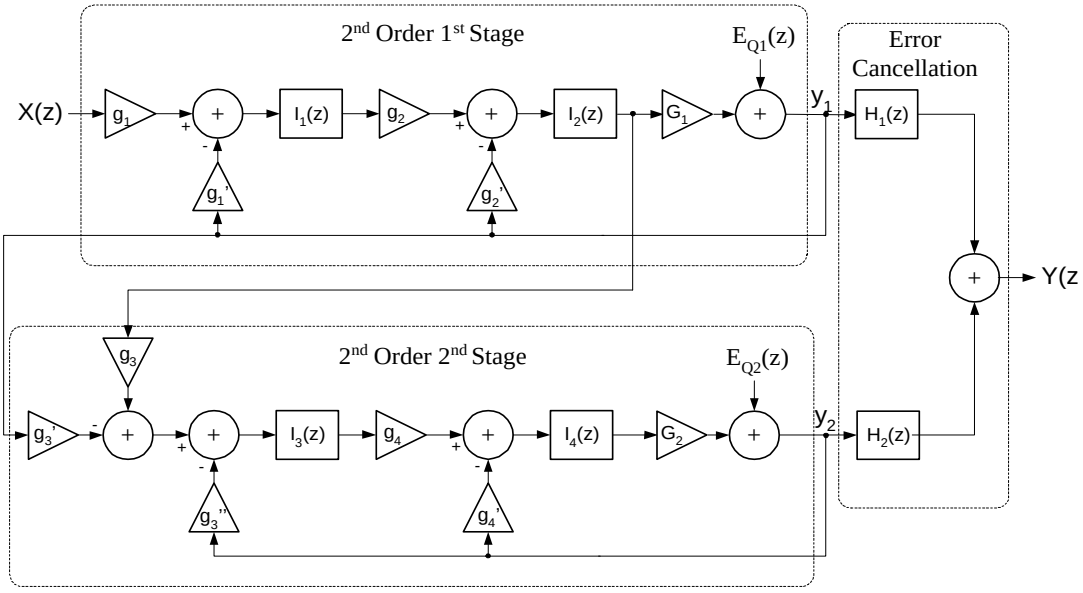


Figure 3.3 2-2 cascade modulator architecture.

Assuming the relationships

$$g_2' = 2g_1'g_2 \ , \tag{3.4}$$

and

$$g_1 = g_1', \tag{3.5}$$

the expression for $Y_1(z)$ reduces to the ideal function for a 2nd-order modulator given as

$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_{Q1}(z) \ . \tag{3.6}$$

Likewise, if

$$g_4' = 2g_3''g_4 \tag{3.7}$$

and

$$g_1 = g_1', \tag{3.8}$$

then the transfer function for $Y_2(z)$ reduces to

$$Y_2(z) = \left(\frac{1}{g_3''}\right) z^{-2}X_2(z) + (1 - z^{-1})^2 E_{Q2}(z) \ . \tag{3.9}$$

The output of these two modulator loops are processed to produce the desired output function for the 4th-order modulator:

$$Y(z) = z^{-4}X(z) + \beta(1 - z^{-1})^4 E_{Q1}(z) . \tag{3.10}$$

Here β is a scaling parameter defined by the fixed integrator gains:

$$\beta = \frac{g_3''}{g_1 g_2 g_3} . \tag{3.11}$$

3.3 Digital Noise Cancellation

As previously described, the second loop of the 2-2 cascade is used to shape the quantization noise of the first loop. The outputs of both 2nd-order loops, $Y_1(z)$ and $Y_2(z)$, are input to the digital noise cancellation block that ideally produces the desired result -- an output signal composed only of a delayed version of the input signal and the 4th-order shaped quantization noise of the second loop (see Eqn. 3.10). The output of the noise cancellation block is given by

$$Y(z) = Y_1(z)H_1(z) + Y_2(z)H_2(z) \ . \tag{3.12}$$

Substituting the desired form of the output for $H_2(z)$, solving for $H_1(z)$, and rearranging into a different form to minimize function implementation results in the topology of Fig. 3.4 where

$$H_{N1}(z) = z^{-2} \tag{3.13}$$

and

$$H_{N2}(z) = (1 - z^{-1})^{-2}. \tag{3.14}$$

Fig. 3.4 shows the basic block diagram of the noise cancellation circuitry. The constants d_0 and d_1 are defined using the integrator gain values:

$$d_0 = 1 - \frac{g_3'}{(g_1 g_2 g_3)}, \tag{3.15}$$

and

$$d_1 = \frac{g_3''}{g_1 g_2 g_3}. \tag{3.16}$$

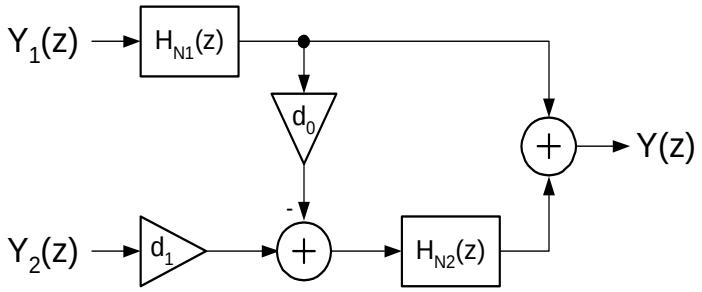


Figure 3.4 Digital noise cancellation for 2-2 cascade architecture.

A more detailed diagram showing specifics of the functions and required bit widths is found in Fig. 3.5. Note that all mathematical operations are performed using 2's complement arithmetic. The sign bit is not included in the bit widths shown in Fig. 3.5.

Using the classical gain weights produces a slightly reduced overall dynamic range under ideal conditions, but shows improved dynamic range in the presence of integrator gain mismatch [127]. In addition, the classical gain weights produce a reduced-complexity modulator implementation. Using the classical gain weights given by Boser [13] ($g_3' = 0$, and $g_1 = g_1' = g_2 = g_2' = g_3 = g_3'' = g_4 = g_4' = 0.5$) results in d_0=1 and d_1=4.

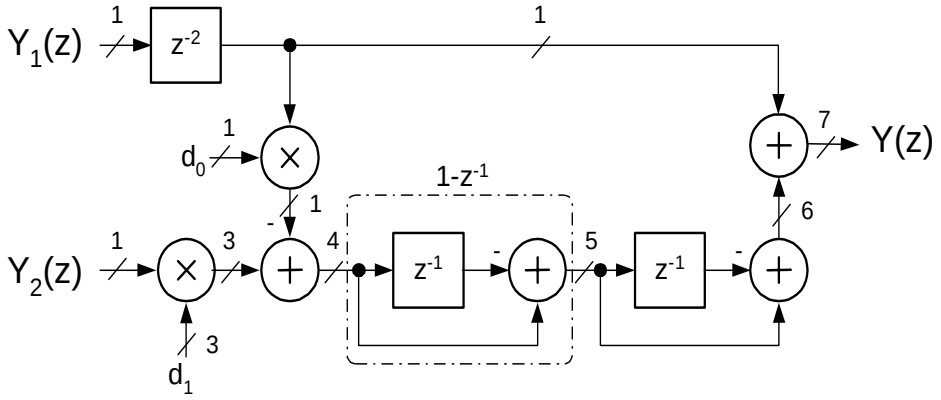


Figure 3.5 Digital noise cancellation diagram (data widths shown for d_0=1 and d_1=4).

CHAPTER 4

REVIEW OF THE LITERATURE

The application of ΣΔ modulation techniques to high-resolution data conversion is perhaps the single most investigated topic in integrated circuit design literature over the past decade. The method is well understood, and a mass of literature has been devoted to topology variations, sources of error, sensitivity analyses, performance simulation, target fabrication technology (CMOS, BiCMOS, Bipolar, SOS, SOI), circuit implementation specifics, and to numerous applications examples from low-speed, high-resolution instrumentation associated with seismic and medical applications [2,88,110], to moderate-resolution, high-speed communications applications [17,91,183,187,193]. In this section an attempt is made to summarize this vast wealth of work, with a particular emphasis on addressing the application of this research - high-resolution, high-temperature data converters for seismic imaging.

A compilation of representative work in the area of sigma delta modulation techniques from 1988 - 2001 is shown in Tables 4.1 and 4.2. Each table is devoted to a class of modulator architectures and provides parameters needed to perform useful comparisons: measured resolution, digital output rate (DOR), measured power consumption, fabrication process, supply voltage, oversampling ratio (OSR), and internal resolution. Table 4.1 summarizes the published single loop architectures while Table 4.2 details the cascaded architectures. Though this research is associated only with switched capacitor implemen-

Table 4.1: Published single-loop ΣΔ modulators from 1988-2001 ([1]estimated power).

Reference	Res. (bits)	DOR (S/s)	Power (mW)	Process	Supply (V)	Architecture	OSR	Int. Res. (bits)	FOM-w	FOM-v	FOM-t
Boser88	14.5	11700	12	3µm CMOS	5	2nd-order	256	1	44.26	16.60	199.19
Nors89	14.4	80000	75	1.75µm CMOS	5	2nd-order	128	1	43.36	2.60	195.14
DelSig90	20.1	1000	125	3µm CMOS	—	4th-order	256	1	111.23	—	—
Brandt91a	16	50000	13.8	1µm CMOS	5	2nd-order	256	1	4.21	1.37	18.95
Eynde91	14	500000	160	1.5µm CMOS	5	4th-order	64	1	19.53	0.55	87.89
Riton91	16.7	48000	200	2µm CMOS	5	5th-order	64	1	39.14	0.88	176.12
Bert93	21	10	6	2µm CMOS	5	1st-order + PWM	—	—	286.10	214.58	1287.46
Kert94	20	800	50	3µm CMOS	10	4th-order	320	1	59.60	11.32	566.24
Mats94	9.3	384000	1.56	0.5µm CMOS	1	RC, swing supp	—	2-bit	6.44	2.07	3.22
Nadeem94	13.7	2000	0.94	2µm CMOS	5	3rd-order	250	1	35.32	169.07	158.93
Thom94	20	984	45	2µm CMOS	10	5th-order		3-level	43.61	9.21	414.32
Yam94	17.1	160	1.1	1.2µm CMOS	5	4th-order	205	1	48.94	200.21	220.23
Chen95	15.7	40000	67.5	1.2µm CMOS	5	2nd-order	64	3-bit	31.70	2.11	142.65
Mino95	11	200000	94	0.8µm CMOS	3	7th-order	—	—	229.49	6.10	573.73
Saue95	12	32000	1	1.5µm CMOS	2.3	3rd-order	16	1	7.63	13.73	13.73
Tan95a	10	19200	2	0.8µm CMOS	3.3	2nd-order, SI	128	1	101.73	142.42	284.83
Tan95b	10	15625	0.78	0.8µm CMOS	1.2	2nd-order, SI	64	1	48.75	43.75	34.13
Baird96	13.7	500000	58	1.2µm CMOS	5	4th-order	16	4-bit	8.72	0.68	39.22
Gril96	15.3	7000	2	0.6µm CMOS	1.8	2nd-order	285	1	7.08	4.60	9.21
Zwan96	13	8000	0.2	0.5µm CMOS	2.2	4th-order, cont. loop filt.	64	1	3.05	25.94	5.19
Au97	11.8	16000	0.34	1.2µm CMOS	1.95	3rd-order, local feedback	64	1	5.96	25.42	8.64
Leun97[1]	19.6	44000	760	0.8µm CMOS	5	7th-order	140	3-level	21.74	0.13	97.81
Medeiro97a	16	20000	5.5	1.2µm CMOS	5	2nd-order	256	1	4.20	3.43	18.88
Medeiro97d	17.1	4800	1.71	0.7µm CMOS	5	2nd-order	512	1	2.54	6.67	11.41
Nys97	19	800	1.32	2µm CMOS	5	2nd-order	512	9-level	3.15	10.73	14.16
Peluso97	12	6800	0.1	0.7µm CMOS	1.5	2nd-order	74	1	3.59	35.90	3.59
Send97	14.3	20000	0.55	0.5µm CMOS	1.5	2nd-order, double sampling	50	1	1.36	2.48	1.36
Thanh97	13.4	195000	25.9	1.2µm CMOS	5	2nd-order	128	1	12.29	2.13	55.29
Zwan97	15.7	40000	2.3	0.8µm CMOS	3.3	4th-order, gm-C	—	—	0.62	0.76	1.74
Burger98	14	200000	2.8	0.5µm CMOS	3	3rd-order	48	1	0.85	0.76	2.14
Falak98	13.8	10000000	75	0.5µm CMOS	2.5	4th-order	12	6-bit	0.53	0.01	1.05
Ma98	14	14000	0.425	0.6µm CMOS	1	2nd-order	143	1	1.85	2.18	0.93
Marques98	14.8	2000000	230	1µm CMOS	5	4th-order	24	1	4.03	0.08	18.14
Peluso98	12.5	32000	0.04	0.5µm CMOS	0.9	3rd-order	48	1	0.22	2.16	0.09
Yasuda98	12.8	200000	9.6	0.6µm CMOS	2.7	3rd-order, dyn. el. match.	25	9-level	6.73	1.54	14.81
Coban99	16	40000	1	0.5µm CMOS	1.5	4th-order	64	1	0.38	0.38	0.38
Lin99	10.5	5000000	12	1.2µm CMOS	3	2nd-order, cont. time	16	1	1.66	0.35	4.14
Dess00	14.3	50000	1	0.35µm CMOS	1	3rd-order	100	1	0.99	0.50	0.50
Geerts00a	15.8	2500000	152	0.65µm CMOS	5	3rd-order	24	4-bit	1.07	0.03	4.80
Geerts00b	11.5	12500000	152	0.65µm CMOS	5	3rd-order	8	4-bit	4.20	0.12	18.89
Maulik00	15.3	500000	210	0.6µm CMOS	5	5th-order	64	1	10.41	0.22	46.85
Nagari00	11.7	270000	4	0.5µm CMOS	2.7	2nd-order, double sampling	48	1	4.45	2.45	9.80
Naik00	21.6	2000	21	0.6µm CMOS	3	4th-order	512	1	3.30	0.39	8.26
Thom00	18.3	240	41	—	5	4th-order	—	—	529.33	58.10	2381.97
Dess01	14.3	50000	0.95	0.35µm CMOS	1	3rd-order	100	1	0.94	0.50	0.47
Fogle01	16.7	48000	70.4	0.5µm CMOS	3.3	2nd-order	64	33-level	13.78	0.55	38.57
Li01	12.2	6800	0.038	0.35µm CMOS	1.2	2nd-order, sig. adapt cntrl.	64	1	1.19	21.88	0.83
Snoeij01	16.7	22000	1.5	0.5µm CMOS	2.5	4th-order	64	1	0.64	0.85	1.28

Table 4.2: Published cascade ΣΔ modulators from 1988-2001 ([1]estimated power).

Reference	Res. (bits)	DOR (S/s)	Power (mW)	Process	Supply (V)	Architecture	OSR	Int. Res. (bits)	FOM-w	FOM-v	FOM-t
Longo88	13	160000	20	1.5µm CMOS	5	2-1 Cascade	16	1	15.26	3.43	68.66
Brandt91b	12	2100000	41	1µm CMOS	5	2-1mb Cascade	24	1-3b	4.77	0.52	21.45
Yin93	15.7	320000	65	1.2µm CMOS	5	2-1 Cascade	64	1	3.82	0.26	17.17
Dedi94	14.7	200000	40	1.2µm CMOS	5	2-2-2mb Cascade	16	3-level	7.51	0.85	33.81
Will94	17	50000	47	1µm CMOS	5	2-1 Cascade	128	1	7.17	0.69	32.27
Yin94	16.5	1500000	180	2µm BiCMOS	5	2-1-1 Cascade	32	1	1.29	0.03	5.83
Chang95[1]	12	1540000	250	0.7µm CMOS	5	2-1-1 Cascade	32	1	39.63	0.71	178.35
Rabii96	15	50000	5.4	1.2µm CMOS	1.8	2-1 Cascade	80	1	3.30	0.79	4.28
Medeiro97b	16.7	40000	10	1.2µm CMOS	5	2-2 Cascade	128	1	2.35	1.06	10.57
Medeiro97c	12.9	2200000	55	0.7µm CMOS	5	2-1-1mb Cascade	16	1-1-3b	3.27	0.27	14.72
Fuji97	18.2	48000	500	0.7µm CMOS	5	2-2mb Cascade	128	3-level	34.59	0.31	155.67
Rabii97	16.1	50000	2.5	0.8µm CMOS	1.8	2-1 Cascade	80	1	0.71	0.37	0.93
Feld98	12.5	1400000	81	0.72µm CMOS	3.3	2-2-2mb Cascade	16	1-1-3level	9.99	0.35	27.97
San98	15.3	64000	79	2µm CMOS	6.6	2-1-1-2 Cascade	16	1	30.60	2.36	186.65
Medeiro99	12.9	2200000	55	0.7µm CMOS	5	2-1-1mb Cascade	16	1-1-3b	3.27	0.27	14.72
Fuji00	16	2500000	165	0.5µm CMOS	5	2-1-1mb Cascade	8	4b-4b-4b	1.01	0.03	4.53
Gomez00	16.6	44100	13	0.6µm CMOS	3	2-1 Cascade	128	1	2.97	0.57	7.42
Moriz00a	12	2200000	109	0.35µm CMOS	3.3	2-2mb Cascade	24	1-5b	12.10	0.31	33.87
Moriz00b	13	2200000	165	0.35µm CMOS	3.3	2-2-2 Cascade	24	1-1-1	9.16	0.16	25.63
Oli01	13.7	360000	5	0.35µm CMOS	1.8	2-2 Cascade	36	1	1.04	0.27	1.36
Vleugels01	15.5	4000000	150	0.5µm CMOS	2.5	2-2-1mb Cascade	16	5b-3b-3b	0.81	0.01	1.62
Wang01	18.5	25000	75	0.6µm CMOS	5	2-2 Cascade	64	1	8.67	0.52	39.03

tations, publications using other methods including switched current (SI) and continuous time (cont. time) are presented for completeness.

Performance comparisons of ΣΔ modulators can be made using a figure of merit (FOM) that incorporates the three primary metrics of modulator performance: power consumption, effective resolution, and digital output rate (DOR). A common form given by Mediero97 [129] is

$$FOM - w = \frac{Power(W)}{2^{resolution(bit)} \times DOR(S/s)} \cdot 10^{12}. \qquad (4.1)$$

However, many applications exist where other performance parameters are of interest such as supply voltage. An alternative FOM (FOM-v) has been defined for this research to emphasize supply voltage efficiency, resolution, and DOR, and is given as:

$$FOM-v = \frac{Vsupply - 0.5}{2^{resolution(bit)} \times DOR(S/s)} \cdot 10^9 \tag{4.2}$$

The numerator of FOM-v represents the useful dynamic range of the actual circuit implementation. Thus, a 0.5 volt factor is subtracted to account for circuit dynamic range limitations in implementation associated with input stage current sources and output stage voltage swing limitations. An alternative form that includes all of the parameters of both FOM-w and FOM-v into account is shown below:

$$FOM-t = \frac{(Vsupply - 0.5) \times Power(W)}{2^{resolution(bit)} \times DOR(S/s)} \cdot 10^9 \tag{4.3}$$

In Tables 4.1 & 4.2, all three forms of the FOM are provided for comparison and demonstrate similar performance for both single-loop and cascaded architectures. Note that for all FOMs, a lower value indicates improved performance relative to the metrics considered. In terms of FOM-w, Peluso [152] produces the lowest value using a 3rd-order single-loop architecture operating with a 0.9V supply. Ignoring power consumption and considering supply efficiency, both Falakshahi [53] and Vleugels [196] produce a FOM-v of 0.01, using a 4th-order single-loop and a 5th-order cascaded architecture, respectively. Incorporating all metrics, including power and supply efficiency (FOM-t), Peluso [152] produces the best FOM result at 0.09. The extremely low-power consumption achieved in this design differentiates it from most published designs.

Further comparisons of the published designs of Table 4.1 and Table 4.2 are shown in Fig. 4.1 and Fig. 4.2. Fig. 4.1 shows the resolution-speed plane for both single-loop and cascaded architectures. Obviously, single-loop architectures have been published for a wide range of resolutions and speeds, and have shown the overall highest effective resolution. Conversely, cascaded architectures are more tightly clustered and show on average better performance for high DOR, moderate-resolution applications.

Fig. 4.2 shows the published work of Table 4.1 and Table 4.2 placed in the power-speed plane. Here the single loop architectures span the broadest area and produce the lowest power designs. In general, the cascaded architectures provide the highest DOR performance with similar power consumption to the single-loop designs. A more detailed discussion of both the single-loop and cascaded architectures and associated attributes is provided in following sections.

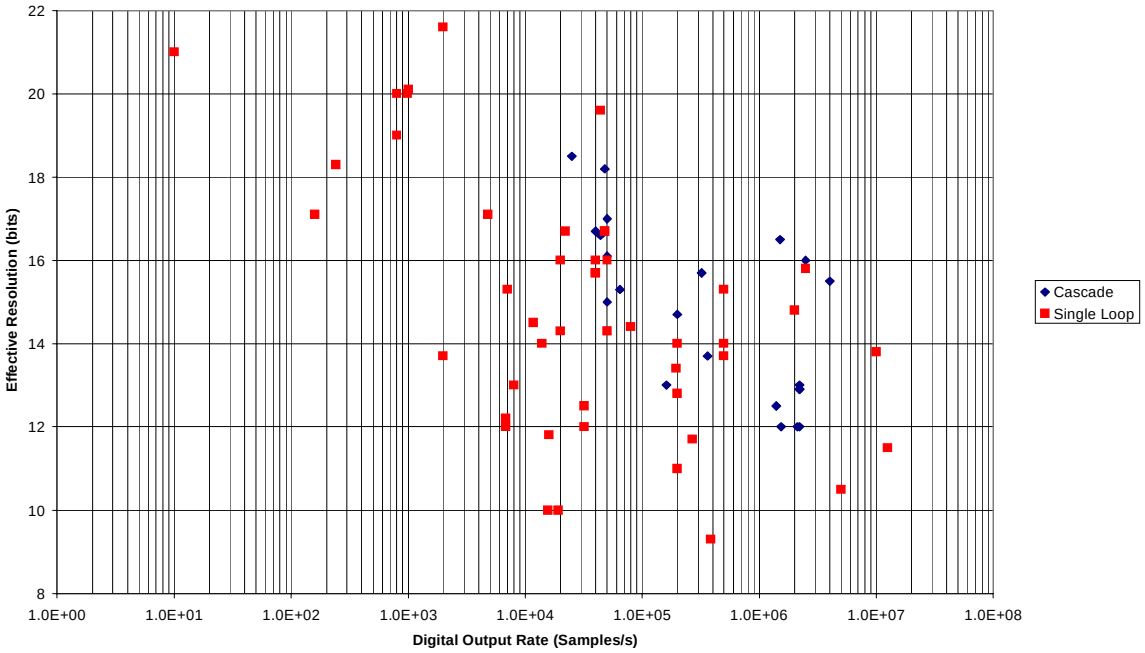


Figure 4.1 Resolution vs. speed (published modulators 1988-2001).

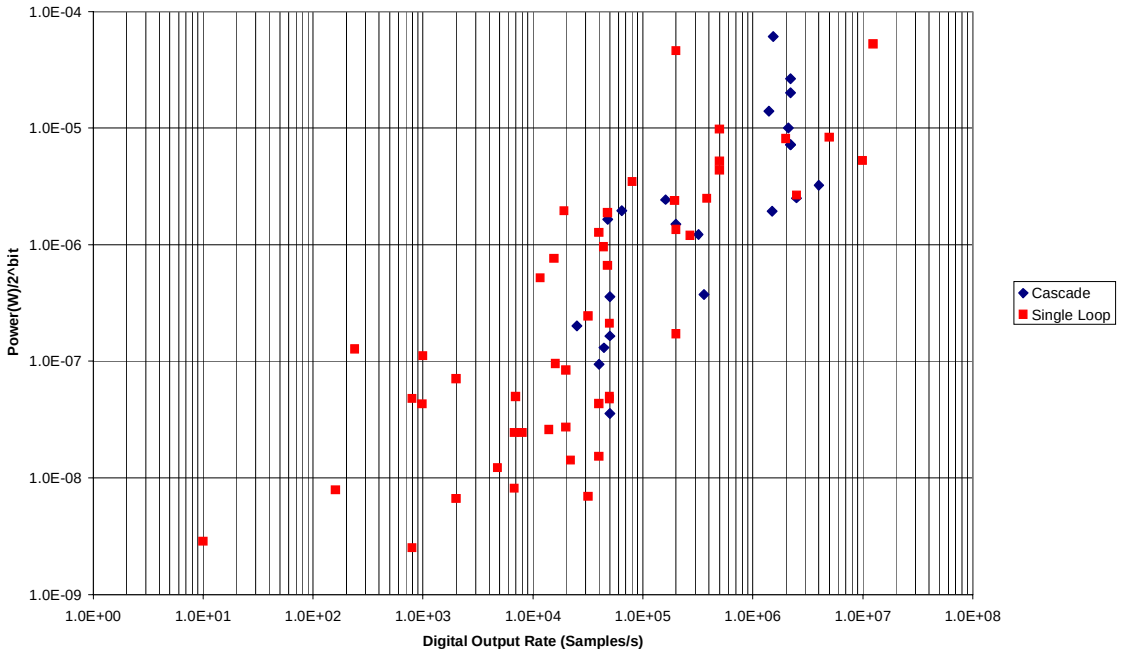


Figure 4.2 Power efficiency vs. speed (published modulators 1988-2001).

In addition to the BiCMOS and CMOS designs reported in research literature, a number of designs have been published using alternative implementation techniques and alternative target processes such as InGaP/InGaAs HEMT [148], SiGe HBT [74], and superconducting fabrication methods [66,167,171] with sampling frequencies as high as 30 GHz. These designs, however, are directed towards very high-speed conversion and therefore offer poor resolution.

The most promising fabrication technologies suitable for general high-temperature implementation are Silicon-on-Insulator (SOI) and Silicon-on-Sapphire (SOS) [39,60,61,64,65,67,76]. Only a few publications reporting the use of SOI/SOS for modulator implementation exist, targeting three specific application areas: high-temperature [198,199], low-voltage low-power [181], and radiation tolerant data converters [45]. Viviani [198,199] reports 1st- and 2nd-order modulator designs, respectively, in fully-depleted

Table 4.3: Published SOS/SOI ΣΔ modulators from 1988-2001. (*indicates peak SNR).

Reference	T (C)	Resolution (bits)	DOR (S/s)	Power (mW)	Process / Supply	Architecture	OSR	Internal Resolution
Viviani96	27	9.3*	781	0.06	3μm SOI-CMOS / 2V	1st order	128	1-bit
	350	4.7*	3906	0.5	3μm SOI-CMOS / 2V	1st order	128	1-bit
Viviani99	30	11	15625	---	SOI-CMOS / 5V	2nd order	64	1-bit
	250	10	15625	---	SOI-CMOS / 5V	2nd order	64	1-bit
	300	9	15625	---	SOI-CMOS / 5V	2nd order	64	1-bit
Swaminathan99	27	8*	400000	0.3	0.25μm SOI-CMOS / 1V	2nd order	125	1-bit
Edwards99	27	9.7	126000	---	1.5μm SOS-CMOS / 5V	1st order	128	4-bit

SOI CMOS with measurement results up to 350°C. [199] provides the most promising data in terms of high-temperature performance reporting 9-bit resolution at 300°C using a 2^{nd}-order modulator. The specifics of these designs are shown in Table 4.3. These references show progress regarding the implementation of sigma delta structures in SOI/SOS processes, but implement only low-order, low-resolution modulator designs.

As demonstrated, the area of ΣΔ modulation continues to be a popular research topic, with most current research being directed towards high-speed moderate-resolution designs suitable for RF system application. The majority of the published work uses standard CMOS fabrication technologies following the electronic industry's move to smaller feature size, lower supply voltage processes. This work continues to progress and has shown impressive improvement for standard temperature applications. A small number of SOI or SOS designs have been published using low-order modulator architectures to obtain low-resolution results for both high-temperature and high-radiation environment applications. In addition, much work has been reported showing applicability of SOI/SOS to low-voltage low-power applications. The goal of this research is to address this missing component of high-temperature converters by demonstrating the first high-resolution, high-temperature modulator suitable for extreme environment applications. Successful demon-

stration of this design will extend the application of sigma delta modulation techniques to a variety of applications currently inaccessible to conventional designs.

Recent published literature in the area of high-temperature data conversion has demonstrated potential application of ΣΔ architectures to the specialized field of high-resolution seismic imaging. The use of silicon-on-sapphire (SOS) and silicon-on-insulator (SOI) processes are commonly employed to elevated temperature applications for reasons previously discussed. However, all reported topologies designed and tested for high-temperature application to date have been single-loop architectures of order 2 or less. These reported developments produce at best 11 bits of resolution at typical seismic temperatures (160°C) falling way short of the resolution needed for the demanding dynamic range requirements of seismic imaging (16-24 bits). Clearly, the research community has not adequately addressed the problem of high-resolution data conversion at elevated temperatures. The primary objective of this research is to demonstrate the first high-resolution ΣΔ modulator capable of 16-18 bit performance at elevated temperatures exceeding 160°C.

As a result of this research several specific contributions to the area of sigma delta modulator design for high temperature applications are evident. First, this work reports the first 4^{th}-order modulator in an SOS or SOI process and provides the first comparison of 2^{nd}- and 4^{th}-order cascaded modulators in a high-temperature process. Additionally, this work presents a thorough description of the modulator test system providing detail on the associated hardware, software, and general testing approach. Finally, this research presents a comprehensive and well organized suite of modulator test results as a function of temperature - a more complete presentation of data than previously detailed in literature.

CHAPTER 5

MODULATOR DESIGN & SIMULATION

This chapter presents a thorough summary of the design of the modulator. The demanding temperature requirements of the target application emphasize the need for special attention in the selection of the modulator design parameters. Many of the design decisions that are acceptable for room temperature designs do not apply in the case of down-hole seismic. Consequently, many conservative decisions are outlined in the following text that ensure stable operation over a wide temperature range, at the cost of reduced room temperature performance.

5.1 Modulator Architectural Selection

As previously mentioned, the two primary design requirements for down-hole seismic digitizers are maximum dynamic range and stability over a wide range of temperatures. Though high-order single-loop modulators with multi-bit internal resolution are capable of the best performance in terms of dynamic range (or effective resolution), there are many opportunities for problems associated with component temperature dependencies. Electronics placed down-hole are not only subjected to extremely high temperatures, but also experience wide swings in temperature, especially during deployment. Additionally, the static operating temperature each of the data collection nodes is subjected to depends largely on geothermal gradients, such that the nodes at either end of the string experience large environmental temperature differences. For these reasons, the cascaded architecture

was selected since unconditional stability is ensured by this topology. Though single-loop high-order modulators ($L \geq 2$) offer some advantages, they are at best conditionally stable when appropriate compensation is incorporated. In addition to simplified compensation, cascaded architectures do not require the integrator initialization and monitoring functions that are required in the high-order single-loop topologies to ensure stability. A properly designed cascaded modulator can provide increased robustness over high-order single-loop architectures, particularly over a wide temperature range, at the acceptable cost of slightly reduced resolution.

Regardless of the loop architecture, the design of the any modulator begins by selection of the three primary design parameters: noise shaping order (L), oversampling ratio (M) and internal resolution (N). Preliminary performance modeling of a modulator as a function of L, M, and N was performed using MATLAB [119] using Eqn. 5.1 and Eqn. 5.2, repeated below for convenience. Fig. 5.1 shows the theoretical resolution for realizable values of L and M with N=1. Table 5.1 summarizes the maximum achievable resolution from selected points on these curves.

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(M^{2L+1})(2^n-1)^2 \tag{5.1}$$

$$B(bit) = \frac{1}{2}\log_2\left(\frac{(2^n-1)^2(2L+1)(M^{2L+1})}{\pi^{2L}}\right) \tag{5.2}$$

The performance goal of this design is to match the 24-bit intrinsic resolution specification published for commercial seismic-grade ΣΔ converters. Theoretically, meeting this goal requires the use of a 3rd-order modulator with M=256. Use of this oversampling ratio

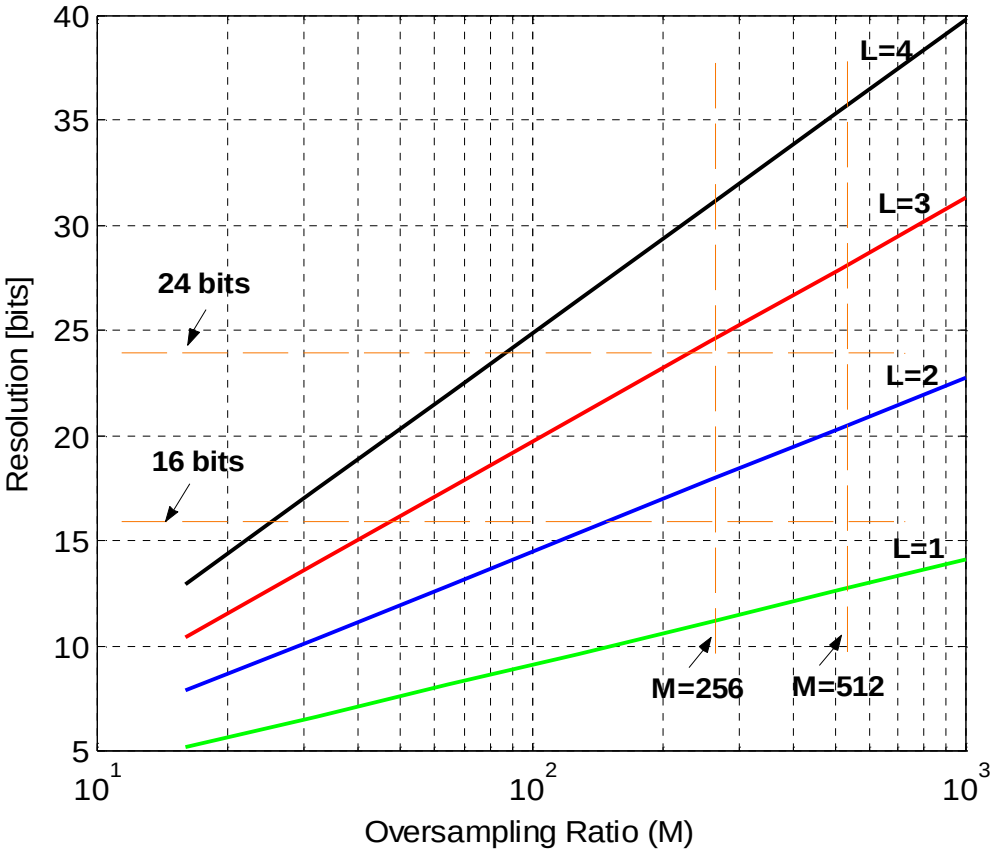


Figure 5.1 Theoretical modulator resolution vs. L and M for N=1.

Table 5.1: Theoretical resolution as a function of M and L (N=1).

Modulator Order	M=64	M=128	M=256	M=512
1	8.14	9.64	11.14	12.64
2	12.86	15.36	17.86	20.36
3	17.45	20.95	24.45	27.95
4	21.98	26.48	30.98	35.48
5	26.47	31.97	37.47	42.97

provides a significant improvement in SNR due to oversampling, while allowing a reasonable settling time for the target sampling frequency of 512 kHz. Note that the calculations used to predict the required L and M are ideal -- the errors associated with an imperfect noise shaping transfer function, input-referred electronic noise, and distortion are omitted. In practice these factors, unaccounted for in these calculations, will ultimately limit the effective resolution of the converter. These sources of error are addressed in later sections of this chapter.

The internal resolution of the modulator (N) was chosen to be 1 bit. Increasing the internal resolution of the modulator from 1 bit using multi-level quantization and error feedback produces roughly the same increase in modulator resolution. However, very precise implementation of the multi-level quantizer and feedback DACs is required or the effective resolution may actually be reduced. For example, in a 2-2 cascade with 3-bit quantization, a non-linearity of 1mLSB causes a 25% reduction in SNR [127]. This is the result of the DAC output being summed at the input of the loop. Due to the difficulty of achieving high linearity over a wide temperature range, a multi-bit architecture was not used in this design, but may be considered for future work. The use of 1-bit quantization ensures linearity.

A 2-2 cascade architecture was chosen for the realization of the modulator due primarily to its inherent unconditional stability. Though there are some slight performance penalties for using a cascaded modulator, the issue of stability over a wide-temperature range is of paramount importance. The primary disadvantages include sensitivity to mismatch of analog and digital gain coefficients, dynamic range penalties, and increased output bit width. For actual implementation, a 4^{th}-order noise shaping transfer function was chosen

for several reasons. First, the quantization noise spectral density is not actually uniform so the SNR calculations performed are optimistic [81,159]. Using a 4^{th}-order modulator will further shape the quantization noise to better suppress the expected spectral tones. In addition, a 2-2 cascade requires nearly the same design and ASIC layout effort as a 2-1 cascade since many of the individual circuit blocks are identical - a similar 2^{nd}-order loop can be used for both loops in the cascade. A 2^{nd}-order first stage was chosen since the literature suggests that a 2^{nd}-order first stage produces a more robust system than a 1^{st}-order first stage [163]. The primary disadvantage of this approach (choosing a 2-2 cascade over a 2-1 cascade) is the increased output data stream bit width from the modulator which increases the complexity and size of the digital filter [142].

Having selected a modulator topology and associated parameters L, M, and N, the integrator gains need to be determined. The integrator gain selection issue can be rather complex because closed form modeling of higher-order modulators is extremely difficult. As a result, the majority of published literature uses simulation or empirical means for gain determination [127,207]. Considering the design complexity issues and sensitivity to gain mismatch errors, the classical gain selection presented by Boser provides the best overall solution for this design [13]. This selection of gains has been shown to minimize the design complexity of the modulator, and provide decreased sensitivity to gain mismatch errors compared to gain selections maximizing the use of available circuit dynamic range [127]. Tolerance of gain mismatch is an especially important attribute in designs that have to operate over wide temperature ranges.

The final 2-2c cascade architecture selected for implementation is shown in Fig. 5.2. Using the classical gain settings, $g_3' = 0$ and all other gain values are set to 0.5. The

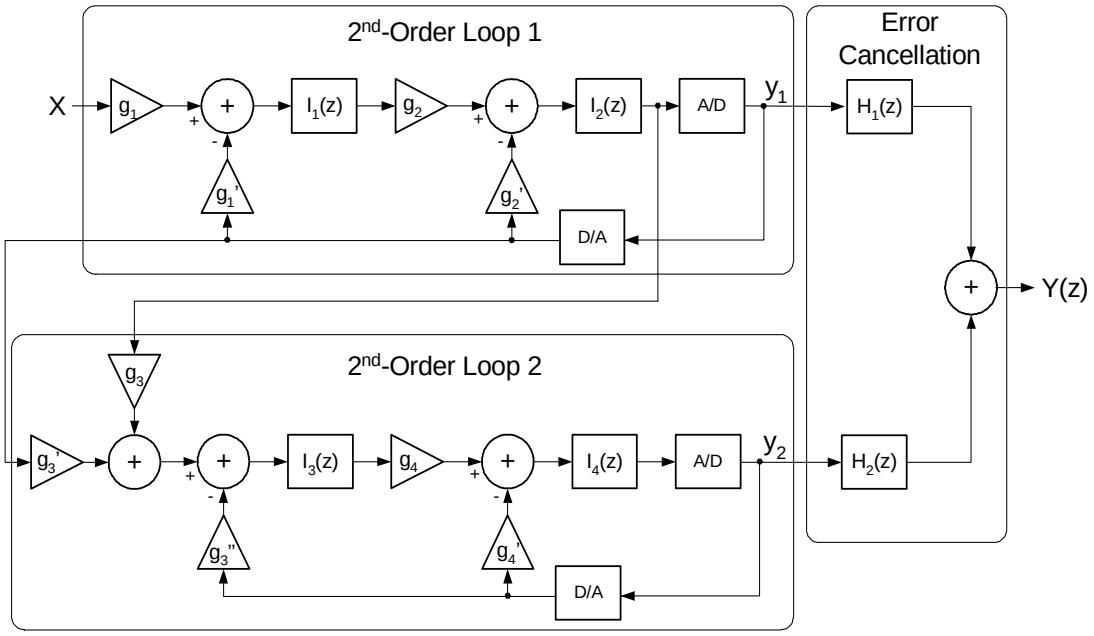


Figure 5.2 2-2 cascade modulator topology selected for implementation.

noise cancellation circuitry is completely digital. Since the architecture is composed of two separate 2^{nd}-order loops, measurement and analysis of both a 2^{nd}- and 4^{th}-order modulator is possible from the same design. This ability to configure the modulator as both a 2^{nd}- and 4^{th}-order modulator provides the flexibility required for thorough evaluation of the design techniques, selected architecture, and performance of the modulator in the target temperature-tolerant integrated circuit technology.

The selection of integrator gains for achieving a specific noise shaping function for a given modulator topology affect the selection and design of several other modulator parameters: the integrator opamp output swing, the feedback voltage levels supplied by the DACs, and ultimately the modulator input dynamic range. The integrator opamp output swing is the limiting factor and is determined first and then used to calculate the other

parameters. When using cascaded architectures, these levels must be selected to prevent input overloading of the second loop. For the 2-2c topology used in this research, the relationships between the opamp output swing (*OS*), the maximum input amplitude (V_{in}), and the feedback reference voltages (V_{ref}) are given as [127]

$$V_{in} \leq V_{ref} \leq (OS)/2 . \tag{5.3}$$

Determination of the maximum integrator opamp output swing is a function of the circuit design and is covered in detail in following sections.

A qualitative verification of the selected topology and associated gains was performed using a Unix-based switched circuit simulator developed at Stanford University called MIDAS [130]. Fig. 5.3 shows the output produced from simulation of the 2-2c cascade modulator for both 2^{nd}-order loops and for the overall 4^{th}-order transfer function produced by the digital noise cancellation circuitry. The results of these simulations verified that the modulator architecture was reasonably constructed, including both modulator loops and associated gains, and the digital noise cancellation circuitry. The expected 40dB/decade and 80dB/decade slopes were observed for the 2^{nd}- and 4^{th}-order modulators, respectively. The spreading of the fundamental is both the result of windowing and limited FFT resolution. In addition to spectral plots of the modulator output, the outputs of each of the integrators were monitored to ensure stable operation with a full-scale single tone input. These simulations are ideal in that only the quantization noise is modeled in the simulation. A discussion of the additional noise sources present in practical modulator implementation and methods for reducing the associated adverse effects on modulator performance are addressed in following sections.

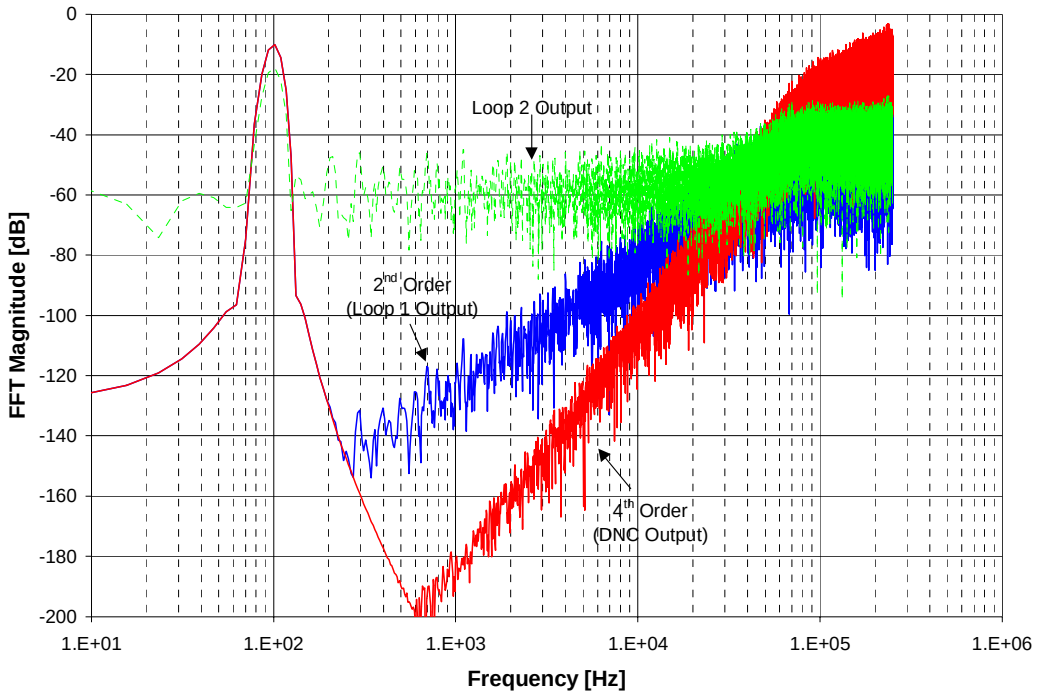


Figure 5.3 MIDAS simulation results for the 2-2c modulator architecture with full-scale, 100Hz single tone input.

5.2 Modulator Noise Analysis

There are a number of noise sources that limit the performance of a ΣΔ modulator: namely, modulator quantization noise and the electronics noise associated with the integrator opamp, comparator, and integrator switches. If sufficient modulator noise shaping order is employed, the quantization noise is reduced sufficiently in the input signal frequency bandwidth causing the sources of electronic noise to become the primary limiting factor. This input-referred noise power spectral density is composed of two primary sources, white noise and $1/f$ or flicker noise, and can be expressed as

$$\xi(f) = \xi_w + \frac{K}{f} \tag{5.4}$$

Here ξ_w represents the white noise and K is a constant associated with the 1/*f* noise. The development of the expressions in the remaining parts of this section closely follow the published work of Williams [207].

A common phenomenon in modulators that must be carefully considered in the design stage is noise folding or aliasing. The noise bandwidth of the modulator will be greater than the sampling frequency causing noise power at frequencies > f_s to alias into the base-band. This results in additional baseband noise equal to the sum of the noise power in baseband frequency windows centered at multiples of f_s. The number of windows summed, or the folding factor, Υ, is determined by the modulator noise bandwidth (*NBW*) and the sampling frequency:

$$\Upsilon = \frac{NBW}{f_s}. \tag{5.5}$$

Mathematically, the total baseband noise power at the output of the modulator including folding can be expressed as

$$S_N = \sum_{m=-\Upsilon}^{\Upsilon} \int_{f_1}^{f_2} \xi(|f - mf_s|)\,df. \tag{5.6}$$

Here f_1 and f_2 are the baseband lowest and highest frequency, respectively. Assuming $f_1 << f_2 << f_s$, and the modulator bandwidth is sufficient such that the settling time meets the requirement $\tau < 1/(\pi f_s)$, the approximate total inband noise power is given by

$$S_N = \frac{\xi_w}{4M\tau} + K\ln\frac{f_2}{f_1}. \tag{5.7}$$

Thus the white noise power is reduced by increased oversampling, and increased by reduced settling time, which is inversely proportional to the noise bandwidth. In $\Sigma\Delta$

modulators fabricated in CMOS (bulk and SOS/SOI), the flicker noise term is typically the dominant factor limiting the dynamic range of the modulator, provided the integrator amplifiers are designed such that excess bandwidth does not fold excessive white noise into the baseband. The next section will present two candidate approaches for reducing the 1/*f* noise in practical modulator implementations.

5.3 Noise Reduction Methods

As demonstrated above, the effect of noise aliasing or folding in the modulator can appreciably increase the input-referred noise, resulting in significant reduction of the obtainable dynamic range. There are two primary approaches to reduce this degradation effect: reduce the sources of noise, or shape the noise with a transfer function that reduces the input-referred portion. In practice, both of these techniques are routinely employed. Reducing the noise sources is primarily a function of integrator opamp design and will be covered in following sections. This section introduces two methods for noise shaping reduction: chopping and correlated double sampling.

5.3.1 Chopping Technique

Chopping is a technique which reduces the baseband noise power by modulating a portion of the low-frequency noise out of band [52,89]. This is accomplished by multiplying the input signal by +1 and -1 at one-half the sampling frequency, which centers the input spectrum at $\pm f_s/2$. The low frequency electronics noise power is then added to the spectrum at the modulator integrator input. At the output of the integrator, the total signal (input + noise) is multiplied by ± 1 shifting the input signal back to baseband and the unwanted low-frequency noise to $\pm f_s/2$. The resultant noise spectrum consists of 1/*f*

noise copies centered at odd multiples of $f_s/2$. As before, this noise is sampled by the modulator and aliased into the baseband. The total baseband noise power resultant from the use of the chopper becomes

$$S_N = \sum_{m=-\Upsilon}^{\Upsilon} \int_{f_1}^{f_2} \xi\left(\left|f-\left(m+\frac{1}{2}\right)f_s\right|\right)df. \tag{5.8}$$

Applying the same assumptions used in the development of Eqn. 5.7, the approximate baseband noise power as a result of chopping is given by

$$S_N = \frac{\xi_w}{4M\tau} + \frac{4K}{M}. \tag{5.9}$$

Comparing the result after chopping (Eqn. 5.9) to that before chopping (Eqn. 5.7), the white noise power remains constant, but the 1/*f* noise power in-band is reduced by approximately the oversampling ratio, *M*.

5.3.2 Correlated Double Sampling

Correlated double sampling (CDS) is another method commonly used for noise reduction in switched capacitor circuits [52,89]. In this method, the noise from successive modulator samples is differenced, resulting in a noise shaping function described by

$$\xi_s(f) = \xi(f)\left|1-e^{((-j2\pi f)/f_c)}\right|^2, \tag{5.10}$$

where f_c is the correlator sampling rate [207]. Sampled at f_s, the noise shaping function produces nulls at multiples of the modulator sampling clock, causing significant reduction in the folded noise components. The total baseband noise power becomes [207]

$$S_N = \frac{\xi_w \pi^2}{12M^3\tau} + \frac{K\pi^2}{2M^2}. \tag{5.11}$$

CDS significantly reduces the flicker noise contribution to the baseband noise, and is theoretically more effective at 1/*f* noise reduction than chopping. Fig. 5.4 shows the noise shaping transfer function magnitude, $|H_{CDS}(f)|$, produced by CDS at a correlation frequency of f_s.

There are many sources of electronic noise in a modulator that potentially contribute in some way to the input-referred noise. These sources include the input-referred noise of the integrator opamps (denoted n_1, n_2, n_3, n_4), the comparators, and the DACs. Referring to Fig. 5.2, the input-referred noise of the 2-2 cascaded modulator in terms of the integrator opamp noise and gains can be expressed without the integrator delay term as

$$n_{in} = n_1 + n_2\left(\frac{(1-z^{-1})}{g_1}\right) + n_3\left(\frac{(1-z^{-1})^2}{g_1 g_2}\right) + n_4\left(\frac{(1-z^{-1})^3}{g_1 g_2 g_3}\right). \quad (5.12)$$

If the circuit noise is white, the input-referred baseband power can be approximated as

$$S_{Nin} = \left(\frac{1}{M}\right)S_{N1} + \left(\frac{1}{g_1^2}\right)\left(\frac{\pi^2}{3M^3}\right)S_{N2} + \left(\frac{1}{g_1^2 g_2^2}\right)\left(\frac{\pi^4}{5M^5}\right)S_{N3} + \left(\frac{1}{g_1^2 g_2^2 g_3^2}\right)\left(\frac{\pi^6}{7M^7}\right)S_{N4}, \quad (5.13)$$

where S_{N1}, S_{N2}, S_{N3}, and S_{N4} represent the circuit noise power at each of the integrator inputs [158]. From Eqns. 5.12 and 5.13, one can observe the effect of each integrator reducing the input-referred noise contribution of following integrator stages. Likewise, noise and offset errors associated with each of the comparators are reduced by the same effect. In fact, the noise associated with each of the comparator stages is shaped by the same function as the quantization noise of that stage. If designed properly, these shaping effects can easily cause the noise of the first stage modulator to dominate the input-referred noise of the modulator. This can be accomplished by selecting a high oversam-

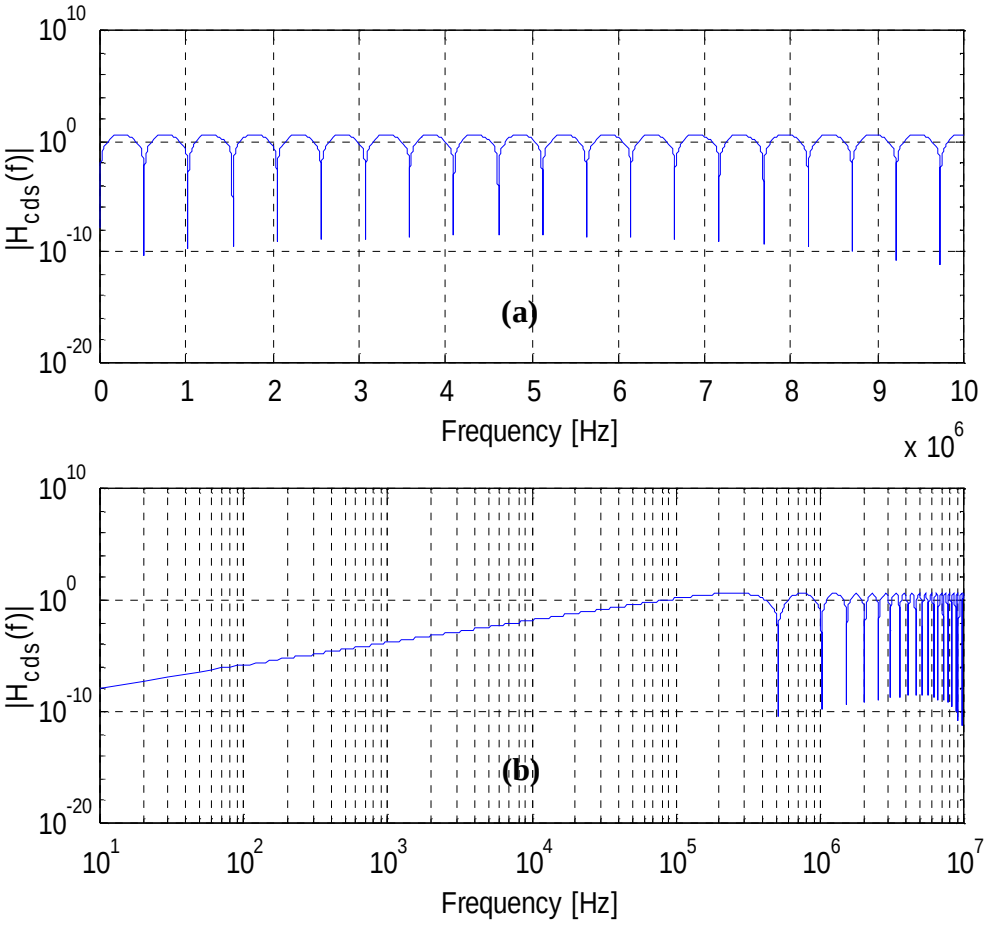


Figure 5.4 CDS noise shaping characteristic. (a) linear frequency scale, and (b) log frequency scale.

pling rate and being careful that the secondary integrator stages do not have excessive noise. In this modulator design, use of these techniques provides for the first stage noise to dominate and consequently only the first stage electronics noise is considered in following analysis.

In addition to the opamp and comparator noise, the DAC and modulator switch noise must also be considered. With regard to the DAC, this block is commonly implemented as a switch between two reference levels that can be heavily filtered such that no appreciable noise is contributed to the modulator. The switch noise can be a significant contributor to the noise and must be carefully considered. The switch noise contribution is actually independent of the switch resistance and contributes a total noise power in the baseband equal to

$$S_N = \frac{kT}{MC}, \tag{5.14}$$

where k is Boltman's constant, T is the temperature in Kelvin, and C is the capacitor value associated with the switch-capacitor circuit [207]. This noise can be reduced by proper selection of the oversampling ratio and the sampling capacitor value. Note that this analysis only incorporates the effect of switch white noise. This is traditionally accepted practice since the trap centers associated with $1/f$ noise are being continually reset by the on/off operation of the switches, and empirical evidence supports this assumption [158,207].

5.4 Modulator Integrators

Two approaches were considered for implementation of the modulator integrators: continuous time and sampled time. Continuous time approaches use passive devices (resistors and capacitors) to achieve the desired transfer function. For monolithic imple-

mentations, this approach is undesirable for two primary reasons: the large value passive devices often needed are not easily realizable on-chip due to area constraints, and the accuracy of the transfer function characteristics rely on the absolute component values, which have poor tolerance values. In addition, these approaches have been shown to demonstrate increased sensitivity to clock jitter and do not allow the use of 1/*f* noise reduction techniques [207], as previously discussed. Conversely, sampled-time circuits implemented using switched-capacitor techniques are monolithically compatible, provide precise placement of poles and zeros that are set by the sampling frequency and capacitor ratios which can be tightly controlled on-chip with proper layout techniques, and allow the use of 1/*f* noise reduction techniques. For these reasons, switched-capacitor circuits were chosen for implementation of the modulator integrators.

A fully differential switched-capacitor integrator block diagram is shown in Fig. 5.5, along with the associated clock signals required for operation [127]. Use of a fully differential topology is essential for high-resolution conversion as it eliminates many common-mode error sources. Precise timing control of the integrator is accomplished using two non-overlapping clocks, delayed versions of these non-overlapping clocks, and inverted copies of each for a total of eight precisely generated clock signals.

During phase1, switches S_1 and S_3 sample and store the difference between V_{mid} and V_{in} across capacitors C_{s1} and C_{s2}. During phase2, switches S_2 and S_4 are closed and the charge difference between V_e and V_{in} is stored on capacitors C_{f1} and C_{f2}. Switches S_1 and S_2 are actually operated using delayed versions of the phase1 (S_3) and phase2 (S_4) clocks,

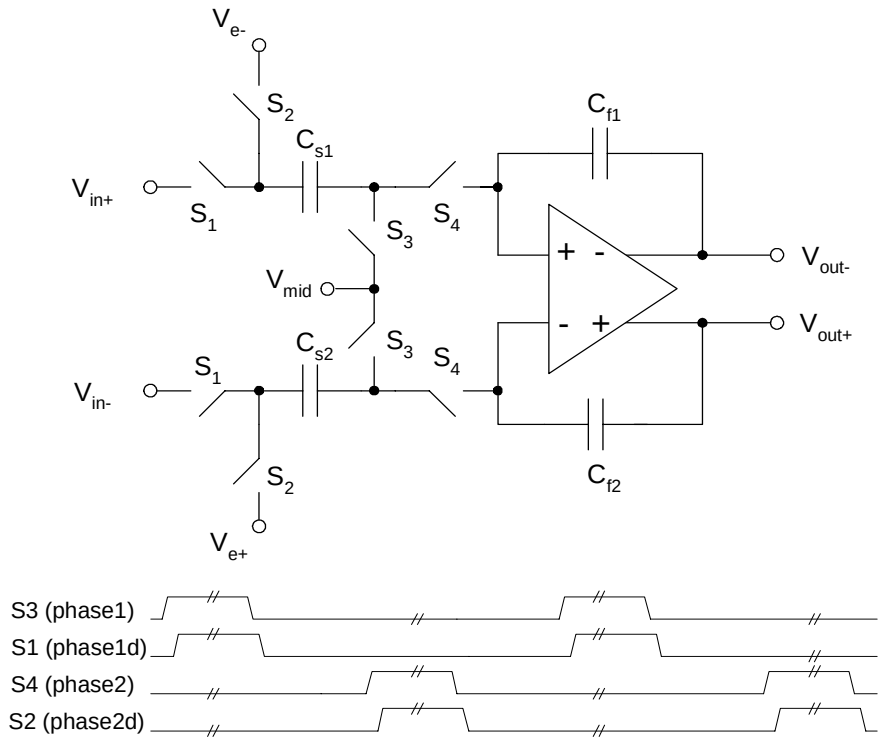


Figure 5.5 Standard switched-capacitor integrator with clocks.

respectively. The use of this delayed timing scheme minimizes the effect of amplitude dependant charge injection [106].

The output of the integrator at time $(n+1)T_s$ is given by

$$V_{out}[(n+1)T_s] = \left(\frac{A}{1+A}\right)V_{out}[nT_s] + \left(\frac{C_s}{Cf}\right)(V_{in}[nT_s] - V_e[nT_s]), \qquad (5.15)$$

where -*A* is the integrator opamp gain and will determine the approximate amount of integrator leakage - the amount of signal from one integration cycle that is lost and not integrated into next cycle. For this reason, the amplifier must be designed to have large open loop dc gain, typically larger than the oversampling ratio.

The integrator topology of Fig. 5.5 is sufficient for use in all the modulator integrators except the first stage where either CDS or chopping techniques are needed to reduce the effects of electronic flicker noise.

An integrator incorporating the chopping technique for 1/*f* noise reduction was chosen for use in the first modulator integrator. This decision was made based on reference materials on-hand at the time and was forced by the immediate need to design and fabricate a modulator to meet scheduling requirements set by our industrial customer. However, the analysis detailed in earlier sections of this chapter, performed after the design was performed and submitted for fabrication, demonstrates that CDS provides significant benefits over chopping methods, particularly when 1/*f* noise is the dominate noise contributor. Measured data presented in Chapters 6 & 7 will demonstrate the flicker noise dominance.

The chopper integrator topology chosen for this design and associated clock signals are shown in Fig. 5.6. The topology is identical to that in Fig. 5.5 except for the addition of switches S_c, S_d, S_{cd}, and S_{dd} which perform the commutation function associated with chopping. These switches are operated at a frequency of $f_s/2$ and require 4 additional pairs of control clocks as compared to the non-chopped integrator. The additional clocks are also two-phase non-overlapping with delayed phases but operate at one-half the frequency of the modulator clock, and transition during the non-overlapping time between the regular integrator clocks. Only the primary eight clocks are shown in Fig. 5.6 as the remaining clocks are inverted copies of those shown.

Referring to Fig. 5.6, switches S_c and S_{cd} are closed during the first phase of the chopper cycle (with S_d and S_{dd} open) allowing the circuit to operate as a normal integrator.

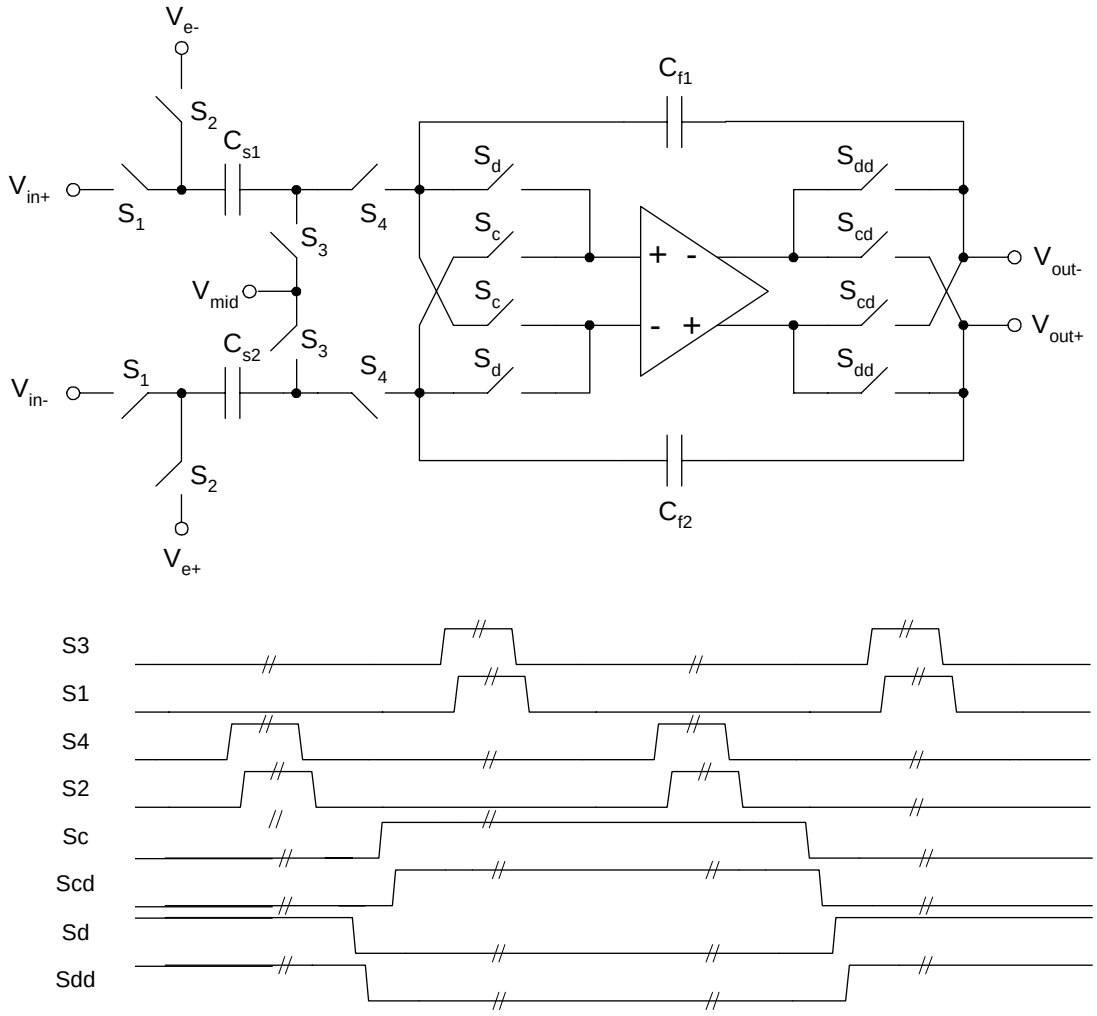


Figure 5.6 Switched-capacitor integrator with chopper and clocks.

During the second phase, S_c and S_{cd} are opened and S_d and S_{dd} are closed switching the input and output terminals of the amplifier. This operation accomplishes a switching of the gain sign each cycle which performs the modulation/demodulation function associated with chopping.

5.5 Modulator Sources of Error

In addition to electronic noise, there are a number of other sources of performance reducing errors in modulators due to non-ideal implementation of the modulator functions. Table 5.2 summarizes these error sources, identifies the associated modulator functional blocks, and lists the resultant effect of each on the modulator performance [127,142]. Each of these error mechanisms will be addressed in the associated building block design sections that follow.

Table 5.2: Modulator sources of error.

Building Block	Non-ideal Parameter	Effect on Modulator Performance
Integrator Opamp	Finite DC gain	Quantization noise increase
Integrator Opamp	Gain non-linear	Harmonic distortion
Integrator Opamp	Slew-rate	Harmonic distortion
Integrator Opamp	Finite GBW	Settling error
Integrator Opamp	Limited Output Swing	Overloading
Switches	Non-zero ON Resistance	Quantization noise increase
Capacitors	Non-linearity & mismatch	Quantization noise increase & harmonic distortion
Clocks	Jitter	Jitter noise
Comparators	Offset, Hysteresis	Quantization noise increase

5.6 Integrator Capacitor Value Selection

Referring to Fig. 5.5, the gain of the integrator is set by the ratio the sampling capacitor (C_{s1}, C_{s2}) and the feedback capacitor (C_{f1}, C_{f2}). Selection of these capacitor values was made by evaluation of the noise contribution. The design criteria chosen was to make the *kT/C* noise just less than the expected opamp white noise, causing the opamp white noise to be the dominant noise source. Assuming a white noise spectral density of $4\text{nV}/\sqrt{Hz}$ was achievable for the selected opamp topology, the equivalent capacitance value needed to match this noise contribution is 1.04pF (at 300K). This value was selected as 5pF. With the sampling capacitor set to 5pF (C_{s1}, C_{s2} in Fig. 5.5) the feedback capacitance needed was 10pF (C_{f1}, C_{f2}) to obtain the desired integrator gain of 0.5. The use of large capacitance values provides a number of advantages including minimization of the effect of parasitic wiring and amplifier input capacitance on the settling behavior, and improved gain matching allowing for a better realization of the desired gain and quantization noise shaping function [175,176]. The primary disadvantages associated with the use of larger capacitor values are the need for higher current drive to meet the slew rate requirements, and larger silicon area required for fabrication. In this design, performance is the primary objective. Power consumption and required layout area are secondary design criteria as long as these parameters are kept reasonable.

5.7 Modulator System Timing Specifications

The overall system timing requirements for this design are consistent with typical seismic applications. The converter is designed for a baseband input signal bandwidth of 1kHz, requiring the digital output rate (DOR) to be 2k samples per second. With an over-

sampling ratio (M) of 256, the sample frequency (f_s) of the modulator is 512kHz. Selection of this frequency will set boundaries for several of the system components whose design is outlined in following sections.

5.8 Integrator Opamp Design & Simulation

As previously discussed, the integrator opamp is the most important single circuit in the modulator design since a number of functional requirements must be met to obtain desired modulator performance. Namely, open loop gain, bandwidth and associated settling time, slew rate, noise bandwidth, output swing, and input-referred noise all are critical parameters that must be carefully considered when selecting an opamp topology. High loop gain is required to maintain sufficient noise shaping and must be maintained over temperature. Insufficient loop gain will cause integrator leakage and result in an increase in the baseband quantization noise power. The slew rate and settling time are both associated with settling errors which can be a significant source of error. Non-linear settling errors associated with slewing result in harmonic distortion and are eliminated by incorporating sufficient slewing capacity. Linear settling errors associated with linear settling of the amplifier result in gain errors, and can be tolerated within limits [142]. The noise bandwidth is a critical parameter that determines how much of the undersampled noise is aliased into the baseband. The output swing limitations of the amplifier ultimately set the upper input dynamic range specifications for the modulator. Operating past these limits in the nonlinear regions of the output swing reduces the loop gain and produces harmonic distortion in the modulator output spectrum. The input-referred white and flicker noise components set the lower limit of the resolution and must be carefully considered -- par-

ticularly in the first integrator stage which dominates the noise performance of the entire modulator. Applying these principles, specifications for the integrator opamp were determined and are summarized in Table 5.3. Determination of the load capacitance at each of the integrator opamp outputs is a critical parameter necessary for proper design of the amplifier as it affects the bandwidth, stability, slew rate, and settling performance of the integrator. Using the capacitance models for the standard integrator shown in Fig. 5.7, the load capacitance can be estimated for each of the 2 clocking phases. The chopper integrator switches contribute insignificant load capacitance and are ignored in this analysis making the model applicable to both the standard and chopper integrator. The load capacitance for phase 1 and phase 2 can be expressed as

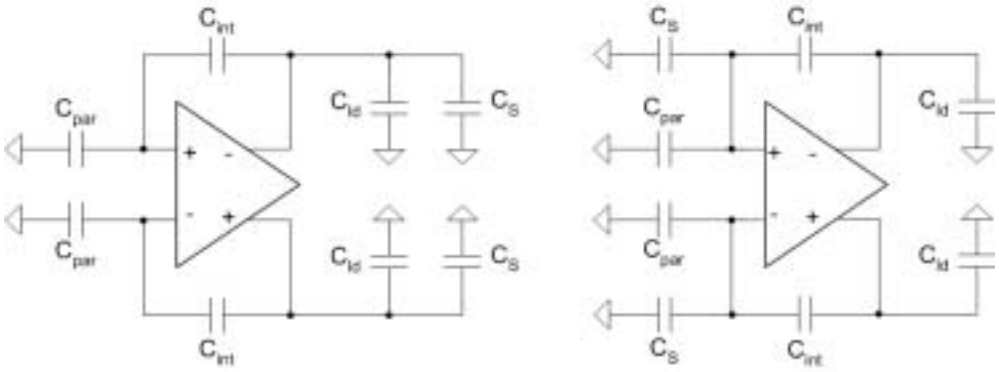
$$C_{load\phi 1} = C_s + C_{ld} + \frac{C_{int}C_{par}}{C_{int} + C_{par}} \approx C_{ld} + C_s \text{ and} \tag{5.16}$$

$$C_{load\phi 2} = C_{ld} + C_{int} \| (C_s + C_{par}) \approx C_{ld} + \frac{C_{int}C_s}{C_{int} + C_s}, \tag{5.17}$$

respectively. Here C_{ld} is the load capacitance, C_s is the sampling capacitance, C_{par} is the parasitic capacitance associated with the opamp large input device, and C_{int} is the integrator feedback capacitance. Selecting C_s=5pF, C_{int}=10pF and C_{ld}=18pF, and assuming $C_s \gg C_{par}$ such that C_{par} can be ignored, results in $C_{load\phi 1} \approx 23pF$ and $C_{load\phi 2} \approx 21.3pF$. The selection of C_{ld} was made for bandwidth and stability reasons as discussed later in this section. Note that the fourth integrator will see a reduced capacitance load due to the absence of a following integrator. As a result of these calculations, an effective load capacitance of 20pF is used in the following integrator amplifier simulations..

Table 5.3: Target integrator opamp design specifications.

Design Parameter	Abbreviation	Target Value
Open Loop DC Gain	A_{ol}	>2000 V/V
Gain Bandwidth	GBW	~10 MHz
Slew Rate	SR	$4V/\mu s$
Output Swing	OS	+- 1V
eni (white)	ξ	$4nV/\sqrt{Hz}$
eni (1/*f*)	K_a	low/unknown



(a) **(b)**

Figure 5.7 Integrator capacitance model. (a) phase 2 and (b) phase 1.

A fully differential folded-cascode topology was selected for the integrator opamp primarily for loop gain reasons. Simulations performed using vendor-supplied models extracted from the targeted SOS fabrication process demonstrate a lower output impedance than typical for bulk CMOS devices. Thus cascoding is needed to obtain loop gains on the order of 1000-2000. An alternative to cascoding is the use of multi-stage amplifier topologies which provide improved output dynamic range but are more difficult to compensate and require multiple common mode feedback (CMFB) control loops [129]. For these reasons, the cascoded topology requiring only one CMFB control loop was selected. The fully differential folded cascode opamp and CMFB control loop are shown in Fig. 5.8. Continuous-time CMFB control was used rather than switched-capacitor CMFB. Though switched-capacitor CMFB is advantageous in terms of lower-power consumption, continuous-time CMFB was selected to allow wider applicability of the design to other projects

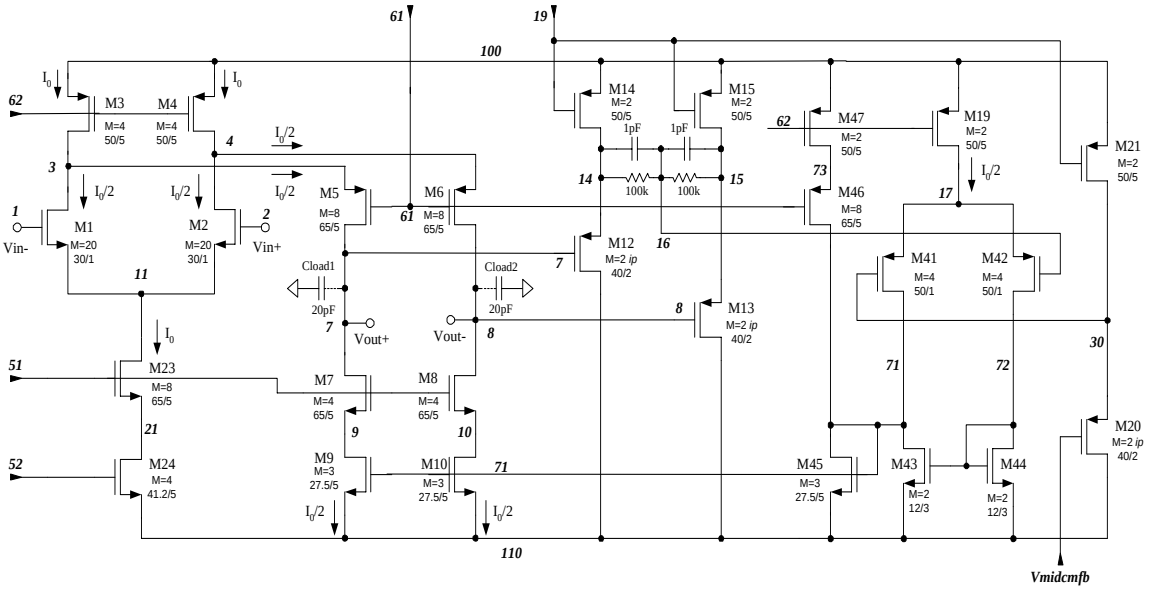


Figure 5.8 Fully differential folded cascode opamp with CMFB loop.

and to simplify the associated circuit simulations. The amplifier bias circuitry is shown in Fig. 5.9. Design techniques and full usage of low- and regular-threshold devices were employed to provide maximum dynamic range and circuit performance in all of the circuits designed.

Referring to Fig. 5.8, transistors M_1-M_{10} form the folded cascode stage. M_5-M_8 are the cascode devices used to increase the output impedance of the amplifier. Transistors M_{12}-M_{15} act as source follower stages to buffer the amplifier output from the resistance divider network used to sample the common-mode output voltage of the amplifier. M_{20} and M_{21} produce a common mode reference signal that is differenced by the differential pair formed by M_{41}-M_{45} that control the gate bias on M_9 and M_{10} to keep the amplifier output common-mode voltage at approximately $v_{midcmfb}$. Note that the CMFB loop is also compensated by the load capacitances, C_{load1} and C_{load2}.

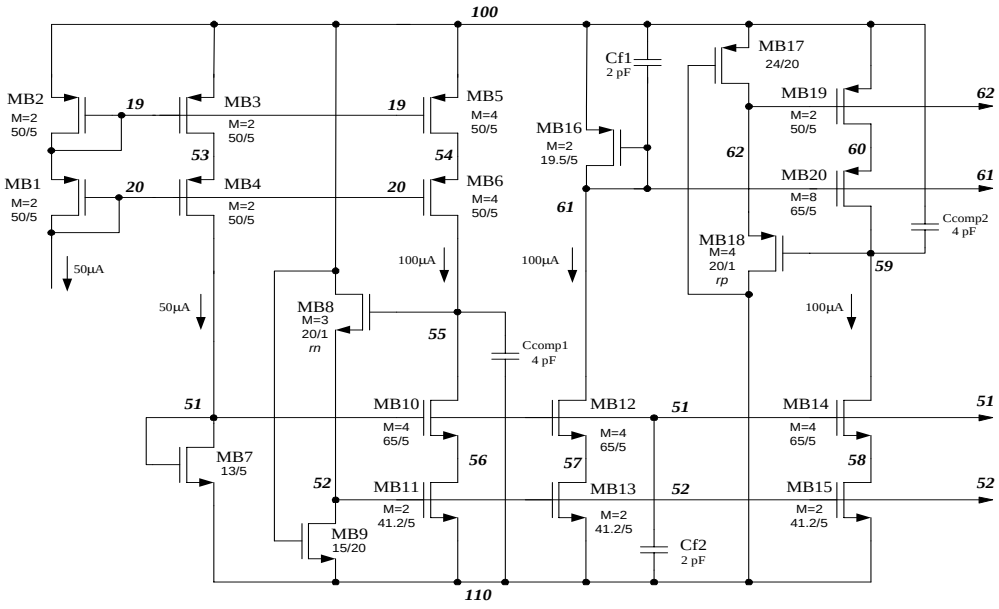


Figure 5.9 Bias generator circuit for Amp2b.

The dc loop gain (A_{ol}) and gain bandwidth product (*GBW*) for this amplifier are given by

$$Aol = g_{m1}[(r_{ds7}r_{ds9}g_{m7}) \parallel (g_{m5}r_{ds5}(r_{ds1} \parallel r_{ds3}))] \text{ and} \tag{5.18}$$

$$GBW = \frac{g_{m1}}{C_{load}}, \tag{5.19}$$

respectively.

The dominant pole is determined by the output resistance and capacitance seen at the load as

$$f_1 = \frac{1}{2\pi R_{out}C_{Load}}. \tag{5.20}$$

A secondary pole, f_2, that determines the stability of the amplifier, is approximately determined at frequencies near the crossover frequency by the impedance looking into the output cascode device, M_5, and the equivalent capacitance of the source node of M_5, typically dominated by the input pair drain capacitance:

$$f_2 \approx \frac{g_{m5}}{C_{s5}}. \tag{5.21}$$

Here, M_5 determines the impedance at this node since the impedance looking into the source is approximately $1/g_{m5}$.

Referring to the integrator amplifier bias circuit shown in Fig. 5.9, a combination of cascoded current sources and low-dropout current sources are used to ensure stable generation of the bias voltages for the amplifier input tail current source and loads, output cascode devices, and common mode feedback control circuits [97].

For the folded cascode amplifier of Fig. 5.8, the primary noise contributors are the input differential pair (M_1 and M_2), the PMOS loads (M_3 and M_4) and the NMOS loads (M_9 and M_{10}). The input-referred cascode device (M_5-M_8) noise is reduced because of source degeneration. Additionally, the tail current bias transistors (M_{23} and M_{24}) introduce only common-mode noise and can be ignored in the analysis. Applying these assumptions, the input-referred noise spectral density of the folded cascode amplifier is expressed as

$$e_n^{\,2} \approx 2\left[e_{n1}^{\,2} + e_n^{\,2}\left(\frac{g_{m3}}{g_{m1}}\right)^2 + e_n^{\,2}\left(\frac{g_{m9}}{g_{m1}}\right)^2\right]. \tag{5.22}$$

Selection of exact device sizes involves a number of performance trade-off associated with sizing and biasing devices. Table 5.4 summarizes the primary performance parameters and the associated equations. High A_{ol} is accomplished in general by maintaining high device output impedance (using large gate L) and designing the input devices for large g_m which is accomplished by increasing the input device drain current or the *W/L* ratio. Large input pair g_m also increases the bandwidth but has associated noise disadvantages covered later in this section. Slew rate increases proportionally with the drain current of M_1 and M_2, but degrades the output swing due to an increase in the output device saturation voltage. In terms of noise, the input pair must be carefully sized for several reasons. In general, enlarging device area will reduce flicker noise contribution which is a major problem in CMOS integrated circuits. For the input pair, both the gate area (WL product) and the g_m should be made large but with caution. The consequences of large input devices (M_1, M_2) include undesirable effects that must be carefully considered including excessive noise folding (due to excessive noise bandwidth) and reduced phase margin (due to input

Table 5.4: Opamp design parameters and associated relationships for folded cascode topology.

Parameter	Symbol	Associated Equations
Open Loop DC Gain	A_{ol}	$A_{ol} = g_{m1}[(r_{ds7}r_{ds9}g_{m7}) \parallel (g_{m5}r_{ds5}(r_{ds1} \parallel r_{ds3}))]$ $r_{ds} = \frac{1}{\lambda I_D} \qquad g_m = \sqrt{2\mu C_{ox}(W/L)I_D}$ (for saturation)
Gain Bandwidth	GBW	$GBW \approx \frac{g_{m1}}{C_{load}} \quad f_1 = \frac{1}{2\pi R_{out}C_{Load}} \quad f_2 \approx \frac{g_{m5}}{C_{s5}}$
Slew Rate	SR	$SR = \frac{I_D}{C_{load}}$
Output Swing	OS	$OS = V_{OS+} - V_{OS-}$ $V_{OS+} = V_{DD} - V_{DSsat3} - V_{DSsat5}$ $V_{OS-} = V_{SS} + V_{DSsat7} + V_{DSsat9}$ $V_{DSsat} = V_{GS} - V_t = \frac{2I_D}{g_m} = \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}}$ (for NMOS in saturation)
Input-referred Noise Voltage	e_n	$e_n^2 \approx 2\left[e_{n1}^2 + e_n^2\left(\frac{g_{m3}}{g_{m1}}\right)^2 + e_n^2\left(\frac{g_{m9}}{g_{m1}}\right)^2\right]$ $e_n^2 = 4kT\left(\frac{2}{3}\right)g_m + \frac{K}{WLC_{ox}f}$ (MOSFET e_n)
Settling Time Constant	τ	$\tau \approx \frac{1}{\beta\omega_t} = \left(\frac{C_f + C_s + C_{par}}{C_f}\right)\left(\frac{C_{load}}{g_{m1}}\right)$ (see Fig. 5.5)
Noise Bandwidth	NBW	$NBW \approx (\pi/2) \times BW$ (single pole approximation)

pair parasitic capacitance that contributes the secondary open loop pole). Reducing the g_m of the load devices (M_3, M_4, M_9, M_{10}) will reduce their contribution to the input-referred noise but will increase their V_{DSsat} values resulting in decreased output swing capability. The device type, threshold type, and size for the opamp and associated bias circuits are listed in Table 5.5 and Table 5.6, respectively. The input devices (M_1 and M_2) were sized with L=1μm to achieve high transconductance (~2 mS) without significantly degrading the phase margin due to excessively large drain capacitance. The other devices of the foldedcascode were sized for L=5μm to provide excellent device matching and increased output impedance to obtain high loop gain.

Using foundry supplied Level 49 BSIM3V3 models, a number of simulations were performed on the finished amplifier design using HSPICE (version 2001.2) [90]. The

Table 5.5: Amp2b device information.

Reference	Type	Threshold	W/L [μm/μm]
M1,M2	NMOS	Low	600/1
M3,M4	PMOS	Low	200/5
M5,M6,M46	PMOS	Low	520/5
M7,M8	NMOS	Low	260/5
M9,M10,M45	NMOS	Low	82.5/5
M12,M13,M20	PMOS	Intrinsic	80/2
M14,M15,M19,M21,M47	PMOS	Low	100/5
M23	NMOS	Low	520/5
M24	NMOS	Low	164.8/5
M41,M42	PMOS	Low	200/1
M43,M44	NMOS	Low	24/3

Table 5.6: Amp2b_bias device information.

Reference	Type	Threshold	W/L [μm/μm]
MB1,MB2, MB3,MB4,MB19	PMOS	Low	100/5
MB5,MB6	PMOS	Low	200/5
MB7	NMOS	Low	13/5
MB8	NMOS	Regular	60/1
MB9	NMOS	Low	15/20
MB10,MB12,MB14	NMOS	Intrinsic	260/5
MB11, MB13,MB15	NMOS	Low	82.4/5
MB16	PMOS	Low	39/5
MB17	PMOS	Low	24/20
MB18	PMOS	Regular	80/1
MB20	PMOS	Low	520/5

simulation input was generated from the extracted integrated circuit layout to include parasitic capacitances associated with the layout and to ensure the proper device sizes were used.

Simulations results of the amplifier open loop dc gain as a function of both bias current and temperature are shown in Figures 5.10 and 5.11 Selected points of this simulation are summarized in Table 5.7. Note the decrease in loop gain as the temperature increases and the sharp decrease near T=200°C, particularly for the lowest bias current value (10μA). Also, note the change in the loop gain as a function of bias current. For all temperatures, the loop gain peaks near a bias current of 50μA. This value was chosen as the nominal target bias current for the design since simulations indicated acceptable slew rate, output swing, and loop gain under this bias condition. Further increasing of this cur-

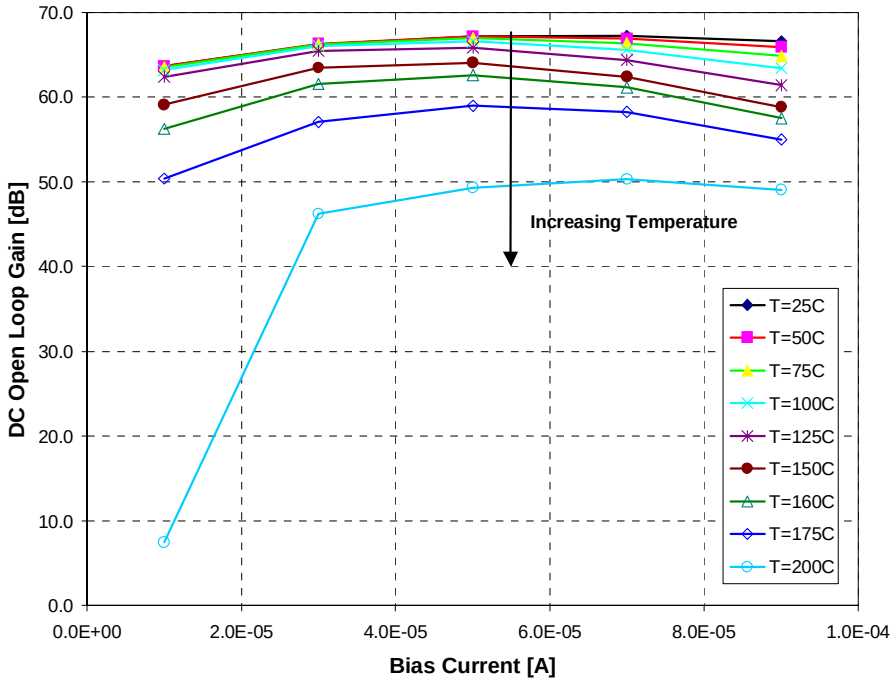


Figure 5.10 Amp2b dc open loop gain vs. bias current and temperature.

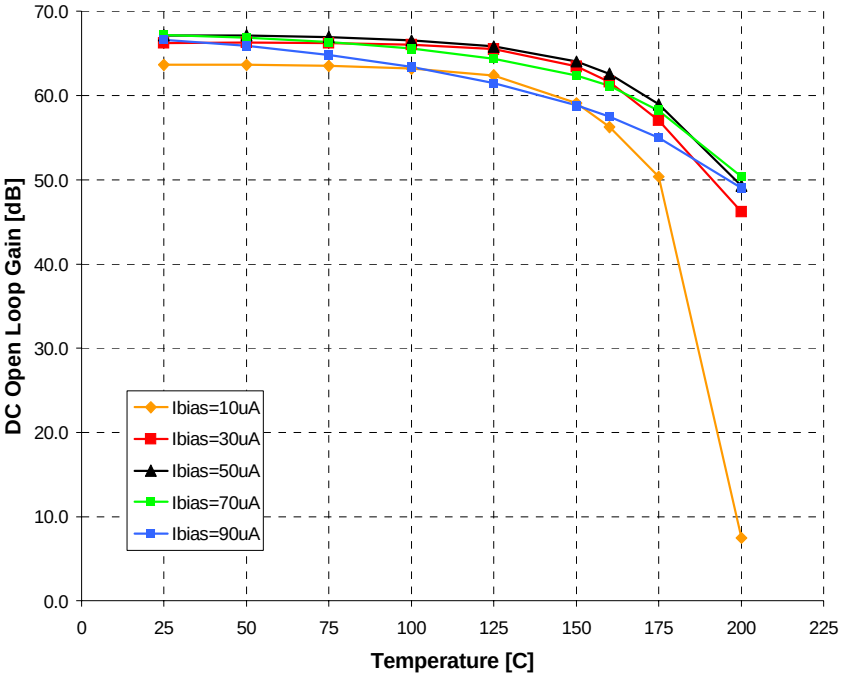


Figure 5.11 Amp2b dc open loop gain vs. temperature and bias current.

Table 5.7: Simulated Amp2b open loop dc gain vs. temperature & bias current.

Temperature [°C]	**A_{ol} [dB]** (Ibias=10μA)	**A_{ol} [dB]** (Ibias=30μA)	**A_{ol} [dB]** (Ibias=50μA)	**A_{ol} [dB]** (Ibias=70μA)	**A_{ol} [dB]** (Ibias=90μA)
25	63.7	66.2	67.2	67.2	66.6
125	62.4	65.6	65.8	64.4	61.4
150	59.1	63.5	64.1	62.4	58.9
175	50.4	57.0	58.9	58.2	55.0
200	7.47	46.2	49.3	50.3	49.1

rent results in decreased output swing, an unwanted increase in amplifier bandwidth (which increases noise folding), and additional power consumption. A number of additional simulations were performed on the amplifier using the selected bias current of 50μA over a temperature range of 25° C to 200° C. All simulations were performed in HSPICE (version 2001.2) using foundry supplied Level 49 models. Figures 5.12 and 5.13 show the open loop gain and phase, respectively. Fig. 5.14 shows the amplifier output under slew conditions. In Fig. 5.15 the simulated slew rates (positive, negative) are plotted as a function of temperature. Fig. 5.16 shows both the maximum amplifier output swing and linear output swing under overdriven conditions. The linear output swing was calculated from the output stage device saturation voltages according to the relationships listed in Table 5.4. A summary of the integrator opamp simulation results as a function of temperature is given in Table 5.8. A decrease in open loop gain due to expected reduction in g_m as temperature increases was observed. In addition, a reduction in GBW with increasing temperature was indicated, due to input pair device g_m degradation with increasing tem-

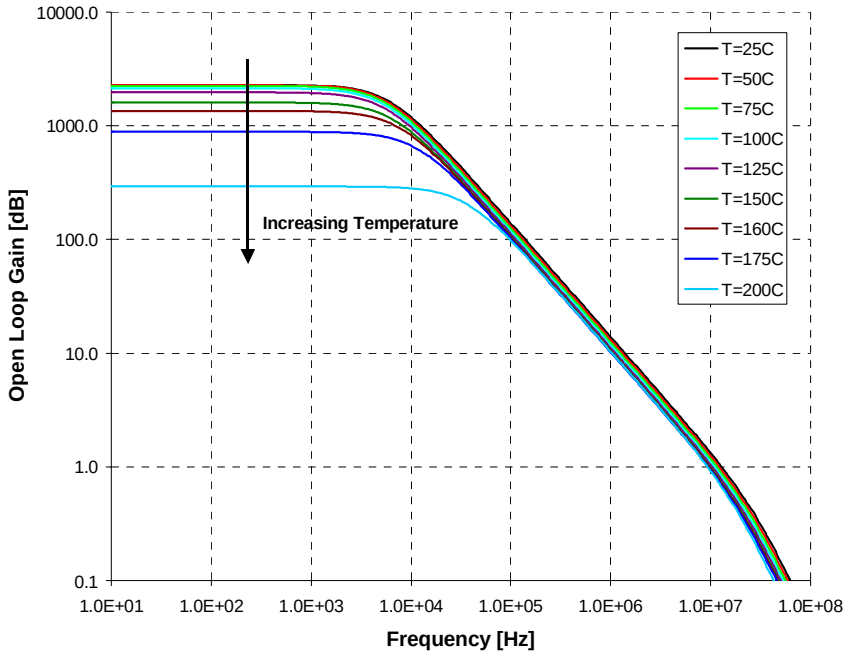


Figure 5.12 Simulated Amp2b open loop gain magnitude (Cload=20pF).

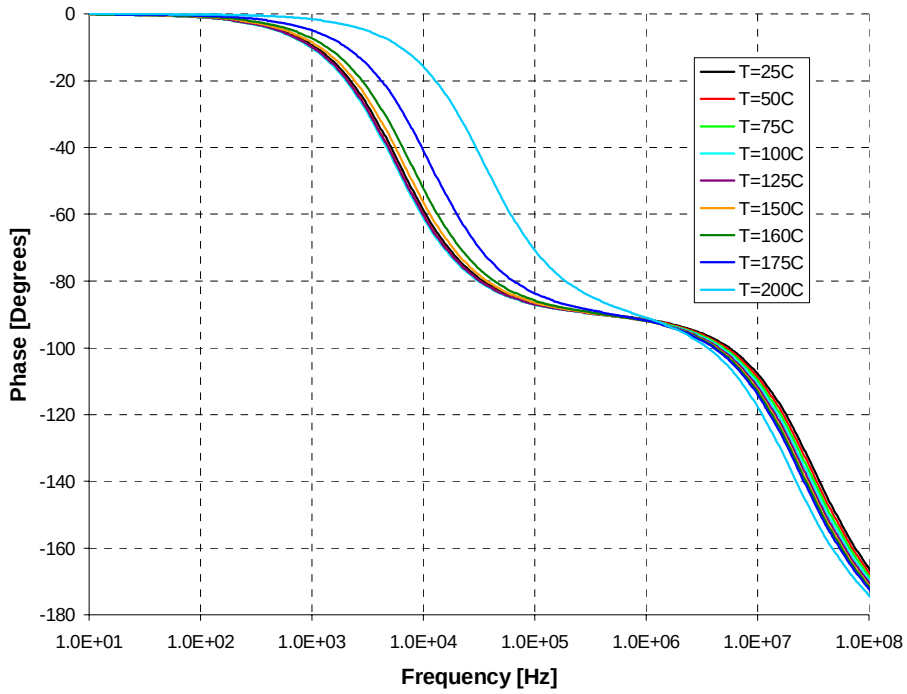


Figure 5.13 Simulated Amp2b open loop gain phase (Cload=20pF).

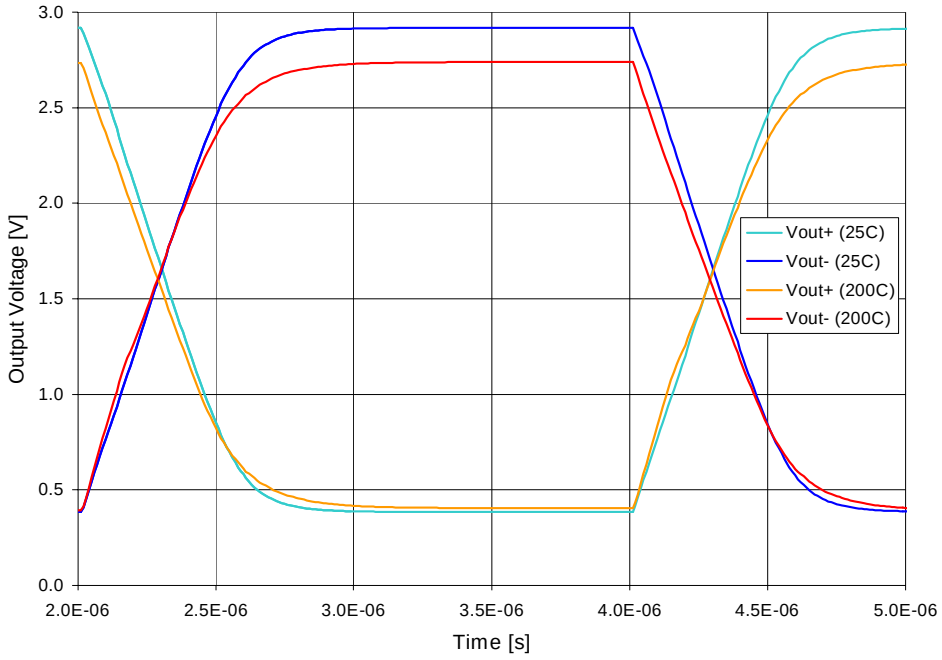


Figure 5.14 Simulated Amp2b output characteristics vs. temperature for T=25° C and T=200° C (Cload=20pF).

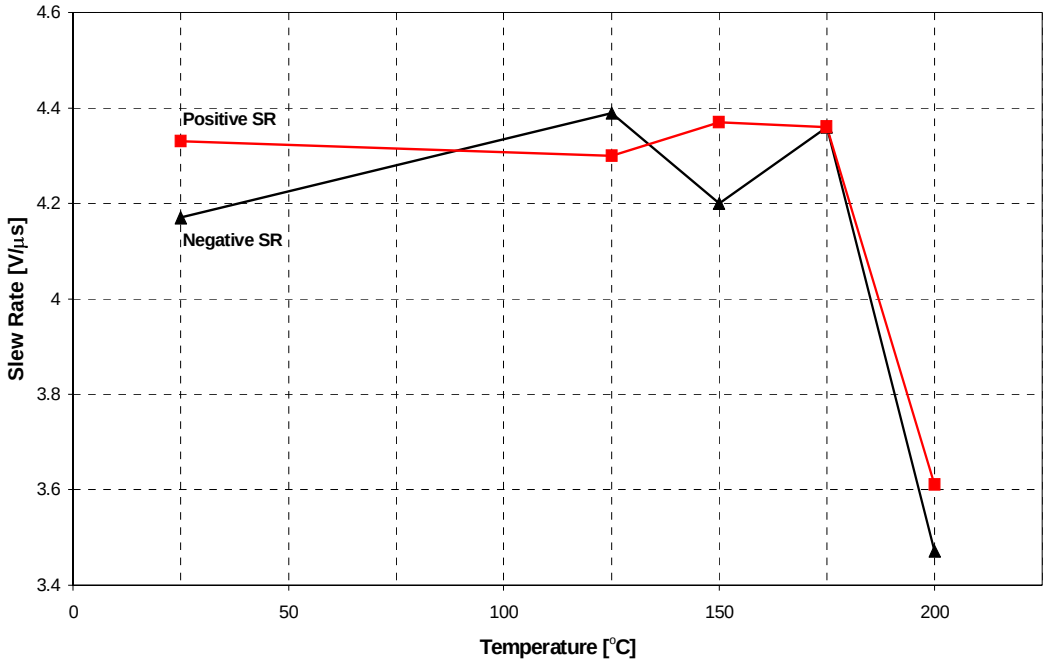


Figure 5.15 Simulated Amp2b slew rate vs. temperature.

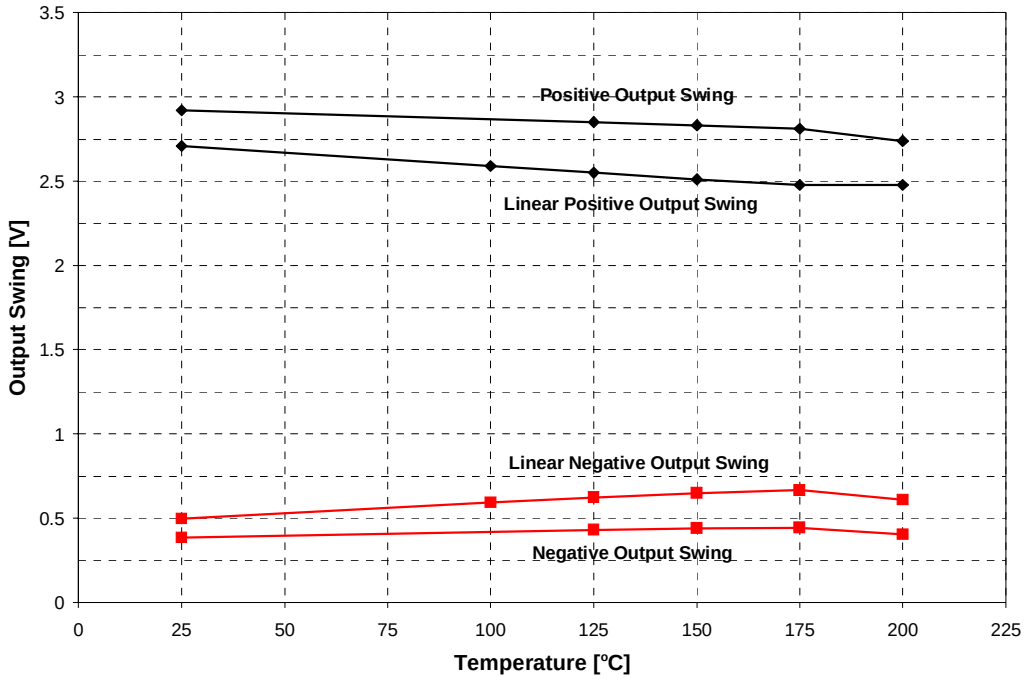


Figure 5.16 Simulated Amp2b output swing characteristics vs. temperature.

Table 5.8: Amp2b simulation summary vs. temperature (ibias=50μA, C_{load}=20pF).

Temp. [° C]	Aol [dB]	GBW [MHz]	Phase Margin [°]	|Slew Rate| (|pos / neg) [V/μs]	Output Swing [V]	Linear Output Swing [V]	Power Consumption [mW]
25	67.18	12.90	67.53	4.17 / 4.33	2.53	2.21	4.48
50	67.15	12.18	67.46	- - -	- - -	2.14	4.42
75	66.95	11.52	67.47	- - -	- - -	2.07	4.37
100	66.55	10.92	67.52	- - -	- - -	2.00	4.33
125	65.83	10.36	67.61	4.39 / 4.30	2.42	1.93	4.30
150	64.06	9.86	67.64	4.2 / 4.37	2.39	1.86	4.28
175	58.94	9.47	67.21	4.36 / 4.36	2.37	1.81	4.28
200	49.31	9.34	64.04	3.47 / 3.61	2.34	1.87	4.29

perature. Consistency in slew rate indicates stability of the opamp bias circuit over temperature. The observed decrease in linear output swing with increasing temperature is also expected due to g_m degradation (see Table 5.4). A number of these phenomenon can be explained by the reduction of g_m due to electron and hole mobility reduction with increasing temperature [154]. These results are compared to a limited set of measurement results in Chapter 6 and provide some insight into the accuracy of the models used, over temperature.

Noise simulations were also performed on the integrator opamp using foundry supplied Level 49 models. The results of these simulations are shown in Fig. 5.17. The accuracy of the foundry supplied noise models was uncertain. Therefore, a very detailed noise analysis was not performed prior to submission of the modulator. The strategy employed was to make reasonable design decisions regarding noise, fabricate both a device test chip and the entire modulator, test both chips, and improve the models and future chip designs where possible. A summary of SOS device noise measurements and the associated noise measurement techniques are detailed in Appendix A.

Selected input referred noise values from the simulations are listed in Table 5.9. Values shown were selected in two areas of the noise characteristic: where white noise dominates and where flicker noise dominates. A general increase in noise was observed as the temperature increased to 175° C. An unexpected decrease in noise was indicated by the simulations at 200° C, relative to the T=175° C values.

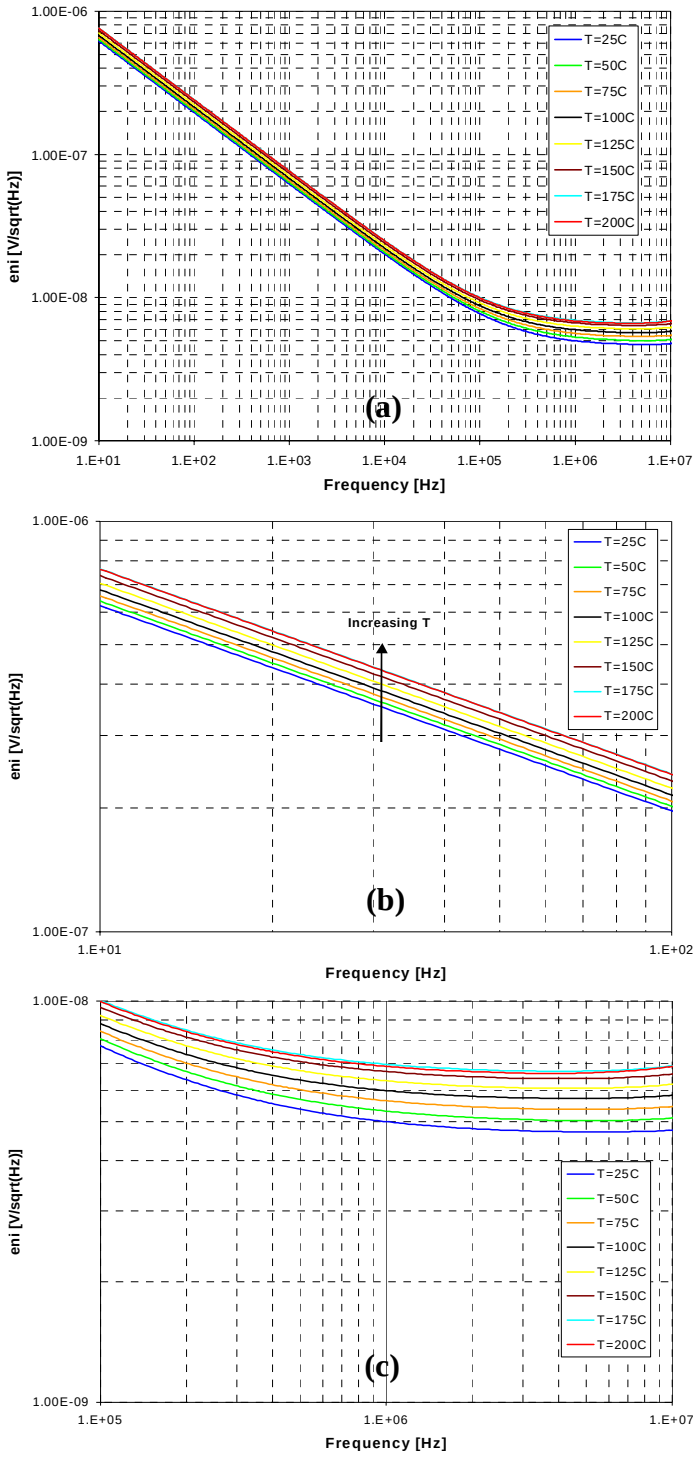


Figure 5.17 Simulated Amp2b input-referred noise vs. temperature (using foundry supplied models). (a) complete curves, (b) flicker noise zoom view, (c) white noise zoom view.

Table 5.9: Simulated integrator opamp noise.

Temperature [° C]	eni white [nV/$\sqrt{Hz}$]	eni flicker @ 1kHz [nV/$\sqrt{Hz}$]
25	4.72	62.4
125	6.07	70.9
150	6.42	73.9
175	6.70	76.8
200	6.63	76.6

5.9 Regenerative Comparator Design & Simulation

A regenerative comparator operating on a 2-phase non-overlapping clock was designed for use in the modulator (see Fig. 5.18). The design is composed of four primary functional modules: an input differential pair (M_1 and M_2), an n-channel flip-flop (M_4 and M_5), a p-channel flip-flop (M_6 and M_7), and an S-R output latch (shown as nand gates). In addition, a number of transistor switches are used to sequence the operation of the comparator. The general topology of the comparator, device sizing recommendations, and complete circuit analysis are described in [214]. Referring to Fig. 5.18, there are three primary time intervals that describe the operation of the comparator. During the interval t_1, the comparator is in a reset state, both flip-flops are forced into a reset state, and a voltage difference proportional to the difference between the input voltages is developed on nodes 1 and 2. During t_3, the n-channel flip-flop is first released and allowed to regenerate during the non-overlapping period between the two clock phases. S1 is then asserted, simul-

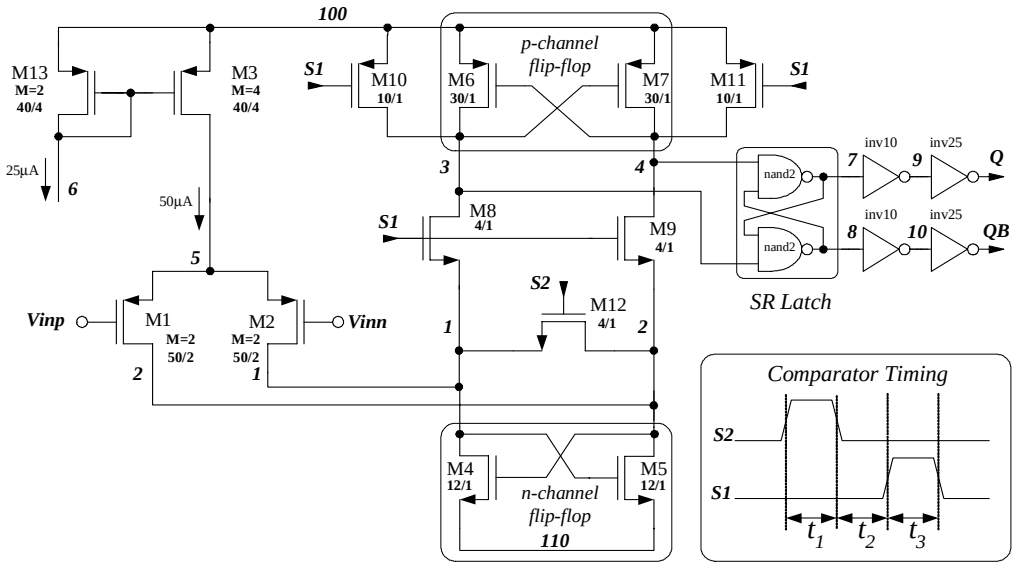


Figure 5.18 Regenerative comparator schematic and timing diagram.

taneously releasing the reset of the p-channel flip-flop and connecting the two flip-flops allowing them to regenerate together, producing voltages on nodes 3 and 4 that are near the supply rails. The SR-latch generates a CMOS-compatible output voltages from the bias on nodes 3 and 4 and maintains these output values during the next reset phase of the comparator (t_1).

The operational specifications of the comparator (primarily gain and offset) are not demanding due to the high gain of the preceding integrator sections in the modulator. The device information for the comparator is shown in Table 5.10. The comparator was simulated at speed from T=25° C to T=200° C with differential input levels of 1mV. The common-mode voltage was 1.65V. The results of these simulations are shown in Figures 5.19 and 5.20 and indicate proper operation at both temperatures. In Figures 5.19 and 5.20, p1

Table 5.10: Regenerative comparator device information.

Reference	Type	Threshold	W/L [μm/μm]
M1,M2	PMOS	Low	100/2
M3	PMOS	Low	160/4
M4,M5	NMOS	Low	12/1
M6,M7	PMOS	Low	30/1
M8,M9	NMOS	Low	4/1
M10,M11	PMOS	Low	10/1
M12	NMOS	Low	4/1
M13	PMOS	Low	80/4

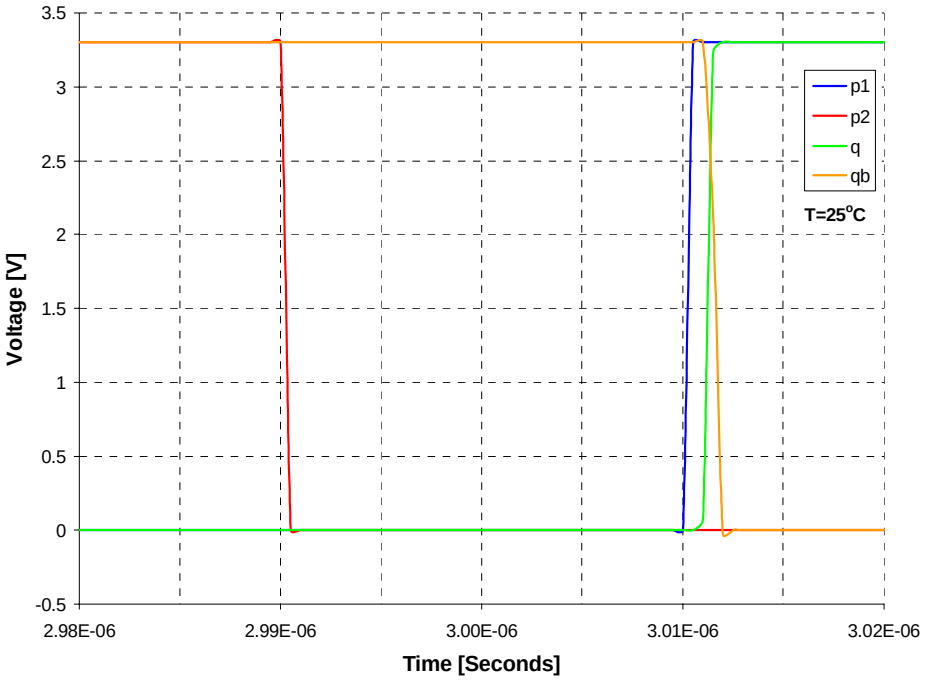


Figure 5.19 Simulated comparator performance at T=25°C (1mV input).

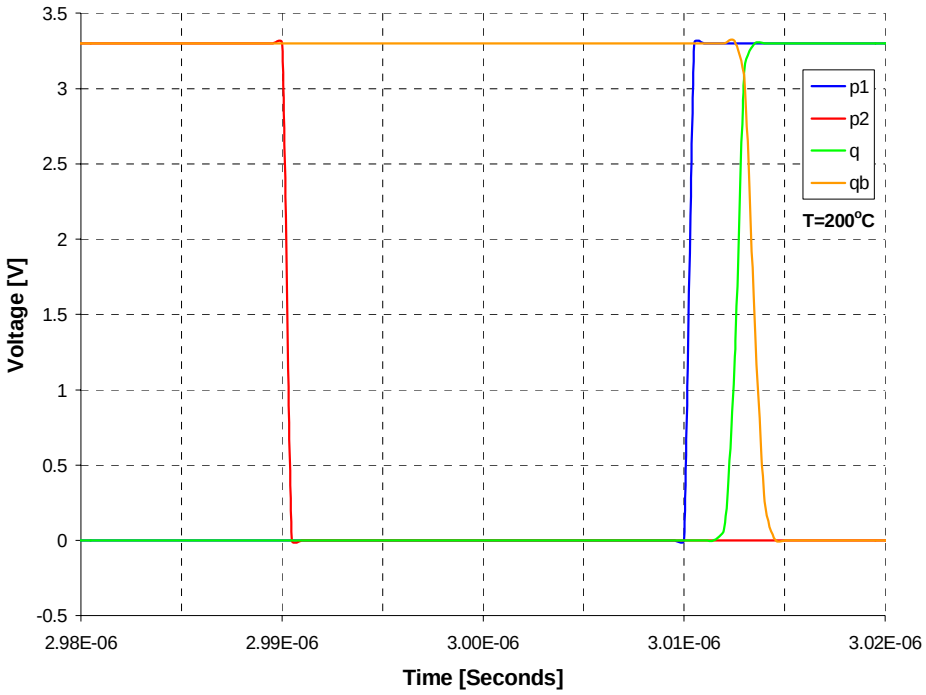


Figure 5.20 Simulated comparator performance at T=200° C (1mV input).

and p2 are the phase1 and phase2 clocks, respectively. In addition, the latched non-inverted and inverted comparator outputs are labeled q and qb, respectively.

5.10 Digital-to-Analog Converter (DAC) Design & Simulation

The error feedback digital-to-analog converter (DAC) circuit is shown in Fig. 5.21. This structure connects the appropriate polarity of the error feedback voltage to its output using low-resistance switches. The buffering of the switch control voltages are designed with appropriate delays to ensure break-before-make operation. HSpice simulations were performed to verify proper operation of the make-before-break delay inverters and the reference switching from T=25° C to T=200° C.

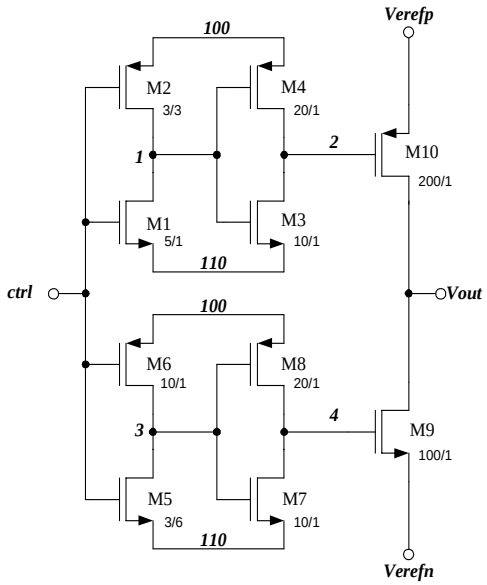


Figure 5.21 DAC circuit diagram with break-before-make switch control.

5.11 Timing Generator Circuits Design & Simulation

Precise timing control of the modulator is accomplished using 2-phase non-overlapping clocks, 2 delayed versions of these non-overlapping clocks, and inverted copies of each for a total of 8 precisely generated clock signals. In an effort to minimize the effect of low-frequency noise, the first integrator stage incorporates a chopper function which requires the addition of another set of 8 clock signals (similar to the regular control clock but at one half the frequency) properly synchronized with the standard modulator control signals. Fig. 5.6 shows the relative timing of these clocks. Only the primary 8 clocks are shown since the remaining clocks are inverted copies. Note that the chopper control clocks transition only during the non-overlapping states of the standard clocks and transition at 1/2 the frequency. Precise generation of these signals is accomplished using the

circuits of Fig. 5.22 and Fig. 5.23. The use of delayed clocking (clocks S_3, S_4, S_{cd}, and S_{dd}) reduces the effect of signal dependant charge injection [106].

Both timing generator circuits are very similar in architecture. A $2xf_s$ clock is input and divided by 2 to produce a 50% duty cycle clock at a frequency of f_s. A nand-feedback structure is used to produce the two primary phases (S_1 & S_2, or S_c & S_d). Each feedback path has an even number of inversions. The delay in the feedback path is generated using properly sized inverter cells that produce the delay between the two non-overlapping phases. Tapping the feedback path is used to produce the various other clocks and inverted clocks. This topology for generating 2-phase non-overlapping clocks is commonly employed in ΣΔ modulators and other switched-capacitor circuits [127,158].

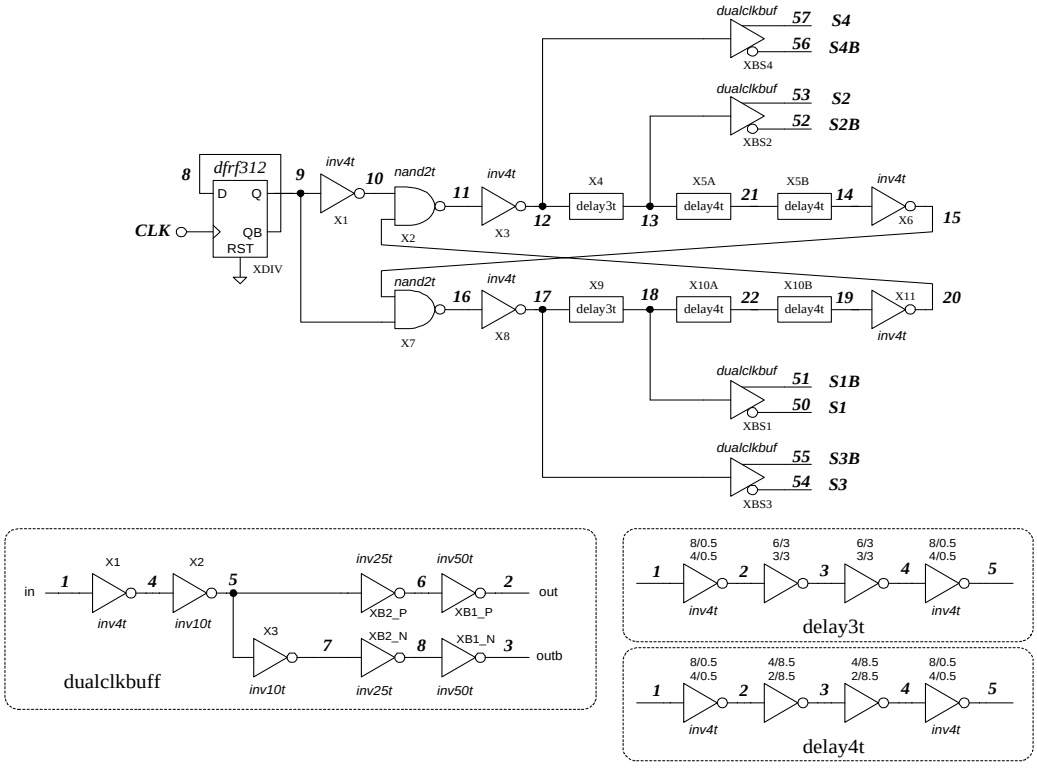


Figure 5.22 2-phase non-overlapping clock generator - standard clocks.

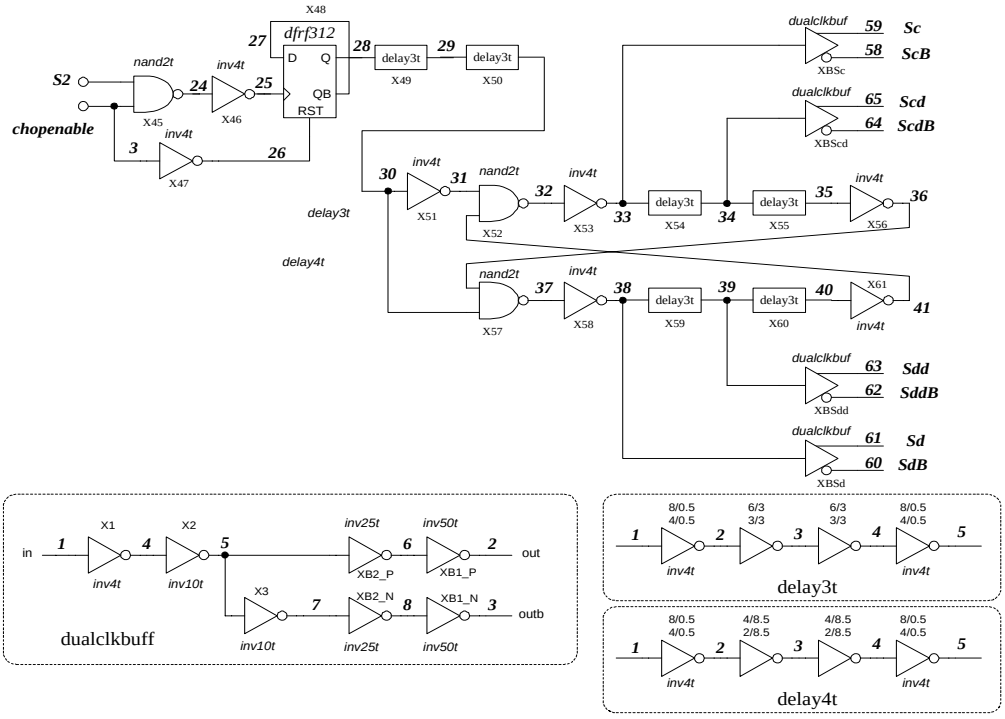


Figure 5.23 2-phase non-overlapping clock generator - chopper clocks.

Simulation results of the timing generator circuits are shown in Figures 5.24 and 5.25 for T=25° C and T=200° C, respectively. Both simulations demonstrate correct operation with increased but acceptable transition delays observed at T=200° C.

5.12 Integrator Switches Design & Simulation

Transmission gates were used for all switches in the modulator and were properly sized to provide similar matched performance of NMOS and PMOS devices (see Fig. 5.26). Dummy devices were used for the NMOS devices and evenly split between the two sides of the switch. The use of complementary switches with dummy devices provided a number of benefits over single device switches: improved cancellation of errors due to switch charge injection and signal feed through, and improved linearity.

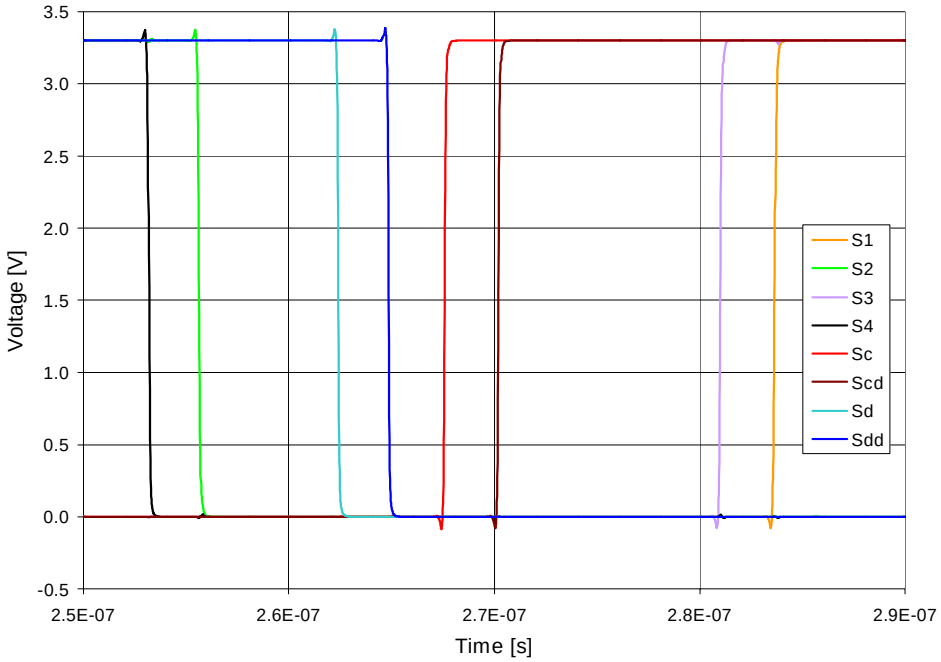


Figure 5.24 Clock generators simulation results at T=25° C.

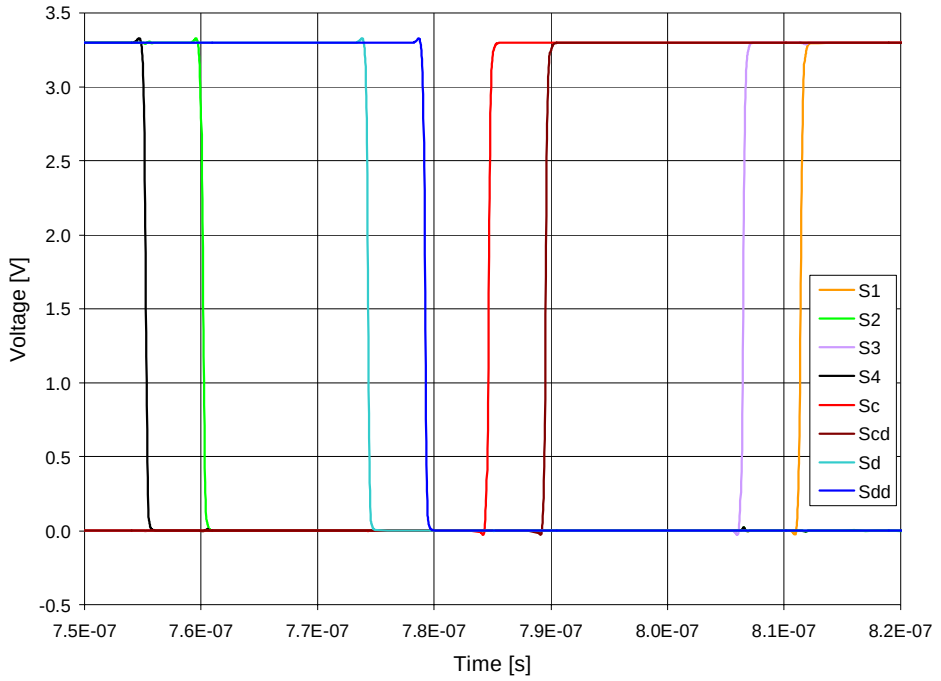


Figure 5.25 Clock generators simulation results at T=200° C.

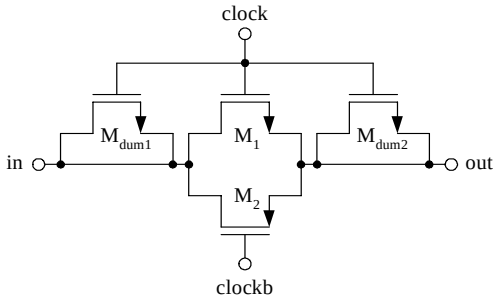
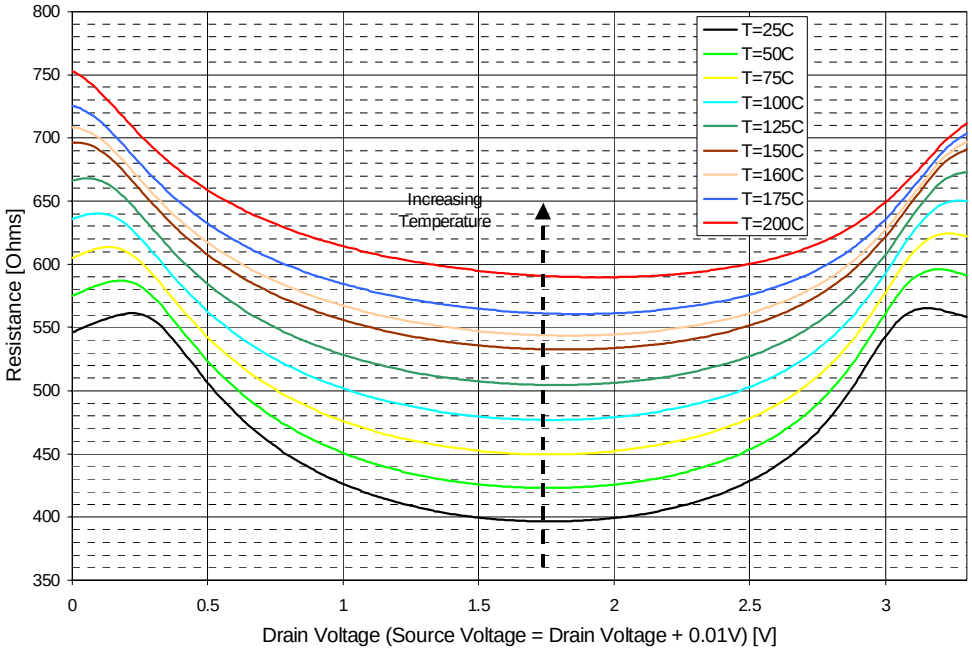


Figure 5.26 Transmission gate switch with dummy devices (tg5, tg10).

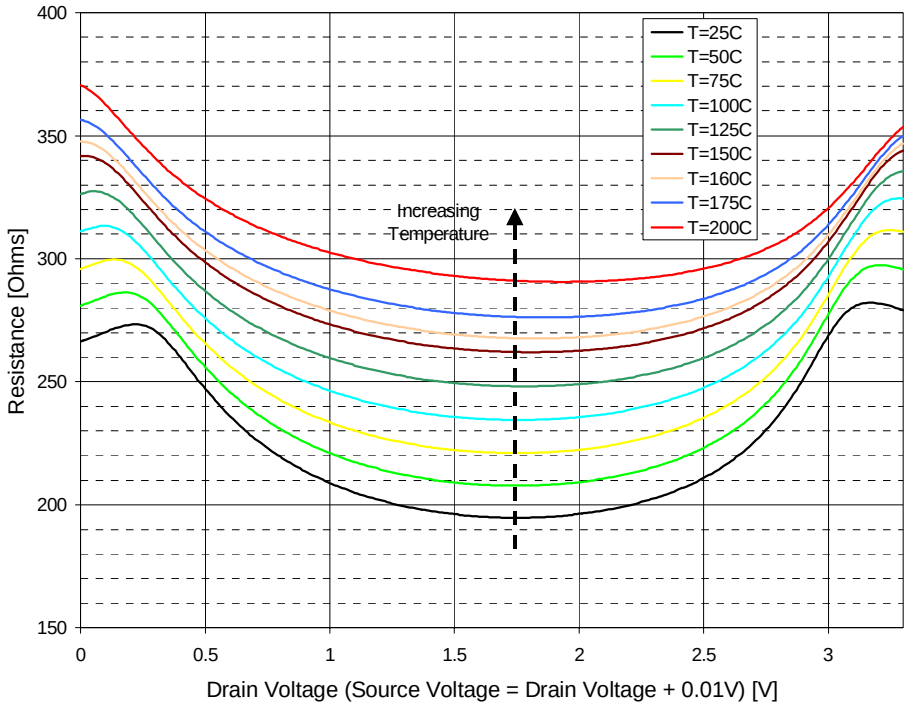
Two different switch designs were used in the modulator: a smaller switch (tg5) for standard integrator switches (operations involving *kT/C* noise), and a larger switch (tg10) for the chopper function. Smaller switches reduce charge injection and signal feed through errors but must have sufficiently low on-resistance to allow adequate settling. In the case of the chopper, the switches are in series with the amplifier inputs, contribute directly to the input noise, and must be sized accordingly. Simulations of the switches on-resistance characteristics are shown in Fig. 5.27 for T=25°C to T=200°C. As expected, the on-resistance of the switches increase with temperature. Note that tg5 has a maximum simulated on-resistance of ~750Ω at T=200°C, resulting in a time constant of ~7.5ns when charging a 10pF capacitor. In addition, the maximum on-resistance of tg10 is ~370Ω, much less than the ~2kΩ anticipated equivalent input thermal noise resistance of the opamp.

5.13 Buffer Amplifier Design & Simulation

A buffer amplifier was incorporated in the modulator design to allow observation of each of the integrator outputs for qualitative assessment of modulator function. The buffers were designed to operate as voltage followers with sufficient bandwidth and input and



(a)



(b)

Figure 5.27 Simulated on-resistance vs. temperature for (a) tg5 and (b) tg10.

output swing to accurately reproduce the integrator output voltages without adding significant load capacitance. The design parameters for this amplifier are shown in Table 5.11.

The 2-stage opamp shown in Fig. 5.28 was designed for this purpose. The device sizes used are summarized in Table 5.12. Simulations of the amplifier with a load capacitance of 20pF were carried out from T=25°C to T=200°C. The simulated open loop characteristics of the amplifier are shown in Figures 5.29 and 5.30.

The simulated performance of the amplifier as a voltage follower with the expected full-scale input in the modulator application is shown in Fig. 5.31. A summary of simulation results is listed in given in Table 5.13. These results indicate acceptable performance for the intended purpose of qualitative monitoring.

5.14 Modulator Bias Cells

Two bias cells were designed to provide the bias current required for each of the 2^{nd}-order single-loop modulators. These cells each multiply a single bias current generated using an off-chip resistor - one for the integrator opamps, and another for the integrator buffer opamps. Schematics of these two bias cells are shown in Fig. 5.32.

Table 5.11: Integrator buffer amplifier target specifications.

Design Parameter	Abbreviation	Target Value
Open Loop DC Gain	Aol	>200 V/V
Gain Bandwidth	GBW	5 MHz
Slew Rate	SR	4V/μs
Output Swing	OS	1.65V +- 1V
Input Dynamic Range	IDR	1.65V +- 1V

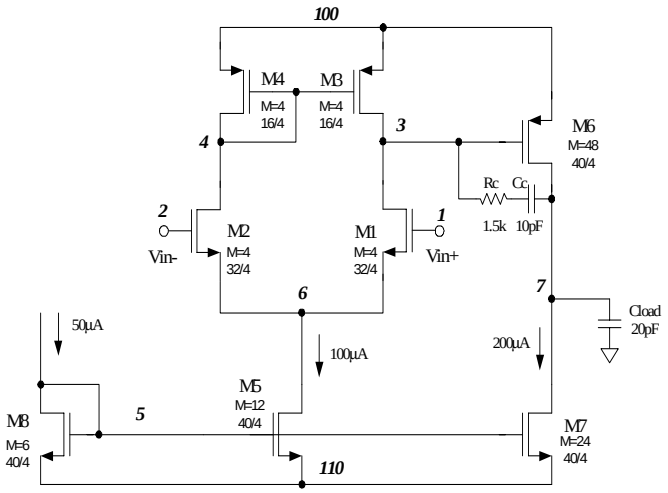


Figure 5.28 Buffer amplifier used for observing integrator outputs.

Table 5.12: Buffer amplifier device information.

Reference	Type	Threshold	W/L [µm/µm]
M1,M2	NMOS	Low	128/4
M3,M4	PMOS	Low	64/4
M5	NMOS	Low	480/4
M6	PMOS	Low	1920/4
M7	NMOS	Low	960/4
M8	NMOS	Low	240/4

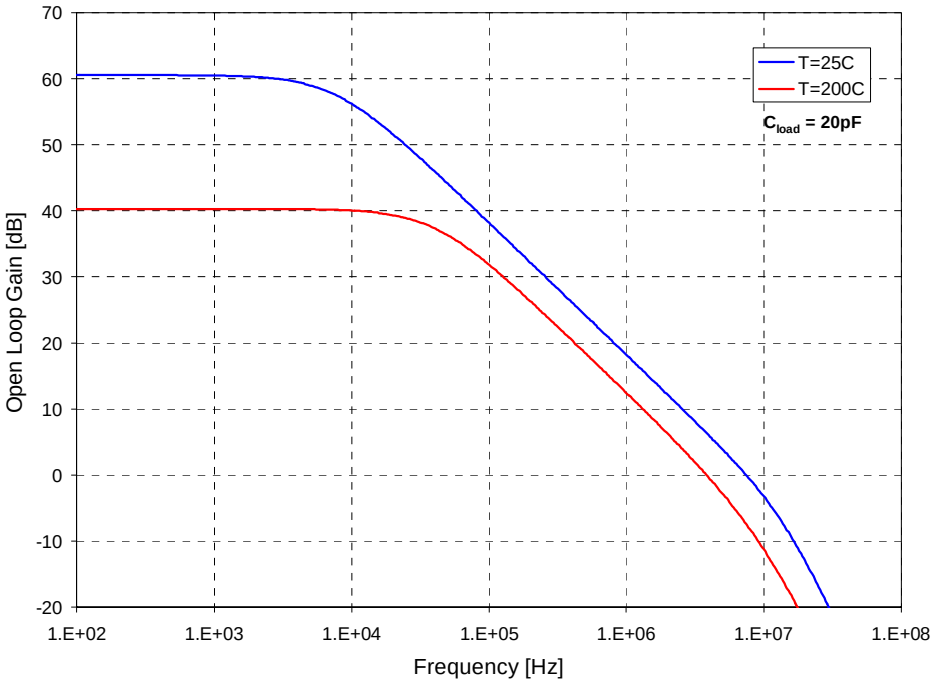


Figure 5.29 Simulated buffer amplifier open loop gain vs. temperature.

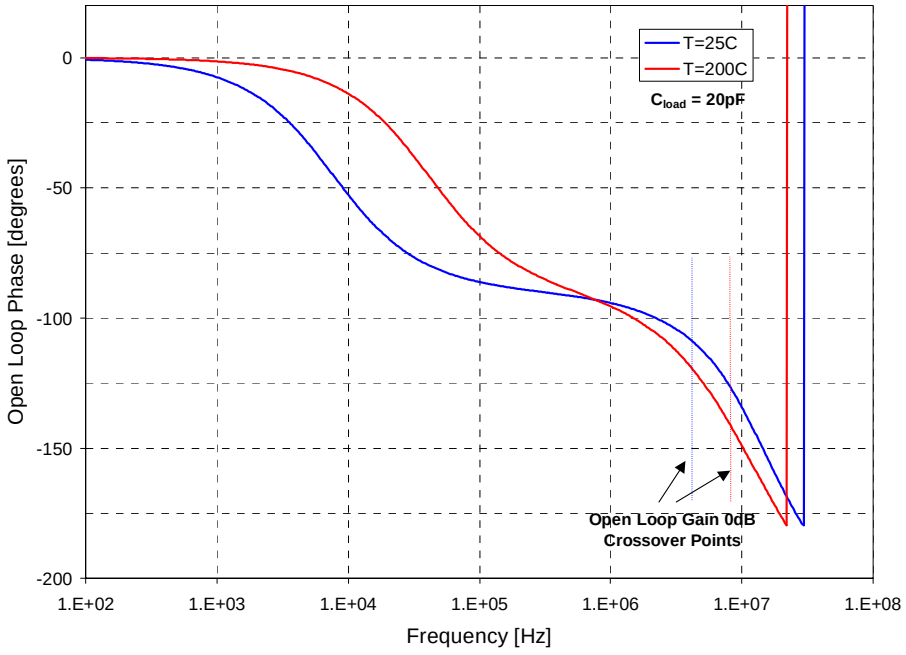


Figure 5.30 Simulated buffer amplifier open loop phase vs. temperature.

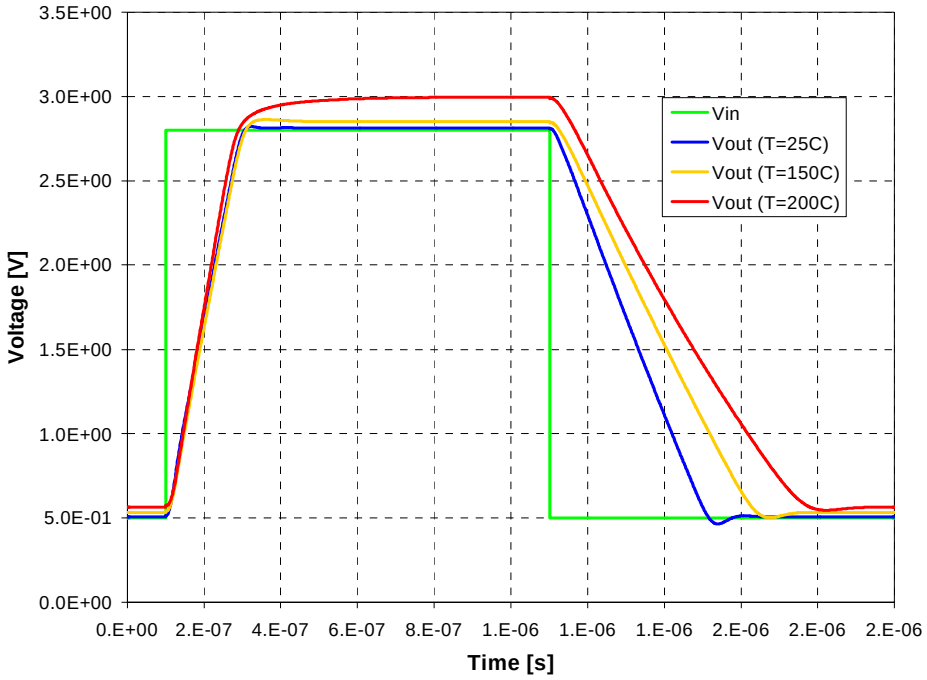


Figure 5.31 Buffer amplifier output characteristics vs. temperature.

Table 5.13: Buffer amplifier simulation summary vs. temperature.

Temp. [° C]	**Aol [dB]**	**GBW [MHz]**	**Phase Margin [°]**	**Slew Rate (pos / neg)** [V/μs]	**Power Consumption** [mW]
25	60.57	7.44	56.6	11.1 / 5.6	1.41
150	---	---	---	11.9 / 4.6	---
200	40.29	3.83	62.8	13.4 / 4.2	1.47

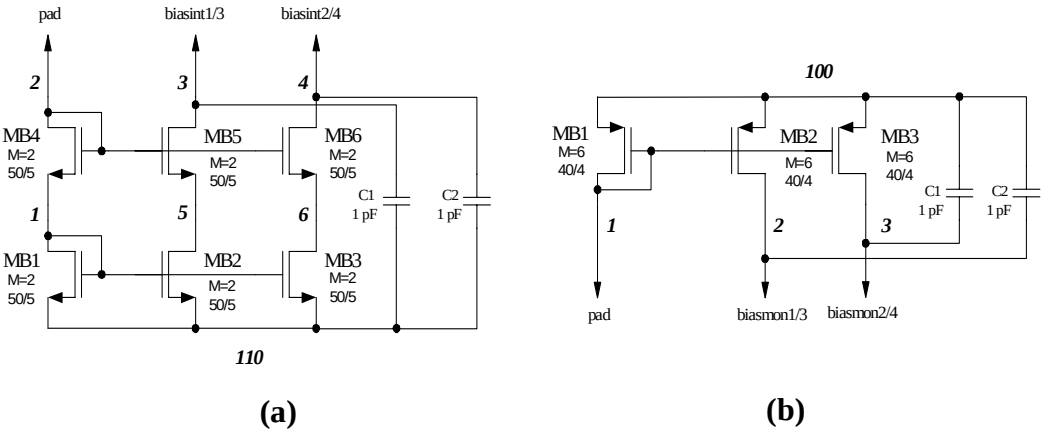


Figure 5.32 Bias cells. (a) integrator opamp, and (b) integrator buffer opamp.

5.15 Switched-Capacitor 2-2c Cascade Modulator

A complete design of the 2-2c modulator architecture of Fig. 5.2 was performed using the building blocks described in previous sections and is shown in Fig. 5.33. The first integrator incorporates a chopper for low-frequency noise reduction. Using both an over-sampling ratio of 256 and the same opamp design and capacitor values in all of the integrators ensures insignificant noise contribution from the 2^{nd}, 3^{rd}, and 4^{th} integrators. The consequences of this decision are increased modulator power consumption and increased layout area.

A simulation model of the modulator was constructed incrementally starting with each of the integrators (standard and chopper), and building first a single 2^{nd}-order modulator and then combining two loops into a cascaded 2-2c modulator. Complete simulations in HSpice of the 2-2c cascaded modulator including all bias generators and clock generators were performed using Level 49 foundry-supplied models at 25°C and 200°C. Entire

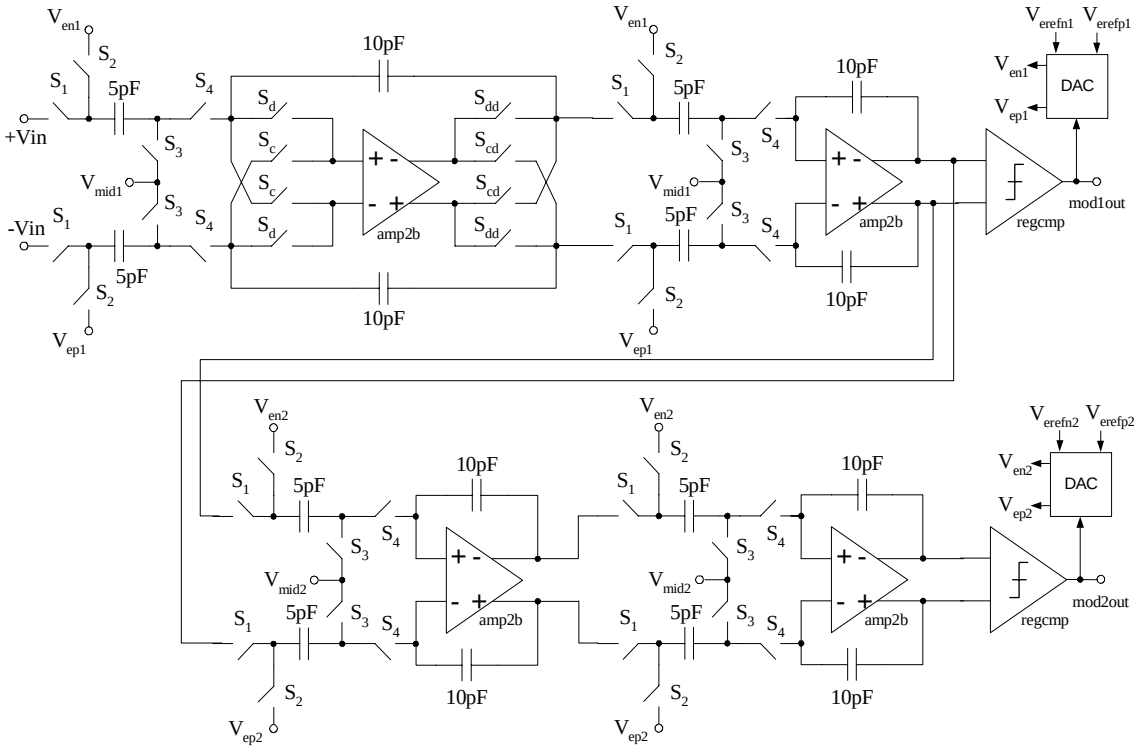


Figure 5.33 Switched capacitor 2-2c cascaded modulator block diagram.

modulator simulations using HSpice require massive computing resources. Consequently, modulator simulations were performed only to obtain sufficient results for bias verification and transient operation showing stable operation, adequate slewing capability, and gross settling behavior. Simulations exceeding 100 sample cycles were not performed allowing no spectral analysis to be performed using the HSPICE output data. Simulation results obtained using the extracted chip layout are shown in Fig. 5.34 and Fig. 5.35 for T=25° C and T=200° C, respectively. In both cases a one-half of full-scale dc input is applied and the chopper is enabled. The differential output of each of the integrators is marked inx and ipx, where *n* and *p* denote the polarity of the output and *x* represents the integrator reference number (1-4). These results indicate stable modulator performance

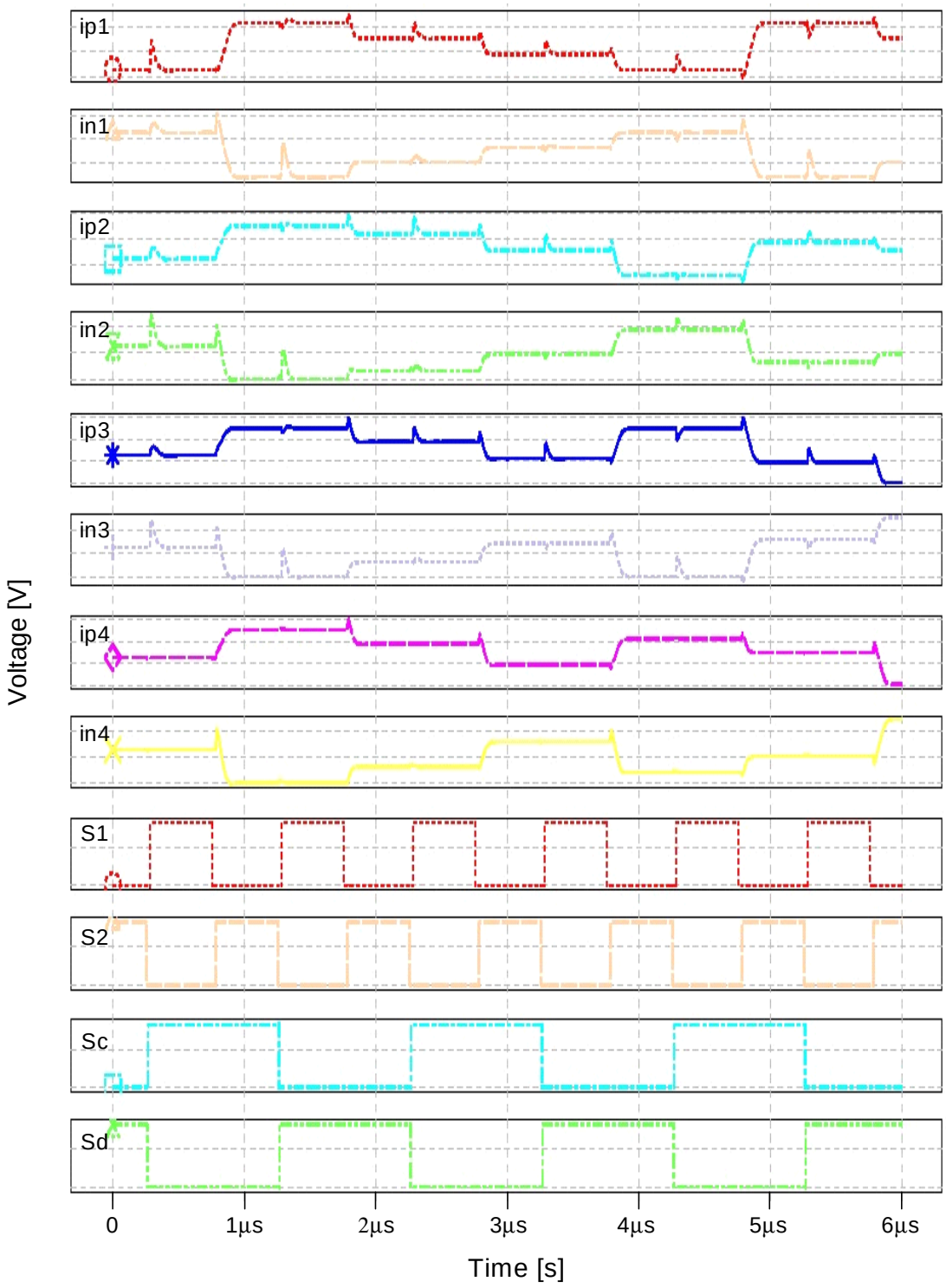


Figure 5.34 Simulation results of modulator layout extraction showing integrator outputs and integrator clocks (T=25° C).

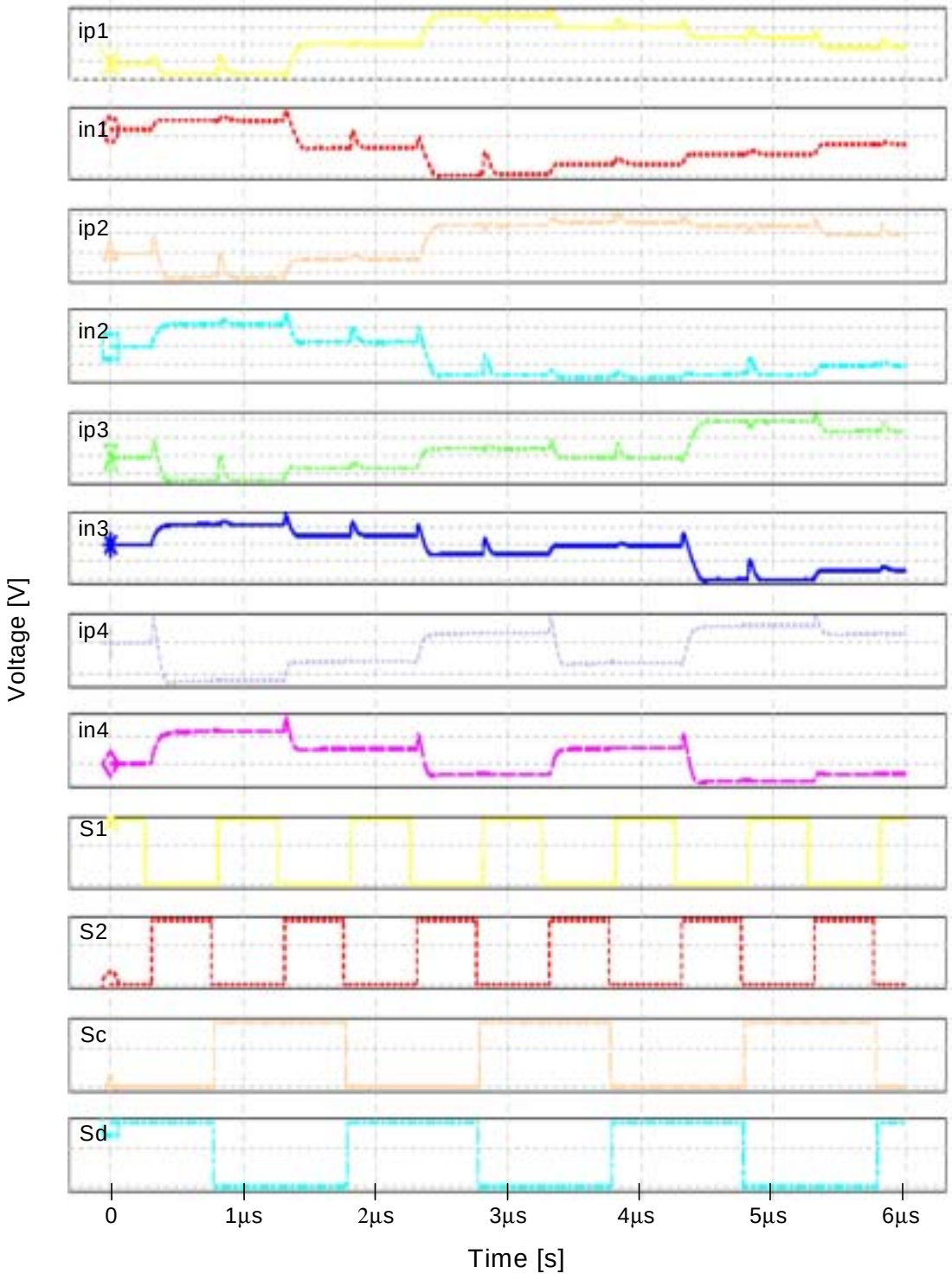


Figure 5.35 Simulation results of modulator layout extraction showing integrator outputs and integrator clocks (T=200° C).

and show reasonable qualitative performance in terms of output swing, and settling and slewing behavior. As will be demonstrated in Chapter 7, detailed performance evaluation of a ΣΔ modulator requires a large sampling of data and complex digital signal processing.

5.16 Summary

This chapter has provided a detailed description of the approach taken in the design of a 2-2c cascade modulator. Functional building block designs were described and simulation results showing adequate performance over temperature were presented. Test results of these blocks and the overall modulator fabricated in 0.5μm SOS are provided in following chapters.

CHAPTER 6

MODULATOR COMPONENT MEASUREMENT RESULTS

A test ASIC was fabricated in a 0.5µm SOS CMOS process incorporating the modulator building blocks: the integrator opamp (amp2b), comparator (regcmp), digital-to-analog converter (dacmodh), and the two switch modules (tg5, tg10) used in the switched capacitor integrators. Limited testing was performed on these blocks over a temperature range of 25°C to 200°C. Special attention was taken in testing the integrator opamp because of its relative importance to overall modulator performance.

In this chapter an overview of the component testing and results is presented including details of the test hardware and method of data collection. Test results are compared to the simulation results of Chapter 5 where appropriate. Finally, the suitability of the foundry-supplied simulation models for use over wide temperature ranges is evaluated.

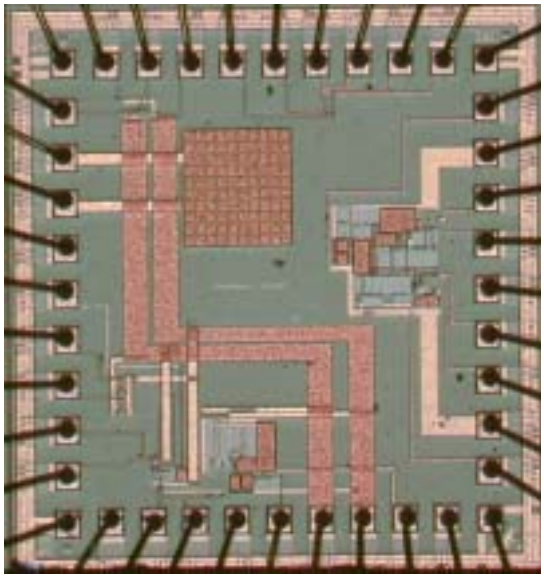


Figure 6.1 Micro-photograph of sdmod4_parts2 test chip.

6.1 Test Method Summary

A generic test board was designed to facilitate testing of the modulator components test ASIC (sdmod4_parts2). The board was equipped with sufficient flexibility to allow connectivity to all of the circuit blocks and to allow configurability for separate characterization. The goal was to produce a single PCB design and populate copies of the design for each specific test setup. With this goal in mind, the board was partitioned into three primary modules that could be kept as a single unit or physically separated and used independently: a single-ended to differential converter, the sdmod4_part2 fixture, and a differential to single-ended converter. Each has separate supply connections, supply filtering, and footprints for I/O connectors. A partitioned test board schematic is shown in Figures 6.2 and 6.3. The partitioning shown in these figures is the only practical configuration used in testing since the differential to single-ended converter cannot be separated from the integrator amplifier due to the latter's inability to drive significant cabling capacitance. The single-ended to differential converter circuit is based on the Analog Devices AD8138 and allows adjustment of the output common mode signal and individual output offset control. This provides means for compensating for offset voltage errors associated with both the AD8138 output and the Amp2b input stage. The differential to single-ended converter circuit was based on the Analog Devices AD8130, having a 300MHz bandwidth and capable of driving a 50 ohm load. Use of this configuration allows testing the fully differential amplifier with common test equipment having only single-ended measurement capability.

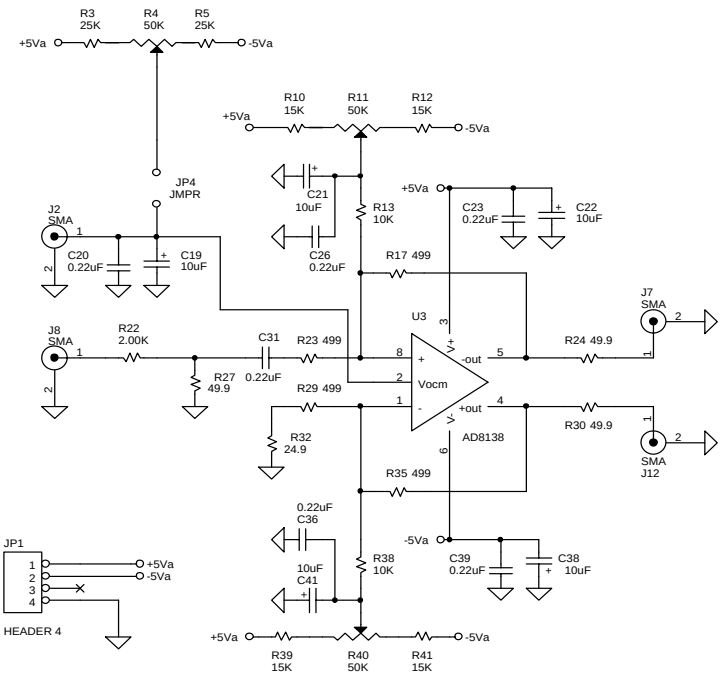


Figure 6.2 Modulator components test PCB schematic - part A.

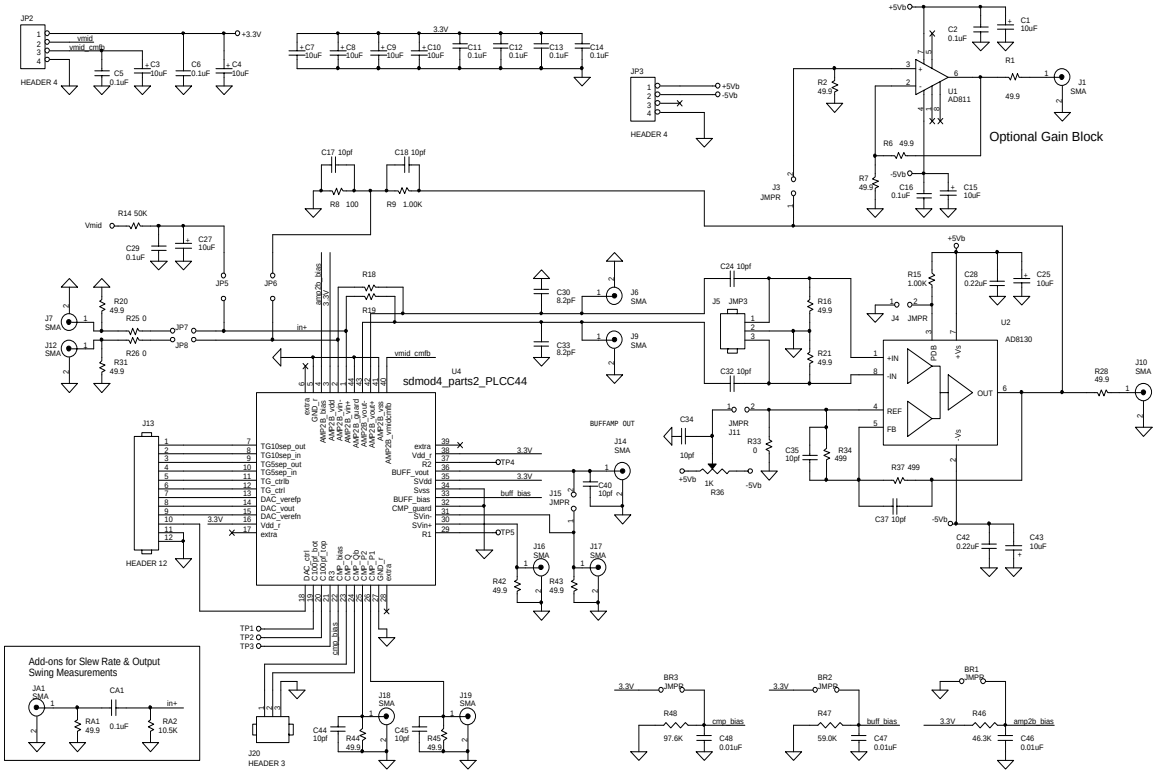


Figure 6.3 Modulator components test PCB schematic - part B.

Figure 6.4 Photograph of modulator components test PCB.

The PCB was fabricated using polyimide board material which is rated for operation up to 225°C. High temperature solder and teflon jacketed connection wires were used to ensure reliable testing at elevated temperatures. A photograph of the test PCB is shown in Fig. 6.4.

6.2 Integrator Opamp Measurements

Thorough testing was performed on the integrator opamp (Amp2b) to verify suitability for use in the switched capacitor integrator. The tests performed are summarized in Table 6.1. A load capacitance of 8.25pF was placed at each of the integrator outputs. By making differential slew rate measurements the equivalent load capacitance of the PCB and buffer was determined to be approximately 15pF. The addition of 8.25pF produced a composite load capacitance of ~ 23pF, which is approximately the expected capacitive

Table 6.1: Amp2b measurement summary.

Test Performed	Measured Parameters	Test Condition Notes
Open Loop	DC gain, 3dB frequency, gain bandwidth product	Versus ibias (T=25°C) Versus T (ibias=50μA) Cload ~ 20pF
Closed Loop	Slew rate, output swing	Versus ibias (T=25°C) Versus T (ibias=50μA) Cload ~ 20pF
Noise	input-referred noise voltage spectral density	ibias=50μA, T=25°C

load in the integrated circuit modulator. Open loop tests were performed as a function of bias current (at T=25°C) and as a function of temperature with fixed bias (Ibias=50μA). The block diagram of the test circuit is shown in Fig. 6.5. Due to the high loop gain of the amplifier, special layout of the PCB and cabling of the system was necessary. The single-ended to differential converter circuit was separated from the rest of the test board and placed in a steel enclosure for shielding. The remainder of the test board was placed in an oven for testing over a temperature range of 25°C to 200°C. For each parameter change (chip, temperature, bias) the offset adjust of the AD8138 was adjusted such that the outputs of the Amp2b remained at a common-mode voltage near 1.65V. The AD8138 circuit being separated and maintained at room temperature eliminated temperature dependant offset drifts and allowed standard components and solder materials to be used in its construction. The amplifier was connected to an HP 5389A Network Analyzer used to sweep the input signal frequency and measure the output magnitude and phase. At each temperature, the amplifier was removed from the PCB, bypassed, and a calibration was per-

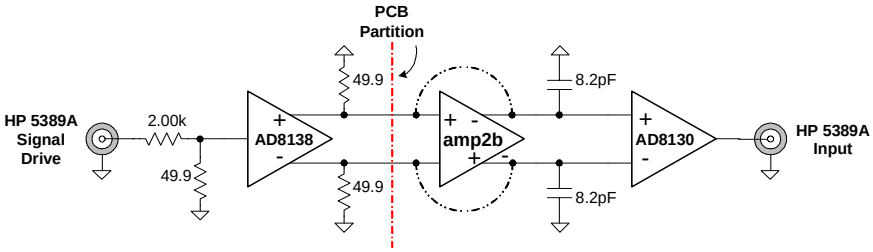


Figure 6.5 Amp2b open loop measurement block diagram.

formed with the rest of the circuits in place for a baseline correction. Data was collected, retrieved from the analyzer using a LabView-based program and the instrument GPIB port, and stored in spreadsheet format for importing into Microsoft Excel.

6.2.1 Open Loop Gain - Fixed Temperature & Variable Bias

Due to the added difficulty of performing measurements on real devices as compared to running simulations, only a subset of the simulations in Chapter 5 are compared to measured data. First, loop gain measurements were made at room temperature for a number of different bias conditions. The measured loop gain as a function of bias current is shown in Fig. 6.6 (for T=25° C). The variation of the dc gain and 3dB frequency with bias current can be seen in the zoomed view of Fig. 6.7. The dc gain values measured for 4 chips are shown plotted as a function of bias current in Fig. 6.8. The gain bandwidth as a function of bias current was extracted from the measured data for chip 3 and is shown in Fig. 6.9.

The results of these measurements that focus on bias current dependencies at room temperature are summarized in Table 6.2. As was indicated by simulations, the selected bias current of 50μA produces near maximum open loop gain and reasonable gain bandwidth.

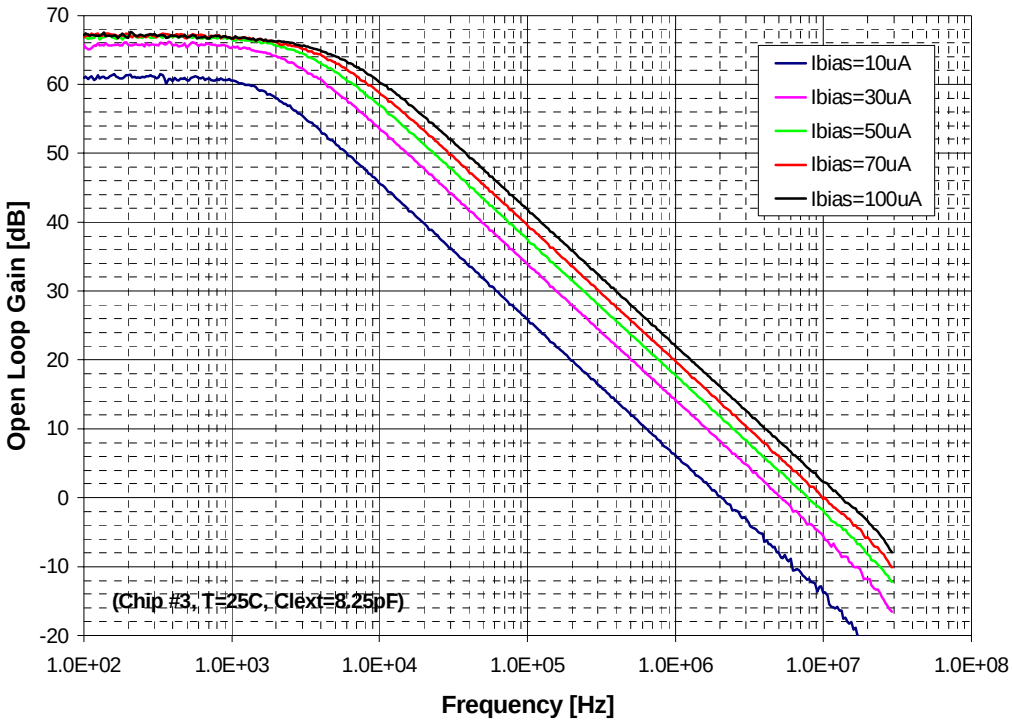


Figure 6.6 Measured Amp2b open loop response vs. bias current (T=25°C).

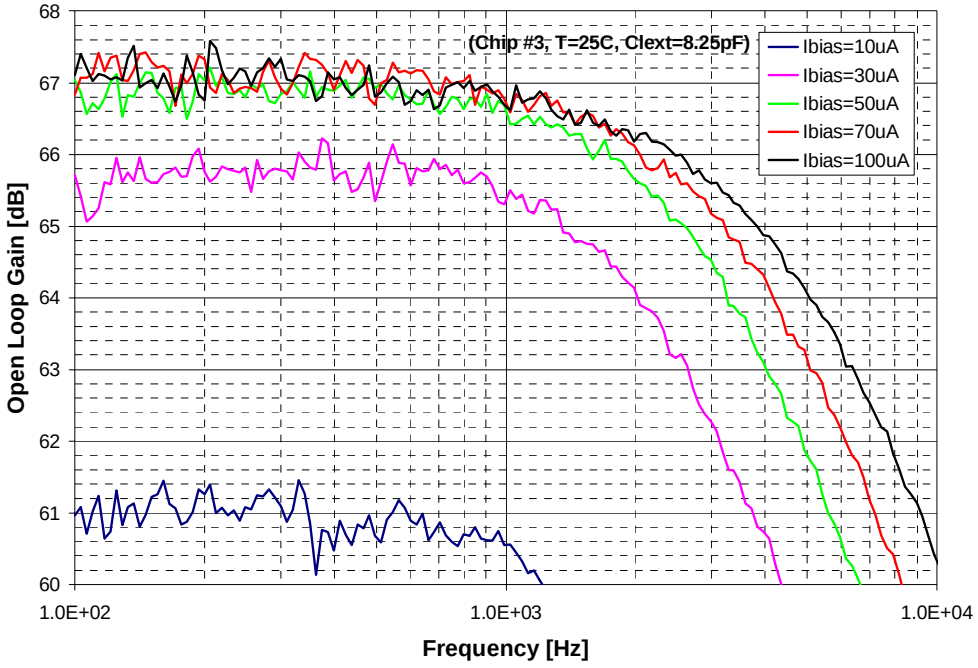


Figure 6.7 Measured Amp2b open loop response vs. bias current (T=25°C).

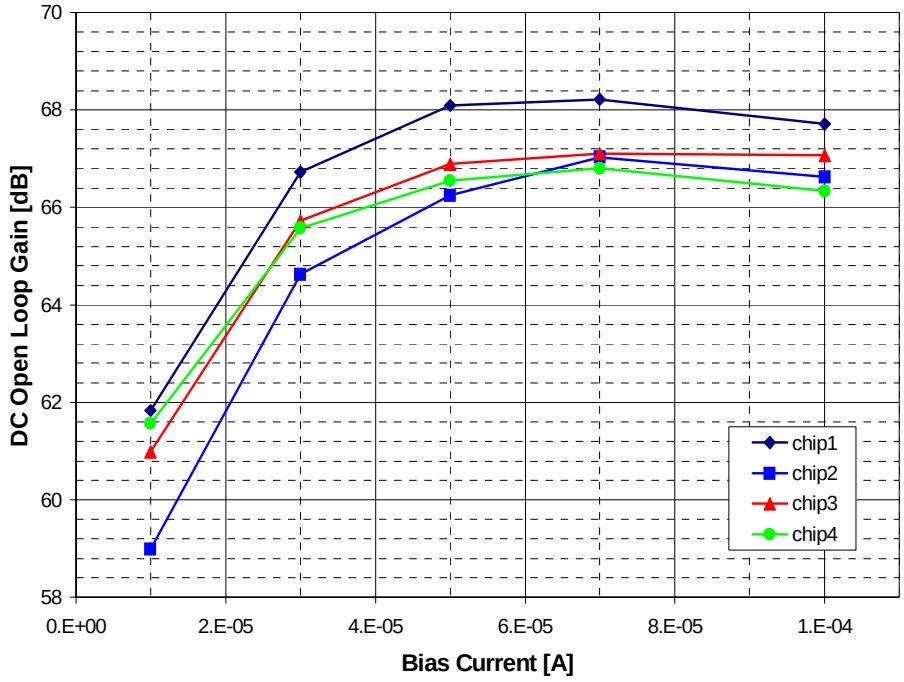


Figure 6.8 Measured Amp2b dc open loop gain vs. bias current (T=25°C).

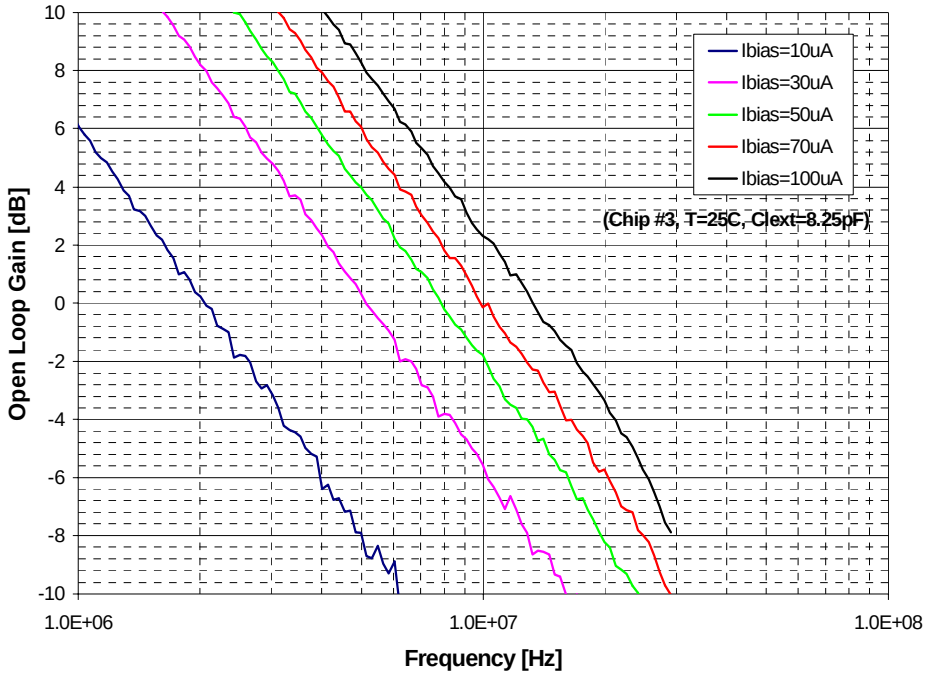


Figure 6.9 Measured Amp2b 0dB crossover vs. bias current (T=25°C).

Table 6.2: Measured Amp2b Aol & GBW vs. Ibias (T=25°C, chip 3).

Ibias [μA]	**Aol [dB]**	**GBW [MHz]**
10	60.99	2.04
30	65.73	5.30
50	**66.89**	**7.85**
70	67.11	9.80
90	67.07	13.2

6.2.2 Open Loop Gain - Fixed Bias & Variable Temperature

Additional integrator opamp measurements were made with fixed bias current over a range of temperatures (Ibias=50μA). Fig. 6.10 shows the measured open loop gain over a temperature range of 25°C to 200°C. A zoomed view showing the low frequency loop gain and dominant pole is presented in Fig. 6.11. For comparison, the dc loop gain was measured as a function of temperature for 3 chips and is shown in Fig. 6.12. The minimum measured values at 25°C and 200°C were 66.4dB (2089 V/V) and 60.4dB (1047 V/V), respectively. The zero crossover frequency as a function of temperature for a single chip is shown in Fig. 6.13. In addition to the open loop characteristics, the large signal transient response for the amplifier was also measured as a function of temperature. The amplifier was configured for a gain of 10 and a sufficiently large square wave was input to cause clipping at the output. The measured waveforms showing the output swing versus temperature are presented in Fig. 6.14. These plots show very little change in the maximum output swing as a function of temperature.

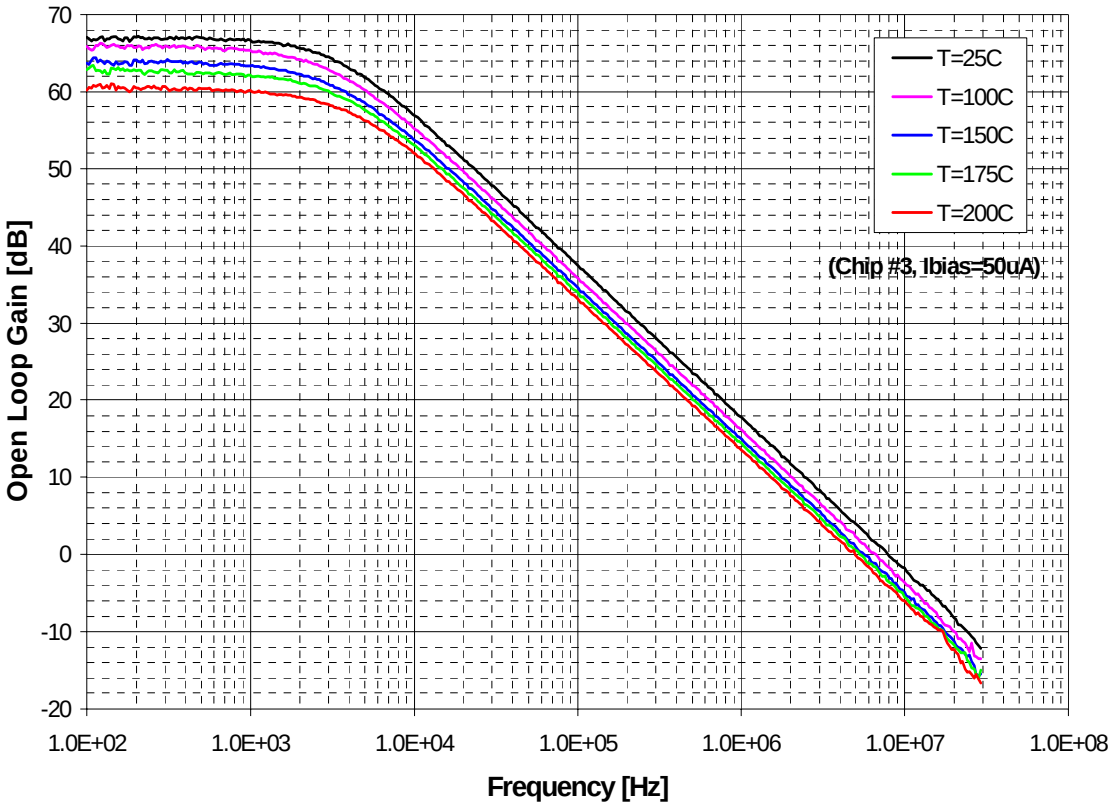


Figure 6.10 Measured Amp2b open loop characteristics vs. temperature.

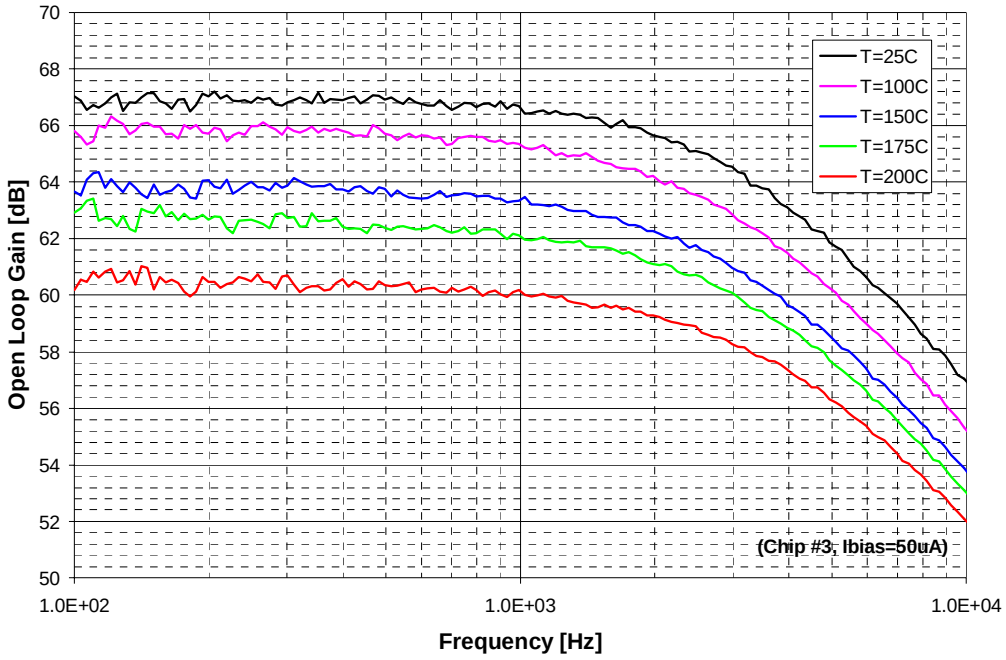


Figure 6.11 Measured Amp2b open loop dc gain vs. temperature (zoom view).

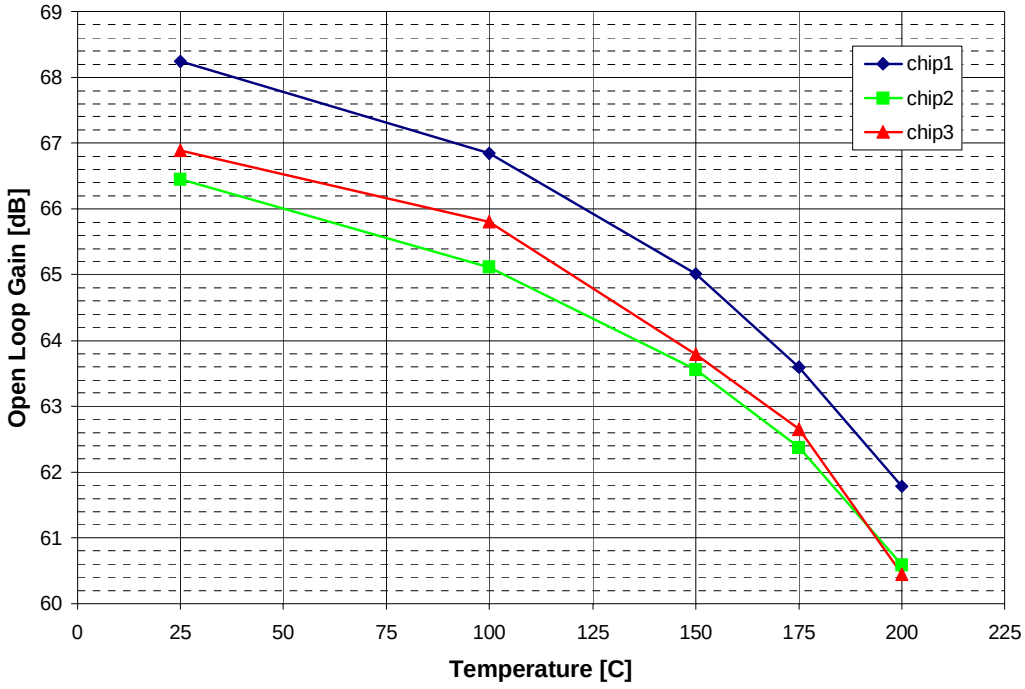


Figure 6.12 Measured Amp2b open loop dc gain in dB vs. temperature.

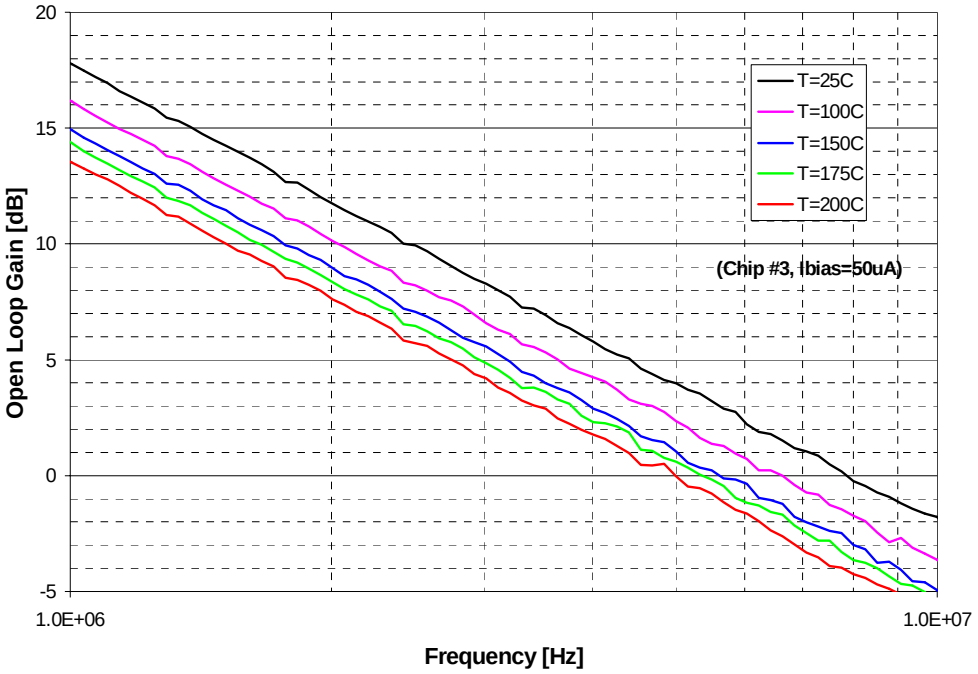


Figure 6.13 Measured Amp2b 0dB crossover vs. temperature (ibias=50μA).

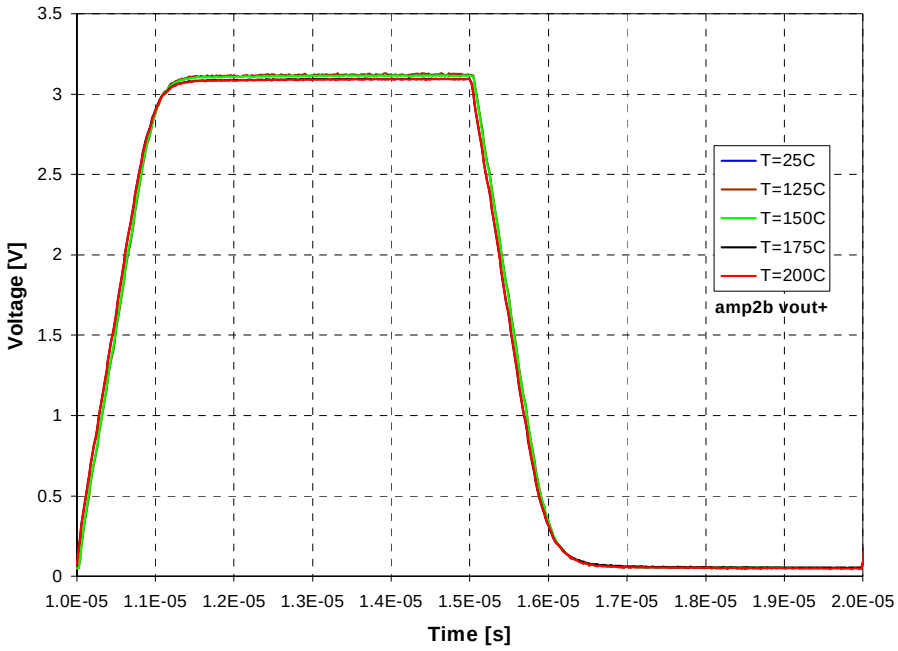


Figure 6.14 Measured Amp2b output swing.

The output slewing behavior of the amplifier is shown in Figures 6.15 and 6.16 for negative and positive transitions, respectively.

6.2.3 Noise Measurements

The noise of the amplifier was measured using the test setup shown in Fig. 6.17 A closed loop gain of 2 was used to balance maintaining high bandwidth and achieving some noise gain to raise the amplifier noise above that of the test circuit. An additional amplifier was placed following the test PCB for additional gain. Care was taken to keep the noise contribution of this amplifier low by appropriate opamp and gain resistor selection. This amplifier produced a voltage gain of approximately 200 with a 3dB frequency of ~15 MHz (see Fig. 6.18). An HP5389A Spectrum/Network Analyzer was used to measure the output noise spectral density of the amplifier. The analyzer was controlled via GPIB using a custom PC-based LabView program. Details of this noise measurement system are provided in Appendix A. Using this approach, the Amp2b output noise was measured as a function of bias current, input referred by the system gain, and is shown in Fig. 6.19 (for T=25°C). The measured input-referred noise (eni) for 2 separate amplifiers at a bias current of 50μA and T=25°C is presented in Fig. 6.20. The foundry supplied noise models produced simulation results much different than measured. In order to improve the models, a number of device noise measurements were made and a set of improved models produced. Simulation results produced using the improved noise models are shown in Fig. 6.20 and demonstrate excellent agreement with measured data, particularly in the lower frequency decades of most concern in this research. Details of the device noise measurement and fitting are provided in Appendix A. Both Fig. 6.19 and Fig. 6.20 show the mea-

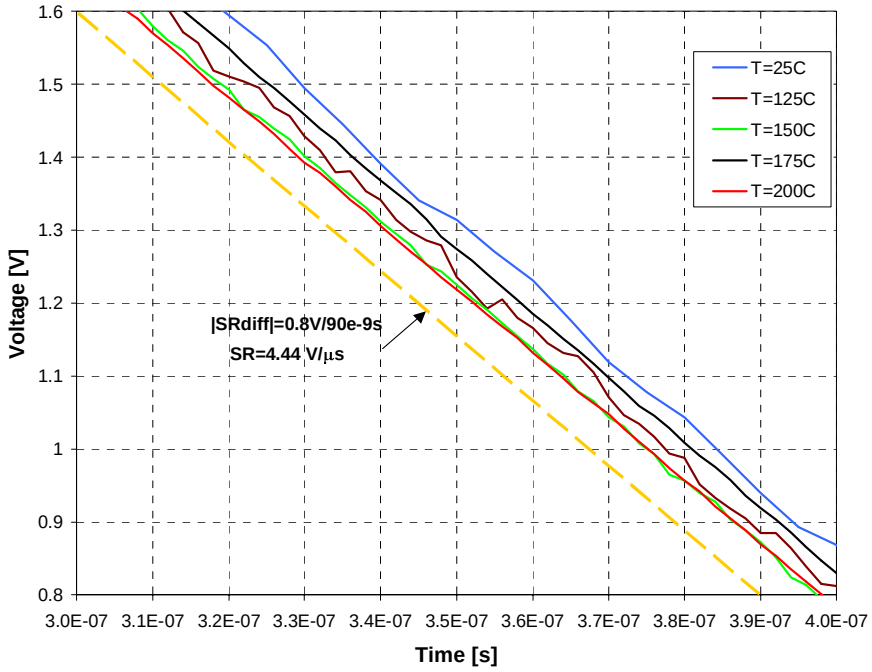


Figure 6.15 Measured Amp2b differential slew rate vs. temperature (neg. transition).

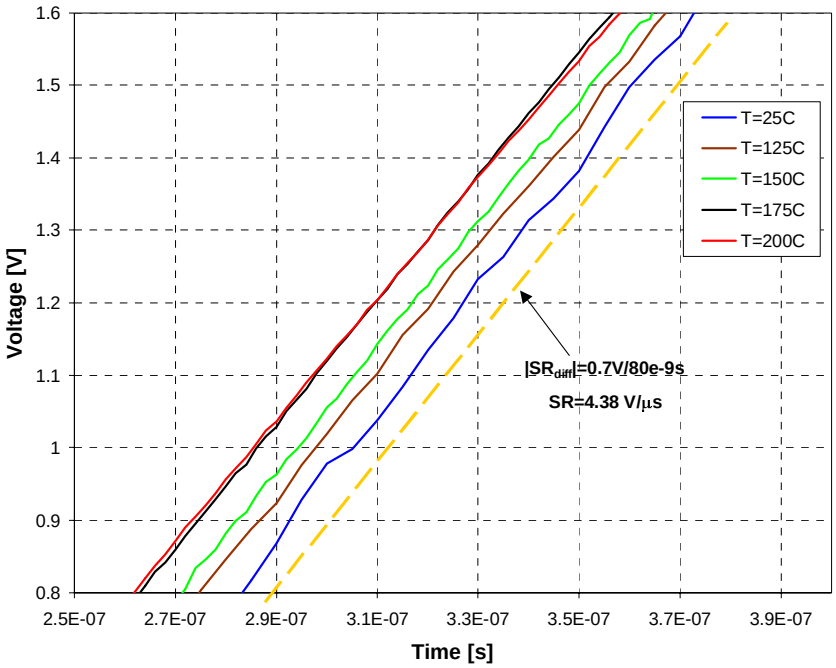


Figure 6.16 Measured Amp2b differential slew rate vs. temperature (pos. transition).

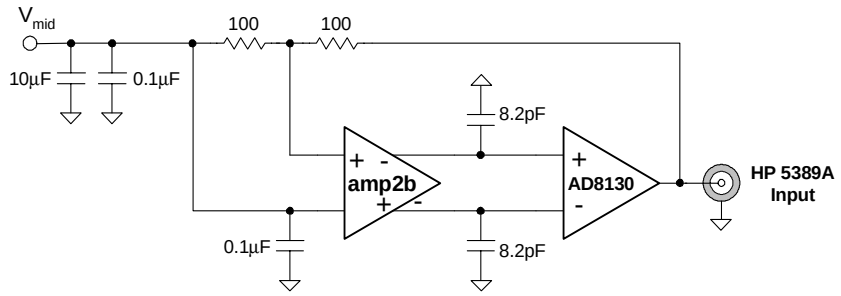


Figure 6.17 Amp2b noise measurement setup.

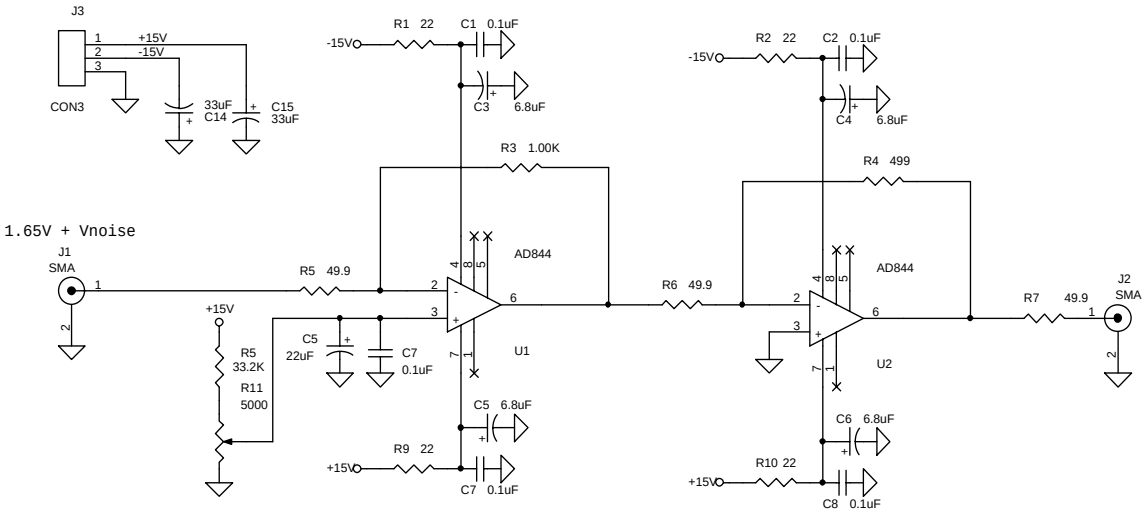


Figure 6.18 Amplifier used for noise measurement.

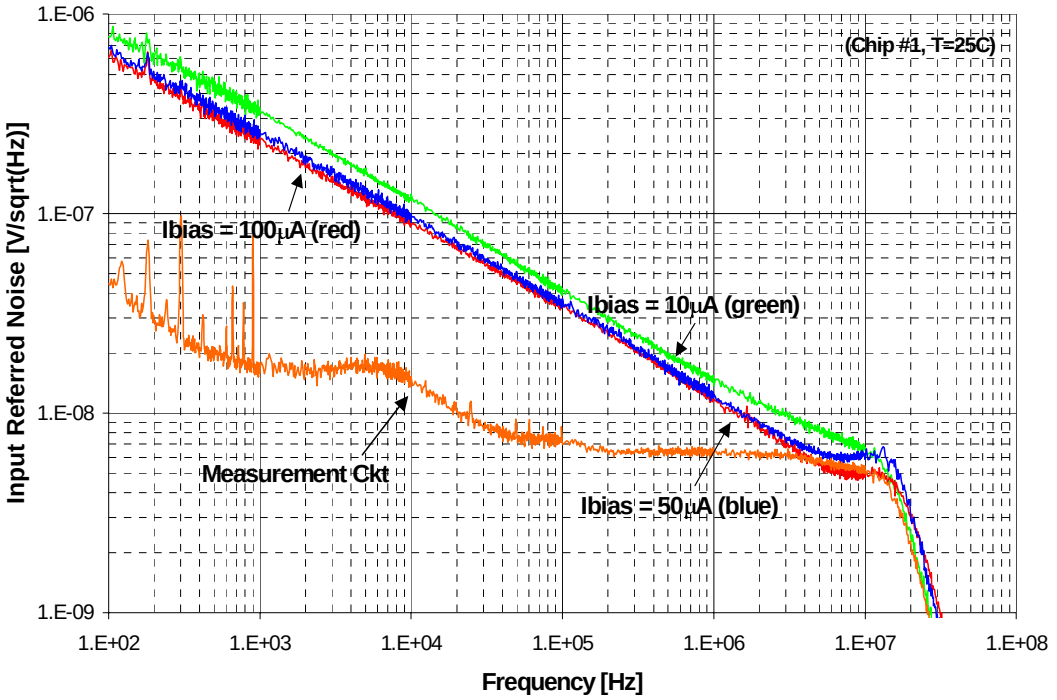


Figure 6.19 Measured Amp2b input-referred noise vs. bias current, T=25° C).

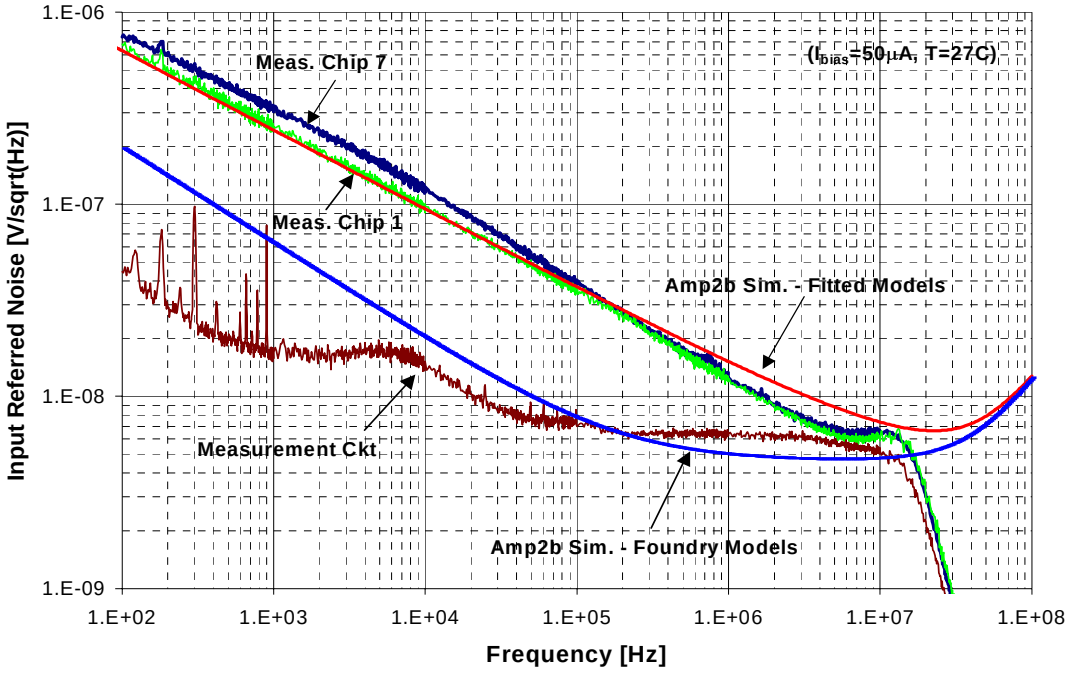


Figure 6.20 Measured and simulated Amp2b input-referred noise (ibias=50μA, T=25° C).

sured test circuit noise where the device under test was removed, and the inputs to AD8130 each terminated with 50Ω. Note that all of the noise measurements performed focus primarily on the lower frequency decades where flicker noise is dominant. However, the input referred noise measurement plots indicate that the high frequency rolloff of the amplifier/gain stage occurs just after the noise corner allowing at least an approximate value of the white noise to be obtained. A summary of the noise measurements is presented in Table 6.3.

6.2.4 Measurement Summary

A summary of results from tests performed on the integrator amplifier over a range of temperatures is given in Table 6.4. Comparing to the target specifications for this amplifier, most of the measured specifications meet the design requirements. The measured loop gain dropped from 2238 V/V at 25°C to 1023 V/V at 200°C. The measured GBW was lower than expected and also dropped with temperature (7.87 MHz at 25°C and 4.99 MHz at 200°C). Both the decrease in loop gain and gain bandwidth with increasing temperature can be at least partially attributed to device transconductance degradation with increasing temperature. The slew rate measurements were very stable over temperature

Table 6.3: Amp2b eni measurement summary (T=25°C).

Ibias [μA]	**Chip 1 eni white** [nV/$\sqrt{Hz}$]	**Chip 1 eni flicker @ 1kHz** [nV/$\sqrt{Hz}$]	**Chip 7 eni white** [nV/$\sqrt{Hz}$]	**Chip 7 eni flicker @ 1kHz** [nV/$\sqrt{Hz}$]
10	6.73	331	- - -	- - -
50	**6.12**	**255**	**6.58**	**307**
100	5.05	237	- - -	- - -

Table 6.4: Amp2b measurement summary vs. temperature (Ibias=50μA).

Temp. [°C]	Aol [dB]	GBW [MHz]	Slew Rate (pos/neg) [V/μs]	Output Swing [V]	eni (1/f @ f=1kHz) $nV/\sqrt{Hz}$	eni (white) $nV/\sqrt{Hz}$	Power Consumption [mW]
25	67.0	7.87	4.4 / 4.4	3.13	255	6.12	4.39
100	65.8	6.60	4.4 / 4.4	3.09	- - -	- - -	4.39(125° C)
150	63.7	5.60	4.4 / 4.4	3.08	- - -	- - -	4.36
175	62.9	5.36	4.4 / 4.4	3.06	- - -	- - -	4.39
200	60.2	4.99	4.4 / 4.4	3.06	- - -	- - -	4.51

and indicate excellent bias circuit temperature performance. The output swing measurements indicate adequate performance and show little dependence on temperature. However, these values indicate the entire output swing range, not just the linear range where the output devices are in saturation, which will be substantially less. Regarding noise, the flicker noise is higher than expected even though large input devices were used to minimize its presence. Comparison of noise simulations using foundry supplied models with measured noise did not agree well. To address this problem, a set of improved noise models was generated that demonstrated excellent agreement with the measured amplifier noise. The measured amplifier white noise of $6\,nV/\sqrt{Hz}$ is approximate due to limitations in the noise measurement system and is reasonably close to the target value of $4\,nV/\sqrt{Hz}$. Overall, amplifier performed well over temperature. The degradation of the loop gain and gain bandwidth over temperature is expected, although the precise amount of expected reduction was not known due to uncertainty in the simulation models employed. In the next section, a comparison of the measured parameters for the integrator opamp with sim-

ulation results is presented as an assessment of the accuracy of the simulation models near room temperature, and the suitability of the models for high temperature simulations.

6.2.5 Comparison of Measured and Simulation Data

Selected results of Amp2b simulations and measurements are summarized in Tables 6.5 and 6.6. Table 6.5 compares the open loop gain and gain bandwidth as a function of temperature. Table 6.6 summarizes the slew rate, output swing and power consumption.

Referring to Table 6.5, the measured and simulated open loop gain agree well up to 150°C where the simulated value begins to degrade severely with increasing temperature (see Fig. 6.21). This discrepancy is most likely related to errors in device output impedance modeling - a common problem in analog circuit simulation. The measured and simulated GBW are plotted together in Fig. 6.22. The simulated values are significantly higher than measured values at each temperature, although the variation with temperature tracks fairly well. An additional curve was added to this plot (GBW Sim. Adj.) that adjusts the simulation values for the same load capacitance seen by the amplifier under

Table 6.5: Amp2b comparison of simulation & measurement data - 1 (Ibias=50μA, C_{load}=20pF).

Temp. [°C]	Measured Aol [dB]	Simulated Aol [dB]	Measured GBW [MHz]	Simulated GBW [MHz]
25	67.0	67.18	7.87	12.90
100	65.8	66.55	6.60	10.92
150	63.7	64.06	5.60	9.86
175	62.9	58.94	5.36	9.47
200	60.2	49.31	4.99	9.34

Table 6.6: Amp2b comparison of simulation & measurement data - 2 (Ibias=50μA, C_{load}=20pF).

Temp. [° C]	Measured Slew Rate (|pos / neg) [V/μs]	Simulated SlewRate (|pos / neg) [V/μs]	Measured Output Swing [V]	Simulated Output Swing [V]	Measured Power Consumption [mW]	Simulated Power Consumption [mW]
25	4.4 / 4.4	4.2 / 4.3	3.13	2.53	4.39	4.48
100	4.4 / 4.4	- - -	3.09	- - -	4.39(125° C)	4.33
150	4.4 / 4.4	4.2 / 4.3	3.08	2.39	4.36	4.28
175	4.4 / 4.4	4.4 / 4.4	3.06	2.37	4.39	4.28
200	4.4 / 4.4	3.5 / 3.6	3.06	2.34	4.51	4.29

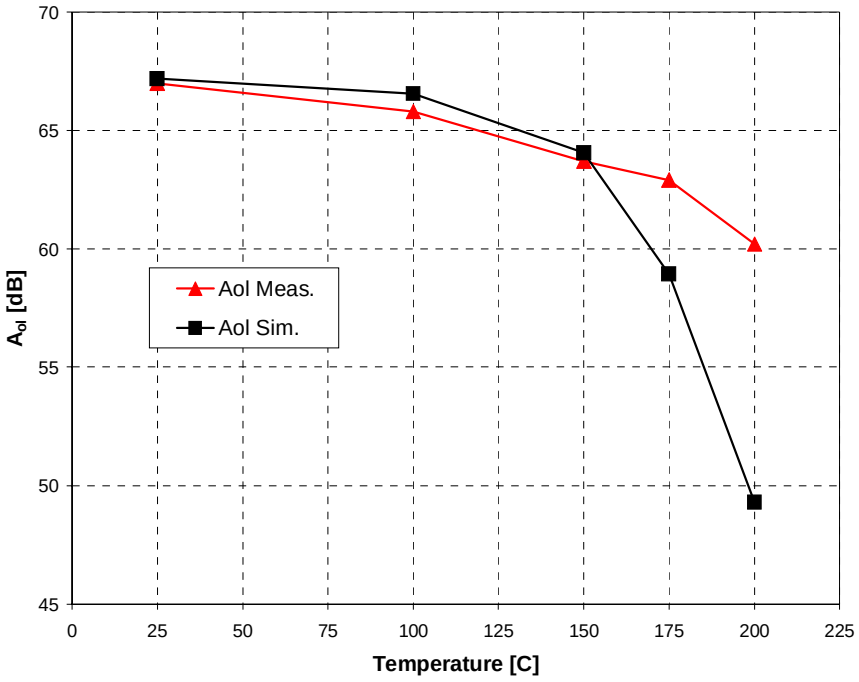


Figure 6.21 Comparison of measured and simulated Amp2b A_{ol} vs. temperature

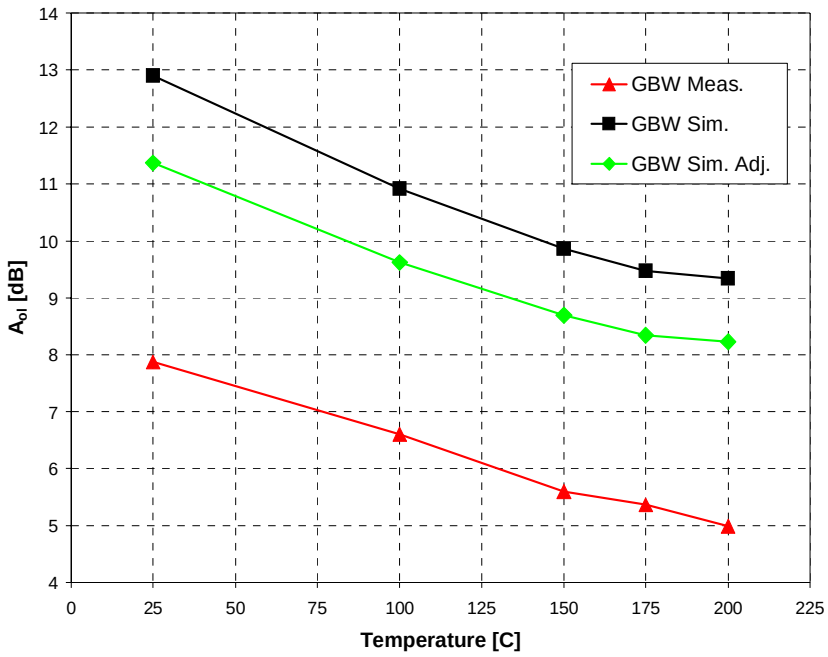


Figure 6.22 Comparison of measured and simulated Amp2b GBW vs. temperature.

measurement conditions. This value was approximately determined using the measured slew rate and expected output stage current. The remaining ~30% discrepancy between the values appears to be due to an over-estimation of the input pair transconductance in the simulation model. Fig. 6.23 shows the simulated and measured loop gain as a function of temperature that shows both the dc gain and crossover frequency characteristics discussed above. The slew rate, output swing, and power consumption comparisons shown in Table 6.6 demonstrate nice agreement between the simulated and measured values for slew rate and power consumption. Some slew rate degradation predicted by the simulations at 200°C was not observed in the measurement (~20% reduction). The output swing comparisons showed significant disagreement. In all cases, the simulations produced output swing values ~600mV less than those measured.

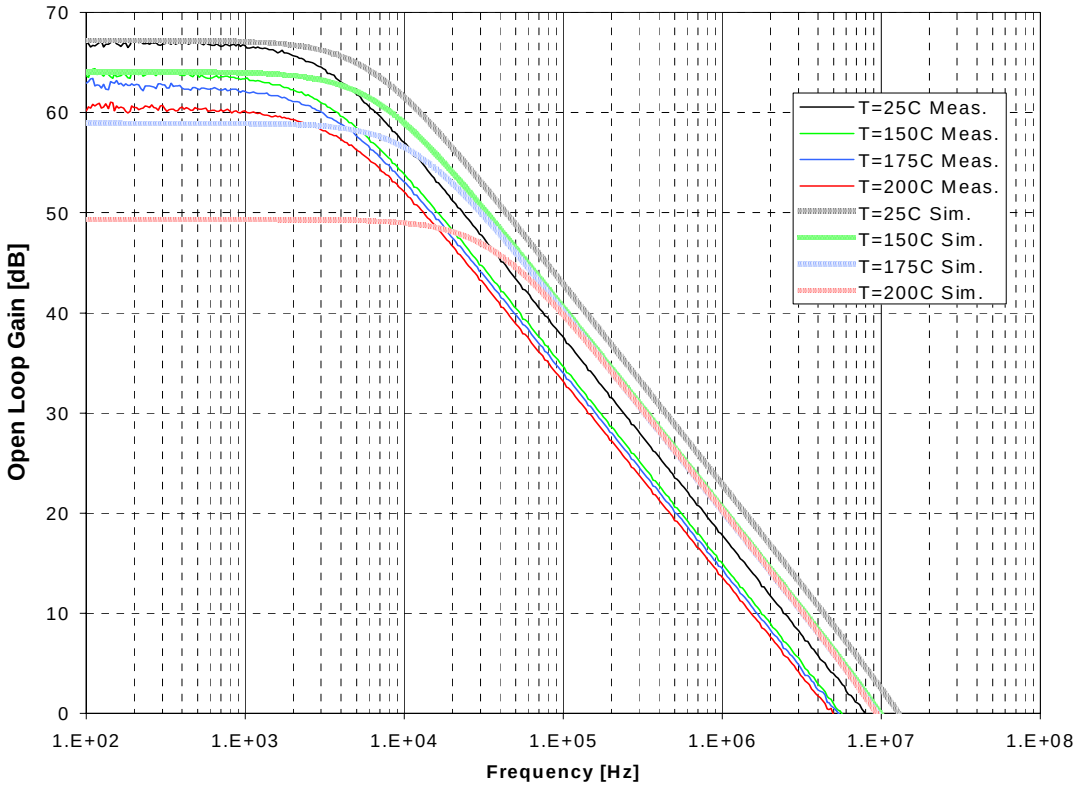


Figure 6.23 Measured and simulated Amp2b loop gain vs. temperature.

In summary, the simulation models appear to produce results consistent with measured data up to 150° C. Some discrepancies associated with poor modeling of the device output impedance and overprediction of device transconductance were observed. However, these errors seemed consistent up to 150° C demonstrating that for this design the foundry supplied L49 models can be used with a reasonable amount of confidence up to 150° C.

6.3 Comparator Measurement Results

The regenerative comparator was tested at room temperature to qualitatively verify proper functioning. A test fixture based on the generic test board was configured for testing this block. In order to ensure proper clocking, the clock generator monitoring outputs from a modulator ASIC (presented in Chapter 7) were used as a source of the two phase clocks. Initially, an attempt was made to use a pulse generator triggered by one of the clock phases to generate a properly timed input signal to the comparator. This approach proved too noisy as the clocking edges were coupled into the comparator inputs. A static approach was used where one input was tied to a dc power supply (supplying vmid) and the other input connected to a adjustable dc voltage supplied by a potentiometer. In order to minimize the noise coupling into the inputs from the two-phase clocks, bypass capacitors were placed on the PCB as close as possible to the inputs. In addition, both ceramic and tantalum surface mount capacitors were soldered to the top of the J-Lead package. Finally, a ceramic bypass capacitor was surface mounted between the comparator inputs (also on the package) for common mode coupling. Under these conditions, an input range of ~30mV was observed to cause the comparator output to transition from continuous high outputs to continuous low outputs. Carefully adjusted to produce adjacent clock output

transitions, the waveforms of Figures 6.24 and 6.25 were captured showing proper output transitioning and delay. The power consumption was measured for 3 chips was approximately 300μW. Due to both the low performance requirements of the comparator and the difficulty associated with making precise measurements, no other tests were performed on the comparator.

6.4 Buffer Amplifier Measurements

A brief testing of the buffer amplifier was performed at room temperature. The dc open loop gain and gain bandwidth were measured as ~52 dB and 8MHz, respectively. The stability of the amplifier connected as a gain of 1 buffer (as it is configured with the modulator) was measured by observing the small signal step response. This measurement was performed at room temperature with a 20pF load. The resultant waveforms from two chips are shown in Fig. 6.26. An approximate overshoot of 10% was observed indicating ~60° phase margin. The accuracy of this measurement was limited by the step signal source but indicates adequate performance for the intended application.

Additional measurements were performed to observe the slewing and output swing behavior of the amplifier when connected as a gain of 1 buffer. The input was driven with a square wave signal exceeding the 1.65V+-1V requirement for the buffer. The resultant output waveforms are shown in Figures 6.27 and 6.28 for the positive and negative transitions, respectively. In both cases, the output dynamic range is sufficient to follow the input signal. The slew rates for the positive and negative transitions were measured as 11.7 V/μs and 6.6 V/μs, respectively. .The measurement results for the buffer amplifier

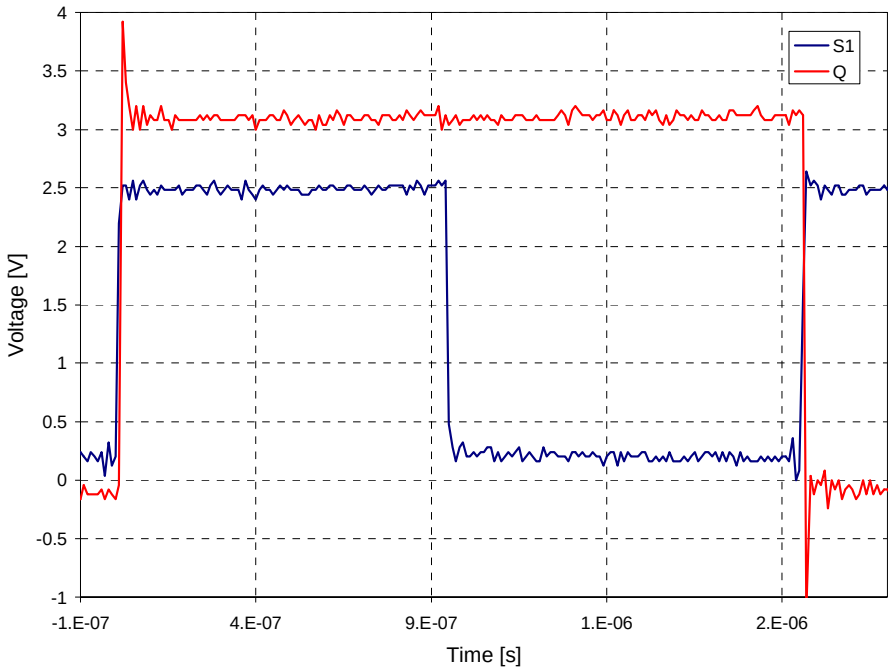
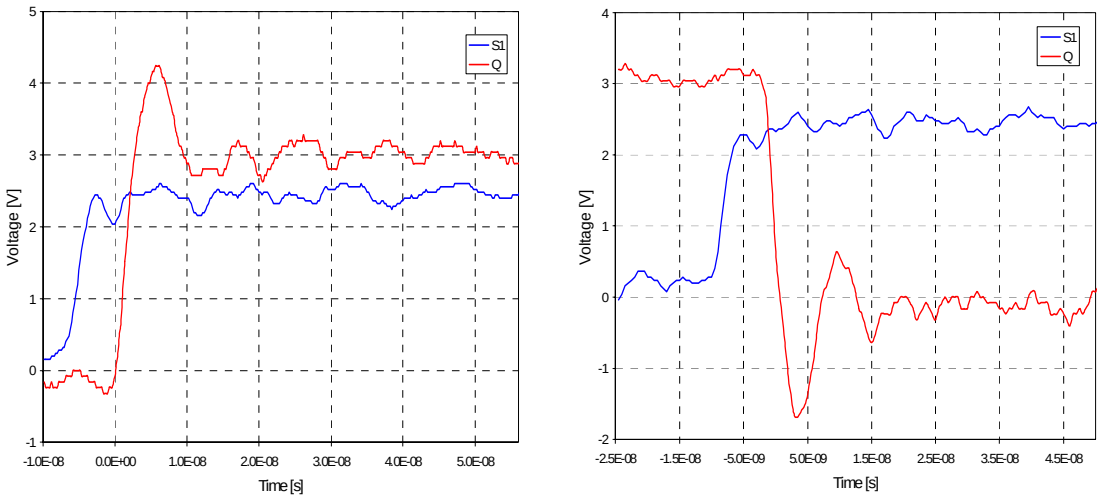


Figure 6.24 Measured comparator output waveforms at T=25° C.



(a) **(b)**

Figure 6.25 Measured comparator output waveforms at T=25° C (zoom). (a) positive Q transition and (b) negative Q transition.

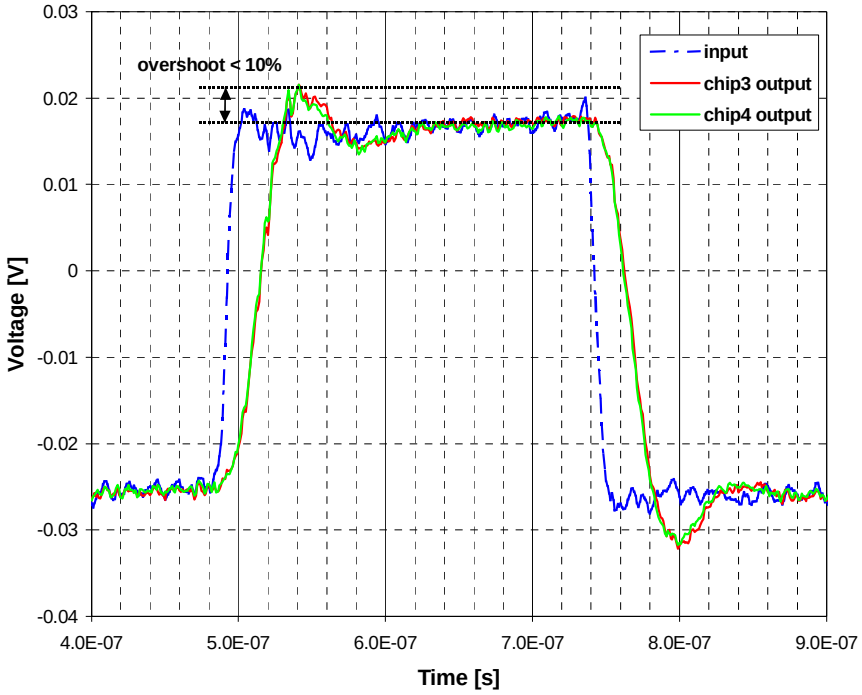


Figure 6.26 Measured buffer amplifier output as 1X buffer (T=25° C).

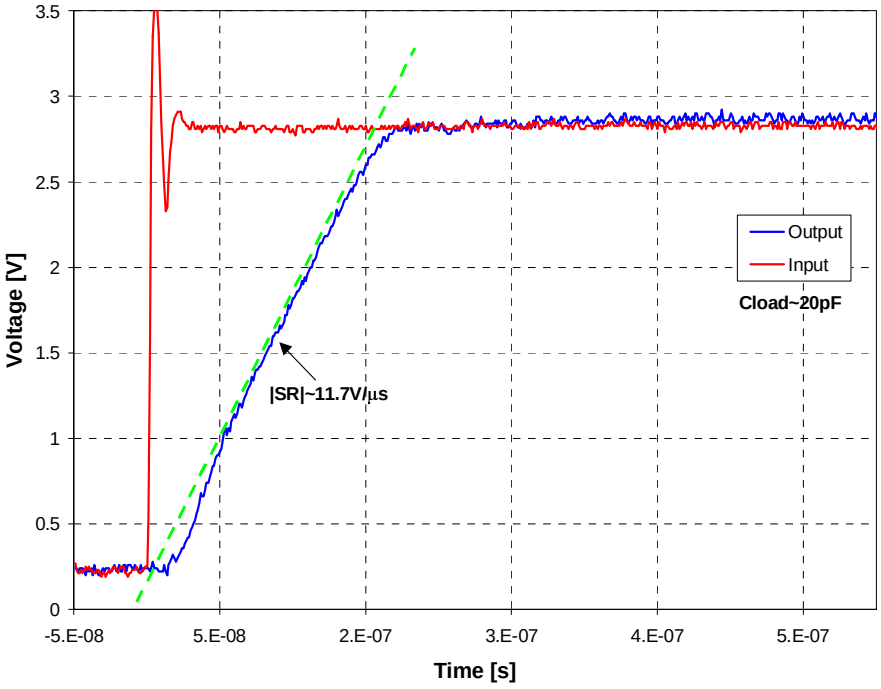


Figure 6.27 Measured buffer amplifier output as 1X buffer - pos. edge (T=25° C).

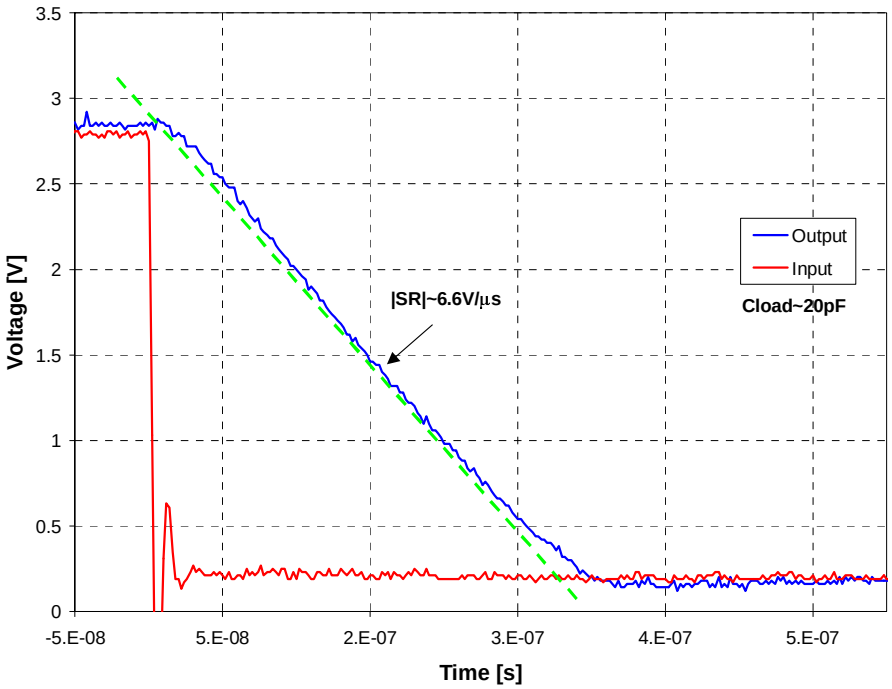


Figure 6.28 Measured buffer amplifier output as 1X buffer - neg. edge (T=25° C).

are compared to the original design target values in Table 6.7. The room temperature test results meet or exceed all of the design targets specified in Chapter 5.

6.5 Other Block Testing

The DAC and switches were thoroughly simulated and a brief test was performed to verify proper gross functioning. No other tests were performed on these modules. However, the circuit blocks are available for further evaluation if overall modulator testing indicates potential errors associated with these circuits.

Table 6.7: Buffer amplifier measurement summary.

Parameter	Measured	Design Target
A_{ol}	~ 52 dB (398 V/V)	> 46dB (200 V/V)
GBW	~ 8 MHz	5 MHz
Slew Rate	11.7 V/µs (+) 6.6 V/µs (-)	4V/µs
Output Swing	> 1.65 +- 1V	1.65V +- 1V
Input DR	> 1.65 +- 1V	1.65V +- 1V

CHAPTER 7

ΣΔ MODULATOR ASIC IMPLEMENTATION & EXPERIMENTAL RESULTS

The modulator design described in Chapter 5 was implemented as an integrated circuit and a test system was designed to facilitate modulator characterization. In this chapter, the results of these tests are presented. Details regarding the ASIC implementation process are discussed including chip layout and partitioning strategies. The overall test system used to characterize the design is described and the associated measurement parameters are defined. Finally, a complete summary of the modulator test results as a function of temperature is presented and discussed.

7.1 ASIC Implementation

The 2-2 cascade modulator was implemented in a 0.5μm SOS-CMOS process available through MOSIS. The chip was designed to maximize testability and observability. A number of layout techniques were employed including functional partitioning, voltage and bias supply partitioning, on-chip supply and bias bypass filtering, and analog layout techniques for device matching and cross-talk minimization. These techniques will be discussed in more detail in this section.

Two primary floor planning approaches were considered in the layout phase of the overall modulator. The first approach, distributed switches, places the integrator switches and capacitors in a symmetric fashion around the integrator amplifier minimizing signal line lengths. However, this approach is area inefficient and requires that clock lines are

distributed throughout the layout causing the clocks to cross many signal lines. The second approach, localized switches, minimizes the clock line lengths by placing the transmission gate switches in groups adjacent to the clock distribution bus. This approach does lengthen the signal line lengths somewhat, but minimizes the clock line lengths and consequently the number clock/signal line crossings. Since the clock lines are strong potential offenders, the localized switch approach was selected to minimize clock signal error injection. The integrator signal lines were also fully differential and closely placed in pairs for common mode noise rejection.

A number of additional partitioning and layout techniques were incorporated into this design. Common centroid structures were employed in all of the opamps and comparators. In addition, device placement to optimize matching of critical components, and internal bias and supply filtering were used wherever practical. The ASIC padframe was partitioned for separate digital, analog, and comparator supplies and ground for each of the 2^{nd}-order loops. An analog shield that encompasses the analog portion of each of the modulator loops was also brought out separately for each modulator. A clock shield consisting of fingers encompassing the perimeter of the each element of the clock distribution bus was incorporated to provide termination of the clock distribution network and was separately brought off-chip for grounding. A number of on-chip filter capacitors were distributed around the padframe perimeter and within the circuit cells where appropriate to provide improved supply high-frequency bypassing. The separation of each of these supply, shield, and ground busses minimizes noise coupling and allows reconfiguring of the connections off-chip to determine the optimum configuration.

Fig. 7.1 shows the fabricated chip. The partitioning of the clock generation circuits and associated distribution bus, the two 2^{nd}-order modulator loops, and pad frame partitioning is evident in this figure. Symmetry about the clock distribution bus can also be observed.

7.2 Parameters for Modulator Performance Evaluation

Dynamic performance metrics of interest in seismic applications include signal-to-noise ratio (SNR), signal-to-noise + distortion ratio (SNDR), total harmonic distortion (THD), and most importantly dynamic range (DR). SNR is defined as the input signal power to the noise power which includes electronic noise and quantization noise but excludes the power in the harmonics of the input signal. SNDR is the ratio of the input

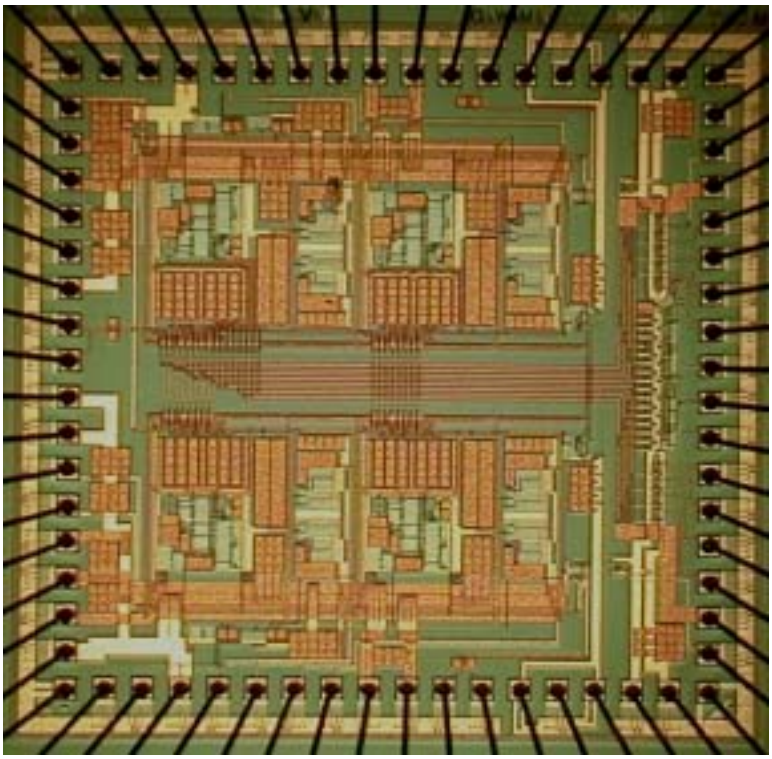


Figure 7.1 Microphotograph of the 2-2c cascade modulator ASIC fabricated in 0.5μm SOS-CMOS process.

signal power to the sum of the noise power and the power in the harmonics. THD is the ratio of the sum of the power in the harmonics to the input signal power. DR is defined as the ratio of the full-scale input signal power to the input signal power when the SNR equals one. The expressions used to calculate these dynamic parameters are given in Eqs. 7.1, 7.2, 7.3, and 7.4. Here, the calculations are performed using *rms* voltages rather than power values, since the output of the FFT operation is a voltage spectral density.

$$SNR_{dB} = 20 \cdot \log\left[\frac{V_f}{\sqrt{V_{n1}{}^2 + V_{n2}{}^2 + \ldots + V_{nm}{}^2}}\right][dB] \tag{7.1}$$

$$SNDR_{dB} = 20 \cdot \log\left[\frac{V_f}{\sqrt{V_{n1}{}^2 + V_{h1}{}^2 + V_{n2}{}^2 + V_{h2}{}^2 + \ldots + V_{nm}{}^2 + V_{hp}{}^2}}\right][dB] \tag{7.2}$$

$$THD_{dB} = 20 \cdot \log\left[\frac{\sqrt{V_{h1}{}^2 + V_{h2}{}^2 + \ldots + V_{hp}{}^2}}{V_f}\right][dB] \tag{7.3}$$

$$DR_{dB} = 20 \cdot \log\left[\frac{V_{in_{fullscale}}}{V_{in_{SNR=1}}}\right][dB] \tag{7.4}$$

In Eqs. 7.1-7.4, V_f represents the fundamental frequency of the input voltage, V_{nm} the noise voltage amplitude with index *m*, and V_{hp} the pth harmonic of the fundamental frequency. Note that in calculating the parameters of Eqs. 7.1-7.3, the *rms* value of V_f must include all of the components of the fundamental, including values spread by the use of an FFT window. From derivations in previous sections, the resolution in bits can be determined as using the dynamic range as follows:

$$Resolution(bits) = \frac{DR_{dB} - 1.76}{6.02} \tag{7.5}$$

Routines were developed in Matlab to calculate these parameters (SNR, SNDR, THD, and DR) from the FFT magnitude using the expressions listed above.

7.3 Modulator Test Method & System

Characterization of high-resolution analog-to-digital converters requires both precise methods and electronics equipment. For the special case of ΣΔ modulators, testing is especially difficult for two primary reasons. First, this class of converters has the capability of achieving very high resolution (on the order of 20 bits) requiring very precise input signal and bias signal generators, as well as careful system construction to prevent external noise coupling. Secondly, the data collection is further complicated by the fact that characterization is performed on a statistical basis, requiring collection and processing of very large data sets. With these objectives in mind, a test system was specifically designed to meet the needs of high-resolution ΣΔ modulator characterization. A description of this test system and associated method is provided in this section. Verification of the test system and analysis software was performed by testing a commercial ΣΔ modulator and comparing measurement results with published modulator specifications. The results of this work are summarized in Appendix B.

7.3.1 Test System Hardware

A block diagram of the overall test system is shown in Fig. 7.2. This system uses an extremely low-distortion signal generator, and low-noise generation and distribution of modulator supply and bias signals. In addition, the system provides proper shielding and grounding to prevent the introduction of noise from external sources including the data collection equipment, other laboratory equipment, and power distribution.

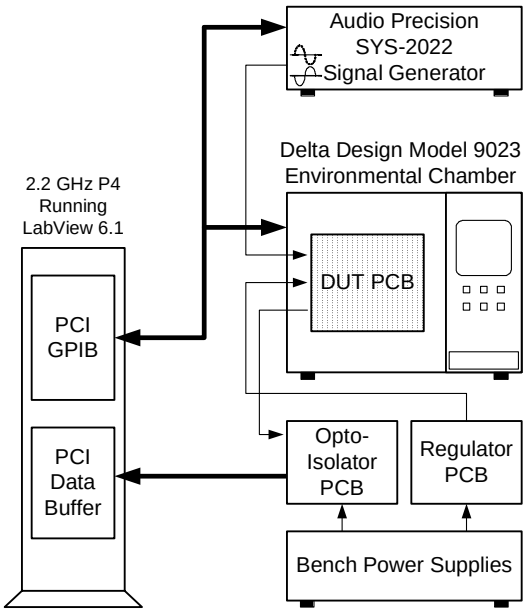


Figure 7.2 Modulator test & characterization system.

The system is PC-based and uses a GPIB (IEEE-488) bus for instrument control. Control of the low-distortion signal source and environmental chamber is accomplished using a GPIB port. The signal source is an Audio Precision 2202 signal source capable of differential signal generation over a wide range of amplitudes (~128dB dynamic range) and frequencies (10Hz - 204kHz). The unit is very low distortion (-120dBc in 20Hz - 20kHz bandwidth, -130dBc @ 1kHz) making it the best commercial unit available for this application. The environmental chamber (Delta Design Model 9023) can also be operated via GPIB and provides temperature control from ~-80° C to 300° C.

Data collection was performed using a National Instruments digital I/O card (PCI-DIO-32HS). This card has a large internal FIFO that allows externally clocking of data. The modulator ASIC produces a clock signal along with two 1-bit digital data streams that

are optically isolated to minimize ground loop and noise injection errors associated with interfacing the modulator with the digital I/O card.

Two custom printed circuit boards (PCBs) were designed for testing the modulator. The modulator test PCB has four conductive layers and is used to fixture the ASIC under test. On this board, the supply and ground partitioning is consistent with the strategy implemented on the ASIC. A number of jumpers are incorporated to allow reconfigurability of the grounding for optimum performance. Fig. 7.3 shows the schematic of this board. The design provides heavy supply and bias filtering. Careful layout of the signal traces and off-board connectivity was performed to minimize noise coupling.

The modulator bias PCB provides all necessary supply voltages to the modulator board and allows adjustability of these voltages for testing. Fig. 7.4 shows the three different regulator designs used on the PCB. These circuits are jumpered to allow the chip supply voltages to be either fixed at 3.3V or adjustable. The other reference voltages (feedback error voltages and mid-scale voltages) are configured as adjustable references.

The system was partitioned to minimize the amount of circuits exposed to high temperatures. The modulator test board is placed in the oven and tethered to the bias board placed outside of the oven. The boards are interconnected using teflon jacketed wires that are permanently soldered to the modulator board and connectorized at the bias board for easy disconnection. Photographs of both test boards and the overall test system are shown in Fig. 7.5 and Fig. 7.6, respectively.

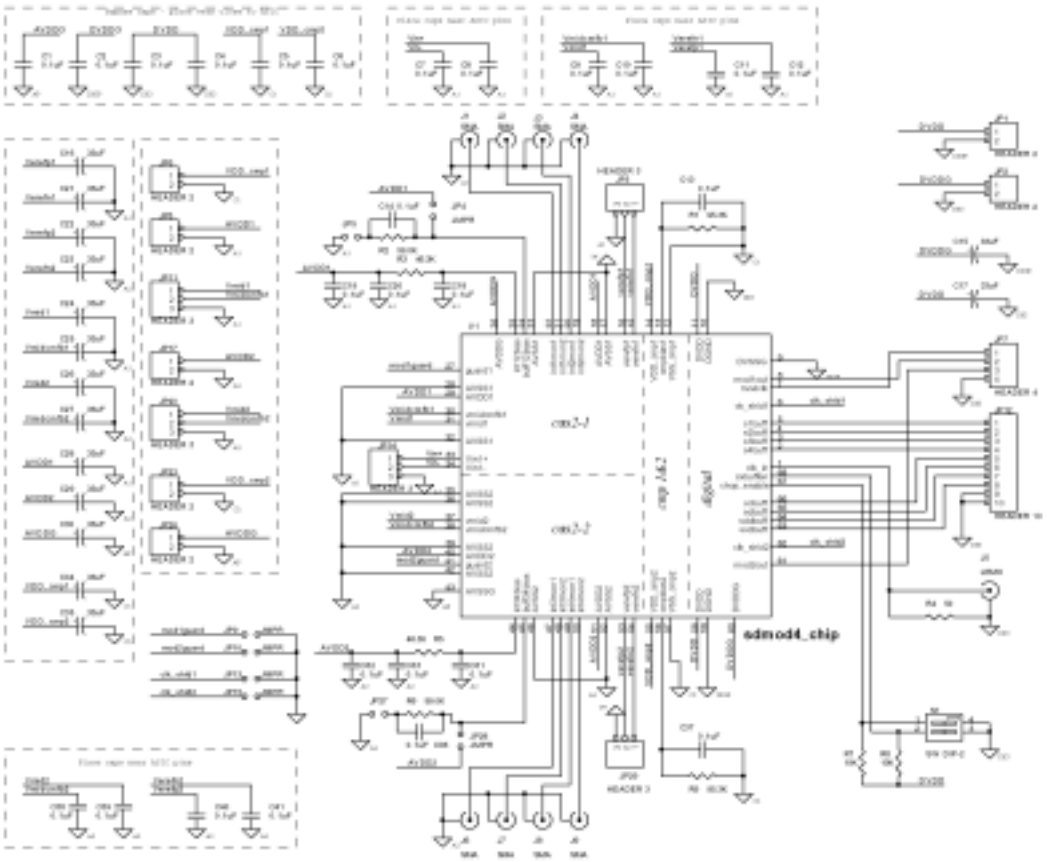


Figure 7.3 Modulator test PCB schematic.

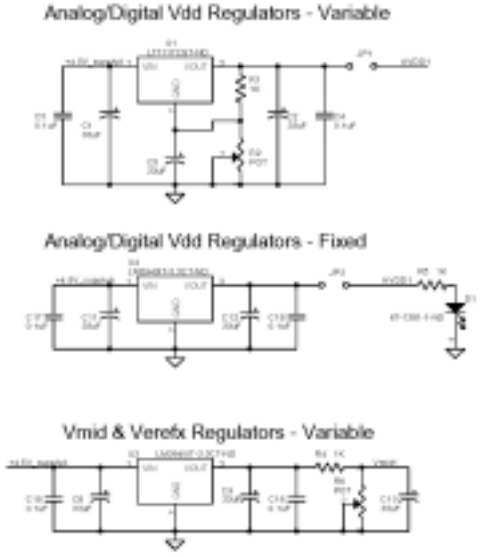
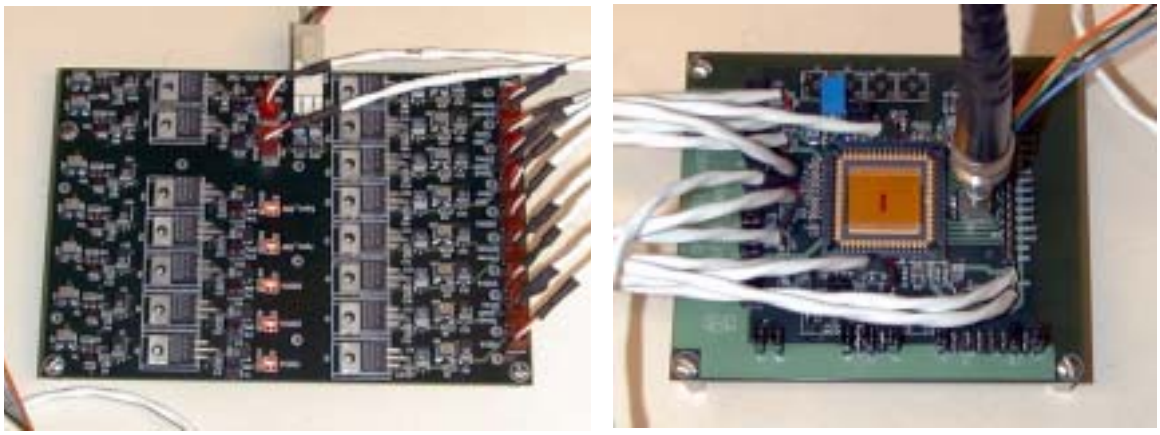


Figure 7.4 Modulator bias circuits.



(a) **(b)**

Figure 7.5 Modulator test system boards. (a) bias generator board and (b) modulator chip board.

Figure 7.6 Photograph of modulator test & characterization system.

7.3.2 Test System Software

Overall control of the test system was performed using a LabView-based program that allows selection of the signal generator settings and sampling parameters, and performs collection, storage, and limited processing of the modulator data. This program is intended primarily for data collection but has full capability to perform FFT analysis and calculation of modulator performance parameters. Fig. 7.7 shows the basic functions associated with the two modes of operation: diagnostics mode and data collection mode. In either mode, the modulator order to be processed must be selected (2^{nd} order, 4^{th} order, or both).

In diagnostics mode, the modulator data is windowed, an FFT applied, performance metrics are calculated (SNR, SNDR and THD), and the resultant FFT plot or plots are displayed on the screen. This mode also supports FFT averaging and saving of both the raw data modulator data streams and FFT output to user specified files. Diagnostics mode is intended only for short checkout runs where the modulator setup is being optimized.

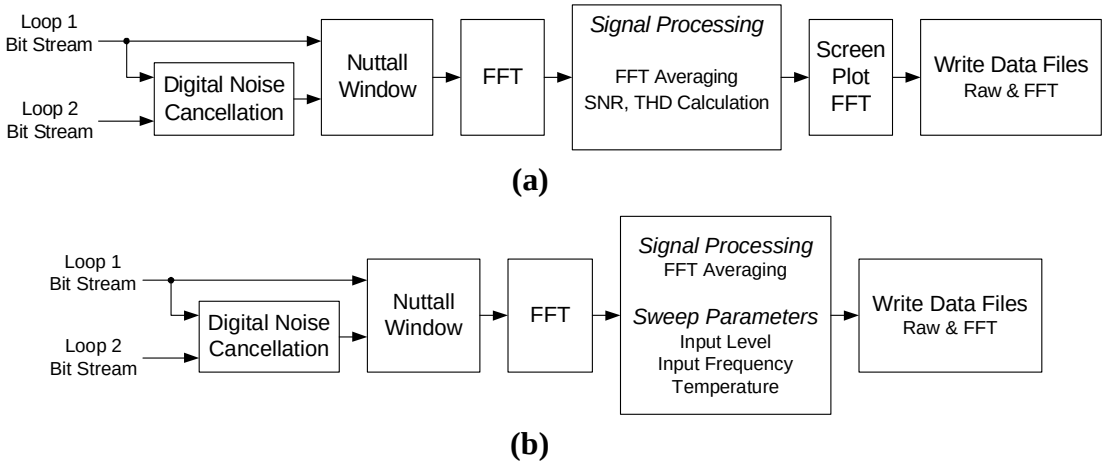


Figure 7.7 LabView based data acquisition software block diagram . (a) diagnostics mode (b) data collection mode.

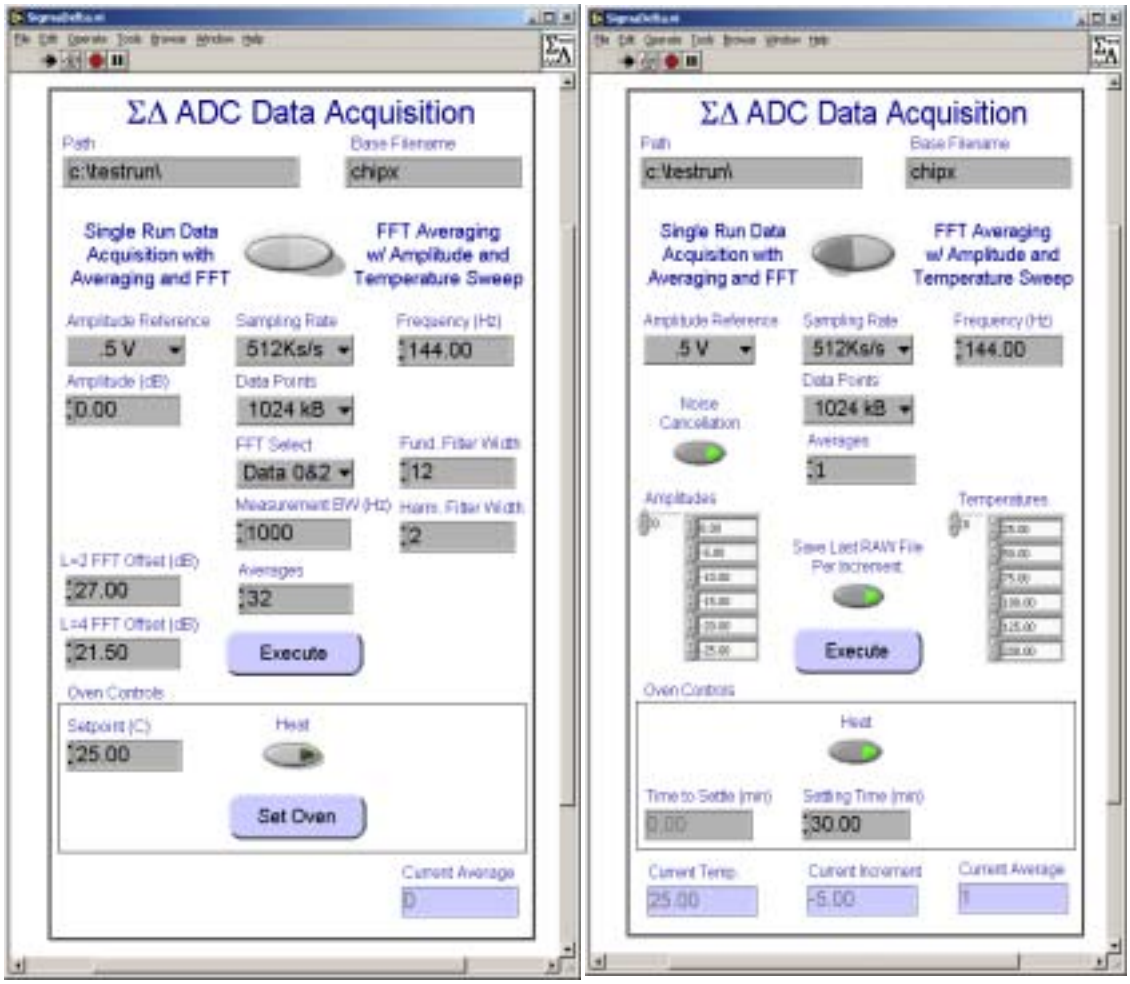
Setup operations may include investigating specific grounding, biasing, filtering, shielding, and cabling issues and involve iterative modulator performance measurements.

Data collection mode is intended for collecting large amounts of raw data for post processing. This mode is similar to diagnostics mode with a few main differences. The FFT results are not plotted to the screen and the ability to sweep test parameters is incorporated. Sweep parameters include input signal frequency, input signal amplitude, and oven temperature. Once set up and initiated, this mode allows automated collection of modulator data over a broad range of test conditions.

Screen shots of the LabView program showing the setup menus for diagnostics mode and data collection mode are presented in Fig. 7.8. An example output screen generated using the diagnostics mode is shown in Fig. 7.9.

Following data collection, the modulator data (raw in the case of non-averaged, FFT data in the case of averaged) was processed using a number of different script files in Matlab. Associated calculations and analyses are processing intensive and can take extended periods of time for large data lengths. These functions were performed on a high-performance computing platform (Pentium 4, 2.2 GHz). Table 7.1 lists the basic MATLAB programs and shows the associated processing functions.

In both software environments (LabView or in Matlab) two procedures were performed on the raw time-domain modulator data -- removal of the artificial dc component and windowing. Removal of the dc component is necessary because any digital bit stream composed of 0's and 1's has a dc component. This can be accomplished by simply converting all of the 0's to -1's. Windowing is performed by multiplying the time domain



(a) **(b)**

Figure 7.8 LabView data acquisition program setup menus. (a) diagnostics mode and (b) sweep mode.

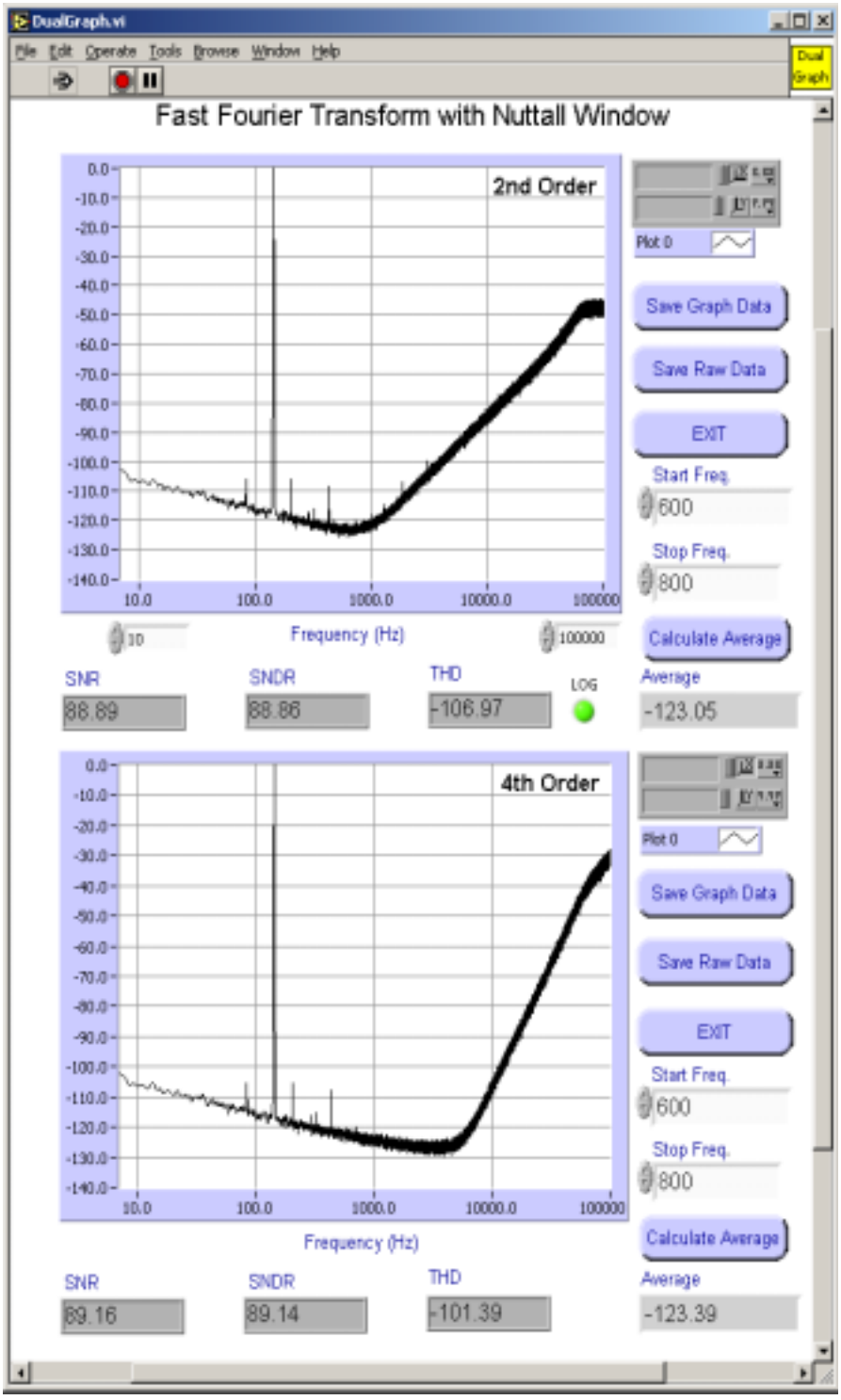


Figure 7.9 Diagnostics mode output plot.

Table 7.1: Matlab signal processing & plotting program summary.

Program	Input	Output
dogendata.m	raw modulator data files (.raw0,.raw1)	3D FFT plots of modulator output vs.input level (.fig format) 2D graphs of SNR, SNDR, and THD vs. input level (.fig format) DR data tables (2 column text)
dofiguredata3d.m	2D files for SNR, SNDR, and THD (.fig format)	3D plots of SNR vs. input level vs. temp (.fig format) 3D plots of SNDR vs. input level vs. temp (.fig format) 3D plots of THD vs. input level vs. temp (.fig format)
osrcalc.m	raw modulator data files (.raw0,.raw1)	2D plots of SNR, SNDR, and THD vs. OSR (.fig format)
multosr.m	2D files of SNR vs. OSR (.fig format)	2D plots of SNR vs. OSR vs. temp (.jpg format)
donoisecancel.m	raw modulator data files (.raw0,.raw1)	4^{th}-order modulator data files (.raw2)
gendoublefft.m	raw modulator data files (.raw0,.raw1)	Screen plot of 2^{nd} and 4^{th} order modulator output together
readfft.m	modulator fft file (.fft)	Screen plot of modulator fft
snr2fft.m	modulator fft file (.fft)	Screen plot of modulator fft, display of SNR & resolution
vsdfit3.m	noise values as text	Screen plot of eni and display of baseband noise components and predicted SNR.

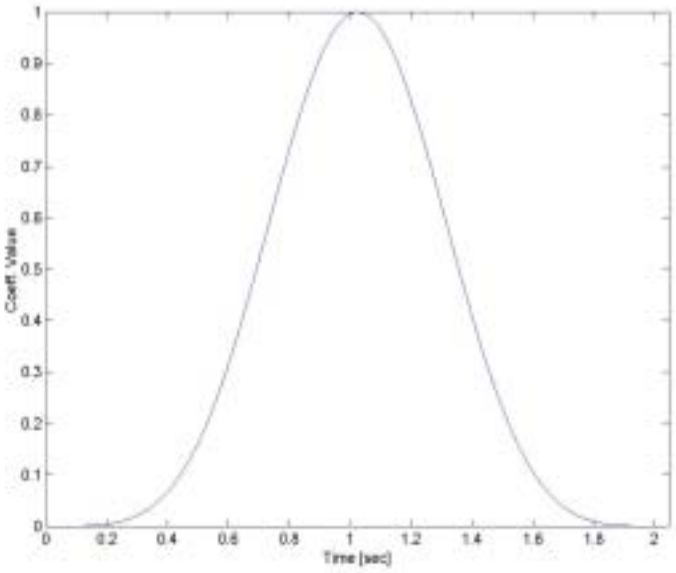
data by an equal length array of window coefficients. The Nuttall window employed in this research has been shown to exhibit excellent side-lobe decay and is commonly used for ΣΔ modulator work [143]. Fig. 7.10(a) shows the Nuttall window coefficients for a 1M-point FFT sampled at 512 kHz (modulator output bit rate = 512 kbits/s). Fig. 7.10(b) shows the frequency domain spreading and side lobe behavior for a single tone input after application of the Nuttall window. As a result of windowing, the fundamental power is spread over a narrow range of frequencies and this entire range must be included when calculating the fundamental signal power.

7.4 Modulator Experimental Results

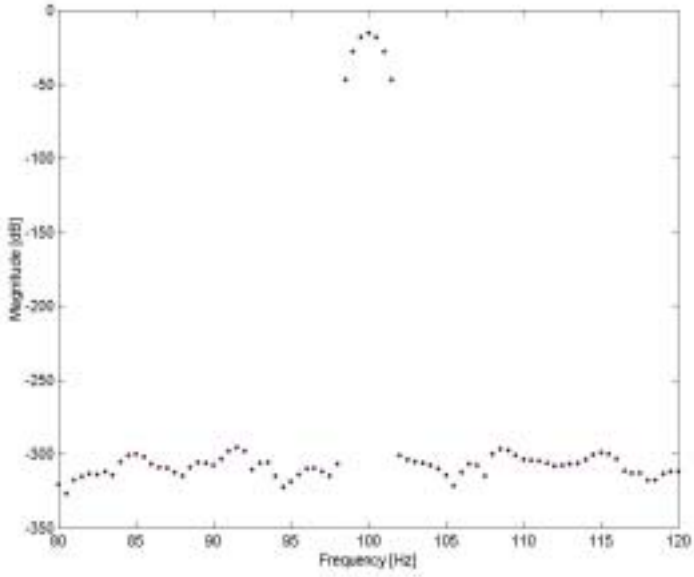
A number of tests were performed on three modulator ASICS in an attempt to fully characterize the dynamic performance of the circuit over temperature. Each ASIC was tested over a temperature range of 25° C to 200° C. At each temperature, three input frequencies were selected as the fundamental input frequency, each having harmonics adequately separated by multiples of 60 Hz, a potentially significant noise source that could cause misinterpretation of the data. The test frequencies used were 24.4 Hz, 144 Hz, 950Hz. For each of the test chips, test temperatures, and input frequencies, the input signal amplitude was swept from full-scale to -100dB of full-scale.

7.4.1 Initial ASIC & Test System Checkout

Prior to collecting large amounts of data, several chips were tested for basic operation to ensure that both the ASIC and the test system were correctly designed and implemented. Supply currents and bias voltages were monitored. The buffer amps were



(a)



(b)

Figure 7.10 Nuttall window characteristics. (a) coefficients (b) frequency domain spreading and side lobes associated with single tone input.

enabled and the modulator integrator monitor outputs were observed for proper shape (gross slew rate & settling behavior) and to ensure stable operation. Finally, the modulator clock monitoring port was enabled and the clocks were observed using both an oscilloscope and a logic analyzer. Measured clock output waveforms are shown in Figs (7.11) and (7.12), for T=25° C and T=200° C, respectively. The increased delay between transitions observed in these plots with respect to simulation data in Chapter 5 is due to the capacitive loading of the cabling and logic analyzer used to make the measurements.

7.4.2 Modulator Output Spectra

The performance metrics SNR, SNDR, THD, and DR are all calculated from modulator output spectral data. However, significant information can be obtained by straight-forward observation of the output spectra. Effects associated with noise shaping efficacy,

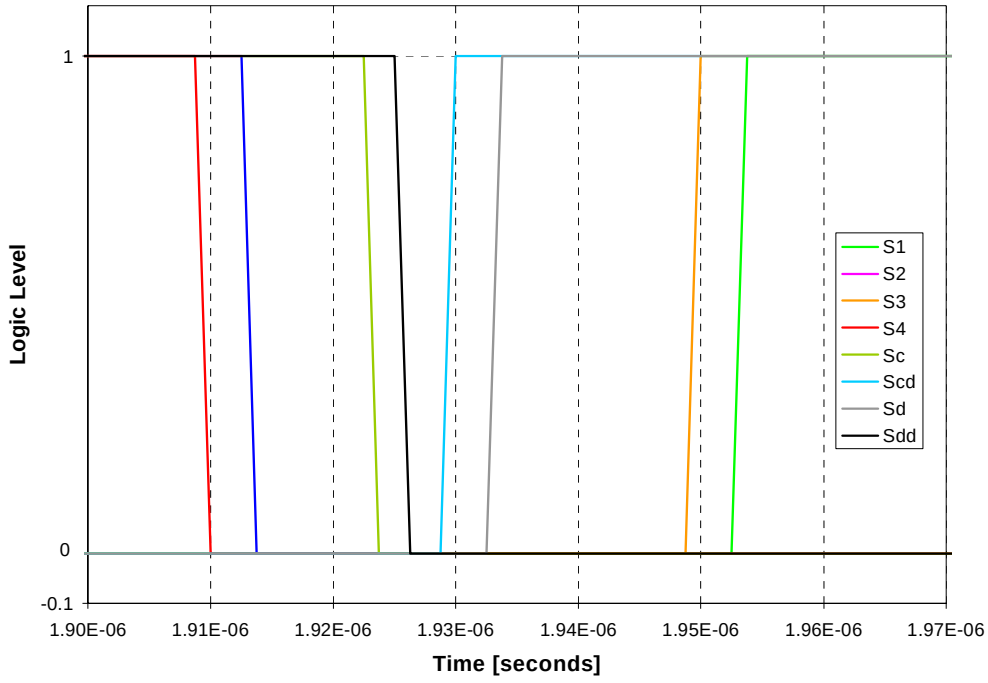


Figure 7.11 Measured modulator clocks for T=25° C.

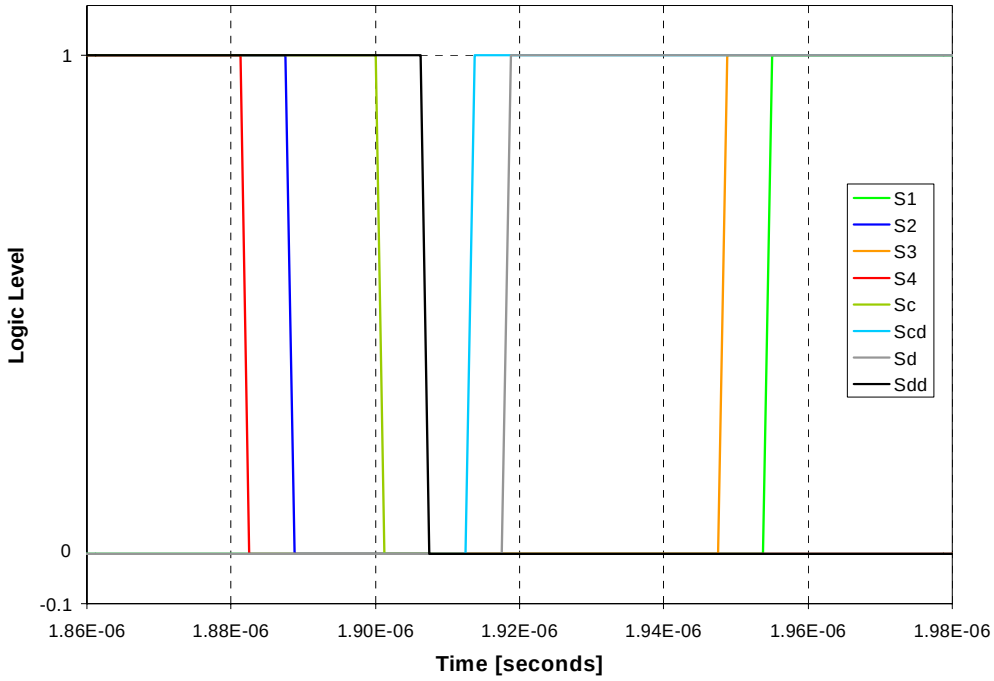


Figure 7.12 Measured modulator clocks for T=200°C.

tonal behavior, harmonic distortion, electronic noise, and coupled external noise (60Hz) can often be visually observed in the modulator output spectrum. This section presents the output spectrum of three modulator chips measured at a number of temperatures and varying input conditions and discuss general trends evident by observation of this data. Note that the data presented in the following sections was taken with the integrator chopper disabled. Operating the chopper introduced undesirable spectral tones that made it difficult to evaluate the modulator performance. Presentation of data taken with the chopper enabled and a discussion regarding the reason for its poor performance is presented in later portions of this chapter.

The modulator output spectrum of chip 4 with a -6dB (referenced to full-scale) 144Hz input is shown in Fig. 7.13 for 2^{nd}- and 4^{th}-order modulators measured at T=25°C and

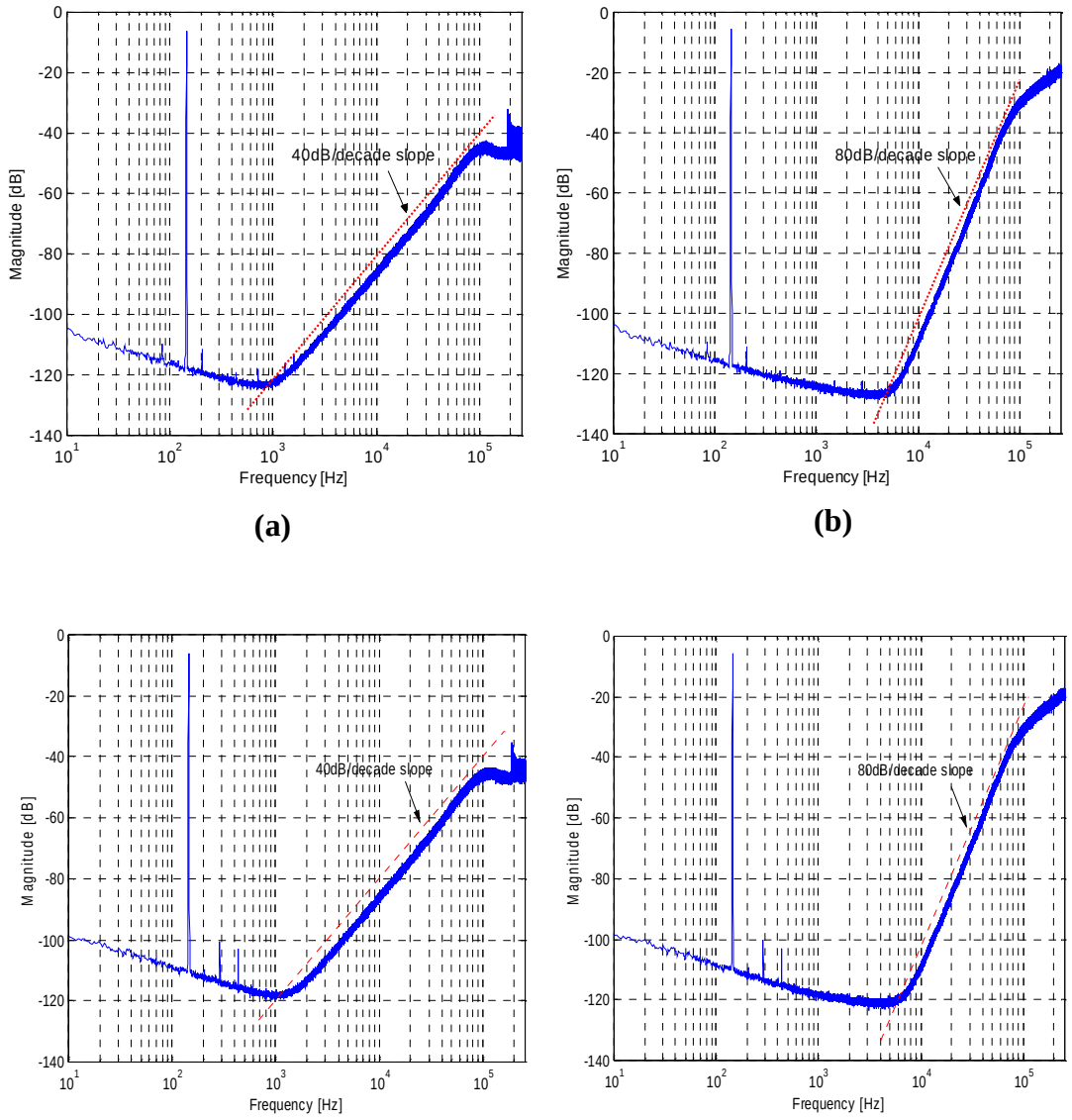


Figure 7.13 Measured modulator output spectra. (a) 2nd order, T=25° C, (b) 4th order, T=25° C, (c) 2nd order, T=200° C, and (d) 4th order, T=200° C.

T=200° C. The data in these plots are each the result of averaging 64, 1M-point FFTs. Averaging reduces the variation of the noise and produces better definition of any tones hidden in the noise. This plot indicates that the modulator is shaping the noise as expected at both temperatures, evident by the 40dB/decade slope and 80db/decade slope observed for the 2^{nd}- and 4^{th}-order modulators, respectively. The maintaining of proper noise shaping at T=200° C indicates sufficient integrator opamp open loop gain. Note the harmonics of the fundamental in the T=200° C plots for both modulator orders. This effect was consistently observed in the high temperature data and is a result of decreased linear output range of the integrator amplifiers at elevated temperatures.

A more exhaustive presentation of the modulator output spectra in the seismic signal bandwidth (1kHz) is presented in Figures (7.14) through (7.19). In these figures, the output spectra of both the 2^{nd}- and 4^{th}-order modulators of chip 2 are plotted as a function of input signal amplitude for the three input signal frequencies (36.6Hz, 144Hz, and 950Hz) and for T=25° C, T=125° C, T=150° C, T=160° C, T=175° C, and T=200° C. The input signal level, referenced to the 2^{nd}-order maximum single-sided input amplitude of 0.5V (2V differential), was swept using a -2dB step from 0dB to 20db, and a -10dB step from -20dB to -100dB. When configured as a 4^{th}-order modulator, the maximum input range must be halved (0.25V maximum, 1V differential) to prevent overloading of the 2^{nd} modulator loop. To accomplish data collection simultaneously for both modulator orders, input values from -26dB to -96dB in -10dB steps were added to the input sweep list. The measured data indicates that the output spectra are independent of the input signal frequency, except for some harmonic distortion observed in the T=175° C and T=200° C

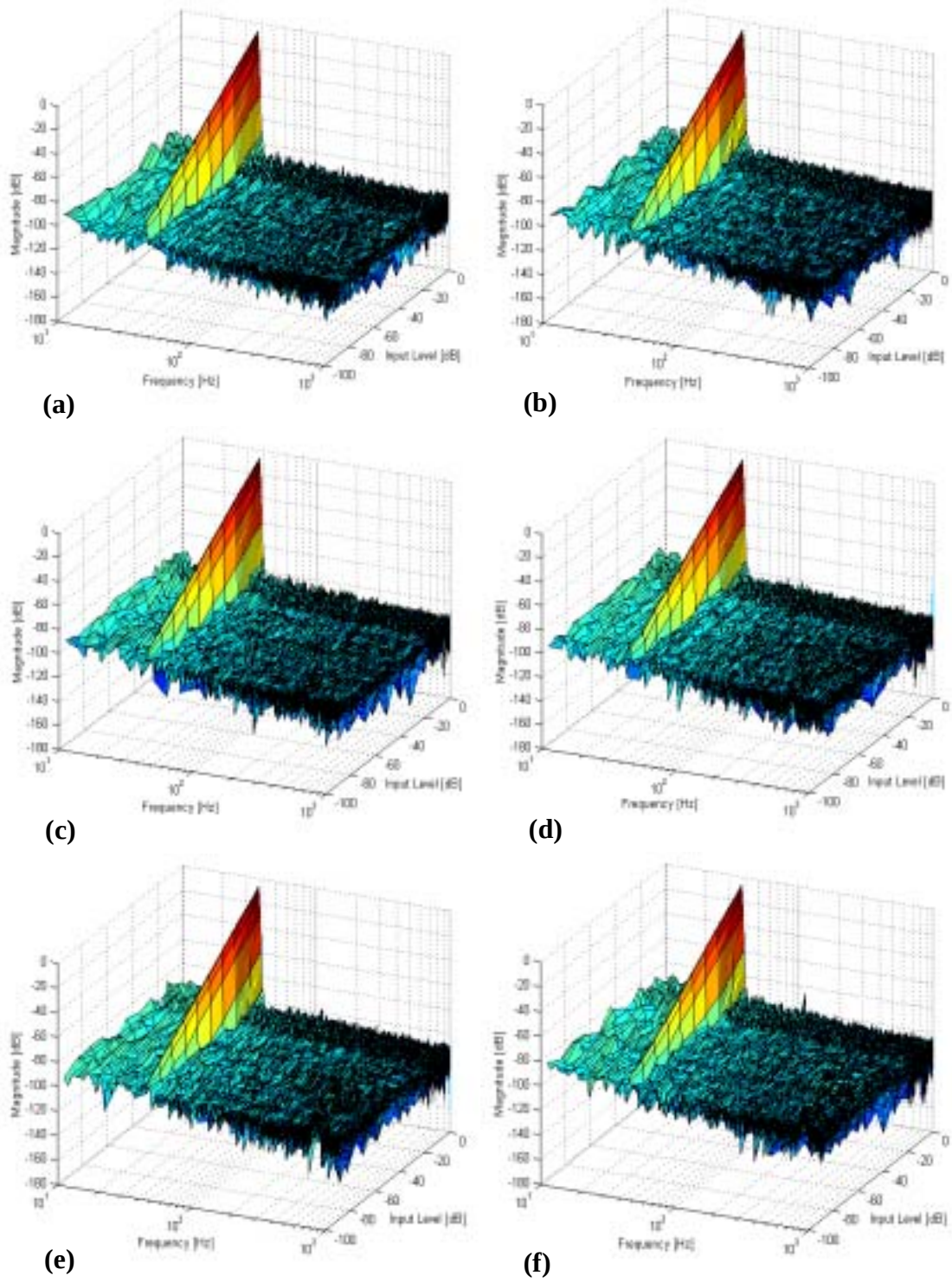


Figure 7.14 2nd-order modulator measured output spectra. (a) 25° C, (b) 125° C, (c) 150° C, (d) 160° C, (e) 175° C, and (f) 200° C. (chip2_36.6).

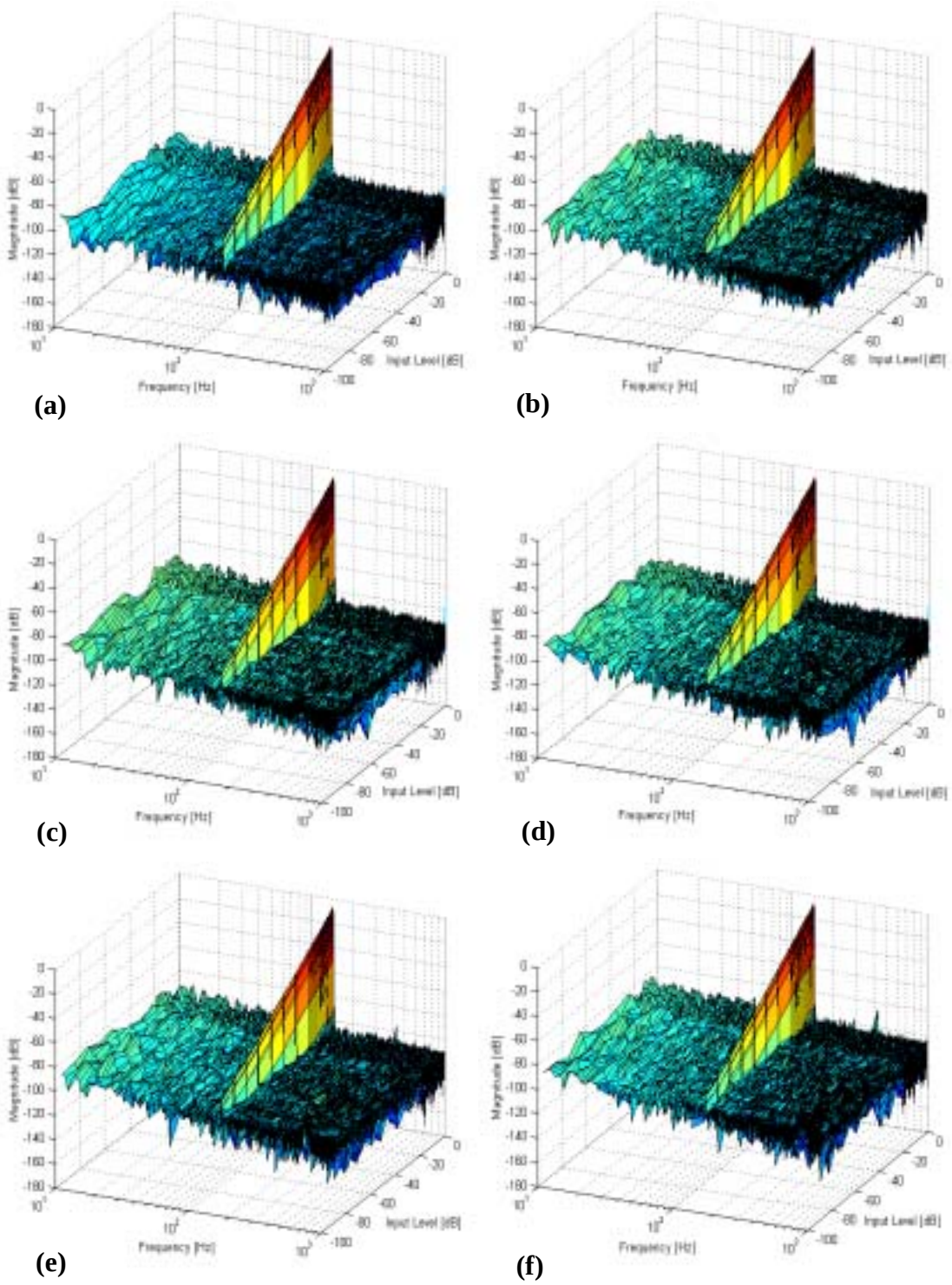


Figure 7.15 2nd-order modulator measured output spectra. (a) 25° C, (b) 125° C, (c) 150° C, (d) 160° C, (e) 175° C, and (f) 200° C. (chip2_144).

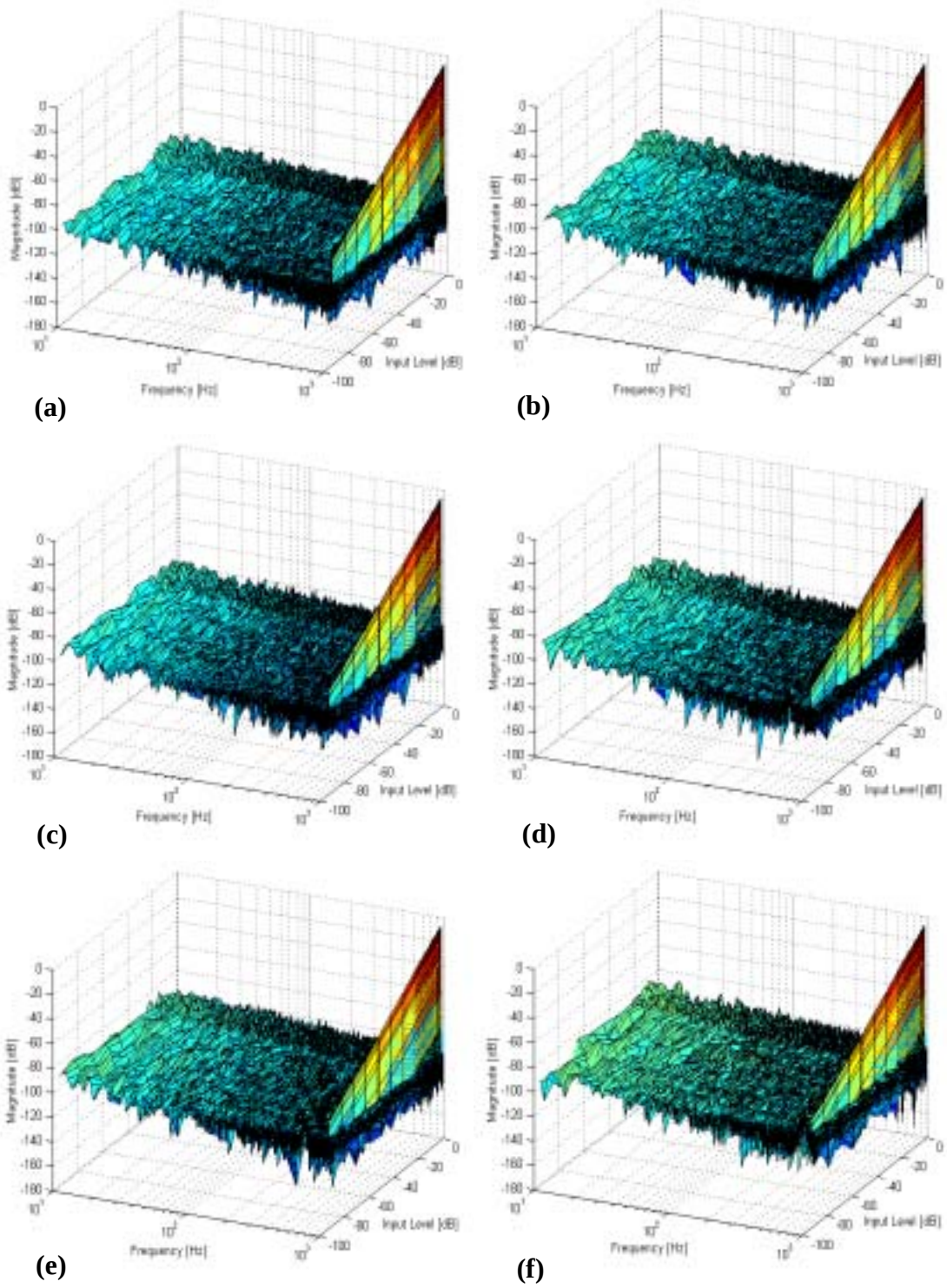


Figure 7.16 2nd-order modulator measured output spectra. (a) 25° C, (b) 125° C, (c) 150° C, (d) 160° C, (e) 175° C, and (f) 200° C. (chip2_950).

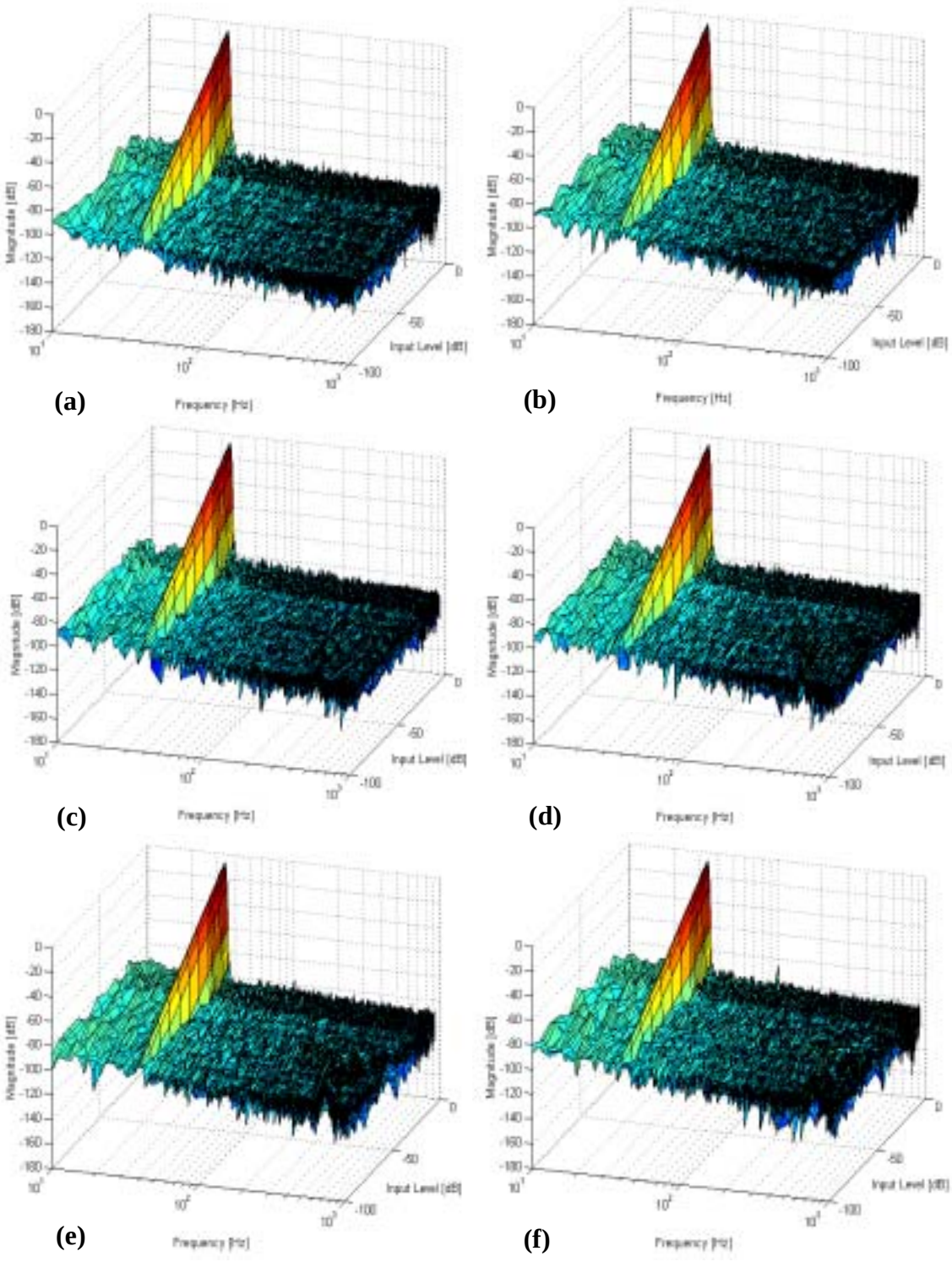


Figure 7.17 4th-order modulator measured output spectra. (a) 25° C, (b) 125° C, (c) 150° C, (d) 160° C, (e) 175° C, and (f) 200° C. (chip2_36.6).

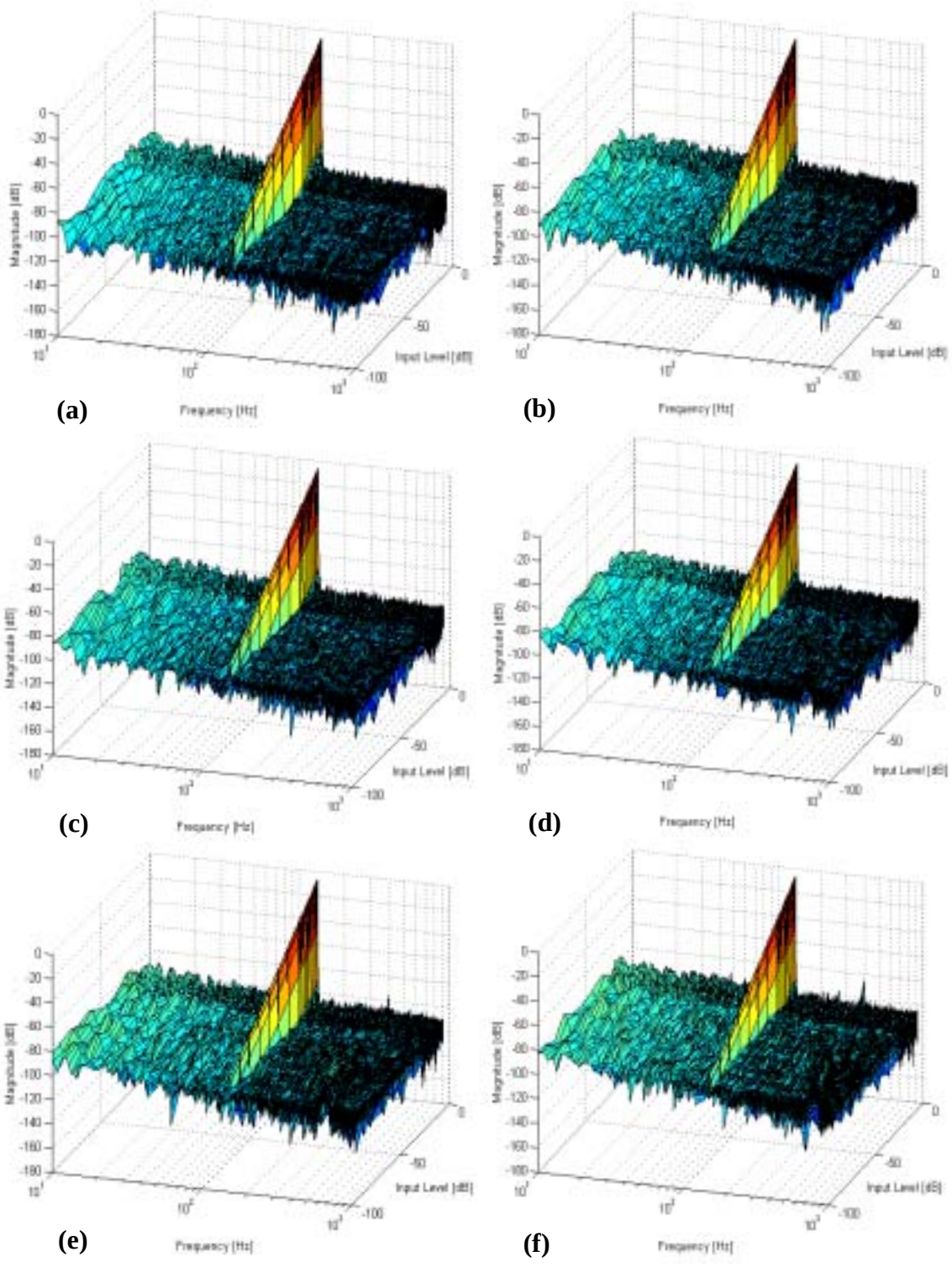


Figure 7.18 4th-order modulator measured output spectra. (a) 25° C, (b) 125° C, (c) 150° C, (d) 160° C, (e) 175° C, and (f) 200° C. (chip2_144).

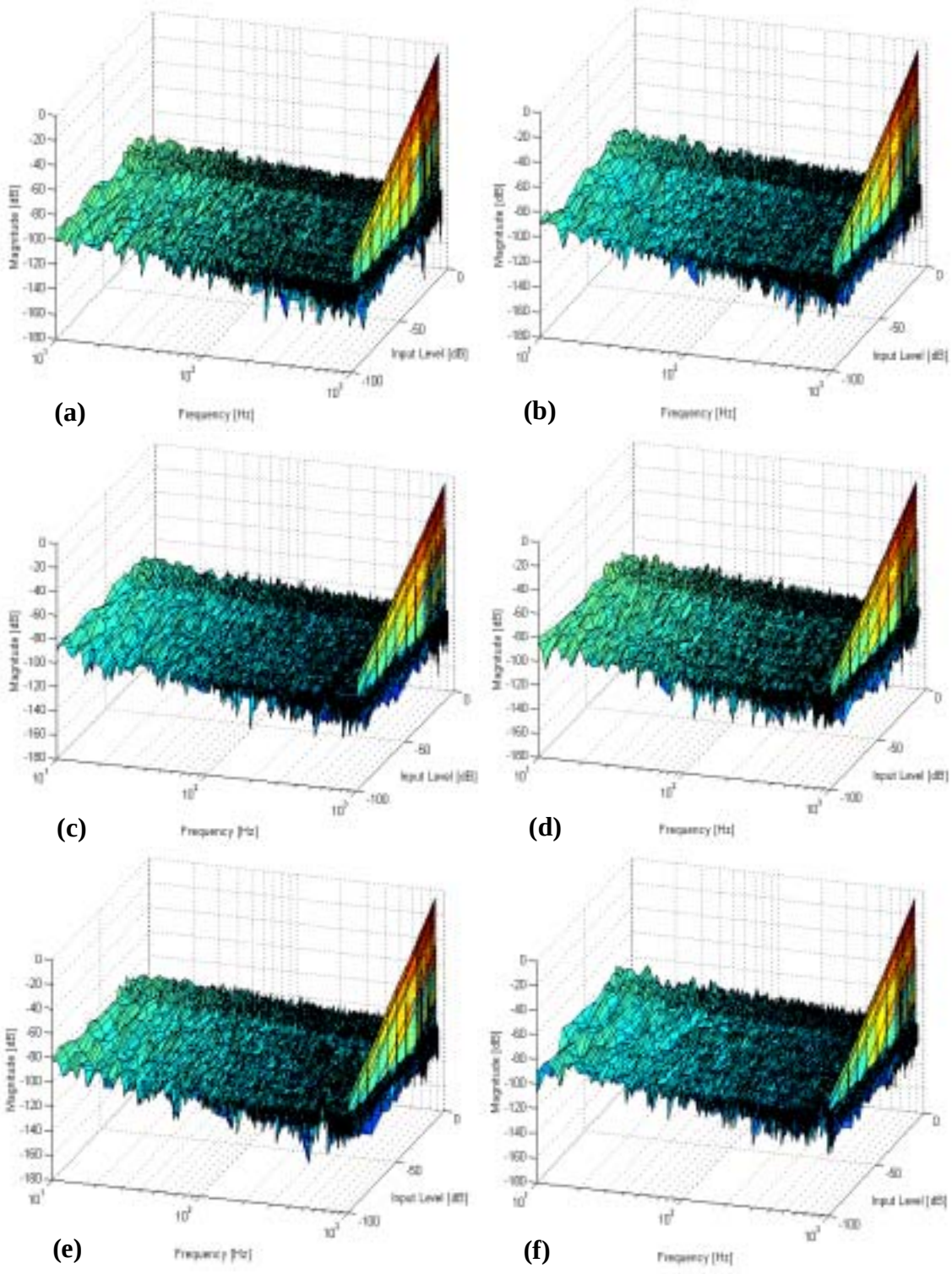


Figure 7.19 4th-order modulator measured output spectra. (a) 25° C, (b) 125° C, (c) 150° C, (d) 160° C, (e) 175° C, and (f) 200° C. (chip2_950).

data. Overall, the spectra are fairly ideal except for the level of the noise floor as is discussed in more detail in later sections.

7.4.3 SNR & SNDR Measurements

Using the relationships given in Eqn. 7.1 and Eqn. 7.2, the Signal-to-Noise Ratio (SNR) and Signal-to-Noise + Distortion Ratio (SNDR) were calculated for the three test chips over the entire range of input frequencies, input amplitudes, and temperatures. Note that one SNR and SNDR value is calculated from a single modulator output spectrum. The results these analyses are presented in Figures (7.20) through (7.25). These plots show SNR and SNDR calculated versus input amplitude and temperature for 3 chips and 3 input frequencies. Results indicate some degradation of SNR at elevated temperatures. However, no measurable roll-off in the SNR level was observed near full-scale input at lower temperatures, suggesting the absence of skirting and coloring of the output spectrum, a phenomenon often observed in modulators driven near full scale. SNDR is the same as SNR except that the power in the harmonics is used in the calculation. For this reason, a decrease in SNDR relative to SNR indicates the presence of harmonics in the modulator output spectrum. For the three chips tested, the measured SNR and SNDR were nearly equivalent under all test conditions, indicating that the power in the harmonics was small compared to the noise power.

The peak SNR measured for the three chips is plotted in Fig. 7.26 as a function of temperature. The peak SNDR values measured were nearly identical to the SNR values in all tests and are not shown. In Fig. 7.26(a) the chip 2 peak SNR is presented for all three input frequencies (2nd and 4th order modulator). These results indicate no appreciable

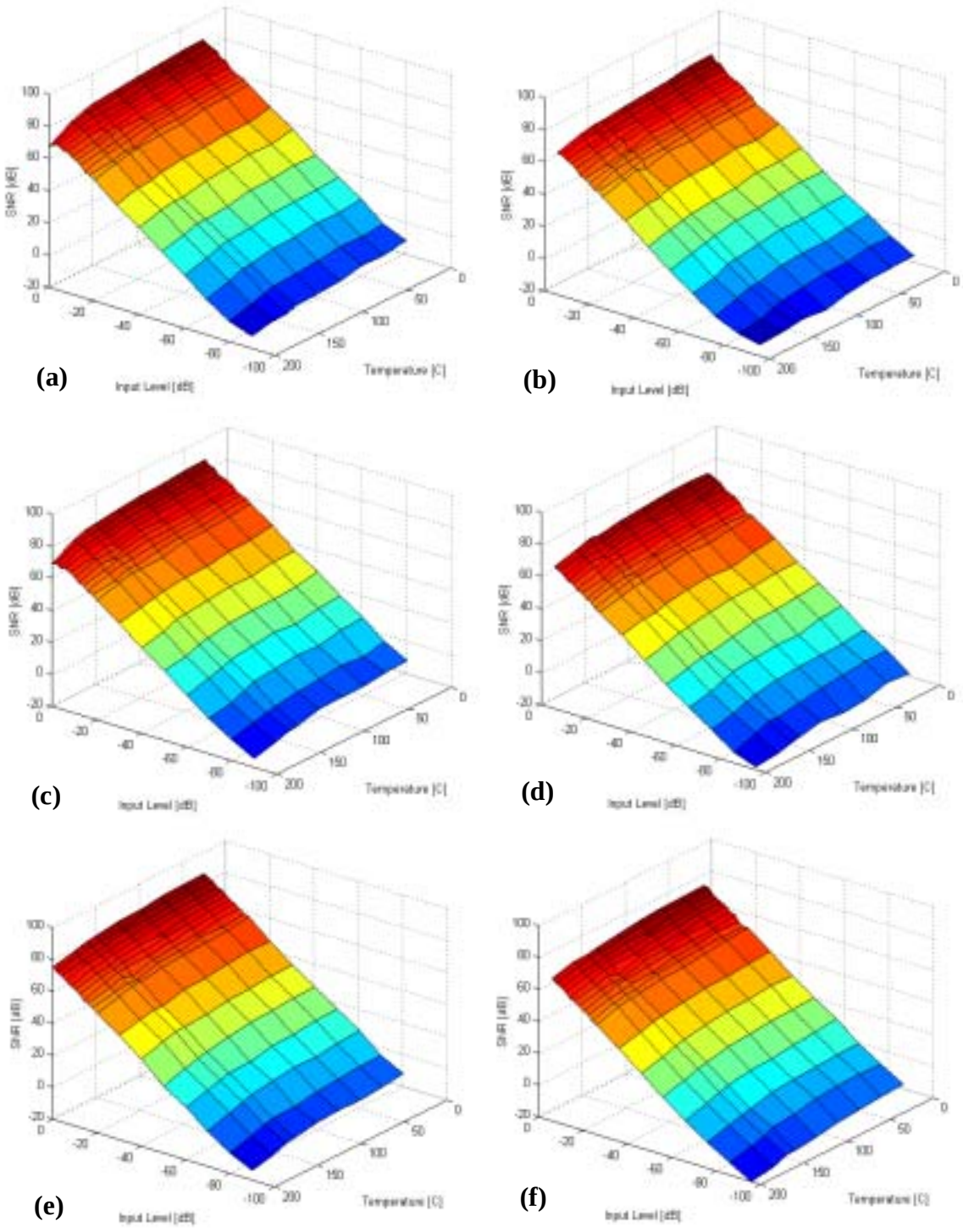


Figure 7.20 Measured SNR vs. input level and temperature - chip 2. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, (d) 4th order, f_{in}=144Hz, (e) 2nd order, f_{in}=950Hz, and (f) 4th order, f_{in}=950Hz.

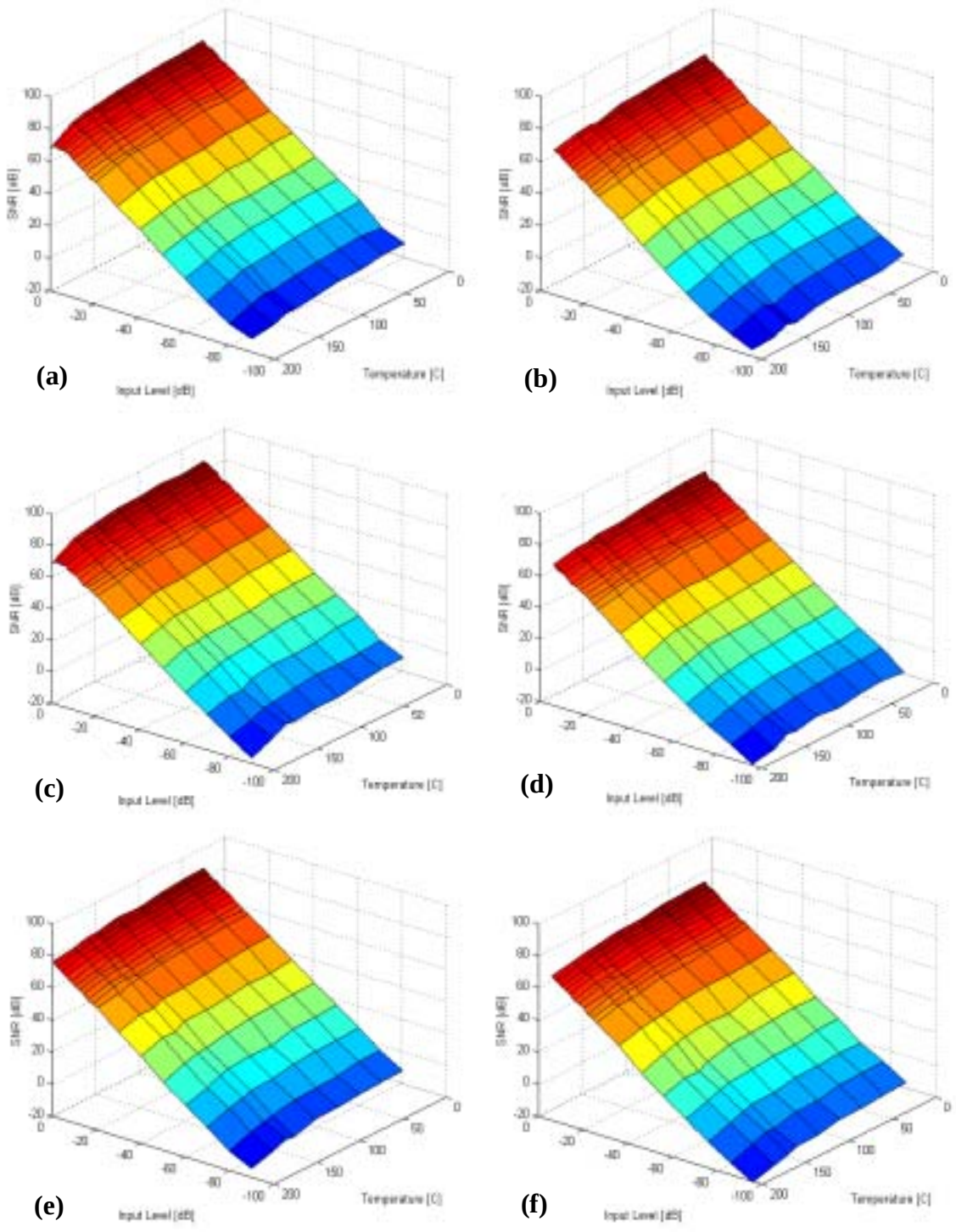


Figure 7.21 Measured SNR vs. input level and temperature - chip 3. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, (d) 4th order, f_{in}=144Hz, (e) 2nd order, f_{in}=950Hz, and (f) 4th order, f_{in}=950Hz.

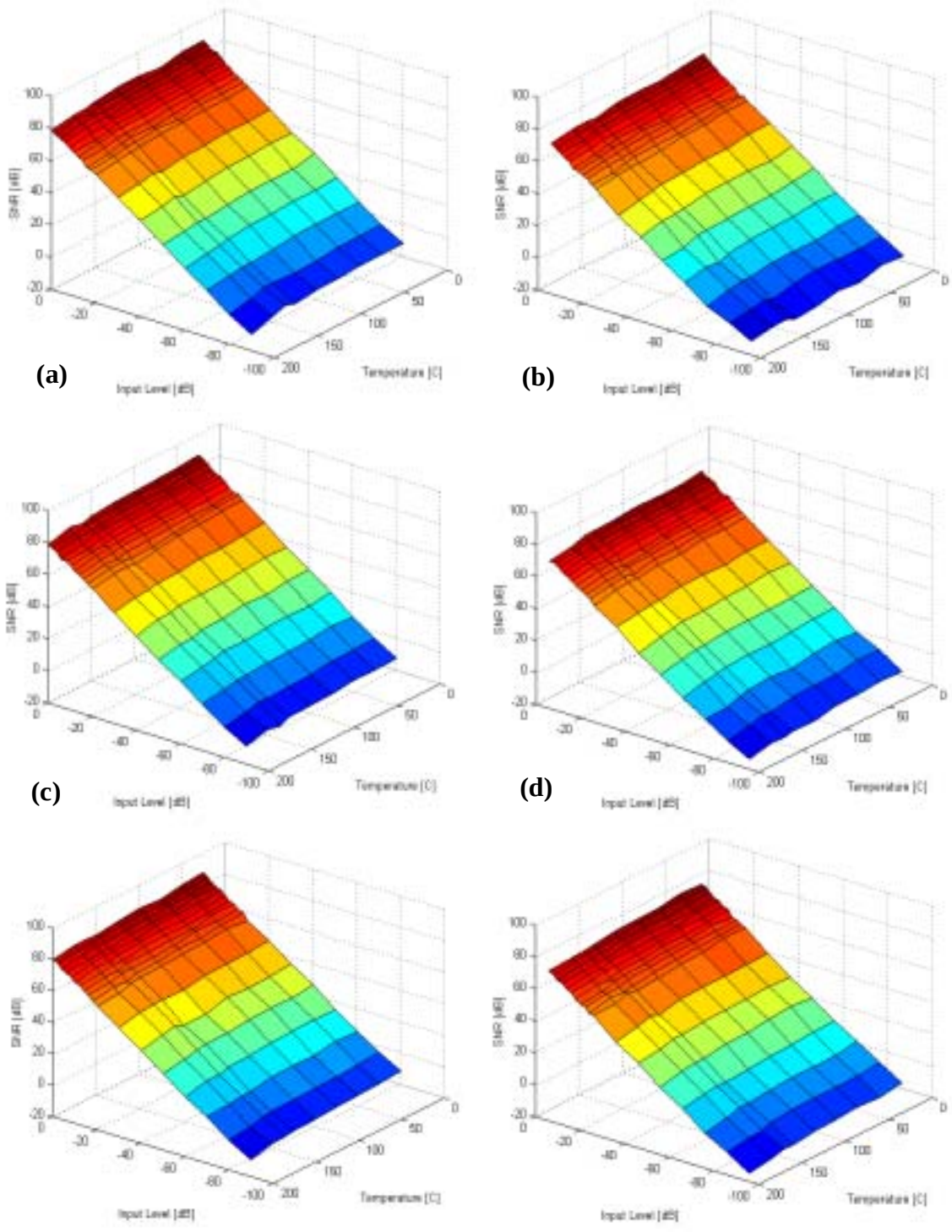


Figure 7.22 Measured SNR vs. input level and temperature - chip 4. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, (d) 4th order, f_{in}=144Hz, (e) 2nd order, f_{in}=950Hz, and (f) 4th order, f_{in}=950Hz.

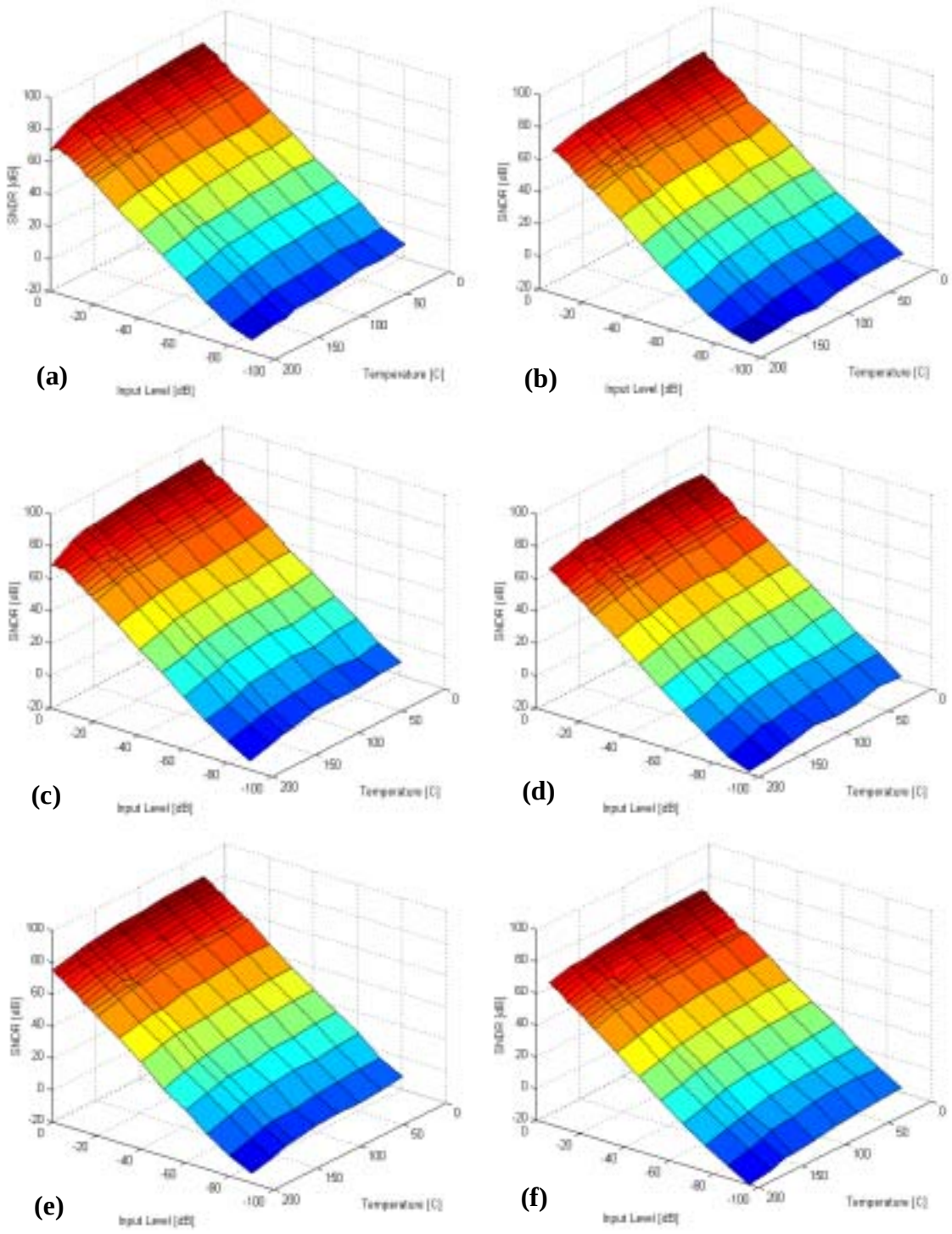


Figure 7.23 Measured SNDR vs. input level and temperature - chip 2. (a) 2^{nd} order, f_{in}=36.6Hz, (b) 4^{th} order, f_{in}=36.6Hz, (c) 2^{nd} order, f_{in}=144Hz, (d) 4^{th} order, f_{in}=144Hz, (e) 2^{nd} order, f_{in}=950Hz, and (f) 4^{th} order, f_{in}=950Hz.

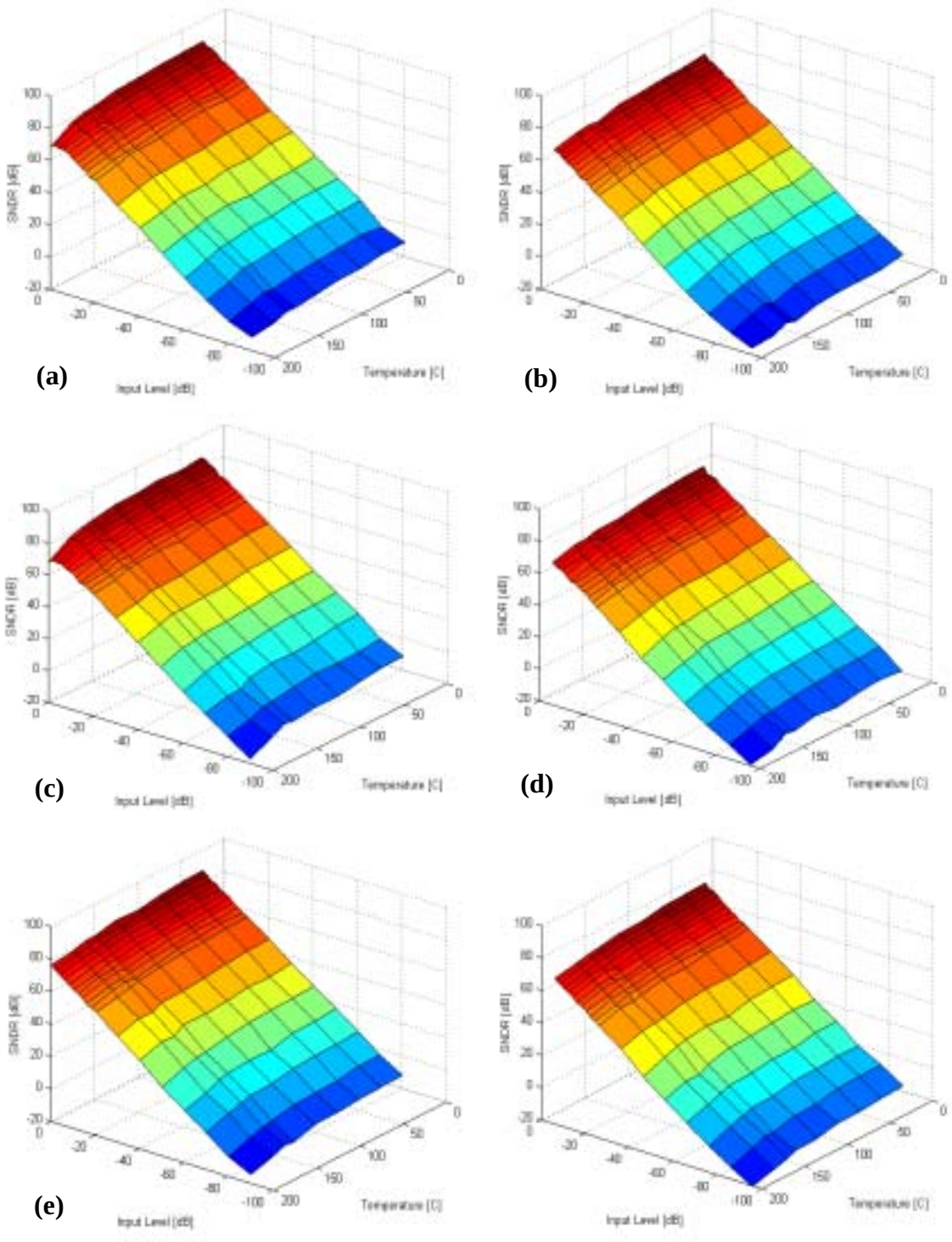


Figure 7.24 Measured SNDR vs. input level and temperature - chip 3. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, (d) 4th order, f_{in}=144Hz, (e) 2nd order, f_{in}=950Hz, and (f) 4th order, f_{in}=950Hz.

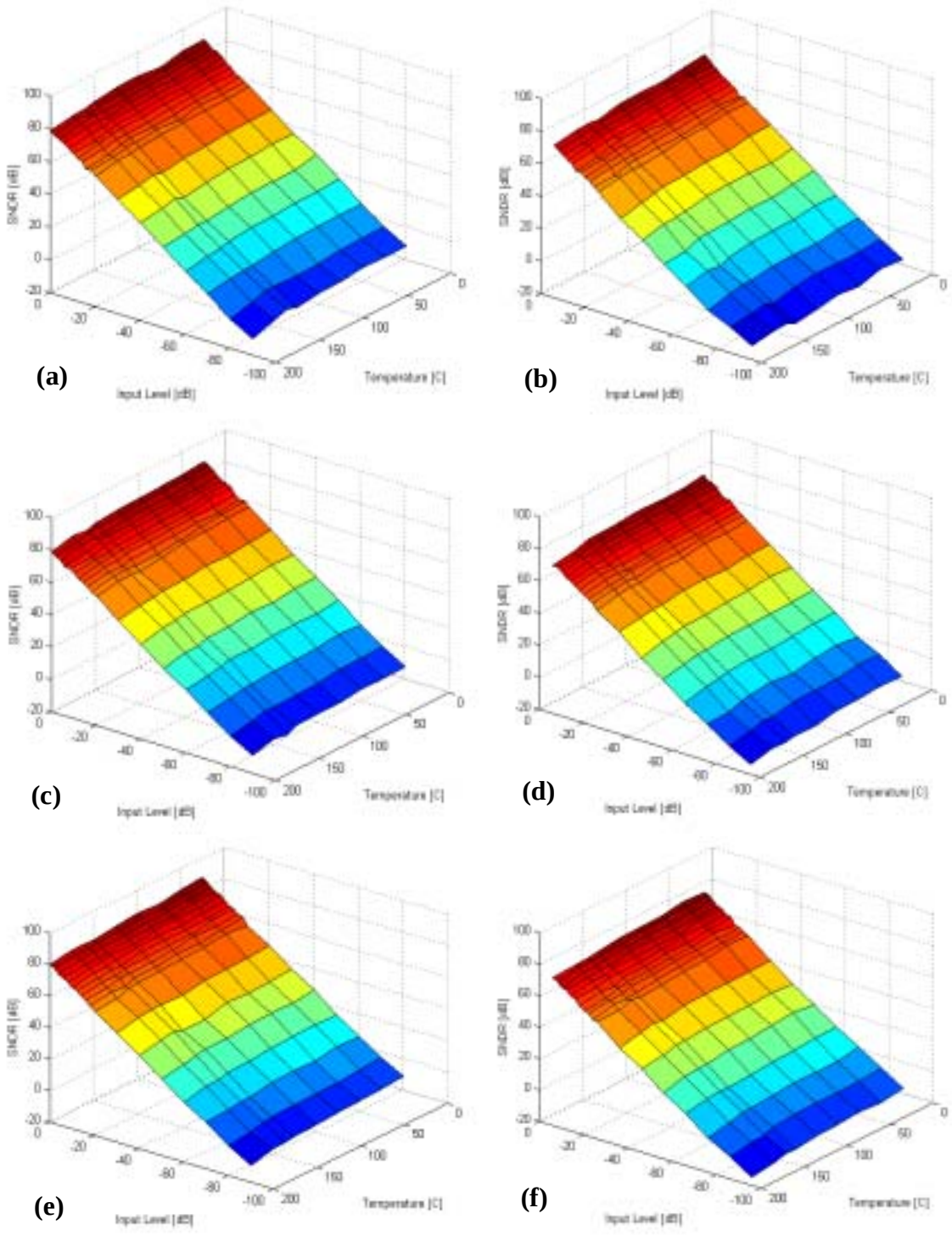


Figure 7.25 Measured SNDR vs. input level and temperature - chip 4. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, (d) 4th order, f_{in}=144Hz, (e) 2nd order, f_{in}=950Hz, and (f) 4th order, f_{in}=950Hz.

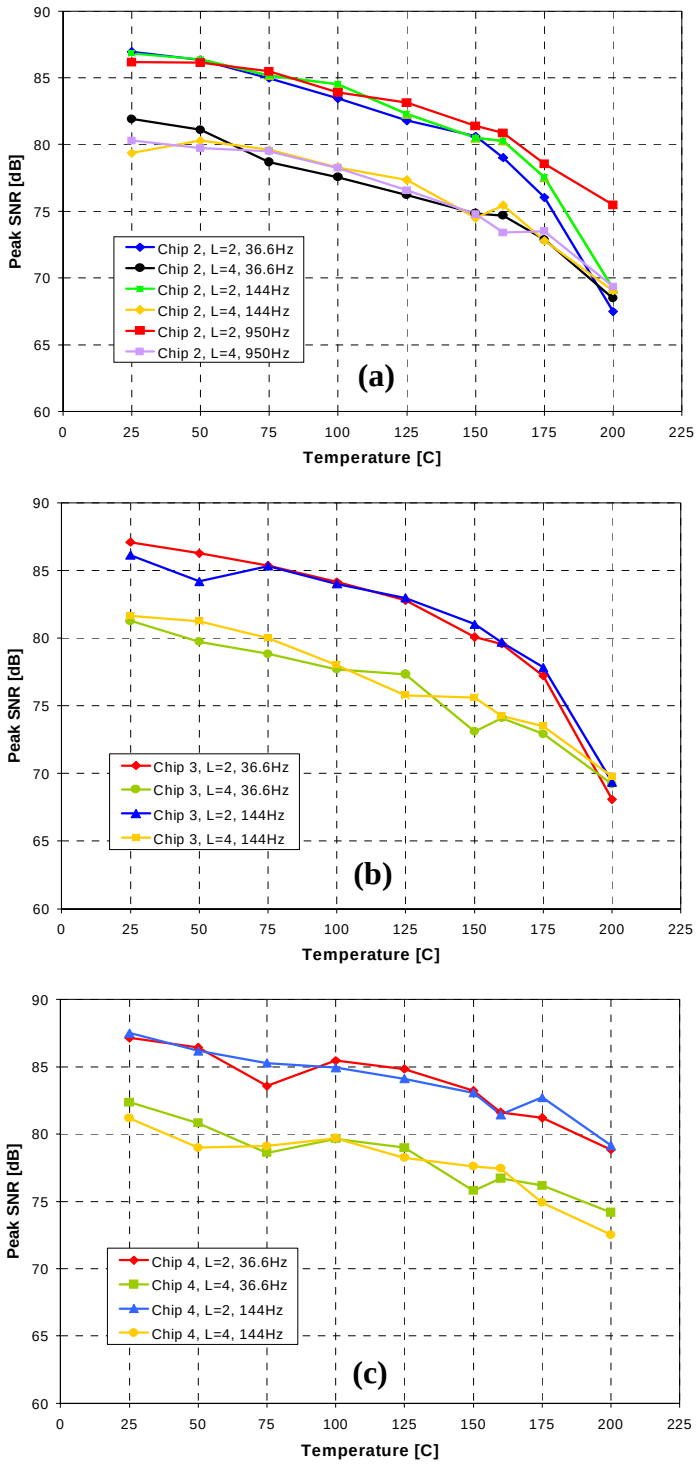


Figure 7.26 Measured peak SNR vs. temperature. (a) chip 2, (b) chip3, and (c) chip 4.

dependence on the input frequency for either order of modulator. In addition, the difference between the 2^{nd}- and 4^{th}-order curves is approximately 6 dB. This is the difference in the maximum signal amplitude input into the modulators. In Fig. 7.26 (b) and (c) the peak SNR plots for chips 3 and 4 also indicate little dependence on the input signal frequency. For further comparison, the peak SNR for all three chips with 144Hz input is shown in Fig. 7.27. Chips 2 and 3 exhibit similar performance. Chip 4 SNR degrades less with temperature than the other two chips. The reason for this is unknown. A larger statistical sampling of chips is needed to determine which temperature characteristic is most probable to occur. The peak SNR results for chips 2 and 4 are listed in Table 7.2 for 144Hz input frequency. These chips produced the best and worst results of the chips tested, in terms of SNR and SNDR.

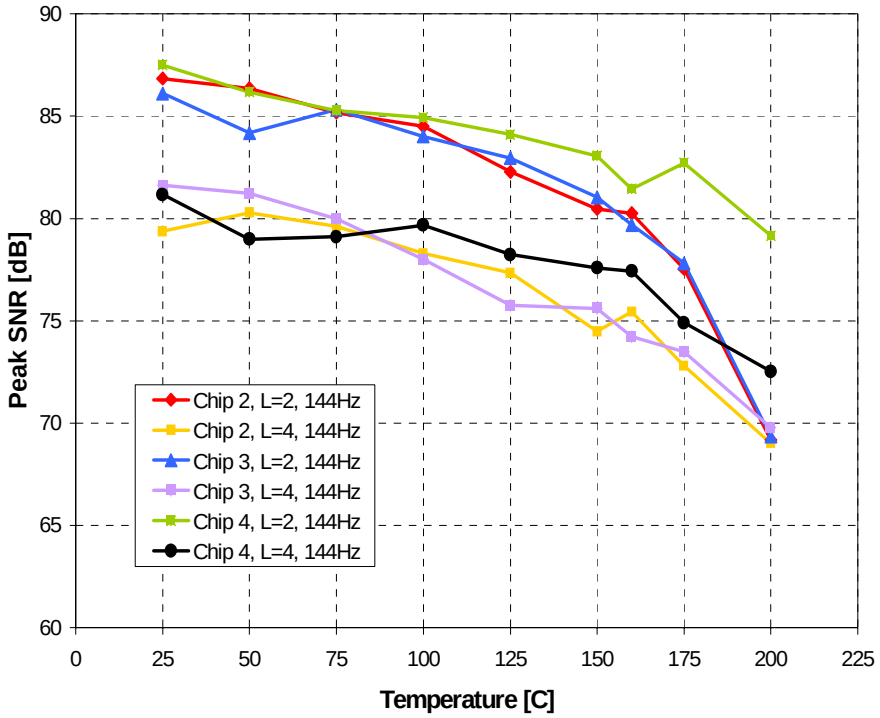


Figure 7.27 Measured peak SNR vs. temperature (all chips, 144Hz).

Table 7.2: Measured peak SNR vs. temperature (144Hz).

Temp. [° C]	Chip 2 Peak SNR (L=2) [dB]	Chip 2 Peak SNR (L=4) [dB]	Chip 4 Peak SNR (L=2) [dB]	Chip 4 Peak SNR (L=4) [dB]
25	86.85	79.37	87.50	81.17
50	86.37	80.29	86.18	78.99
75	85.18	79.61	85.28	79.11
100	84.51	78.29	84.94	79.69
125	82.28	77.34	84.11	78.24
150	80.48	74.49	83.06	77.60
160	80.26	75.45	81.45	77.44
175	77.54	72.80	82.72	74.91
200	69.18	69.04	79.16	72.53

7.4.4 Total Harmonic Distortion (THD) Measurements

THD was calculated from the modulator output spectra for the 3 tested modulator ASICs and is shown in Figures (7.28), (7.29), and (7.30) as a function of input level and temperature. The THD was calculated only for input frequencies of 36.6Hz and 144Hz and included the first 5 harmonic frequencies of these fundamentals. The 950Hz input was not calculated as its harmonics fall well outside of the modulator signal bandwidth (1kHz), and in practice will be significantly attenuated by the ΣΔ ADC digital filter. All chips demonstrate increased harmonic distortion for the 144Hz input than for 36.6Hz input. Note also that the harmonic distortion measured with any input frequency or input amplitude is only significant near 200° C. For temperatures around 150° C and lower, the

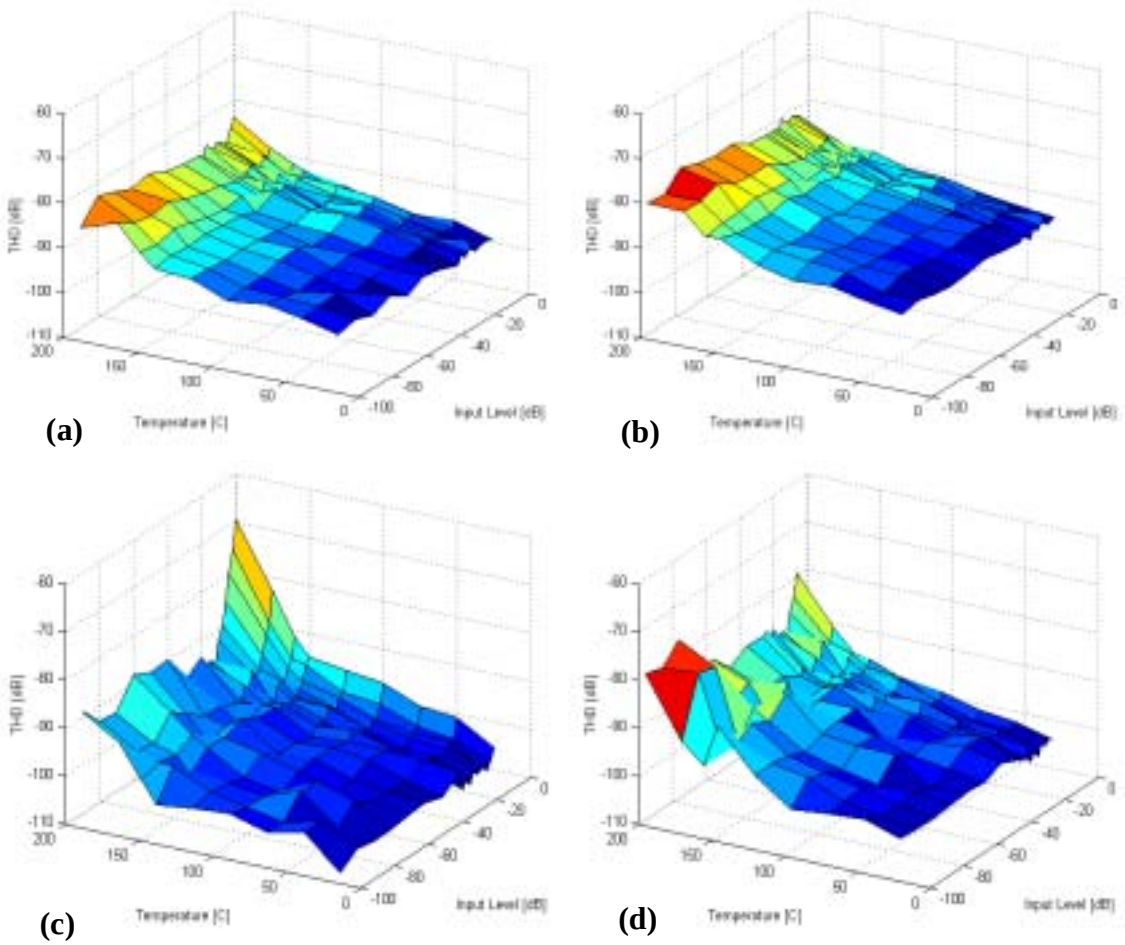


Figure 7.28 Measured THD vs. input level and temperature - chip 2. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, and (d) 4th order, f_{in}=144Hz.

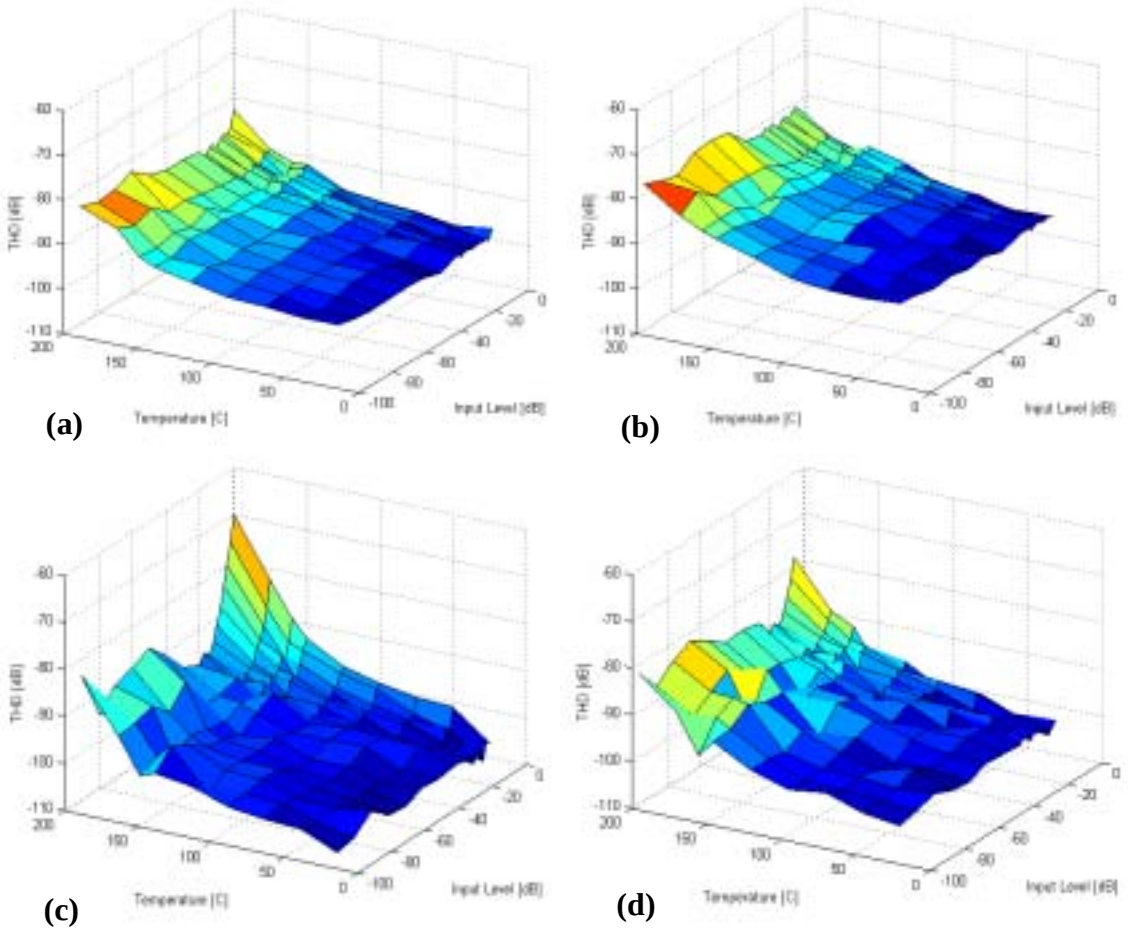


Figure 7.29 Measured THD vs. input level and temperature - chip 3. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, and (d) 4th order, f_{in}=144Hz.

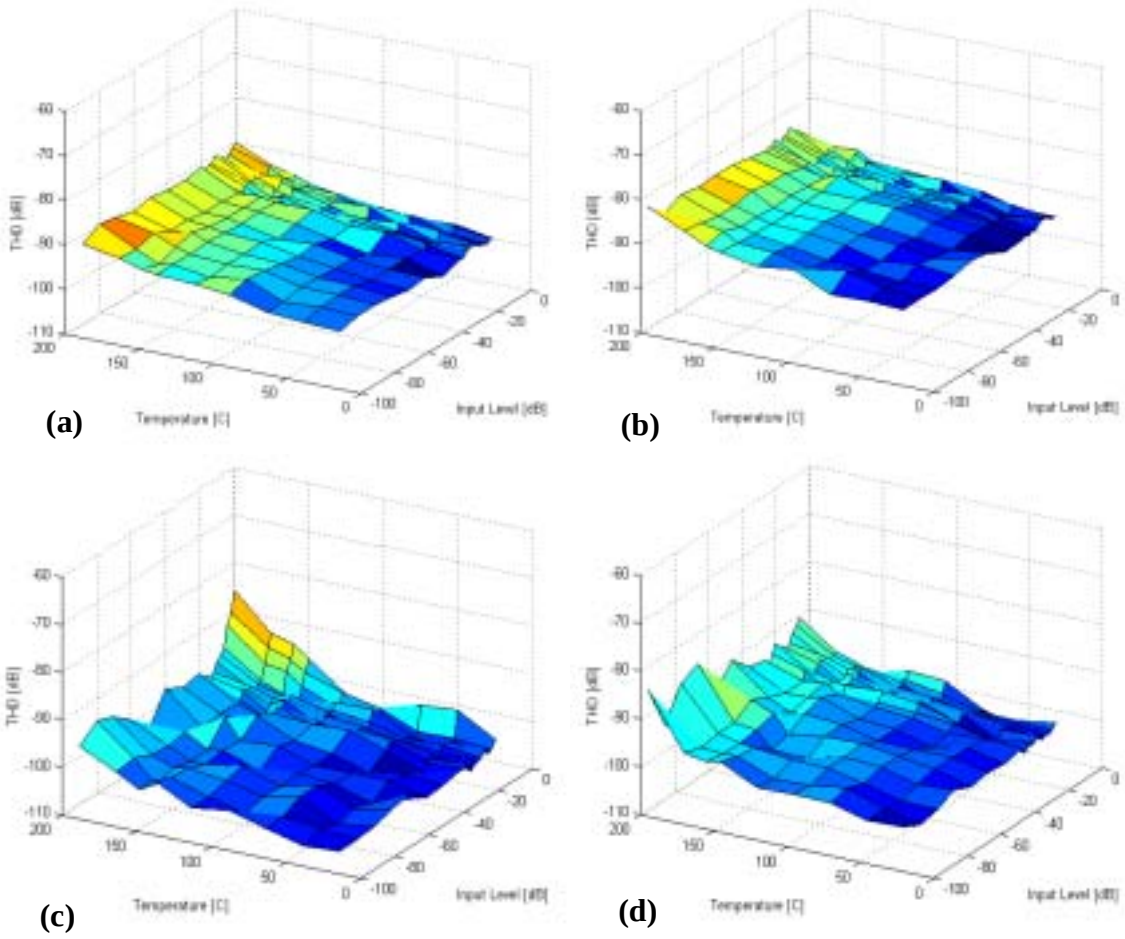


Figure 7.30 Measured THD vs. input level and temperature - chip 4. (a) 2nd order, f_{in}=36.6Hz, (b) 4th order, f_{in}=36.6Hz, (c) 2nd order, f_{in}=144Hz, and (d) 4th order, f_{in}=144Hz.

THD appears to decrease slowly, independent of the input signal amplitude. In this region, the THD is actually tracking the noise floor since there are no significant harmonic peaks to distinguish from the noise. The results of the SNR/SNDR tests indicate that under all test conditions, the harmonic distortion does not significantly degrade the modulator performance.

7.4.5 Dynamic Range Measurements

The dynamic range (DR) was extracted from the SNR plots using the graphical method shown in Fig. 7.31. Here, the x-axis intercept value provides the input signal amplitude (when the SNR equals 0dB) required for the DR calculation (see Eqn. 7.4). The SNR curve is fit to a straight line to compensate for SNR nonlinearity and observed nonlinearity of the signal source at very low amplitude levels.

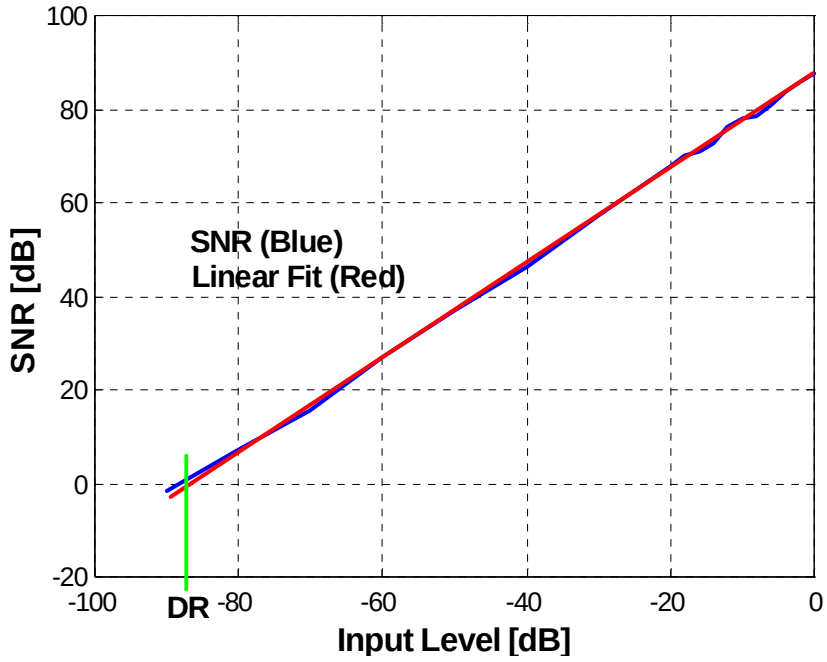
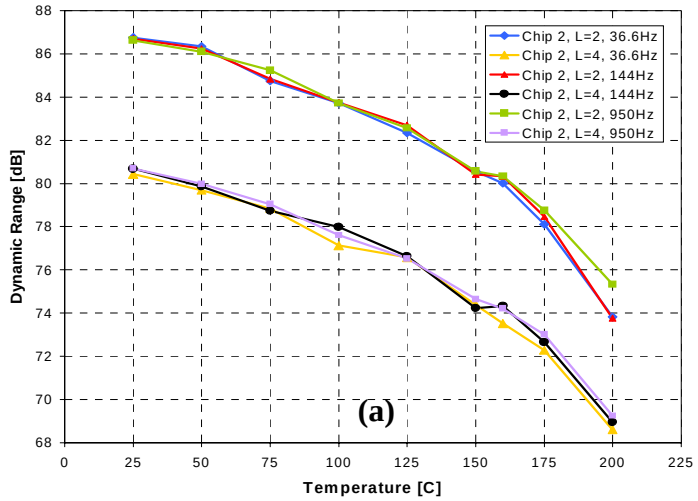
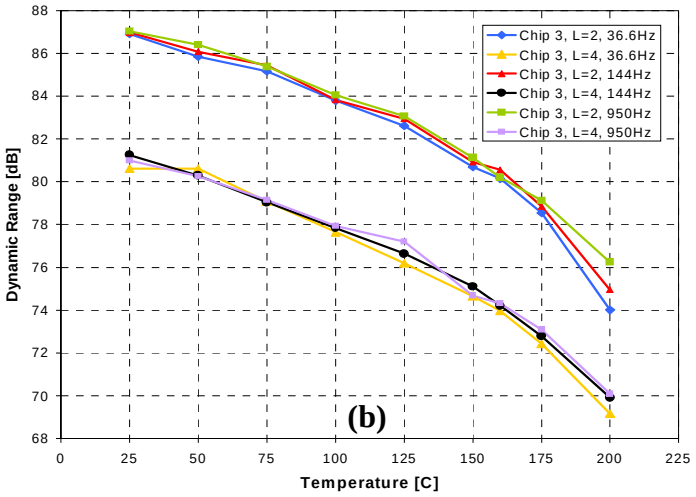


Figure 7.31 Dynamic range (DR) graphical calculation method.

The measured dynamic range values are shown separately for each chip tested in Fig. 7.32, as a function of temperature. Each plot shows curves for all combinations of modulator order (L=2, L=4) and input frequencies (36.6Hz, 144Hz, and 950Hz). Fig. 7.33 shows the same information for all chips on the same plot for comparison. As observed in the SNR measurements, all three chips exhibit approximately equivalent performance at low temperatures. However, chip 4 shows less degradation in SNR at elevated temperatures. Note that the L=4 modulator results are approximately 6dB less than the L=2 case. This is associated with the 50% reduction in input amplitude required for the L=4 modulator. Table 7.3 summarizes the DR results for each of the chips tested (144Hz input).

Notice the DR values are significantly higher at elevated temperatures than the peak SNR values provided earlier in the chapter. Referring to Fig. 7.34, the apparent degradation of the SNR with increasing temperature is primarily the effect of the noise floor increasing with temperature. Both the SNR and DR parameters incorporate this effect. However, at elevated temperatures the peak SNR value degrades near full-scale input. The DR calculation does not include this degradation because its value is calculated using the maximum input amplitude and the input amplitude required for unity SNR. Other large signal effects such as skirting about the fundamental will also not show up in the DR measurement but will degrade the SNR. Thus, the DR will typically be greater than the peak SNR and is usually reported in literature rather than the peak SNR.





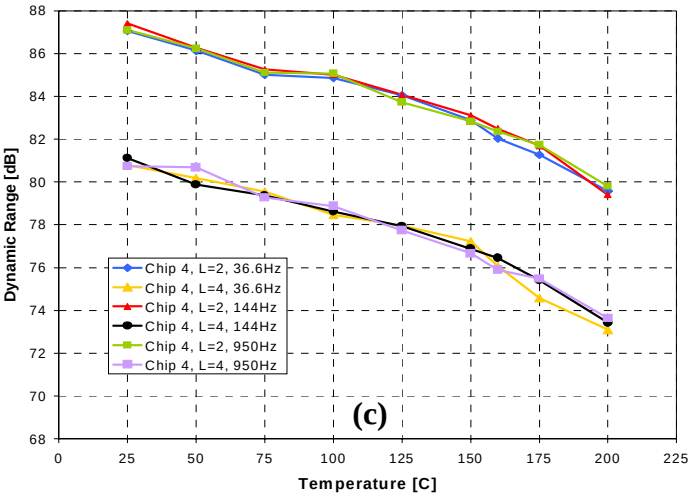


Figure 7.32 Measured DR vs. temperature: (a) chip 2, (b) chip3, and (c) chip 4.

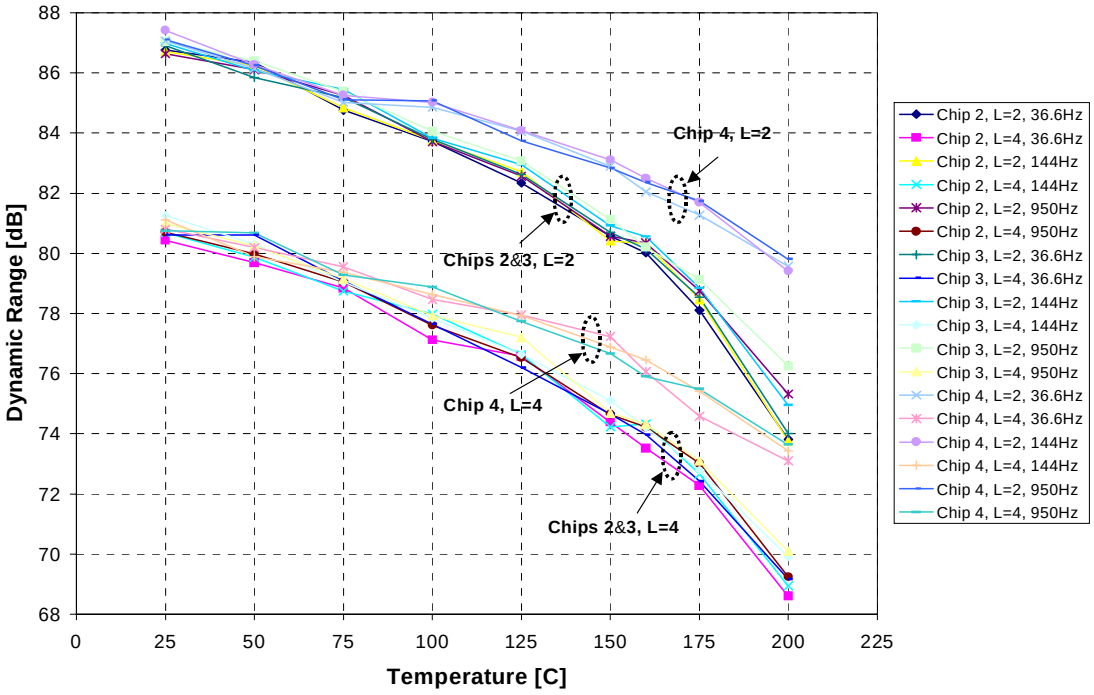


Figure 7.33 Measured DR vs. temperature for 2nd- and 4th-order modulator (chips 2, 3, and 4, f_{in}=36.6Hz, 144Hz, 950Hz)).

Table 7.3: Summary of measured DR vs. temperature.

Temp. [° C]	Chip 2 DR (L=2) [dB / bits]	Chip 2 DR (L=4) [dB / bits]	Chip 3 DR (L=2) [dB / bits]	Chip 3 DR (L=4) [dB / bits]	Chip 4 DR (L=2) [dB / bits]	Chip 4 DR (L=4) [dB / bits]
25	86.70 / **14.11**	80.68 / 13.11	86.97 / **14.15**	81.26 / 13.21	87.41 / **14.23**	81.12 / 13.18
125	82.70 / 13.44	76.63 / 12.44	82.95 / 13.49	76.64 / 12.44	84.08 / 13.67	77.94 / 12.65
150	80.42 / 13.07	74.23 / 12.04	80.92 / 13.15	75.11 / 12.18	83.11 / 13.51	76.89 / 12.48
175	78.46 / 12.75	72.66 / 11.78	78.85 / 12.80	72.78 / 11.80	81.69 / 13.28	75.42 / 12.24
200	73.76 / 11.96	68.94 / 11.16	74.95 / 12.16	69.92 / 11.32	79.41 / 12.90	73.43 / 11.90

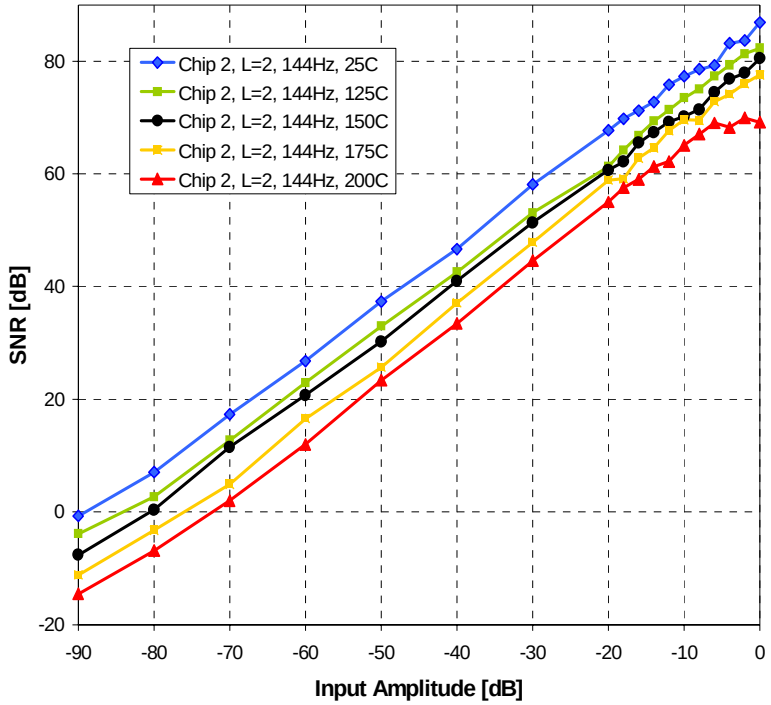


Figure 7.34 Measured SNR vs. input level & temperature (chip 2, L=2, f_{in}=144Hz).

7.4.6 SNR Results vs. Oversampling Ratio

The SNR offered by a particular order modulator is a strong function of the oversampling ratio (M). Recall that for a given signal bandwidth (*BW*), the oversampling ratio can be expressed as

$$M = \frac{f_s}{2BW}. \tag{7.6}$$

Therefore, the oversampling ratio is inversely proportional to the signal bandwidth. For very small bandwidths, the oversampling is large and the noise power in the SNR calculation is often dominated by the electronics noise power. As the input signal bandwidth is increased to frequencies near the point where the quantization noise dominates, the SNR

decreases drastically. This relationship is easily visualized by observing the modulator output spectra (Fig. 7.35). The frequency where the quantization noise comes out of the floor is a function of the modulator order.

The relationship between SNR and M can be best observed by plotting the SNR as a function of the $\log_2(M)$ as demonstrated in Fig. 7.36 for a 4^{th}-order modulator. In the region where M is sufficiently large, the SNR is dominated by electronics noise. Doubling M produces a limited but measurable increase in SNR. For small M, the SNR is dominated by the quantization noise and the performance degrades very quickly, particularly for higher-order modulators.

The measured peak SNR versus M is shown in Fig. 7.37 for chips 2 and 3, and in Fig. 7.38 for chip 4. Both figures show the resultant curves for 2^{nd}- and 4^{th}-order modulators at temperatures of 25°C, 125°C, 150°C, 175°C, and 200°C. The M of 256 chosen for this work appears to be sufficient for the L=2 case and more than sufficient for the L=4

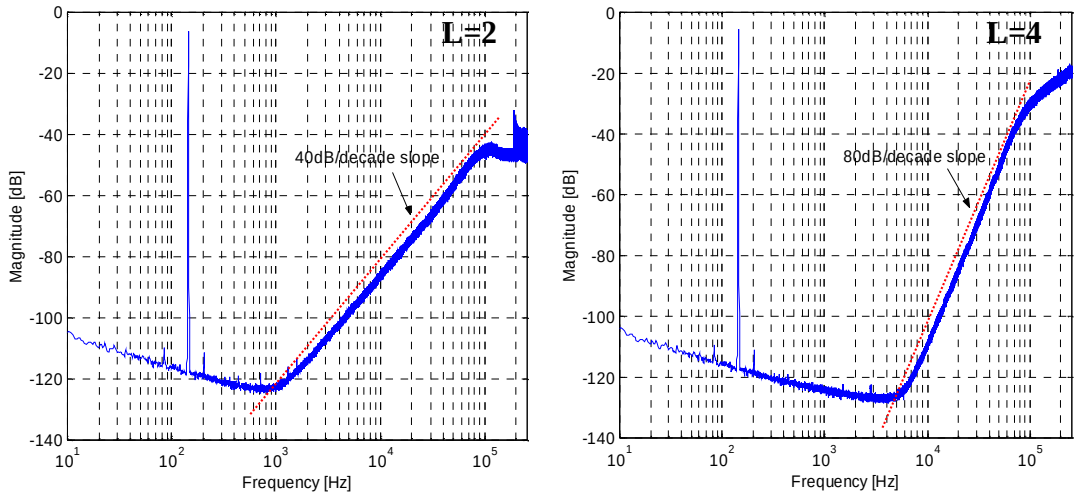


Figure 7.35 2^{nd}-and 4^{th}-order modulator output spectra.

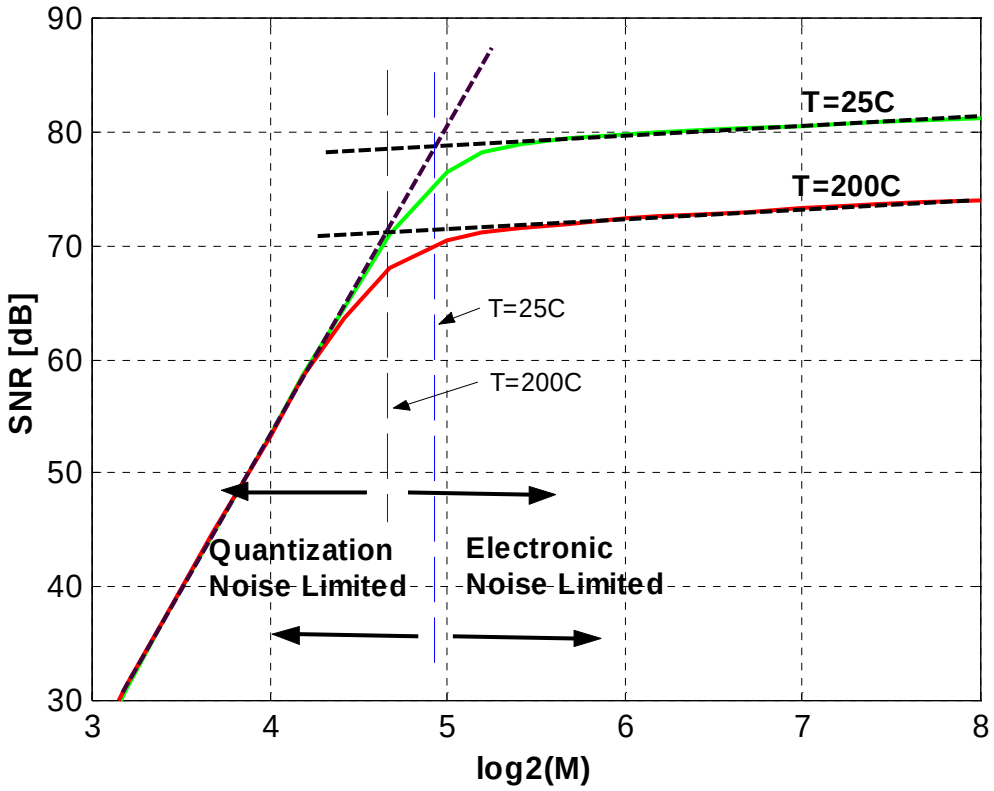


Figure 7.36 Effect of oversampling ratio (M) on modulator SNR performance.

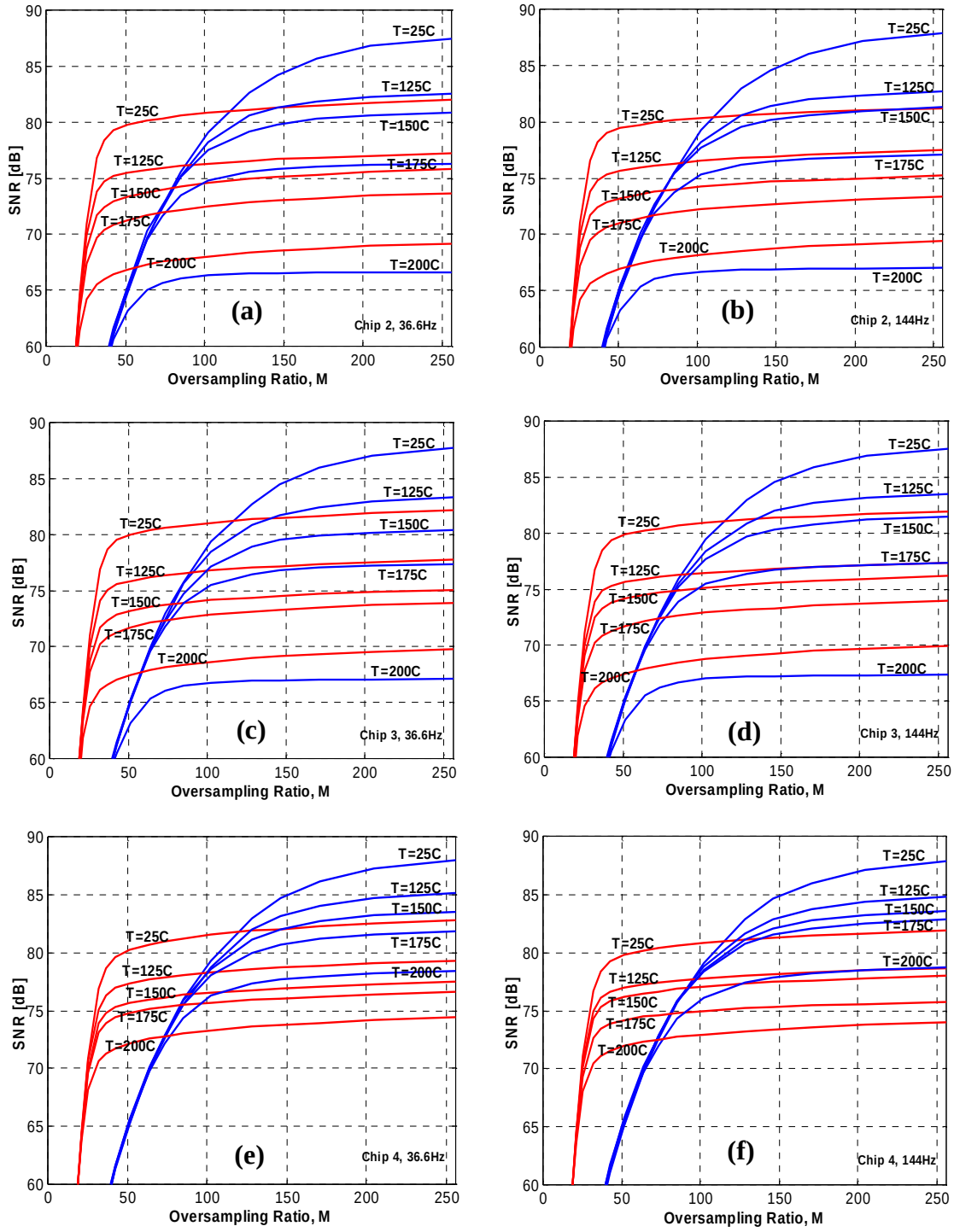


Figure 7.37 Measured peak SNR vs. OSR & temp. for chips 2 & 3. (a) chip 2, f_{in}=36.6Hz, (b) chip3, f_{in}=36.6Hz, (c) chip 2, f_{in}=144Hz, (d) chip 3, f_{in}=144Hz, (e) chip2, f_{in}=950Hz, and (f) chip3, f_{in}=950Hz. (Note: red curves are 2nd order; blue curves are 4th order).

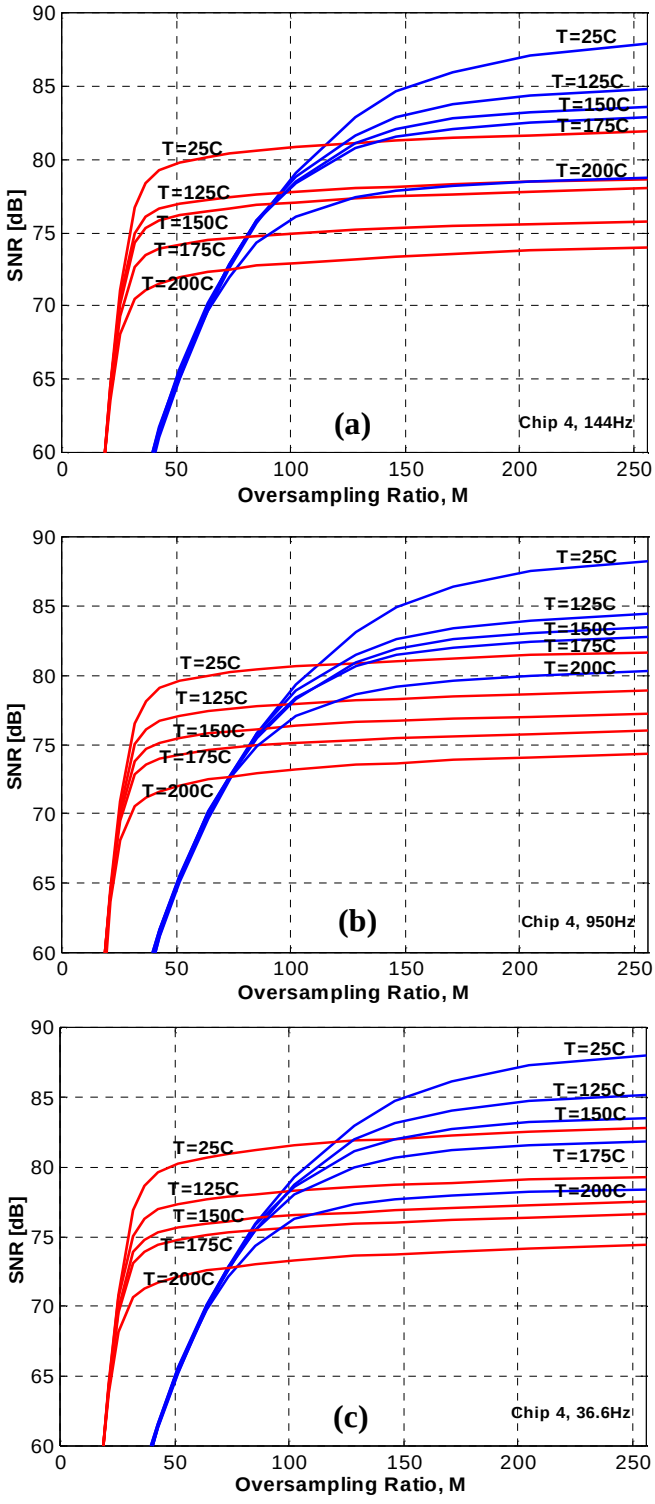


Figure 7.38 Measured peak SNR vs. OSR & temp. for chip 4. (a) f_{in}=36.6Hz, (b) f_{in}=144Hz, and (c) chip3, f_{in}=950Hz. (Note: red curves are 2nd order; blue curves are 4th order).

case. Again, chips 2 and 3 demonstrate similar performance while chip 4 shows less sensitivity to increased temperature. In general the data shows improved performance by the 2^{nd}-order modulator for oversampling ratios of 128 or more due to the reduced input dynamic range of the 4^{th}-order modulator as compared to the 2^{nd}-order modulator. With less oversampling, the 4^{th}-order modulator produces the best results. For oversampling ratios <~64, the 2^{nd}-order topology transitions into the quantization noise limited regime. Under any conditions, the 4^{th}-order becomes the best choice once the in-band 2^{nd}-order total noise is twice that of the 4^{th} order. For either order modulator, reducing the noise floor increases the SNR substantially up to the point where the in-band electronics noise and the in-band quantization noise are equal. With a fixed bandwidth, this noise limit is significantly lower for the 4^{th}-order modulator, due to improved quantization noise shaping.

The value of M associated with the transition from the quantization noise to electronic noise dominated regimes is obviously directly related to the electronic noise level. In future designs where the electronic noise is reduced due to better amplifier design and proper implementation of a $1/f$ noise reduction technique, the 2^{nd}-order modulator will show increased sensitivity to M (as compared to the data presented in this chapter). Given that the baseband quantization noise power is fixed, this sensitivity can only be reduced by reducing the baseband quantization noise power by increasing the sampling rate, the modulator order, or both.

7.4.7 Modulator Noise Measurements and Predictions

As previously mentioned, the flicker noise associated with MOSFET devices is a serious limiting factor in the design of low-noise analog electronics and is expected to dominate the input-referred noise characteristic of this modulator. In Chapter 5, two methods were introduced to reduce the overall effect of flicker noise - chopping and correlated double sampling (CDS). In this section, a comparative analysis of the modulator output noise with the chopper enabled and disabled is presented and discussed. The flicker and white noise components of the noise floor are identified and associated temperature dependencies discussed.

High flicker noise levels were observed in all of the previously presented modulator output spectrums. The level was so high that the 1/f noise corner occurs past the frequency where quantization noise begins to dominate the output spectrum of the 4^{th}-order modulator, completely masking the white noise. In order to push the quantization noise towards frequencies higher than the 1/f noise corner and thus reveal the white noise component, the modulator was operated at 2.048MHz sampling frequency (four times the intended frequency of 512KHz). Tests showed that operating at sampling frequencies higher than 2.048MHz introduced spurs into the output spectrum and artificially raised the apparent white noise level. A plot of the modulator output spectrum with f_s=2.048MHz is shown in Fig. 7.39 (T=25° C, 512 averages, f_{in}=144Hz). Here, the flicker noise component is clearly visible by its characteristic slope of 20dB per 2 decades in frequency. The white noise can be estimated from this plot as ~-127dB, though this value is not absolute due to the windowing and FFT operations. Unfortunately, the shaped quantization noise

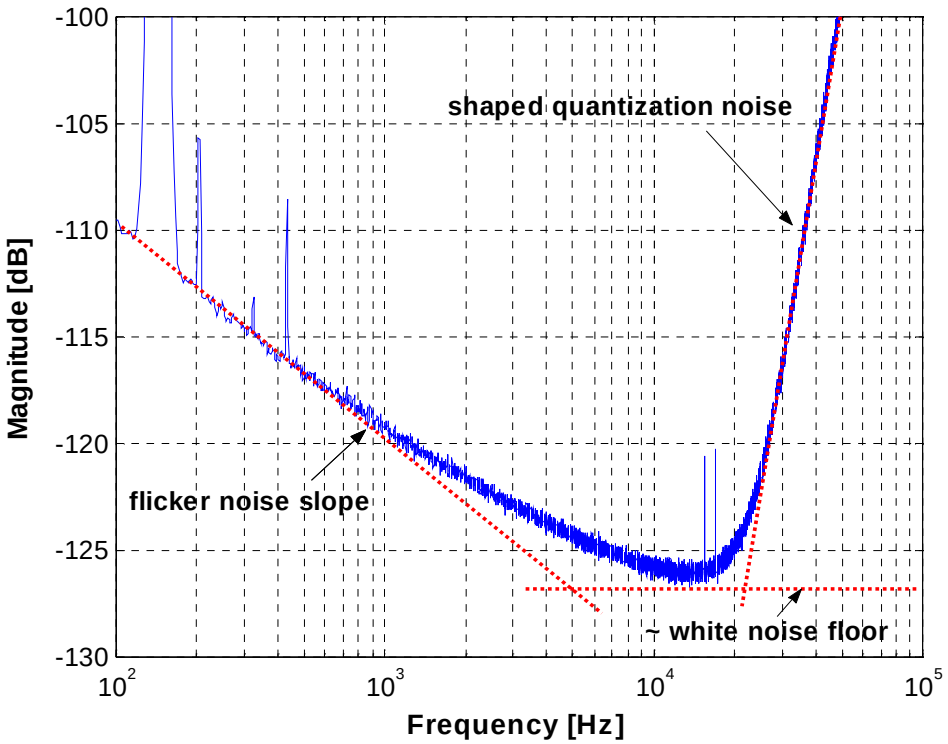


Figure 7.39 Modulator output spectrum showing flicker and white noise components.

begins to dominate before a more accurate value of the white noise is revealed. This plot clearly demonstrates the total dominance of the flicker noise in the signal bandwidth of interest (1kHz) and further supports the use of 1/f noise reduction methods.

The chopper circuit was enabled and the input signal swept from full-scale to -90dB of full-scale. An FFT average of 32 was applied to smooth the data and the output spectrum plotted as a function of input level (T=25°C, f_{in}=144Hz). Fig. 7.40 shows this output spectrum from 2 different perspectives, each plotted versus linear and log frequency scales. Note the spurs at regular intervals in the upper part of the spectrum for input amplitudes in the approximate range of -20dB to -70dB. Another group of less organized spurs occurs at frequencies below the input fundamental and generally increase as the

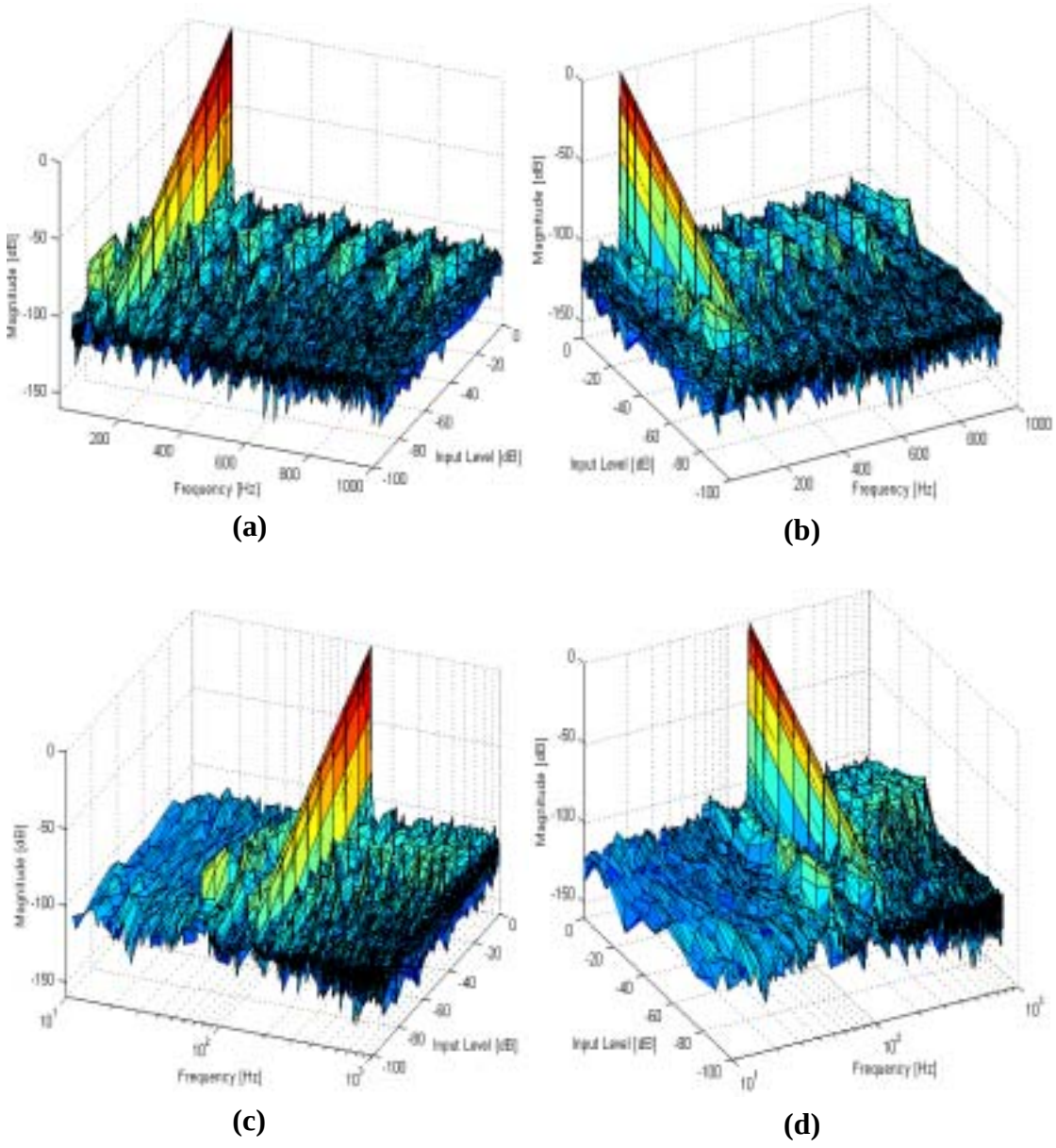


Figure 7.40 Modulator output spectrum with chopper enabled. (a)&(b) linear frequency scale, (c)&(d) log frequency scale.

input signal amplitude is decreased. The general behavior observed shows dependence on the input amplitude suggesting one possible explanation as signal dependent charge injection. However, it is apparent from these plots that the flicker noise observed in the unchopped case is reduced by enabling the chopper. The undesired spectral tones observed in the modulator output spectrum with the chopper enabled will be further discussed in the next section.

Further characterization of the noise was attempted by collecting a set of modulator data over temperature. The tests were performed with a full-scale, 144Hz input (32 averages) with both the chopper enabled and disabled at temperatures of 25° C, 125° C, 150° C, 175° C, and 200° C. The modulator output spectrums generated from this data are shown in Fig. 7.41. Near full-scale input amplitude was used (-6dB) to minimize the chopper-induced spurs. It was hoped that this test would allow observance of both the modulator white noise (with the chopper enabled) and flicker noise (with the chopper disabled). Though the chopper does appear to significantly reduce the flicker noise, the observed white noise floor is much higher than in the unchopped case. As mentioned in chapter 5, the chopping operation ideally does not increase the white noise component. Therefore, it appears the noise floor when chopped is actually additional wide band noise including quantization noise induced by the chopping operation. This undesired effect made it impossible to learn much about the white noise by enabling the chopper.

Although the data presented in Fig. 7.41 does not reveal much about the white noise behavior directly, much can be learned from the unchopped data in terms of both the flicker and white noise and associated temperature dependence. It is clear that the flicker noise component is increasing with temperature. In addition, some estimation of the white

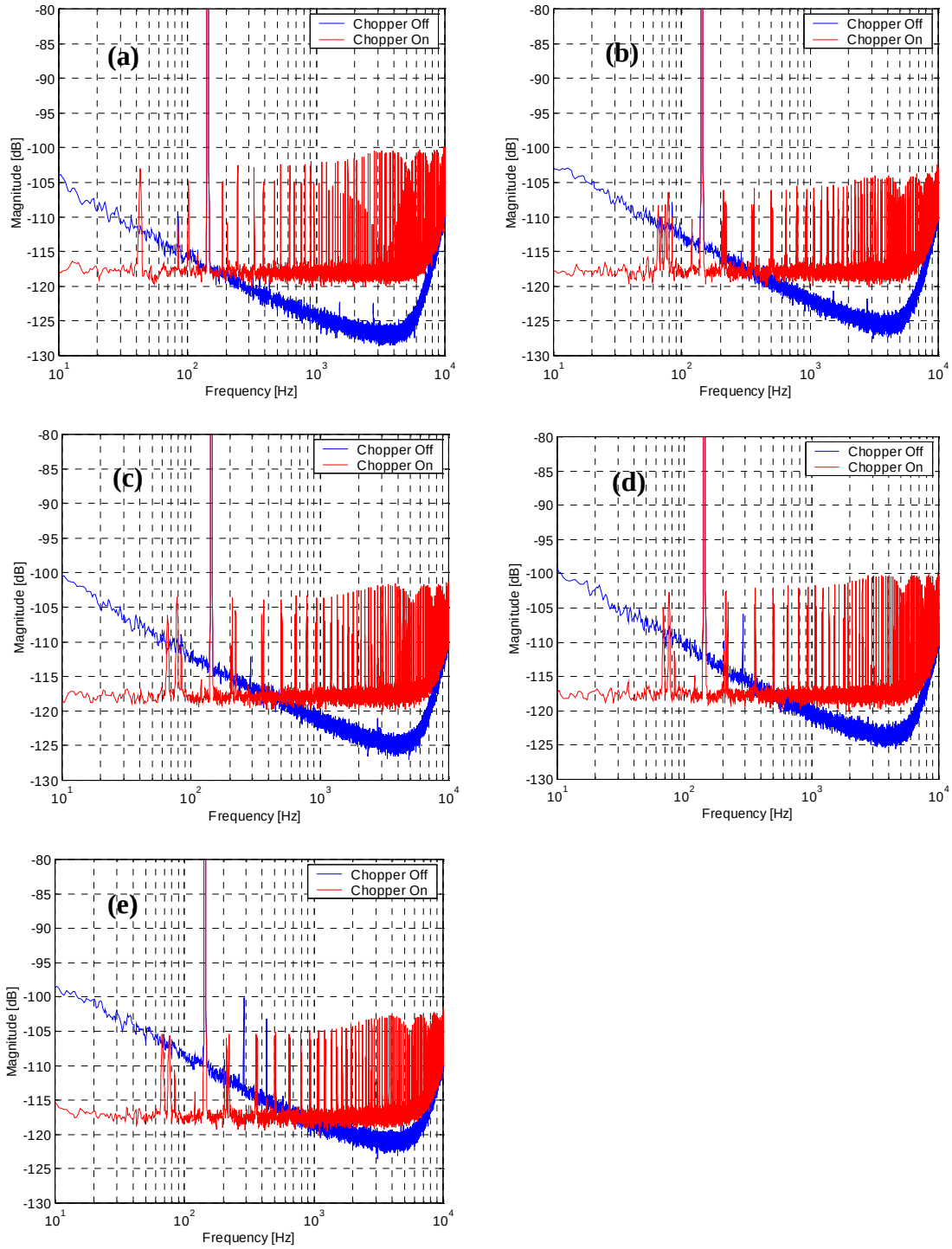


Figure 7.41 Comparison of chopped and unchopped modulator output vs. temperature. (a) T=25° C, (b) T=125° C, (c) T=150° C, (d) T=175° C, and (e) T=200° C.

noise component can be extracted from the unchopped plots by observing the noise near the frequencies where the quantization noise begins to dominate. Using this approach, spot values for the white noise and the flicker noise are shown in Table 7.4. These values are shown plotted in Fig. 7.42. Both the flicker and white noise appear to exhibit similar temperature dependence over the measured temperature range. Note that the spot noise values reported are referenced to the full-scale input signal.

7.4.8 Modulator Performance Prediction

A goal of this research is to provide a reasonable means for predicting the performance of improved modulator designs using both measured parameters from the fabricated modulator and simulation results. Two approaches were developed for addressing this need and are discussed in this section.

The first approach uses only the white noise contribution to predict modulator perfromance. This approach assumes proper implementation of a 1/f noise reduction technique

Table 7.4: Estimated relative output noise densities taken from measured data vs. T.

Temperature [°C]	flicker noise @ 10 Hz $[dBV/\sqrt{Hz}]$	flicker noise @ 100 Hz $[dBV/\sqrt{Hz}]$	flicker noise @ 1kHz $[dBV/\sqrt{Hz}]$	white noise approximation $[dBV/\sqrt{Hz}]$
25	-106	-115	-124	-127
125	-102.5	-112.5	-122	-126
150	-100.5	-112	-121.5	-125
175	-99	-110	-120	-123.5
200	-97.5	-108	-118	-121

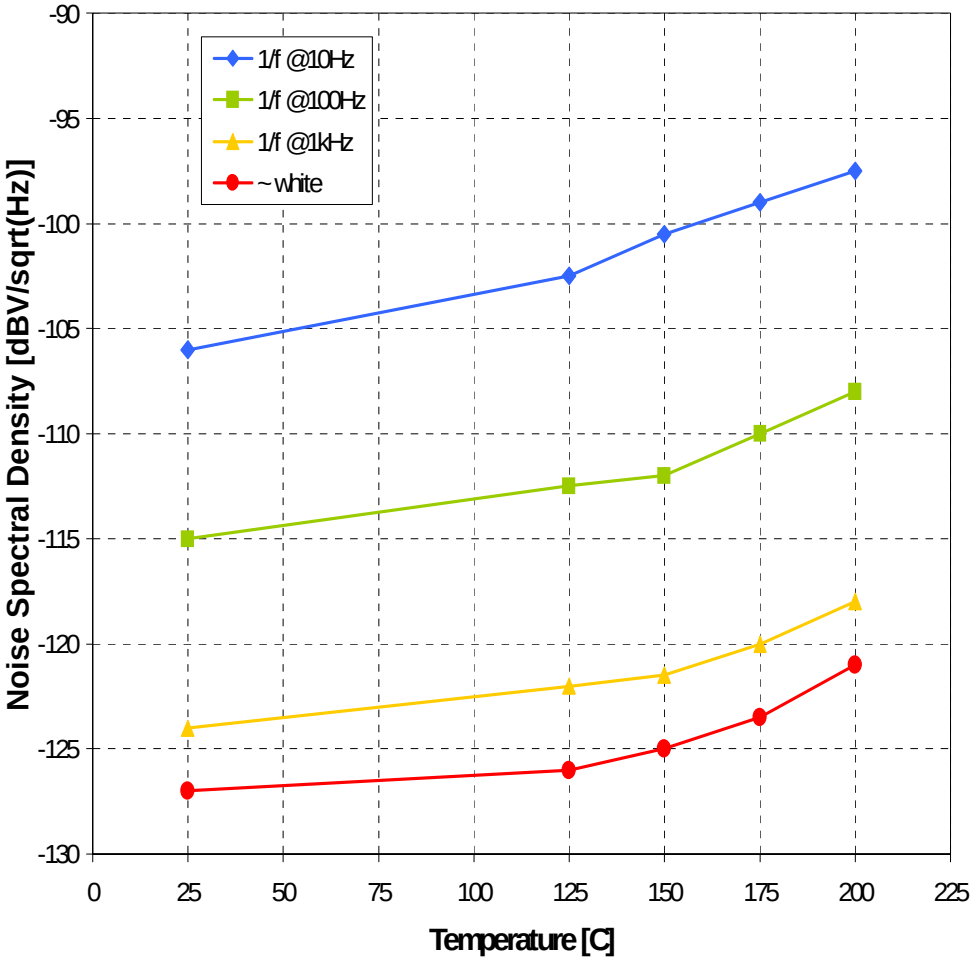


Figure 7.42 Output noise spectral densities from measured data vs. temperature.

such as chopping or CDS. Using the approximate white noise spectral densities of Table 7.4 (measured as a function of temperature), the theoretical SNR was calculated over a 1kHz bandwidth These values are shown in Table 7.5 and are compared to measured SNR data shown earlier in this chapter. Note that the signal power is also calculated assuming a full-scale fundamental signal (equal to 6.64dB for the 2^{nd}-order modulator) For the 4^{th}-order modulator, 6dB was subtracted due to the restricted input range of the cascaded structure. Though somewhat ideal, this method indicates that >16 bits @ T=25°C and >15 bits @ T=200°C are obtainable. Clearly, a significant resolution improvement can be obtained by proper implementation of a 1/f noise reduction technique.

Another approach was also investigated to better predict the potential for improving the resolution of the modulator. Rather than using the measured modulator output spectra and calculating the SNR, both measured and predicted modulator input noise and opamp

Table 7.5: Comparison of measured and predicted modulator performance vs. temperature. (chip 4, 4^{th} order, reference input power = 0.645dB).

Temp. [°C]	Measured Peak SNR [dB]	Resolution (from Meas. Peak SNR) [bits]	Predicted Peak SNR with 1/f reduction [dB]	Predicted Resolution (from Peak SNR) [bits]
25	87.50	14.24	102.3	16.7
125	84.11	13.68	101.0	16.5
150	83.06	13.51	100.5	16.4
175	82.72	13.45	98.7	16.1
200	79.16	12.86	96.3	15.7

characteristics were used to calculate the present design input peak SNR, and to predict the potential peak SNR of a lower flicker noise design. Note that the input SNR and output SNR should have equivalent values. A Matlab noise model was generated that uses input-referred voltage spectral densities measured for the first stage integrator opamp. Two points of the measured flicker eni are input and used to fit a linear-in-log voltage spectral density with 1 Hz frequency resolution. The estimated white noise voltage spectral density is also input along with the estimated amplifier noise bandwidth. Using these parameters, the folding factor is calculated for the modulator and the baseband noise power associated with the opamp flicker noise and aliased white noise is computed. The theoretical baseband quantization noise power is also added to this noise power along with an implementation loss term. Using this approach, the input SNR was determined for the 2^{nd}-order modulator at room temperature using both the current design measured opamp noise data, and simulation results from an improved opamp design using the fitted device noise models (see Fig. 7.43 for noise data summary). Conservative values for the opamp white noise (6 $nV/\sqrt{Hz}$) and implementation loss (1dB) were used. The noise bandwidth used was 40.8 MHz (GBW=13 MHz). The results of this simulation are summarized in Table 7.6. These results indicate that a peak SNR of 15.5 bits is achievable with the 2^{nd}-order modulator without application of a chopper or CDS technique, by careful redesign of the integrator opamp for lower $1/f$ noise. In addition, the peak SNR calculated using the original opamp agrees extremely well with the measured peak SNR for the 2^{nd}-order modulator at room temperature (~14.1 bits). Note that this prediction technique was used only

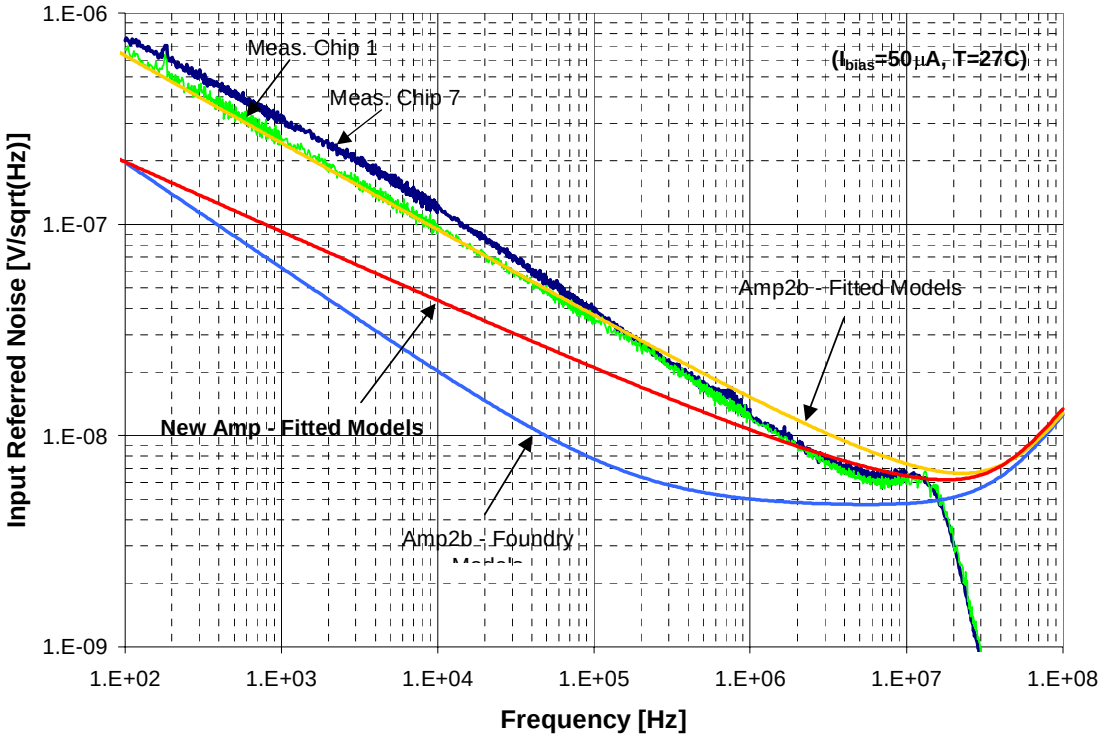


Figure 7.43 Measured and simulated eni using foundry supplied and fitted noise models.

Table 7.6: Calculated peak SNR for 2nd-order modulator (T=25°C).

Design	eni white [$nV/\sqrt{Hz}$]	eni flicker @ 100Hz [$V/\sqrt{Hz}$]	eni flicker @ 1kHz [$V/\sqrt{Hz}$]	Peak SNR [dB / bits]
Original Amp2b	**6.0**	**8e-7**	**3e-7**	**86.7 / 14.1**
Improved Amp2b	**6.0**	**1.9e-7**	**9.3e-8**	**96.9 / 15.8**

with measured room temperature noise data because integrator amplifier noise measurements were not made at any other temperatures.

7.4.9 Tonal Behavior

Tonal behavior is a phenomenon observed in low-order modulators with very low amplitude or dc inputs[142]. Without dynamic input signals, the modulator output bits form pseudo-repetitive patterns that cause idle tones to occur near $f_s/2$. Empirical observations reported by Norsworthy indicate the tonals occur at specific frequencies defined by

$$f_{tones} = \frac{nf_s|A_{dc}|}{2\Delta} \qquad n = \{0, 1, 2, \ldots\} \tag{7.7}$$

where Δ is the quantization step size and $|A_{dc}|$ is the magnitude of the dc input level [142]. These tones may also result from low frequency errors associated with the modulator circuit including opamp input offset voltages, and charge injection errors.

The tones observed in the 2nd-order modulator near $f_s/2$ with an input signal equal to -100dB of full-scale are shown in Fig. 7.44 (chopper disabled). Also shown are the associated baseband spectra of the 2nd- and 4th-order modulators. Note that some very weak tones show up in the baseband of the 2nd-order modulator that are not present in the 4th-order output spectrum. This observed reduction is the result of the additional randomizing effect associated with higher order modulation. With Δ = 2V, (+1V to -1V), the value of $|A_{dc}|$ required to produce the tones observed in the 2nd-order modulator is ~2.5mV (according to [7.2]). This value is consistent with typical CMOS opamp input offset voltages. The demodulation of tones near $f_s/2$ into the modulator baseband exhibited in the

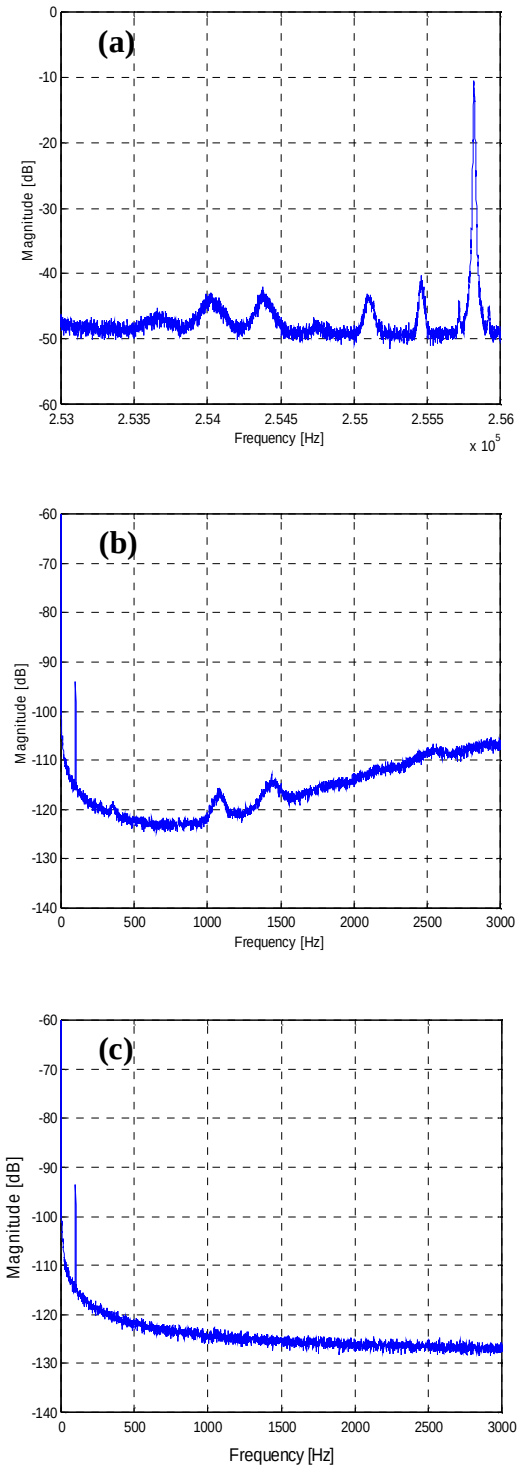


Figure 7.44 Demodulation of tonals into baseband (chopper disabled). (a) tonals near $f_s/2$ (b) 2nd-order modulator baseband spectrum (c) 4th-order modulator baseband spectrum.

2^{nd}-order modulator can be the result of either coupling of clocks into the feedback error voltage references, or integrator opamp non-linearity. Effective bypassing and opamp design usually keep these undesired effects minimized.

The tones observed in the 2^{nd}-order modulator near $f_S/2$ with the chopper enabled are shown in Fig. 7.45. Also shown are the associated baseband spectra of the 2^{nd}- and 4^{th}-order modulators, also with the chopper enabled. Tones similar to those observed with the chopper off, were observed around $f_S/2$ with the chopper on. However, a significant amount of spectral tones were seen in the baseband due to demodulation. The reason for this undesirable effect is due to a poor choice of chopping frequency. Though choosing the chopper to operate at $f_S/2$ minimizes the $1/f$ noise contribution from the frequency shifted images, this selection of chopping frequency causes a direct demodulation of the tones near $f_S/2$ into the baseband. This is clearly demonstrated in Fig. 7.45 where the tones in (a) are mirrored into the spectra of (b) and (c). There are two ways to address this problem: eliminate the source of tonals or change the chopper frequency. Eliminating the tonals requires implementation of a higher-order single-loop modulator, which involves an overall redesign of the modulator. Therefore, better selection of the chopping frequency is the preferred solution. The chopper frequency determines how far the flicker noise is shifted in frequency from the baseband, and resultantly determines the amount of flicker noise power present in the baseband. In addition, since the chopper clock is a square wave, it contains the fundamental frequency as well as the even harmonics of the chopper fundamental. This will cause additional images of the flicker noise spectrum that must also be considered in determining the efficacy of the chopper frequency chosen. The

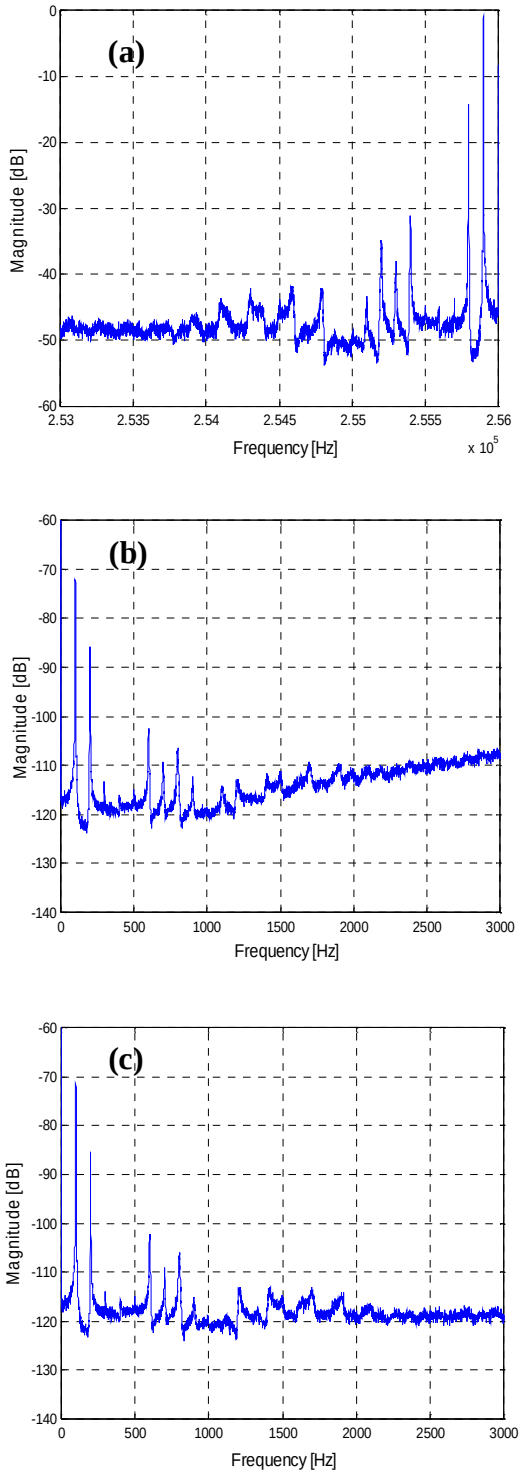


Figure 7.45 Demodulation of tonals into baseband (chopper enabled). (a) tonals near $f_s/2$ (b) 2nd-order modulator baseband spectrum (c) 4th-order modulator baseband spectrum.

selection of chopper frequency will require additional modeling and is considered part of the future work associated with this research.

7.4.10 Modulator Power Measurements

The power consumption of the partitioned power supplies of the modulator chip operating with a sampling clock of 512kHz were measured as a function of temperature. The supply partitions are defined in Table 7.7 and the measured power consumption is summarized in Table 7.8.

7.4.11 Modulator Experimental Results Summary

A summary of the modulator test parameters is given in Table 7.9. The modulator test results over temperature for chip 4 are summarized in Table 7.10. Experimental results indicate that the 2^{th}-order modulator is capable of 87.41dB (14.23 bits) of resolution at T=25°C and 79.41dB (12.90 bits) at T=200°C. The 4th-order produced 81.12dB (13.18 bits) and 73.43dB (11.90 bits) at T=25°C and T=200 °C, respectively. The additional quantization noise shaping advantages offered by the 4^{th}-order structure were unrealized due to the high flicker noise of the first stage integrator opamp. However, the 4^{th}-order modulator demonstrated improved idle tone suppression and was shown to operate far into the electronic noise limited regime, allowing increased input bandwidths with moderate decrease in SNR. Using estimated values for measured white noise, the modulator is theoretically capable of achieving resolutions of 16.7 bits at 25°C and 15.7 bits at 200°C. Improvements in chopper performance can be obtained by better selection of a chopping frequency that minimizes folding of the spectral tones near $f_s/2$ into the baseband. As the

Table 7.7: Modulator power supply partitioning.

Supply	Function Partition
A_{Vdd1}	Integrator 1 & 2 (Loop 1)
A_{Vdd2}	Integrator 3 & 4 (Loop 2)
$A_{Vddcmp1}$	Comparator (Loop 1)
$A_{Vddcmp2}$	Comparator (Loop 2)
D_{Vdd}	All digital circuits

Table 7.8: Modulator measured power consumption vs. temperature.

Temperature [° C]	A_{Vdd1} [mW]	A_{Vdd2} [mW]	$A_{Vddcmp1}$ [mW]	$A_{Vddcmp2}$ [mW]	D_{Vdd} [mW]	Total [mW]
25	9.27	9.87	0.293	0.309	13.46	33.21
125	9.17	9.60	0.288	0.296	13.23	32.60
150	9.17	9.57	0.287	0.295	13.20	32.53
175	9.21	9.64	0.289	0.295	13.17	32.59
200	9.31	9.70	0.292	0.297	13.13	32.73

Table 7.9: Modulator test parameters.

Sampling Rate	512kHz
Oversampling Ratio	256
Supply Voltage	3.3V
Signal Bandwidth	1kHz
Differential Input Range	2V
Differential Error Ref	4V
Active Area	~ 10 mm^2
Technology	0.5μm SOS-CMOS

Table 7.10: Measured performance summary vs. temperature (chip 4).

Temp. [° C]	**DR (L=2) [dB]**	**DR (L=4) [dB]**	**Peak SNR (L=2) [dB]**	**Peak SNR (L=4) [dB]**	**Power Dissipation [mW]**
25	87.41	81.12	87.50	81.17	33.21
125	84.08	77.94	84.11	78.24	32.60
150	83.11	76.89	83.06	77.60	32.53
175	81.69	75.42	82.72	74.91	32.59
200	79.41	73.43	79.16	72.53	32.73

flicker noise is reduced in future versions of this modulator design, the 4th-order modulator will quickly demonstrate improved DR over the 2nd-order design. This is due to the higher quantization noise magnitude in the baseband that becomes more prevalent in the 2nd-order design as the flicker noise floor is reduced. However, calculations using both measured and simulated data indicate that the 2nd-order modulator can achieve a peak SNR of ~15.8 bits by redesigning the integrator opamp, without the use of a chopper or CDS technique.

CHAPTER 8

CONCLUSION & FUTURE DIRECTIONS

8.1 Conclusion

ΣΔ modulation techniques have emerged as the dominant technique for high-resolution analog-to-digital conversion. The method has become common in applications including medical instrumentation, seismic recorders, and most recently communications. Room temperature applications have reported effective resolutions of over 20 bits. However, the general lack of progress in applying this technique to high-temperature applications is evident in the relative scarcity of associated publications.

This research reports the first 4^{th}-order ΣΔ modulator implemented in a SOS or SOI fabrication process and provides the first comparison of 2^{nd}- and 4^{th}-order cascaded modulators in a high-temperature process. Both 2^{nd}- and 4^{th}-order modulators were fabricated in 0.5μm SOS-CMOS and tested over a temperature range of 25° C-200° C. The modulator design was the result of a thorough investigation of published modulator topologies. The 2-2c cascade architecture was chosen due to its inherent stability and tolerance of gain mismatch. A comprehensive test system was developed for thorough, automated data collection, signal processing, and data visualization and reporting. The modulator building blocks were fabricated as separate pieces and characterized over temperature. Special attention was given to the integrator opamp testing with an emphasis on open loop gain and noise measurements over temperature. As a result of this thorough modeling and testing, the major performance limiting phenomenon including flicker noise, white noise,

tonals, and harmonic distortion were studied over temperature and well understood. Topology and circuit design modifications that will contribute to better modulator performance were identified and discussed.

A thorough investigation of the modulator noise was performed to explain both the measured modulator and integrator opamp noise and to provide means for predicting the performance of future lower noise designs. A number of SOS devices were characterized and the results were used to establish valid noise models. Using the improved noise models, excellent agreement was observed between measured and simulated noise data for the integrator opamp. A simulation model for the modulator noise was developed and used to verify the measured modulator performance. Collective use of both the improved device noise models and modulator noise model provides a powerful means for predicting overall modulator SNR performance based on measured or simulated integrator opamp noise.

Experimental results indicate the 2^{th}-order modulator achieves 87.41dB (14.23 bits) of resolution at T=25°C and 79.41dB (12.90 bits) at T=200°C. The 4^{th}-order modulator produced 81.12dB (13.18 bits) and 73.43dB (11.90 bits) at T=25°C and T=200°C, respectively. The 4^{th}-order modulator demonstrated general improved performance over the 2^{nd}-order for OSR < 64 (DOR > 8KHz). The need for increased modulator order will become more evident as the electronics noise floor is lowered in future designs. In terms of tonal behavior, the 4^{th}-order modulator suppressed spectral tones present in the 2^{nd}-order modulator.

Testing revealed flicker noise as the dynamic range limiting factor in both the 2^{nd}- and 4^{th}-order modulators. Both measured and simulation data indicate the first-stage integrator opamp is the dominant noise source. Device noise characterization and simulation

indicate that the design can be improved to achieve an effective resolution as high as 16.7 bits at T=25° C and 15.7 bits at T=200° C (both at DOR of 2KS/s) with the incorporation of effective 1/*f* noise reduction methods. In addition, simulations of an improved integrator opamp indicate that resolutions on the order of 16 bits can be achieved without the use of chopping or CDS.

The results of this work demonstrate the potential of high-resolution data converters in SOS/SOI for high-temperature applications. The resolution reported for these modulators represents a significant improvement over reported modulators in SOI/SOS and provides a foundation for future high-temperature, high-resolution converter research. Eventual realization of the stated goals of this work will allow high-resolution data conversion to be applied to many new areas including down-hole seismic, geothermal, engine and exhaust monitoring, and space flight applications.

8.2 Future Research Areas

There are several areas revealed during this research that warrant further study. First, methods for 1/*f* noise reduction need to be further investigated with a special emphasis on improved device noise modeling and simulation. Success in this area will require improved simulation methods that incorporate electronic noise, and device and circuit non-ideal behavior. In addition, the simulation models must incorporate accurate layout extraction that incorporates the parasitics that often cause undesirable modulator behavior. Both the chopping technique and correlated double sampling should be further explored using improved simulation and modeling methods.

The use of a cascaded architecture in this research offered loop stability at the cost of reduced input dynamic range. The integrator gains were selected based on improved tolerance of gain mismatch over other published gain configurations. Dynamic range can be increased by one of several approaches. The selection of integrator gain coefficients can be performed with an emphasis on integrator output swing minimization. In addition, high-order single-loop modulators could be used instead of cascaded architectures to provide increased dynamic range. Though these methods are well understood, the sensitivity of these architectures to temperature induced errors is not well understood. A thorough sensitivity analysis of effects resulting from temperature induced errors needs to be performed in order to assess the feasibility of these additional approaches.

BIBLIOGRAPHY

BIBLIOGRAPHY

[1] R. Aliahmad, C. Andre, and T. Salama, "Integration of a short-loop SLIC in a low-voltage submicron BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 850 -858, June 1998.

[2] P. J. Amantia, M. J. Kane, E. A. Kimball, S. L. Garverick, "A Mixed-Signal IC For a Semi-Implantable Hearing Aid," *ISCAS '99 Proc.*, pp. I-186 - I-189, 1999.

[3] Stephen Au, and Bosco H. Leung, "A 1.95-V, 0.34-mW, 12-b Sigma-Delta Modulator Stabilized by Local Feedback Loops," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 321-328, March 1997.

[4] J.N. Babanezhad, "A low-output-impedance fully differential op amp with large output swing and continuous-time common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1825 -1833, Dec. 1991.

[5] Rex T. Baird and Terri S. Fiez, "A Low Oversampling Ratio 14-b 500-kHz ΔΣ ADC with a Self-Calibrated Multibit DAC," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 312-320, March 1996.

[6] Rex T. Baird and Terri S. Fiez, "Linearity Enhancement of Multibit ΔΣ A/D and D/A Converters Using Data Weighted Averaging", *ITOCAS*, vol. 42, no. 12, pp. 753-762, Dec. 1995.

[7] M. Banu, J. M. Khoury, and Y. Tsividis, "Fully differential operational amplifiers with accurate output balancing," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1410 -1414, Dec. 1988.

[8] A. Baschirotto, and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1979 -1986, Dec. 1997.

[9] Bazes, M., "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165 -168, Feb. 1991.

[10] Bennett, W., "Spectra of quantized signals," *Bell System Tech. Journal*, vol. 27, pp. 446-472, 1948.

[11] Bernhard E. Boser and Bruce A. Wooley, "Quantization Error Spectrum of Sigma-Delta Modulators," *ISCAS '98 Proc.*, pp. 2331-2334, 1988.

[12] Bernhard E. Boser and Bruce A. Wooley, "Design of a CMOS Second-Order Sigma-Delta Modulator", 1998 IEEE International Solid-State Circuits Conference Proceedings, pp. 258-259, 395, 1998.

[13] Bernhard E. Boser and Bruce A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters", *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

[14] Brian P. Brandt and Bruce A. Wooley, "A Low-Power, Area-Efficient Digital Filter for Decimation and Interpolation," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 679-687, June 1994.

[15] Brian P. Brandt and Bruce Wooley, "A 50-MHz Multibit Sigma-Delta Modulator for 12-b 2-MHz A/D Conversion," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1746-1756, Dec. 1991.

[16] Brian P. Brandt, Drew E. Wingard, and Bruce A. Wooley, "Second-Order Sigma-Delta Modulation for Digital-Audio Signal Acquisition", *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 618-626, April 1991.

[17] Lucien J. Breems, Eric J. van der Zwan, and Johan H. Huijsing, "A 1.8-mW CMOS ΣΔ Modulator with Integrated Mixer for A/D Conversion of IF Signals," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 468-475, April 2000.

[18] Todd L. Brooks, David H. Robertson, Daniel F. Kelly, Anthony Del Muro, and Stephen W. Harston, “A Cascaded Sigma-Delta Pipeline A/D Converter with 1.25 MHz Signal Bandwidth and 89 dB SNR,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1896-1906, Dec. 1997.

[19] Thomas Burger, and Qiuting Huang, “A 3 V 2.8 mW CMOS ΣΔ-Modulator for GSM Applications, “ *IEEE 1998 Symp. on VLSI Circuits Digest of Technical Papers*, pp. 90-91, 1998.

[20] Klaas Bult, and Govert J.G.M. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379-1384, Dec. 1990.

[21] Ted Vinko Burmas, Kenneth C. Dyer, Paul J. Hurst, and Stephen H. Lewis, “A Second-Order Double-Sampled Delta-Sigma Modulator Using Additive-Error Switch,” *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 284-293, March 1996.

[22] Woog Cho Byung, Pyung Choi, and Byung Ki Sohn, "Modeling modulators for A/D signal conversion," *IEEE Circuits and Devices Magazine*, vol. 14, no. 6, pp. 26-31, Nov. 1998.

[23] J.M.G. Cama, S.A. Bota, E. Montane, and J. Samitier, "A MOSFET-only second order delta-sigma modulator for capacitive sensor interfaces," *Proc. of ICECS '99*, vol. 3, pp. 1689 -1692, 1999.

[24] Paul E. Carroll and Ralph A. Harris, "Digital dc offset removal method for data systems," U.S. Pat. No. 3,819,864, June 25, 1974.

[25] G. Cauwenberghs, and G.C. Temes, "Adaptive digital correction of analog errors in MASH ADCs. I. Off-line and blind on-line calibration," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Proc.*, vol. 47, no. 7, pp. 621-628, July 2000.

[26] Tsung-Yuan Chang, and Steven B. Bibyk, “Exact analysis of second order bandpass delta-sigma modulator with sinusoidal inputs,” *ISCAS '99 Proc.*, vol. 2, pp. II-372 - II-375, 1999.

[27] Zhong-Yuan Chang, Damien Macq, D. Haspleslagh, Paul M. P. Spruyt, and Bernard L. A. G. Goffart, “A CMOS Analog Front-End Circuit for an FDM-Based ADSL System,” *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1449-1456, Dec. 1995.

[28] Feng Chen and Bosco H. Leung, “A High Resolution Multibit Sigma-Delta Modulator with Individual Level Averaging,” *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453-460, April 1995.

[29] A.L. Coban,and P.E. Allen, "A 1.5 V 1.0 mW audio Delta Sigma modulator with 98 dB dynamic range," *1999 IEEE ISSCC*, pp. 50-51, 1999.

[30] J.P. Colinge, D. Flandre, and F. Van de Wiele, "Subthreshold Slope Of Long-Channel Accumulation-Mode p-Channel SOI MOSFETs," *Solid State Electronics*, vol. 37, no. 2, pp. 289-294, 1994.

[31] J.P. Colinge, J.P. Eggermont, D. Flandre, P. Francis, and P.G.A. Jespers, "Potential of SOI for Analog and Mixed Analog-Digital Low-Power Applications," *1995 IEEE ISSCC*, pp. 194-195, 366, 1995.

[32] F. Colodro, A. Torralba, F. Munoz, and L.G. Franquelo, "New class of multibit sigma-delta modulators using multirate architecture," *Electronics Letters*, vol. 36, no. 9, pp. 783-785, April 27, 2000.

[33] David P. Corkhill and Francis R Freeman, "Automatic gain control for seismometer recorders," U.S. Pat. No. 3,947,806, March 30, 1976.

[34] A.J. DaviIs, G. Fischer, H.-H. Albrecht, and J. Hess, "Digital correction of circuit imperfections in cascaded Sigma Delta modulators composed of 1st-order sections," *ISCAS '00 Proc.*, Geneva, vol. 5, pp. 689-692, 2000.

[35] I.J. Dedic, “A 16X oversampled CMOS ADC with 100KHz bandwidth and 90dB SNR,” *Advanced A-D and D-A Conversion Techniques and their Applications*, pp. 82-89, July 6-8, 1994.

[36] R. Del Rio, F. Medeiro, B. Perez-Verdu, and A. Rodriguez-Vazquez, "High-order cascade multibit Sigma Delta modulators for xDSL applications," *ISCAS '00 Proc*., Geneva, pp. 37-40, 2000.

[37] Bruce P. Del Signore, Donald A. Kerth, Navdeep S. Sooch, Eric J. Swanson, "A Monolithic 20-b Delta-Sigma A/D Converter", *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1311-1317, Dec. 1990.

[38] Laurent Demeus, Vincent Dessard, Albert Viviani, Stephane Adriaensen, and Denis Flandre, "Integrated Sensor and Electronic Circuits in Fully Depleted SOI Technology for High-Temperature Applications," *IEEE Trans. on Industrial Electronics*, vol. 48, no. 2, pp. 272-280, April 2001.

[39] L. Demeus, A. Viviani, and D. Flandre, "High-temperature analog instrumentation system in thin-film fully-depleted SOI CMOS technology," *1998 HITEC Proc*., pp. 51 -54, 1998.

[40] L. Demeus, and D. Flandre, "Comparison on Charge Injection in SOI and Bulk MOS Analog Switches," *1997 IEEE Int. SOI Conf. Proc*, pp. 104-5, Oct. 1997.

[41] V. Dessard, J.P. Eggermont, and D. Flandre, "Thin-Film SOI n-MOSFET Low-Frequency Noise Measurements at Elevated Temperatures," *ESSDERC '98 Proc*., pp. 604-7, 1998.

[42] M. Dessouky, and A. Kaiser, "A 1 V 1 mW digital-audio Delta Sigma modulator with 88 dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349-355, March 2001.

[43] Y. Dong and A. Opal, "Time-domain thermal noise simulation of switched capacitor circuits and delta-sigma modulators," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 4, pp. 473-481, April 2000.

[44] J.F. Duque-Carrillo, G. Torelli, J.M. Valverde, M.A. Deminguez, "1-V rail-to-rail operational amplifiers in standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 33-44, Jan. 2000.

[45] C.F. Edwards, W. Redman-White, M. Bracey, B.M. Tenbroek, M.S.L Lee, and M.J. Uren, "A multibit Sigma Delta modulator in floating-body SOS/SOI CMOS for extreme radiation Environments," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 937 -948, July 1999.

[46] Eggermont Jean-Paul, Denis De Cuester, Denis Flandre, Bernard Gentinne, Paul G. A. Jespers, Jean-Pierre Colinger, "Design of SOI CMOS Operational Amplifiers for Applications up to 300^{o}C," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 179-186, Feb. 1996.

[47] Jean-Paul Eggermont, Denis Flandre, Jean-Pierre Raskin, and Jean-Pierre Colinge, "Potential and Modeling of 1-µm SOI CMOS Operational Transconductance Amplifiers for Applications up to 1 GHz," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 640-643, April 1998.

[48] J.P. Eggermont, V. Dessard, A. Vandooren, D. Flandre, and J.P. Colinge, "SOI Current and Voltage Reference Sources for Applications up to 300°C," *4th High Temperature Electronics Conference*, pp. 55-59, 1998.

[49] Christian C. Enz and Gabor C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584-1614, Nov. 1996.

[50] C.C. Enz and Yuhua Cheng, "A CMOS delta-sigma true RMS converter," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 248 -257, Feb. 2000.

[51] F.O. Eynde, P. Wambacq and W. Sansen, "On the relationship between the CMRR or PSRR and the second harmonic distortion of differential input amplifiers," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1740 -1744, Dec. 1989.

[52] Frank Op't Eynde, Guang Ming Yin and Willy Sansen, "A CMOS Fourth-Order 14b 500k-Sample/s Sigma-Delta ADC Converter," *1991 IEEE ISSCC*, pp. 62, 289-290, 1991.

[53] K. Falakshahi, C.-K.K. Yang, and B.A.Wooley, "A 14-bit, 10-Msamples/s D/A converter using multibit Sigma Delta modulation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 607 -615, May 1999.

[54] L. Fang, and K.S. Chao, "A gain-compensated switched capacitor integrator," *Proc. 1998 Midwest Symp. on Circuits and Systems*, pp. 229 -232, 1998.

[55] John Fattaruso, Sami Kiriaki, Michiel de Wit, Greg Warwar, "Self-Calibration Techniques for a Second-Order Multibit Sigma-Delta Modulator", *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1216-1223, Dec. 1993.

[56] Arnold R. Feldman, Bernhard E. Boser, Paul R. Gray, "A 13-Bit, 1.4-MS/s Sigma-Delta Modulator for RF Baseband Channel Applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1462-1469, Oct. 1998.

[57] Flandre, D., and F. Van de Wiele, "Second-Order Analytical Modeling of Thin-Film SOI MOSFETs," *1989 IEEE SOS/SOI Tech. Conf. Proc.*, pp. 27-28, 1989.

[58] D. Flandre, and F. Van de Wiele, "A Physical Model for the Characterization of SOI MOSFETs in Linear Operation," *ESSDERC '89 Proc.*, pp. 755-8, 1989.

[59] D. Flandre, B. Gentinne, J.P. Eggermont, and P. Jespers, "Design of Thin-Film Fully-Depleted SOI CMOS Analog Circuits Significantly Outperforming Bulk Implementations," *Proc. of the 1994 IEEE Int. SOI Conf.*, pp. 99-100, Oct. 1994.

[60] D. Flandre, "Status and trends of SOI," *ESSDERC '89 Proc.*, pp. 18-27, 1994.

[61] Denis Flandre, "Silicon-on-insulator technology for high temperature metal oxide semiconductor devices and circuits," *Materials Science and Engineering*, B29, pp. 7-12, 1995.

[62] D. Flandre, and D. Vanhoenacker, "Thin-film Fully-depleted SOI CMOS Technology, Devices and Circuits For LVLP Analog/Digital/Microwave Applications," *1998 International Semiconductor Conf.*, pp. 115-24, 1998.

[63] D. Flandre, L.F. Ferreira, P.G.A. Jespers, and J.P. Colinge, "Modelling and Application of Fully Depleted SOI MOSFETs for Low Voltage, Low Power Analogue CMOS Circuits," *Solid State Electronics*, vol. 39, no. 4, pp. 455-60, 1996.

[64] D. Flandre, et al., "Fully-Depleted SOI CMOS Technology for Low-Voltage Low-Power Mixed Digital/Analog/Microwave Circuits," *Analog Integrated Circuits and Signal Processing*, vol. 21, pp. 213-228, 1999.

[65] D. Flandre, "High-temperature electronics applications of SOI CMOS technology," *Revue-HF*, no. 4, pp. 17-30, 1997.

[66] M. G. Forrester, B. D. Hunt, D.L. Miller, J. Talvacchio, and R. M. Young, "Analogue demonstration of a high temperature superconducting sigma-delta modulator with 27 GHz sampling," *Superconductor Science Technology*, 12, pp. 698-700, 1999.

[67] Francis, P., A. Terao, B. Gentinne, D. Flandre, and J.P. Colinge, "SOI Technology for High-Temperature Applications," *Int. Electron Dev. Meeting Technical Digest*, pp. 353-356, 1992.

[68] E. Fogelman, I. Galton, W. Huff, and H. Jensen, "A 3.3-V single-poly CMOS audio ADC delta-sigma SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 297 -307, March 2000.

[69] E. Fogelman, Ian Galton, William Huff, and Henrik Jensen, "A 3.3V Single-Poly CMOS Audio ADC Delta-Sigma Modulator with 98dB Peak SINAD and 105-dB Peak SFDR," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 297-307, March 2000.

[70] Eric Fogelman, Jared Welz and Ian Galton, "An Audio ADC Delta-Sigma Modulator with 100-dB Peak SINAD and 102-dB DR Using a Second-Order Mismatch-Shaping ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 339-348, March 2001.

[71] Ichiro Fujimori, Kazuo Koyama, David Trager, Fred Tam, and Lorenzo Longo, “A 5-V Single-Chip Delta-Sigma Audio A/D Converter with 111 dB Dynamic Range,” *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 329-336, March 1997.

[72] Ichiro Fujimori, Lorenzo Longo, Armond Hairapetian, Kazushi Seiyama, Steve Kosic, Jun Cao and Shu-Lap Chan, “A 90-dB SNR 2.5-MHz Output-Rate ADC Using Cascaded Multibit Delta-Sigma Modulation at 8x Oversampling Ratio,” *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820-1828, Dec. 2000.

[73] V. Friedman, "Oversampled data conversion techniques," *IEEE Circuits and Devices Magazine* , vol. 6, no. 6, pp. 39-45, Nov. 1990.

[74] Weinan Gao, James A. Cherry, and W. Martin Snelgrove, “A 4GHz Fourth-Order SiGe HBT Band Pass ΣΔ Modulator,” *IEEE 1998 Symp. on VLSI Circuits Digest of Tech. Paper*s, pp. 174-175.

[75] Yves Geerts, Michel S. J. Steyaert and Willy Sansen, “A High-Performance Multibit ΔΣ CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829-1840, Dec. 2000.

[76] B. Gentinne, J.P. Eggermont, D. Flandre, and J.P. Colinge, "Fully depleted SOI-CMOS technology for high temperature IC applications," *Materials Science and Engineering*, B46, pp. 1-7, 1997.

[77] Ronald G. Gillespie, "Floating point amplifier means and method," U. S. Pat. No. 4,194,163, March 18, 1980.

[78] R. Gillon, J.P. Colinge, D. Flandre, J.P. Raskin, and D. Vanhoenacker, "Silicon-On-insulator for RF and microwave low-power applications," *Microwave Engineering Europe*, pp. 49-50, 53-54, June 1998.

[79] Gabriel J. Gomez, “A 102-dB Spurious-Free DR ΣΔ ADC Using a Dynamic Dither Scheme,” *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 47, no. 6, pp. 531-535, June 2000.

[80] A. Gothenberg, Li Bingxin, and H. Tenhunen, "A method for stability and performance analysis of low oversampling ratio higher order sigma delta noise shaper architectures," *42nd Midwest Symp. on Circuits and Systems, 2000*, vol. 1, pp. 348 -351, 2000.

[81] Robert M. Gray, “Quantization Noise Spectra,” *IEEE Trans. on Information Theory*, vol. 36, no. 6, pp. 1220-1244, Nov. 1990.

[82] I. Grech, J. Micallef, C.J. Debono, P. Malcovati, and F. Maloberti, "A 1 V second order sigma-delta modulator," *Proc. ICECS '99*, vol. 3, pp. 1511 -1514, 1999.

[83] Roubik Gregorian and Gabor C. Temes, Analog MOS Integrated Circuits For Signal Processing, John Wiley & Sons, New York, ISBN 0-471-09797-7, 1986.

[84] Jorge Grilo, Edward MacRobbie, Raouf Halim, and Gabor Temes, “A 1.8V 94dB Dynamic Range ΣΔ Modulator for Voice Applications,” *1996 IEEE ISSCC*, pp. 230-231, 451, 1996.

[85] K. Gulati and Hae-Seung Lee, "A high-swing CMOS telescopic operational amplifier," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2010 -2019, Dec. 1998.

[86] J. Harrison, and N. Weste, "Analytic limitations on sigma-delta modulator performance," *ISCAS ‘00 Proc.*, Geneva.,vol. 3, pp. 746 -749, 2000.

[87] R. K. Henderson and O.J.A.P. Nys, "Dynamic Element Matching Techniques With Arbitrary Noise Shaping Function", *ISCAS '96 Proc.*, vol. 1, pp. 293-296, 1996.

[88] C. Hierold, B. Clasbrummel, D. Behrend, T. Scheiter, M. Steger, K. Oppermann, H. Kapels, E. Landgraf, D. Wenzel, and D. Etzrodt, “Implantable Low Power Integrated Pressure Sensor System For Minimal Invasive Telemetric Patient Monitoring,” *MEMS 98, Proceedings of The Eleventh Annual Int. Workshop on Micro Electro Mechanical Systems*, pp. 568-573, 1998.

[89] K. C. Hsieh, P. R. Gray, D. Senderowicz, and D. Messerschmitt: “A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique,” *IEEE J. Solid-State Circuits*, vol. 16, pp. 708-715, Dec. 1981.

[90] HSPICE, http://www.synopsys.com/products/avmrg/star_hspice_ds.html.

[91] Issac Hsu and Howard C. Luong, “A 70-MHz Continuous-time CMOS Band-pass ΣΔ Modulator for GSM Receivers,” *ISCAS ‘00 Proc.*, pp. III-750 - III-753, 2000.

[92] Huang Qiuting, "Mixed Analog/Digital, FIR/IIR Realization of a Linear-Phase Lowpass Filter," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1347-1350, Sept. 1996.

[93] Seppo Ingalsuo, Tapani Teitoniemi, Teppo Karema, and Hannu Tenhunen, “A 50 MHz cascaded sigma-delta A/D modulator,” *Proc. of the IEEE 1992 Custom Integrated Circuits Conf.*, pp. 16.3.1-16.3.4, 1992.

[94] B. Iniguez, M. Tabmani, V. Dessard, and D. Flandre, "Unified 1/f noise SOI MOSFET modelling for circuit simulation," *Electronics Letters*, vol. 33, no. 21, pp. 1781-2, Oct. 1997.

[95] H, Inose, Y. Yasuda and J. Murakami, “A Telemetering System by Code Modulation-Δ–Σ Modulation,” *IRE Trans. on Space Electronics and Telemetry*, vol. 8, pp. 204-209, Sept. 1962.

[96] J.E. Johnston, "A 24-bit delta-sigma ADC with an ultra-low noise chopper-stabilized programmable gain instrumentation amplifier," *Third Int. Conf. on Advanced A/D and D/A Conversion Techniques and Their Applications*, (Conf. Publ. no. 466), pp. 179 -182, 1999.

[97] D.A. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, New York, NY, ISBN 0-471-14448-7, 1997.

[98] A. N. Karanicolas et al, "A high-frequency fully differential BiCMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 26 no. 3, pp. 203 -208, March 1991.

[99] Teppo Karema, Tapani Ritoniemi and Hannu Tenhunen, “An oversampled sigma-delta A/D converter circuit using two-stage fourth order modulator,” *ISCAS ‘90 Proc.*, vol. 4, pp. 3279-82, 1990.

[100] Donald A. Kerth, Dan B. Kasha, Tony G. Mellissinos, Douglas S. Piasecki and Eric J. Swanson, “A 120dB Linear Switched-Capacitor Delta-Sigma Modulator,” *Proc. 1994 IEEE Solid-State Circuits Conf.*, pp. 196-197,337, 1994.

[101] Kidiyarova-Shevchenko, A. Yu., D.E. Kirichenko, Z. Ivanov, F. Komissinsky, E.A. Stepancov, M.M. Khapaev, and T. Claeson, "Single flux quantum comparators for HTS AD converters," *Physica C: Superconductivity Applications*, vol. 326, pp. 83-92, 1999.

[102] Eric A. M. Klumperink, Sander L. J. Gierkink, Arnoud P. van der Wel, and Bram Nauta, “Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing,” *IEEE J. Solid-State Circuits*, vol. 35, no. 7., pp. 994-1001, July 2000.

[103] L. Lah, J. Choma Jr., and J. Draper, "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing* , vol. 47 no. 4, pp. 363 -369, April 2000.

[104] H. Lampinen, and O. Vainio, "An optimization approach to designing OTAs for low-voltage sigma-delta modulators," *Proc. of the 17th IEEE Instr. and Meas. Tech. Conf.*, ,vol. 2 , pp. 1066 -1070, 2000.

[105] H.-S. Lee, D. Hodges and P. Gray, “A self-calibrating 15 bit CMOS A/D converter,” *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 813-819, Dec. 1984.

[106] K. Lee and R. Meyer, “Low-distortion switched-capacitor filter design techniques,” *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1103-1113, Dec. 1985.

[107] Hans A. Leopold, Gunter Winkler, Paul O'Leary, Karl Ilzer, Juergen Jernej, "A Monolithic CMOS 20-b Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 910-916, July 1991.

[108] A. Leuciuc, and C. Mitrea, On the effect of op-amp finite gain in delta-sigma modulators," *ISCAS '00 Proc.*, Geneva.,vol. 3, pp. 754 -757, 2000.

[109] Ka. Y. Leung, Eric J. Swanson, Kafai Leung, and Sarah S. Zhu, "A 5V 118dB ΣΔ Analog-to-Digital Converter for Wideband Digital Audio," *Proc. 1997 IEEE Int. Solid-State Circuits Conf.*, pp. 218-219, 460, 1997.

[110] S. W. Leung, and Y. T. Zhang, "Digitization of Electrocardiogram (ECG) Signals Using Delta-Sigma Modulation," *Proc. of the 20th Annual Int. Conf. of the IEEE Eng. in Med. and Biol. Society*, vol. 20, no. 4, pp. 1964-1966, 1998.

[111] Chi-Hung Lin, Chunlei Shi, Mohammed Ismail and Moon Gyu, "A 5MHz Nyquist Rate Continuous-Time Sigma-Delta Modulator for Wideband Wireless Communication,", *ISCAS '99 Proc.*, vol. 2, pp. 36 -371, 1999.

[112] Li, Qunying, Jan Van der Spiegel and Kenneth R. Laker, "A 1.2V, 38μW Second-Order ΔΣ Modulator with Signal Adaptive Control Architecture," *Proc. of the IEEE 2nd Dallas CAS Workshop on Low Power/Low Voltage Mixed-Signal Circuits and Systems, (DCAS-01)*, pp. 23-26, 2001.

[113] Longo Lorenzo, Miles Copeland, "A 13 bit ISDN-band Oversampled ADC using Two-Stage Third Order Noise Shaping", *1998 IEEE ICICC Proc.*, pp. 21.2.1-21.2.4, 1998.

[114] Loai Louis, John Abcarius, and Gordon W. Roberts, "An Eighth-Order Bandpass ΔΣ Modulator for A/D Conversion in Digital Radio," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 423-431, April 1999.

[115] Ma. Stanley Jeh-Chun, and C. Andre T. Salama, "A 1V Second-Order Sigma-Delta Modulator," *ISCAS '98 Proc.*, vol. 1, pp. 348-351, 1998.

[116] Marques Augusto Manuel, Vincenzo Peluso, Michel S. J. Steyaert, Willy Sansen, "A 15-b Resolution 2-MHz Nyquist Rate ΔΣ ADC in a 1-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1065-1075, July 1998.

[117] MathCAD Reference Manual, http://www.mathsoft.com.

[118] Mathematica Reference Manual, http://www.wolfram.com.

[119] Matlab Reference Manual, http://www.mathworks.com.

[120] Yasuyuku Matsuya, Kuniharu Uchimura, Atsushi Iwata, Tsutomu Kobayashi, Masayuki Ishikawa, Takeshi Yoshitome, "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping", *IEEE J. Solid-State Circuits*, vol. sc-22, no. 6, pp. 921-929, Dec. 1987.

[121] Yasuyuki Matsuya and Junzo Yamada, "1 V Power Supply, Low-Power Consumption A/D Conversion Technique with Swing-Suppression Noise Shaping," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1524-1530, Dec. 1994.

[122] Prabir C. Maulik, Mandeep S. Chadha, Wai L. Lee, and Philip J. Crawley, "A 16-Bit 250-kHz Delta-Sigma Modulator and Decimation Filter," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 458-467, April 2000.

[123] F. Patrick McCluske, Richard Grzybowski, and Thomas Podlesak, High Temperature Electronics, CRC Press, New York, ISBN 0-8493-9623-9.

[124] J. McCreary, "Matching properties, and voltage and temperature dependence of MOS capacitors," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 608-616, Dec. 1981.

[125] F. Medeiro, B. Perez-Verdu, J. M. de la Rosa, and A. Roduriguez-Vazquez, “Quick Design of High-Performance ΣΔ Modulators using CAD Tools: A 16.4b 1.71mW CMOS ΣΔM for 9.5ksample/s A/D Conversion,” *Proc. of the 1997 2nd IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design*, pp. 22-27, 1997.

[126] F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez, and J.L. Huertas, "A vertically integrated tool for automated design of Sigma Delta modulators," *IEEE J. Solid-State Circuits*, vol. 30 no. 7, pp. 762 -772, July 1995.

[127] F. Medeiro, Angel Perez-Verdu, and Angel Rodriguez-Vazquez, Top-Down Design of High-Performance Sigma-Delta Modulators, Kluwer Academic Publishers, Boston, ISBN 0-7923-8352-4, 1999.

[128] F. Medeiro, B. Perez-Verdu, and A. Rodriguez-Vazquez, "A 13-bit, 2.2-MS/s, 55-mW multibit cascade Sigma Delta modulator in CMOS 0.7 µm single-poly technology," *IEEE J. Solid-State Circuits*, vol. 34 no. 6, pp. 748 -760, June 1999.

[129] Fernando Medeiro, Belen Perez-Verdu, Jose Manuel de la Rosa, and Angel Rodriguez-Vazquez, “Fourth-Order Cascade SC ΣΔ Modulators: A Comparative Study,” *IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications*, vol. 45, no. 10, pp. 1041-1051, Oct. 1998.

[130] MIDAS Reference Manual, http://cis.stanford.edu/icl/wooley-grp/midas.html.

[131] Paschal Minogue, “A 3 V GSM Codec,” *IEEE J. Solid-State Circuits*, vol. 30, no. 12., pp. 1411-1420, Dec. 1995.

[132] George T. Mioduski, "Gain Ranging Amplifier System," U. S. Pat. No. 4,031,504, June 21, 1977.

[133] Moeneclaey Nicolas, Andreas Kaiser, "Design Techniques for High-Resolution Current-Mode Sigma-Delta Modulators," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 953-958, July 1997.

[134] James C. Morizio, et. al., “14-bit 2.2-MS/s Sigma-Delta ADC’s,” *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 968-976, July 2000.

[135] J. Morizio, M. Hoke, T. Kocak, C. Geddie, C. Hughes, J. Perry, S. Madhavapeddi, M. Flood, W. Huffman, T. Okuda, H. Noda, Y. Morimoto, T. Kumamoto, M. Ishiwaki, H. Kondoh, M. Nakaya, and T. Miki, "SNDR sensitivity analysis for cascaded ΣΔ modulators," *ISCAS 2000 Proc.*, Geneva.,vol. 3, pp. 765 -762, 2000.

[136] J.C. Morizio, I.M. Hoke, T. Kocak, C. Geddie, C. Hughes, J. Perry, S. Madhavapeddi, M.H. Hood, G. Lynch, H. Kondoh, T. Kumamoto, T. Okuda, H. Noda, M. Ishiwaki, T. Miki, and M. Nakaya, "14-bit 2.2-MS/s sigma-delta ADC's," *IEEE J. Solid-State Circuits* , vol. 35 no. 7, pp. 968 -976, July 2000.

[137] Nadeem Shujaat, Charles G. Sodini, Hae-Seung Lee, "16-Channel Oversampled Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1077-1085, Sept. 1994.

[138] Angelo Nagari, Alessandro Mecchia, Ermes Viani, Sergio Pernici, Pierangelo Confalonieri and Germano Nicollini, “A 2.7V 11.8mW Baseband ADC with 72 dB Dynamic Range for GSM Applications,” *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 798-806, June 2000.

[139] R. Naiknaware, and T. Fiez, "142 dB Delta Sigma ADC with a 100 nV LSB in a 3 V CMOS process," *Proc. IEEE 2000 ICICC*, pp. 5-8, 2000.

[140] G. Nicollini, F. Moretti, and M. Conti, "High-frequency fully differential filter using operational amplifiers without common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 24 no. 3, pp. 803 -813, June 1989.

[141] Steven R. Norsworthy, Irving G. Post, H. Scott Fetterman, "A 14-bit 80-kHZ Sigma Delta A/D Converter: Modeling, Design, and Performance Evaluation," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 256-266, April 1989.

[142] Steven R. Norsworthy, Richard Schreier, Gabor C. Temes, editors, Delta-Sigma Data Converters Theory, Design, and Simulation, IEEE Press, Piscataway, NJ, ISBN 0-7803-1045-4, 1997.

[143] A. Nuttall, “Some windows with very good sidelobe behavior, “I*EEE Trans. on Acoustics, Speech, and Signal Processing*, vol. ASSP-29, pp. 84-91, Feb. 1981.

[144] Olivier Nys and Robert K. Henderson, “A 19-Bit Low-Power Multibit Sigma-Delta ADC Based on Data Weighted Averaging,” *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 933-942, July 1997.

[145] K. Olejarczyk, "A geometric view of multiple feedback Delta Sigma modulator," *Third Int. Conf. on Advanced A/D and D/A Conv. Tech. and Their Applications*, (Conf. Publ. no. 466), pp. 66 -69, 1999.

[146] Omid Oliaei, Patrick Clement and Philippe Gorisse, “A 5mW ΣΔ Modulator with 84dB Dynamic Range for GSM/EDGE,” *2001 IEEE ICICC*, pp. 46-47, 428, 2001.

[147] O. Oliaei, "Thermal noise analysis of multi-input sc-integrators for delta-sigma modulator design ,". *ISCAS ‘00 Proc*., Geneva., vol. 4, pp. 425 -428, 2000.

[148] A. Olmos, T. Miyashita, M. Nihei, E. Charry, and Y. Watanabe, “A 5GHz Continuous Time Sigma-Delta Modulator Implemented in 0.4µm InGaP/InGaAs HEMT Technology,” *ISCAS '98 Proc.*, vol. 1, pp. I575-I578, 1998.

[149] M. Padure, "Sigma Delta data modulators behavioral simulation with MIDAS," Semiconductor Conference, *CAS '99 Proc.*, vol. 1, pp. 257 -260, 1999.

[150] D. Pastorello, A. Amar, Q. Yu, and B. Del Signore, "Below ground measurements with a single supply delta-sigma A/D converter," *Proc. 1999 Advanced A/D and D/A Conv. Tech. and Their Applications*, (Conf. Publ. no. 466), pp. 172 -174, 1999.

[151] V. Peluso, M. Steyaert, and W. Sansen, “A Switched Opamp 1.5V - 100mW ΣΔ Modulator with 12 bits Dynamic Range,” *Proc. 1996 ESSCC*, pp. 256-259, Sept. 1996.

[152] V. Peluso, P.Vancorenland, A.M. Marques, M.S.J. Steyaert, and W. Sansen, "A 900-mV low-power ΔΣ A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33 no. 12, pp. 1887-1897, Dec. 1998.

[153] Vincenzo Peluso, Michiel S. J. Steyaert, and Willy Sansen, "A 1.5-V-100-µW ΔΣ Modulator with 12-b Dynamic Range Using the Switched-Opamp Technique," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 943-952, July 1997.

[154] Robert R. Pierret and Gerold W. Neudeck, Editors, Modular Series on Solid State Devices Volume VI - Advanced Semiconductor Fundamentals, Addison-Wesley, Reading Mass., ISBN 0-201-05338-1, 1983.

[155] L. Quiquerez, A. Kaiser, and D. Billet, "A 112 dB sigma-delta converter with a mixed continuous-time/sampled-data architecture," *1999 Southwest Symp. on Mixed-Signal Design, SSMSD '99*., pp. 52 -57, 1999.

[156] Shahriar Rabii and Bruce A. Wooley, “A 1.8V, 5.4mW, Digital-Audio ΣΔ Modulator in 1.2µm CMOS,” *1996 IEEE ISSCC*, pp. 228-229, 450, 1996.

[157] Shahriar Rabii and Bruce A. Wooley, “A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS,” *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783-796, June 1997.

[158] Shahriar Rabii and Bruce A. Wooley, The Design of Low-Voltage, Low-Power Sigma-Delta Modulators, Kluwer Academic Publishers, Boston, ISBN 0-7923-8361-3, 1999.

[159] Rangan Sundeep and Bosco Leung, “Quantization noise spectrum of double-loop sigma-delta converter with sinusoidal input,” *IEEE Trans on Circuits and Systems - II: Analog and Digital Signal Processing*, vol. 41, no. 2, pp. 168-173, Feb. 1994.

[160] Jean-Pierre Raskin, Alberto Viviani, Denis Flandre, and Jean-Pierre Colinge, "Substrate Crosstalk Reduction Using SOI Technology, *IEEE Transactions on Electron Devices*, vol. 44, no. 12, pp. 2252-2261, Dec. 1997.

[161] Mike Rebeschini, Nicholas R. Van Bavel, Patrick Rakers, Robert Greene, James Caldwell, John R. Haug, "A 16-b 160-kHz CMOS A/D Converter Using Sigma-Delta Modulation", *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 431-440, April 1990

[162] David B. Ribner, Richard D. Baertsch, Steven L. Garverick, Donald T. McGrath, Joseph E. Krisciunas, Toshiaki Fujii, "A Third-Order Multistage Sigma-Delta Modulator with Reduced Sensitivity to Nonidealities," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1764-1774, Dec. 1991.

[163] D. B. Ribner, "A comparison of modulator networks for high-order oversampled ΣΔ analog-to-digital converters," *IEEE Trans. Circuits Systems*, vol. 38, pp. 145-159, Feb. 1991.

[164] Ritoniemi Tapani, Eero Pajarre, Seppo Ingalsuo, Timo Husu, Ville Eerola, Tapio Saramaki, "A Stereo Audio Sigma-Delta A/D-Converter," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1514-1523, Dec. 1994.

[165] Ritoniemi Tapani, Teppo Karema and Hannu Tenhunen, "A fifth order sigma-delta modulator for audio A/D converter," *Int. Conf. on Analogue to Digital and Digital to Analogue Conv.*, pp. 153-158, 1991.

[166] Ritoniemi Tapani, Teppo Karema, Hannu Tenhunen; "Design of Stable High Order 1-Bit Sigma-Delta Modulators", *ISCAS '90 Proc.*, vol. 4, pp. 3267-3270, 1990.

[167] B. Ruck, Y. Chong, R. Dittmann, A. Engelhardt, E. Sodtke, and M. Siegel, "A high-temperature superconducting delta-sigma modulator based on a multilayer technology with bicrystal Josephson junctions," *Superconductor Science Technology*, vol. 12, pp. 701-3, Nov. 1999.

[168] Ho Yoon San, and S. M. Rezaul Hasan, "A Sixth-Order CMOS Sigma-Delta Modulator," *Proc. of the Eleventh Annual IEEE Int. ASIC Conf.*, pp. 63-66, 1998.

[169] J. Sauerbrey, and M. Mauthe, "12 Bit 1-mW ΣΔ-Modulator for 2.4V supply voltage," *Proc. 1995 ESSCC*, pp. 138-141, 1995.

[170] Richard W. Scott and Marvin D. Laymon, "Adaptive gain control and method for signal processor," U.S. Pat. No. 3,958,213, May 18, 1976.

[171] Vasili K. Semenov, and Yuri A. Polyakov, "Superconducting Delta ADC with On-chip Decimation Filter," *IEEE Trans Applied Superconductivity*, vol. 9, no. 2, pp. 3026-3029, June 1999.

[172] Daniel Senderowicz, "Low-Voltage Double-Sampled ΣΔ Converters," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1907-1919, Dec. 1997.

[173] Liu Shen-Iuan, Kuo Chien-Hung, Tsai Ruey-Yuan and Wu Jingshown, "A double-sampling pseudo-two-path bandpass Delta Sigma modulator," *IEEE J. Solid-State Circuits*, vol. 35 no. 2, pp. 276 -280, Feb. 2000.

[174] SimuLink Reference Manual, http://mathworks.com.

[175] Rajinder Singh and A. B. Bhattacharyya, "Matching Properties of Linear MOS Capacitors," *IEEE Trans. on Circuits and Systems*, vol. 36, no. 3, pp. 465-467, March 1989.

[176] R. Singh et. al, "Roles of Corners in Matching of Linear MOS Capacitors," *IEEE Trans. on Circuits and Systems*, vol. 36, pp. 467-469, March 1989.

[177] M. A. Smither, "Instantaneous floating point amplifier," U. S. Pat. No. 4,104,596, Aug. 1, 1978.

[178] M. A. Smither, "Instantaneous floating point amplifier," U. S. Pat. No. 4,158,819, Jun. 19, 1979.

[179] M. A. Smither, "Instantaneous floating point amplifier," U.S. Pat. No. 4,357,577, Nov. 2, 1982.

[180] M.F. Snoeij, O. Bajdechi, and J. H. Huijsing, "A 4th-Order Switched-Capacitor Sigma-Delta A/D Converter Using A High-Ripple Chebyshev Loop Filter," *ISCAS '01 Proc.*, vol. 1, pp. 615-618, 2001.

[181] A. Swaminathan, N. Fong, P. Lauzon, Yang Hong-Kui, M. Maliepaard, C. Plett, and M. Snelgrove, "A low power Sigma Delta analog-to-digital modulator with 50 MHz sampling rate in a 0.25 μm SOI CMOS technology," *1999 IEEE Int. SOI Conf. Proc.*, pp. 14 -15, 1999.

[182] Li Suet-Fei and J. Wetherrell, "A compact low-power decimation filter for sigma delta modulators," *Conf. on Acoustics, Speech, and Signal Processing, ICASSP '00 Proc.*, vol. 6, pp. 3223 -3226.

[183] Ali Tabatabaei, Kambiz Kaviani, and Bruce Wooley, "A Two-Path Bandpass ΣΔ Modulator with Extended Noise Shaping," *2000 IEEE ISSCC*, pp. 342-343, 2000.

[184] Nianxiong Tan and Sven Eriksson, "A Low-Voltage Switched-Current Delta-Sigma Modulator," *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 599-603, May 1995.

[185] Nianxiong Tan "A 1.2-V 0.8-mW SI ΣΔ A/D Converter in Standard Digital CMOS Process," *Proc. 1995 ESSCC*, pp. 150-153, 1995.

[186] Y. Tang and M.Ismail, "The Chip. A methodology for fast SPICE simulation of frequency synthesizers,"*IEEE Circuits and Devices Magazine*, vol. 16 no. 4, pp. 10 -15, July 2000.

[187] Hai Tao and John M. Khoury, "A 100MHz IF, 400 MSamples/s CMOS Direct-Conversion Bandpass ΣΔ Modulator," *1999 EEE ISSCC*, pp. 60-61,445, 1999.

[188] Chuck Thanh, Stephen H. Lewis, and Paul J. Hurst, "A Second-Order Double-Sampled Delta-Sigma Modulator Using Individual-Level Averaging," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1269-1273, Aug. 1997.

[189] A. Thomsen, D.B. Kasha, L. Wang, and W.L. Lee, "A 110-dB-THD, 18-mW DAC using sampling of the output and feedback to reduce distortion," *IEEE J. Solid-State Circuits*, vol. 34 no. 12 , pp. 1733 -1740, Dec. 1999.

[190] Axel Thomsen, Edwin de Angel, Sherry Xiaohong Wu, Aryesh Amar, Lei Wang, and Wai Lee, "A DC Measurement IC with 130n$V_{pp.}$ Noise in 10Hz," *2000 IEEE ISSCC*, pp. 334-335, 2000.

[191] Yannis P. Tsividis, "Integrated Continuous-Time Filter Design-An Overview," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 166-176, March 1994.

[192] B.J. van den Dool and J.K. Huijsing, "Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative roll," *IEEE J. Solid-State Circuits*, vol. 28 no. 7, pp. 743 -749, July 1993.

[193] Eric J. van der Zwan, Kathleen Philips, and Corne A. A. Bastiaansen, "A 10.7-MHz IF-to-Baseband ΣΔ A/D Conversion System for AM/FM Radio Receivers,' *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1810-1819, Dec. 2000.

[194] Eric J. van der Zwan, E. Carel Dijkmans, "A 0.2-mW CMOS, ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1873-1880, Dec. 1996.

[195] T. Vanisri and C. Toumazou, "Integrated high frequency low-noise current-mode optical transimpedance preamplifiers: theory and practice," *IEEE J. Solid-State Circuits*, vol. 30 no. 6, pp. 677 -685, June 1995.

[196] Katelijn Vleugels, Shrahriar Rabii and Bruce A. Wooley, "A 2.5V Broadband Multi-Bit ΣΔ Modulator with 95dB Dynamic Range," *2001 IEEE ISSCC*, pp. 50-51, 428, 2001.

[197] A. Viviani, J.P. Raskin, D. Flandre, J.P. Colinge, and D. Vanhoenacker, "Extended study of crosstalk in SOI-SIMOX substrates," *Int. Electron Devices Meeting*, pp. 713-6, 1995.

[198] A.Viviani, D. Flandre, and P. Jespers, "A SOI-CMOS micro-power first-order Sigma-Delta modulator," *Proc. 1996 IEEE Int. SOI Conf.*, pp. 110-111, Oct. 1996.

[199] A.Viviani, D. Flandre, and P. Jespers, "High-temperature sigma-delta modulator in thin-film fully-depleted SOI technology," *Electronics Letters*, vol. 35, no. 9, pp. 749-751, April 1999.

[200] S.P. Wainwright, S. Hall, and D. Flandre, "The Effect of Series Resistance on Threshold Voltage Measurement Techniques for Fully Depleted SOI MOSFETs," *Solid-State Electronics*, vol. 39, no. 1, pp. 89-94, 1996.

[201] Chris Binan Wang, Jim Todsen and Tim Kalthoff, "A Dual Channel 20 Bit Current-Input A/D Converter for Photo-Sensor Applications," *2000 Southwest Symp. on Mixed-Signal Design, SSMSD*, pp. 57-60, 2000.

[202] Chris Binan Wang, "A 20-bit 25-kHz Delta-Sigma A/D Converter Utilizing a Frequency-Shaped Chopper Stabilization Scheme," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 566-569, March 2001.

[203] Feng Wang and Ramesh Harjani, Design of Modulators For Oversampled Converters, Kluwer Academic Publishers, Boston, MA, ISBN 0-7923-8063-0, 1998.

[204] Williams III Louis A., "An Audio DAC With 90dB Linearity Using MOS to Metal-Metal Charge Transfer", *IEEE J. Solid-State Circuits*, pp. 58-59, 1998.

[205] Louis A. Williams III and Bruce A. Wooley, "Third-Order Cascaded Sigma-Delta Modulators", *ITCS*, vol. 38, no. 5, pp. 489-498, May 1991.

[206] Louis A. Williams III and Bruce A. Wooley, "A Third-Order Sigma-Delta Modulator with Extended Dynamic Range", *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 193-202, March 1994.

[207] Louis Albert Williams III, "Modeling and Design of High-Resolution Sigma-Delta Modulators," PhD. Dissertation, Stanford University, 1993.

[208] Wittman Reimund, Werner Schardein, Bedrich J. Hosticka, Gert Burbach, and Juergen Arndt, "Trimless High Precision Ratioed Resistors in D/A and A/D Converters," *IEEE J. Solid-State Circuits*, vol. 30, no. 8, pp. 935-939, Aug. 1995.

[209] S. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," *IRE Trans. Circuit Theory*, vol. CT-3, pp. 266-276, Dec. 1956.

[210] Li Xiaopeng and M. Ismail, "Fast simulation of sigma-delta modulators using SPICE," *IEEE Circuits and Devices Magazine* , vol. 15 no. 1, pp. 7 -9, Jan. 1999.

[211] Wang Xuesheng, Qin Wei and Ling Xieting, "Cascaded parallel oversampling sigma-delta modulators," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 2, pp. 156 -161, Feb. 2000.

[212] Ken Yamamura, Akihiko Nogi and Allen Barlow, "A Low Power 20 Bit Instrumentation Delta-Sigma ADC," *1994 IEEE ICICC*, pp. 519-522, 1994.

[213] Akira Yasuda, Hiroshi Tanimoto, and Tetsuya Iida, "A Third-Order Δ–Σ Modulator Using Second-Order Noise-Shaping Dynamic Element Matching," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1879-1886, Dec. 1998.

[214] G. M. Yin, F. Op't Eynde, and W. Sansen, "A High-Speed CMOS Comparator with 8-b Resolution," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 208-211, Feb. 1992.

[215] Yin Guangming, Frederic Stubbe, Willy Sansen, "A 16-b 320-kHz CMOS A/D Converter Using Two-Stage Third-Order ΣΔ Noise Shaping," *IEEE J. Solid-State Circuits*, vol. 28, no. 6, pp. 640-647, June 1993.

[216] Yin Guangming, Willy Sansen, "A High-Frequency and High Resolution Fourth-Order ΣΔ A/D Converter in BiCMOS Technology," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 857-865, Aug. 1994.

[217] Gao Yonghong, H. Tenhunen, "A 71 msample/sec fifth order sigma-delta digital modulator," *42nd Midwest Symp. on Circuits and Systems*, vol. 1, pp. 456 -459, 2000.

[218] P.C. Yu and Lee Hae-Seung, "A 2.5-V, 12-b, 5-MSample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 31 no. 12, pp. 1854 -1861, Dec. 1996.

[219] CS5394 Data Sheet, Cirrus Logic, Inc., http://www.crystal.com

[220] ADS1210/11 Data Sheet, Burr Brown, Inc., http://www.burr-brown.com

[221] AD1555/56 Data Sheet, Analog Devices, Inc., http://analog.com

APPENDICES

APPENDIX A

DEVICE NOISE MEASUREMENTS & ANALYSIS

Assuming the noise shaping is sufficient to essentially eliminate the quantization noise contribution at low frequencies, the dynamic range of a ΣΔ modulator is limited by the input-referred noise of the first integrator stage. Since maximizing dynamic range is the primary objective of this research, careful design and noise analysis of the first integrator stage is essential. Thus, a study of the device noise characteristics is warranted for two reasons: to obtain improved noise simulation models allowing more accurate prediction of circuit noise performance, and to produce noise minimization strategies that can be employed in the design of future modulators fabricated using the SOS fabrication process targeted for this research.

In this appendix, the noise associated with MOSFET devices is summarized. Inversion coefficient representation is introduced and the significance of this method for describing device biasing and its relation to noise is summarized. Details of a noise measurement system used for individual device measurement are provided and noise data obtained for a number of SOS MOSFET devices are presented. Results of this analysis will lead to a better understanding of the measured noise performance of a fabricated ΣΔ modulator, and will help produce noise minimization strategies for improving the dynamic range of ΣΔ modulator circuits fabricated in SOS CMOS.

1 Noise in MOSFETs

In MOSFETs the input-referred voltage noise spectral density is composed of two primary noise sources:

$$S_e^{\,2}(f) = S_W^2 + \left(\frac{K_a}{C_{ox}^2 WL}\right)\left(\frac{1}{f}\right). \tag{1}$$

The first term in Eqn. 1 represents the white noise and the second term the $1/f$ or flicker noise. Here K_a is a process specific parameter, C_{ox} is the gate capacitance per unit area, W and L are the gate width and length, and f is the frequency in Hz.

When the device is operated in strong inversion and saturation, the white noise term can be expressed as

$$S_W^2 = 4kT\left(\frac{\alpha}{g_m}\right), \tag{2}$$

where k is Boltzman's constant, T is the temperature in Kelvin, α is a constant usually equal to 2/3 for long-channel devices, and g_m is the device transconductance. In weak inversion, the white noise term can be expressed as

$$S_W^2 = \frac{2qI_D}{g_m^{\,2}}. \tag{3}$$

In strong inversion the transconductance can be expressed as

$$g_m = \sqrt{2\mu C_{ox} I_D\left(\frac{W}{L}\right)}, \tag{4}$$

where μ is the channel mobility and I_D is the device drain current. In weak inversion, g_m is a function of the subthreshold slope factor (n), the thermal voltage (U_T), and the drain current (I_D) as follows:

$$g_m = \frac{I_D}{nU_T}. \tag{5}$$

The flicker noise term from Eqn. 1 is inversely proportional to the gate area, $1/(WL)$. However, the dependence of the flicker noise term on the inversion coefficient is not clearly described in literature and will be initially considered independent for this research.

Combining the previous expressions, the noise spectral density in strong inversion becomes

$$S_e{}^2(f) = \frac{4kT\alpha}{\sqrt{2\mu C_{ox} I_D \left(\frac{W}{L}\right)}} + \left(\frac{K_a}{C_{ox}^2 WL}\right)\left(\frac{1}{f}\right). \tag{6}$$

Likewise, in weak inversion the noise spectral density is approximated by

$$S_e{}^2(f) = \frac{2qn^2 U_T^2}{I_D} + \left(\frac{K_a}{C_{ox}^2 WL}\right)\left(\frac{1}{f}\right). \tag{7}$$

Note that in strong inversion, the white noise term varies inversely with both $\sqrt{I_D}$ and $\sqrt{(W/L)}$, or inversely proportional to g_m. In weak inversion, the white noise term is inversely proportional to I_D. In both inversion regimes the flicker noise term is inversely proportional to the gate area. Given a specific fabrication process, these are the only variables the designer can control to obtain acceptable circuit noise performance.

2 Inversion Coefficient Representation

Inversion coefficient analysis was employed in the design of many circuits that make up the modulator, and in the presentation and analysis of the device noise measurements. A short summary of the inversion coefficient representation and associated equations are given below to familiarize the reader with this new technique.

Presentation of data in terms of the inversion coefficient (IC) was introduced by Vittoz[ref] and provides a measure of the inversion level of a MOSFET. A new design methodology that emphasizes use of this parameter was recently presented by Binkley [ref]. For values of IC < 0.1, the device is defined to be in weak inversion and exhibits an exponential I-V characteristic. Moderate inversion is defined for values of IC between 0.1 and 10. For values of IC > 10, the device is said to be in strong inversion and ideally has a square law I-V characteristic. The point where IC = 1 defines the center of moderate inversion. This is the point where the asymptotes of the strong inversion and weak inversion g_m efficiency curves (g_m/I_D) intersect.

The weak inversion drain current is approximated using

$$I_D \cong I_{D0}\left(\frac{W}{L}\right)e^{\left(\frac{qV_{GS}}{nkT}\right)} \tag{8}$$

where I_{D0} is an empirically determined constant, typically around 20nA for a bulk CMOS process[ref].

The strong inversion drain current is given by

$$I_{D0} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2[1 + \lambda(V_{DS} - V_{eff})] \tag{9}$$

where λ is the channel length modulation parameter, V_{th} is the threshold voltage, and V_{eff} is the effective voltage equal to V_{GS}-V_{th}.

The inversion coefficient can be calculated for a device based on its drain current using the following expression:

$$IC = \frac{I_D}{I_0(W/L)_{eff}} \tag{10}$$

Here, W and L are the effective device channel width and length, respectively. I_0 is the technology current and is defined in terms of the weak-inversion slope factor, n, the thermal voltage ($U_T = (kT)/q$), and the parameter KP,

$$I_0 = 2nKPU_T^2 \tag{11}$$

KP is defined in terms of the mobility, μ_0, and the gate oxide capacitance, C_{ox}

$$KP = \mu_0 C_{ox} \tag{12}$$

Note that the technology current is a constant (at a fixed temperature) and is normalized for a W/L ratio of 1.

Substituting these expressions, the inversion coefficient can be expressed in a number of ways:

$$IC = \frac{I_D}{I_0(W/L)_{eff}} = \frac{I_D}{2n\mu_0 C_{ox} U_T^2 (W/L)_{eff}} = \frac{I_D}{2nKPU_T^2(W/L)_{eff}}. \tag{13}$$

Inversion coefficient representation provides a convenient method for parameterizing the inversion level of MOSFETs and provides the circuit designer with an alternative circuit design methodology that can increase design productivity. Further details of this approach are detailed in [1,2].

3 Noise Measurement System

A noise measurement system was constructed to allow measurement of individual SOS MOSFET devices (see Fig. 1). A custom noise measurement unit (Bink Noise Box, designed by David Binkley and owned by Concorde Microsystems, Inc.) provides a convenient means for biasing the device under test (DUT). A base line restoration (BLR) loop provides the required gate bias to maintain the device at the programmed bias condition (see Fig. 2). Controls for selecting the device type (NMOS or PMOS), and bias parameters V_{DS}, V_{BS}, and I_D as well as a number of other parameters are located on the front panel.

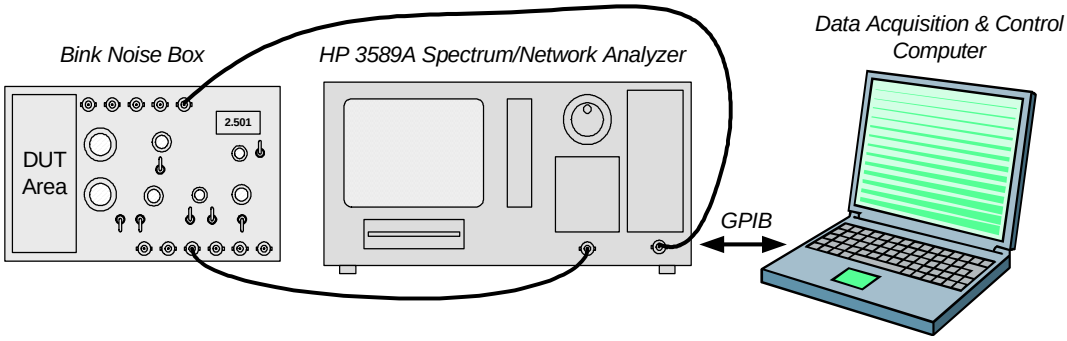


Figure 1 Noise measurement system for SOS device characterization.

An output voltage is generated from the device drain current using a transimpedance amplifier with front panel selectable feedback resistance (R_f) and feedback compensation capacitance (C_c). An LCD display is also located on the front panel that allows monitoring of the device V_{DS}, V_{GS}, V_{BS}, $I_D R_F$, and battery supply levels (see Fig. 3). A Hewlett Packard HP3589A Spectrum/Network Analyzer was used for two primary measurement tasks: to perform the noise measurements, and to determine the system gain used to calculate the device input-referred voltage noise.

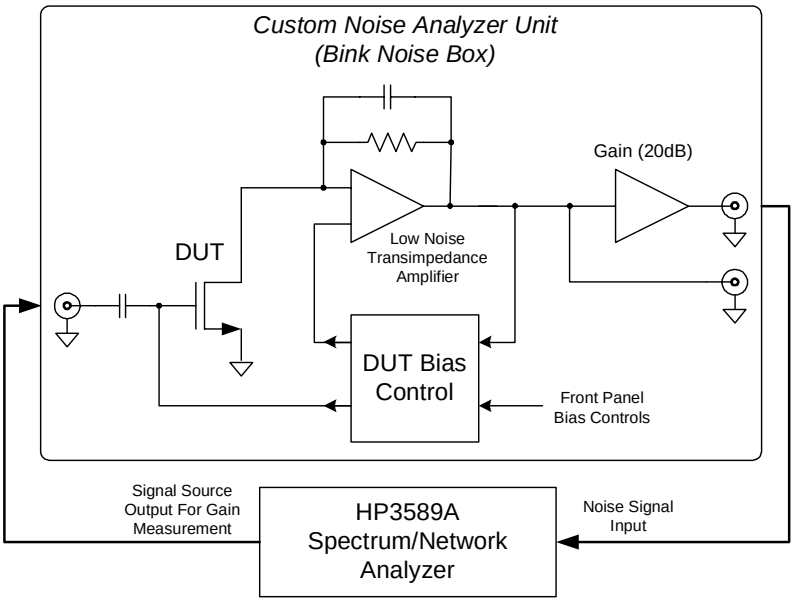


Figure 2 Custom Noise Analysis Unit Block Diagram.

Figure 3 Photograph of Bink Noise Box front panel.

The overall measurement system was controlled using a PC with a custom-designed LabView program and GPIB interface to communicate with the HP 3589A. This program automates a number of functions by allowing the user to setup the experiment, initiate the program, and leave the unit to collect, display, and save the noise measurement data. The user selects the frequency decades for the noise measurements (10 Hz to 1 MHz), the level of noise averaging to perform on each decade, gain fitting including order of fit, and file storage options. In addition, three data plots are shown following each collection cycle: raw analyzer data [dBV/Hz], raw and fitted gain [dB], and input-referred device noise [nV/sqrt(Hz)]. Output data are stored in spreadsheet format allowing direct import into Excel or other suitable graphing software. A screen capture of the custom control program is shown in Fig. 4.

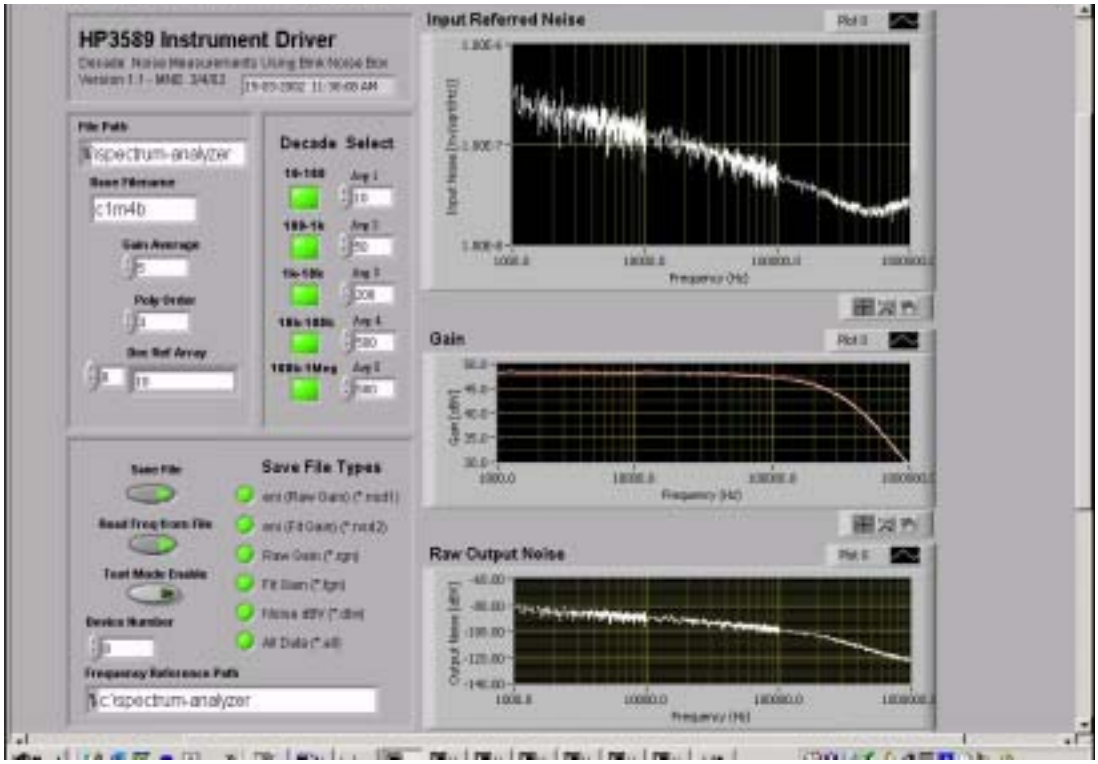


Figure 4 LabView-based noise measurement and control software - front panel.

4 Noise Measurement Results

A test chip was fabricated in a 0.5μm SOS CMOS process having a number of MOS-FET devices for noise characterization. The following table summarizes the devices on this chip (see Table 4.1). A photograph of the chip die is shown in Fig. 5.

Table 4.1: MOSFET device chip (mosdev2_chip) details

Device Ref. [NMOS/PMOS]	**Threshold Type**	**Drawn Size, W/L** [μm/μm]	**Device Area, WxL** [μm^2]	**Drain Pin Number** [NMOS/PMOS]
M1/M8	Low	2/0.5	1.0	10/11
M2/M9	Low	25/0.5	12.5	9/12
M3/M10	Low	50/1	50	8/13
M4/M11	Low	100/2	200	7/14
M5/M12	Low	200/4	800	6/16
M6/M13	Low	400/8	3200	4/17
M7/M14	Low	800/16	12800	3/18
M15/M22	Regular	2/0.5	1.0	31/30
M16/M23	Regular	25/0.5	12.5	32/29
M17/M24	Regular	50/1	50	33/28
M18/M25	Regular	100/2	200	34/27
M19/M26	Regular	200/4	800	36/26
M20/M27	Regular	400/8	3200	37/24
M21/M28	Regular	800/16	12800	38/23

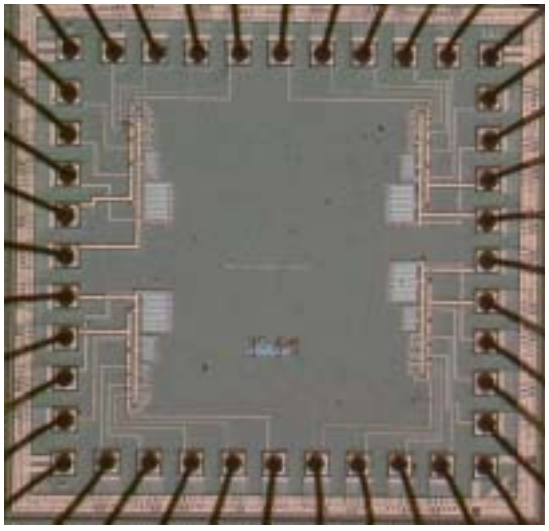


Figure 5 Photograph of device test chip fabricated in 0.5μm SOS CMOS (mosdev2_chip).

A number of noise measurements were performed on the low threshold MOSFET test devices at T=25C using the test system previously described. Figures 6 & 7 show the measured equivalent input noise (eni) for NMOS and PMOS devices in weak inversion, respectively. Fig. 8 shows measured eni for NMOS and PMOS devices together for comparison. In general, the NMOS devices exhibited more ideal noise behavior in terms of single slope for shorter gate lengths and migrated towards a multiple slope characteristic for the longer gate lengths. Conversely, the PMOS devices exhibited multi-slope noise characteristic for short gate lengths gradually moving to a single slope characteristic for longer gate lengths. Both device types exhibited a general slope significantly less than that which is ideal for flicker noise (-1 decades in eni for 2 decades in frequency).

Figures 9 & 10 show both weak inversion (WI) and strong inversion (SI) data measured for the NMOS and PMOS devices, respectively. Here the PMOS devices exhibited little variation in the measured eni from weak inversion to moderate inversion, while the NMOS devices showed significant variation. In general, the NMOS device data shows reduced flicker noise for devices in moderate inversion than in weak inversion, over the measured frequency range of 100 to 100K Hz.

Measured noise values were extracted at specific frequencies (100 Hz, 1kHz, 10kHz, and 100kHz) from the data of Figures 9 & 10 for both moderate and weak inversion. This data is shown plotted in Figures 11 & 12 as a function of gate length (L) for the NMOS and PMOS devices, respectively. These plots further emphasize the NMOS eni dependence on the inversion level, and the PMOS eni lack of dependence on the inversion level. In addition, these curves allow estimation of eni for device lengths not included in the data presented.

The dependence of the flicker noise on the device gate area is demonstrated for the NMOS and PMOS devices in Figures

Theoretically, the flicker noise spectral density should decrease as the square root of the increase in the device area, e.g. increasing WL by 4 should decrease the flicker noise spectral density by 2. The drawn gate area of the test devices used in this research increases by approximately 4 for each doubling of the gate length. From the measured eni noise data of Figures 11 & 12 the values were ratioed for a particular frequency for adjacent device sizes. Specifically, each length device eni was divided by the next longer gate length eni. Theoretically, all ratios should have a value of 2. This data is plotted for both weak inversion and moderate inversion in Figures 13 and 14, for the NMOS and PMOS devices, respectively. The results were very close to the expected values, except for the shortest L NMOS device in WI at low frequencies.

In general, these measurements show that the NMOS devices show some sensitivity to inversion level, particularly at low frequencies. The PMOS devices exhibited very little dependence on the inversion level. However, the tests reported in this work were performed on a very limited set of devices. A more detailed study of SOS MOSFET flicker noise behavior as a function of inversion coefficient is warranted and will help in the design of low-noise analog circuits implemented in SOS-CMOS.

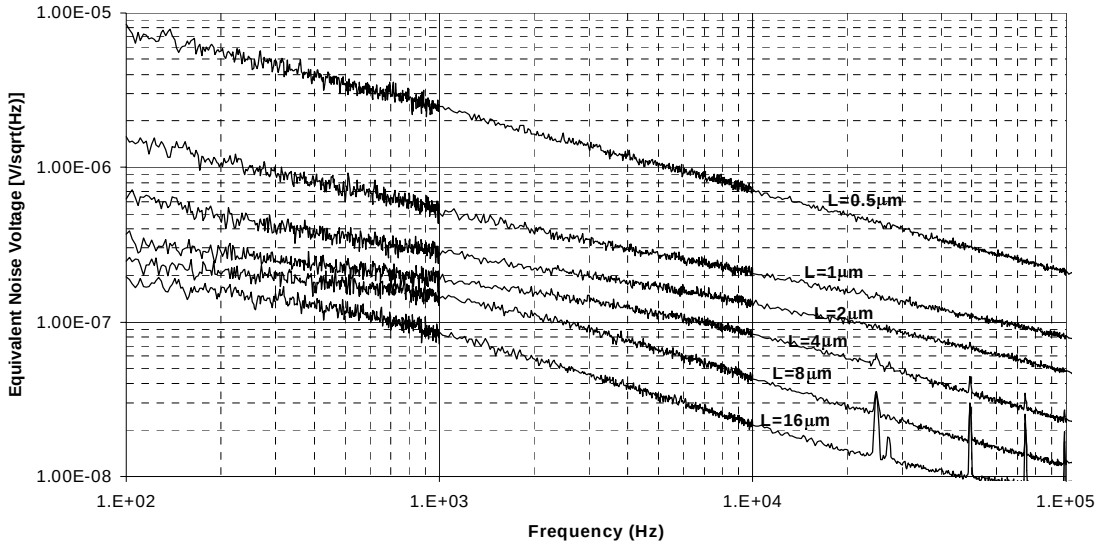


Figure 6 Measured input-referred noise for low threshold NMOS SOS devices in weak inversion.

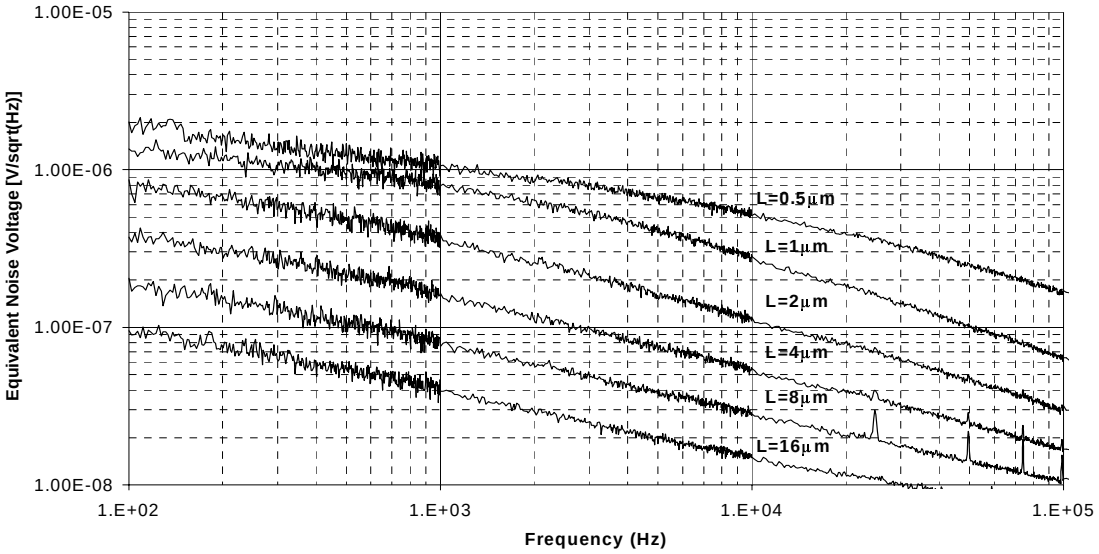


Figure 7 Measured input-referred noise for low threshold PMOS SOS devices in weak inversion.

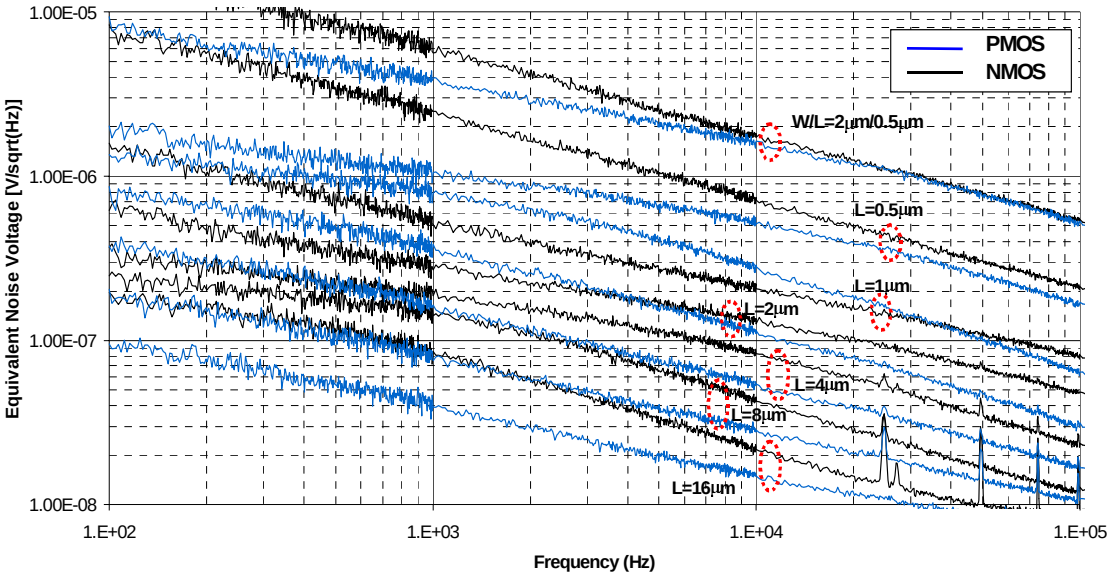


Figure 8 **Measured input-referred noise for low threshold NMOS and PMOS SOS devices in weak inversion.**

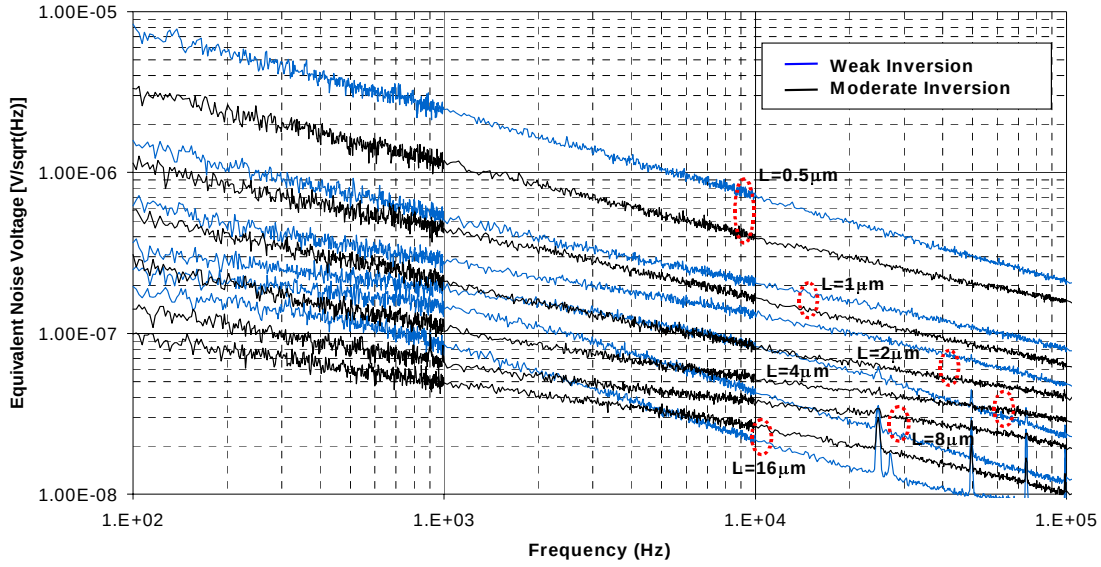


Figure 9 **Comparison of measured noise data for NMOS devices in weak and moderate inversion.**

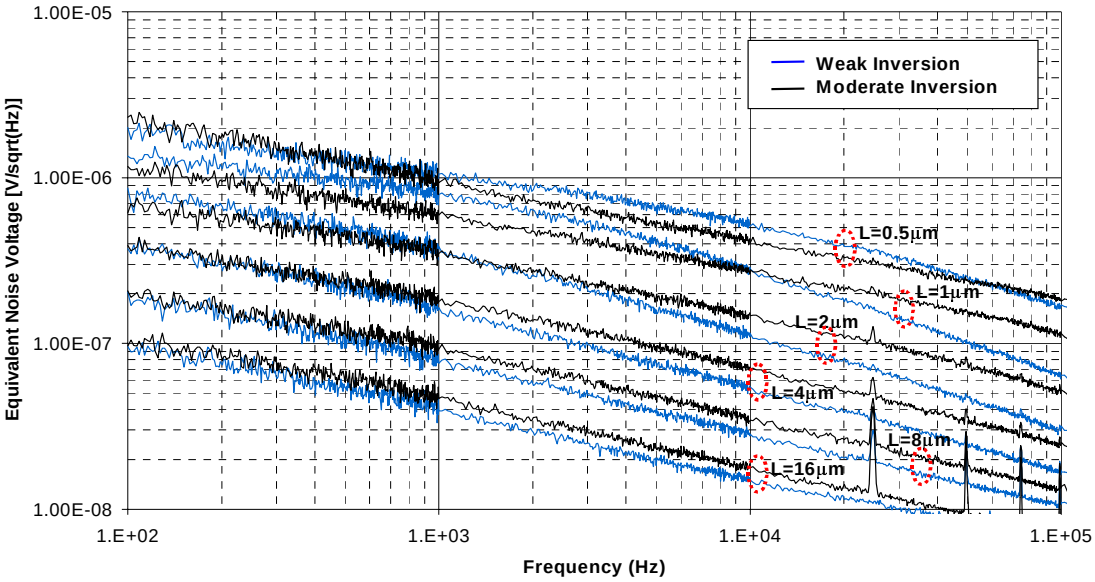


Figure 10 Comparison of measured noise data for PMOS devices in weak and moderate inversion.

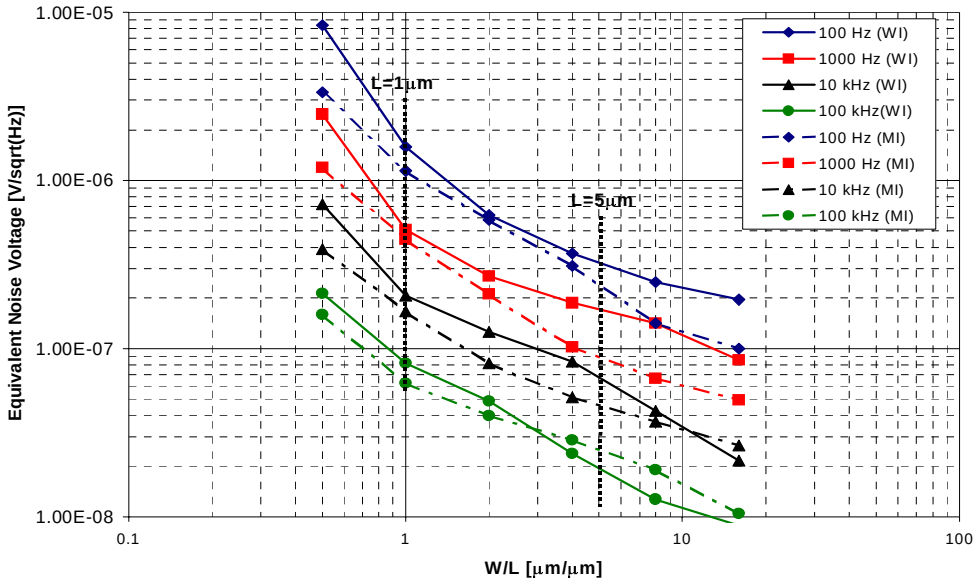


Figure 11 SOS low threshold NMOS device equivalent input noise versus gate length for weak inversion (IC~0.02) and moderate inversion (IC~0.5).

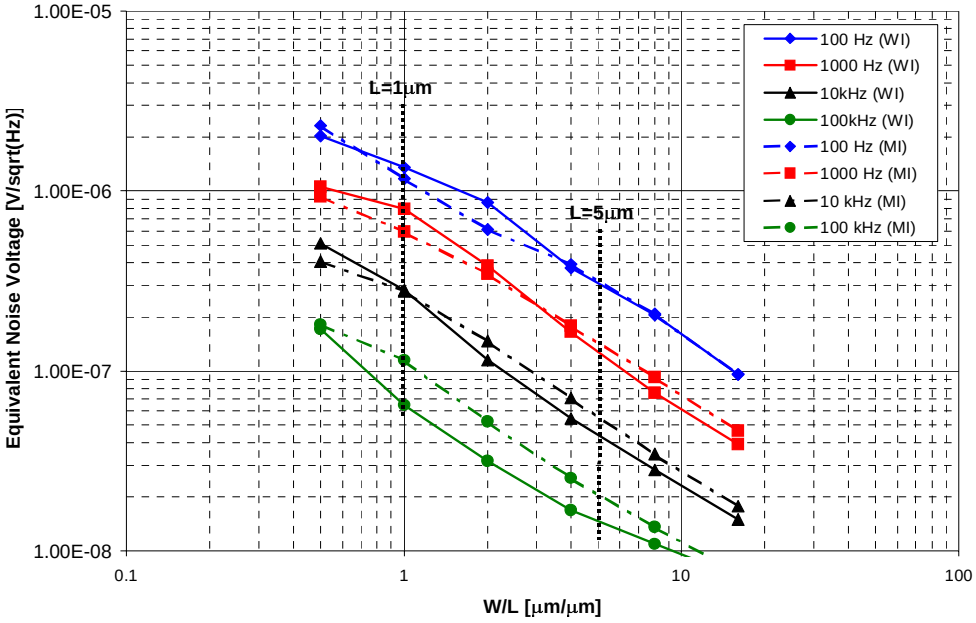


Figure 12 SOS low threshold PMOS device equivalent input noise versus gate length for weak inversion (IC~0.02) and moderate inversion.

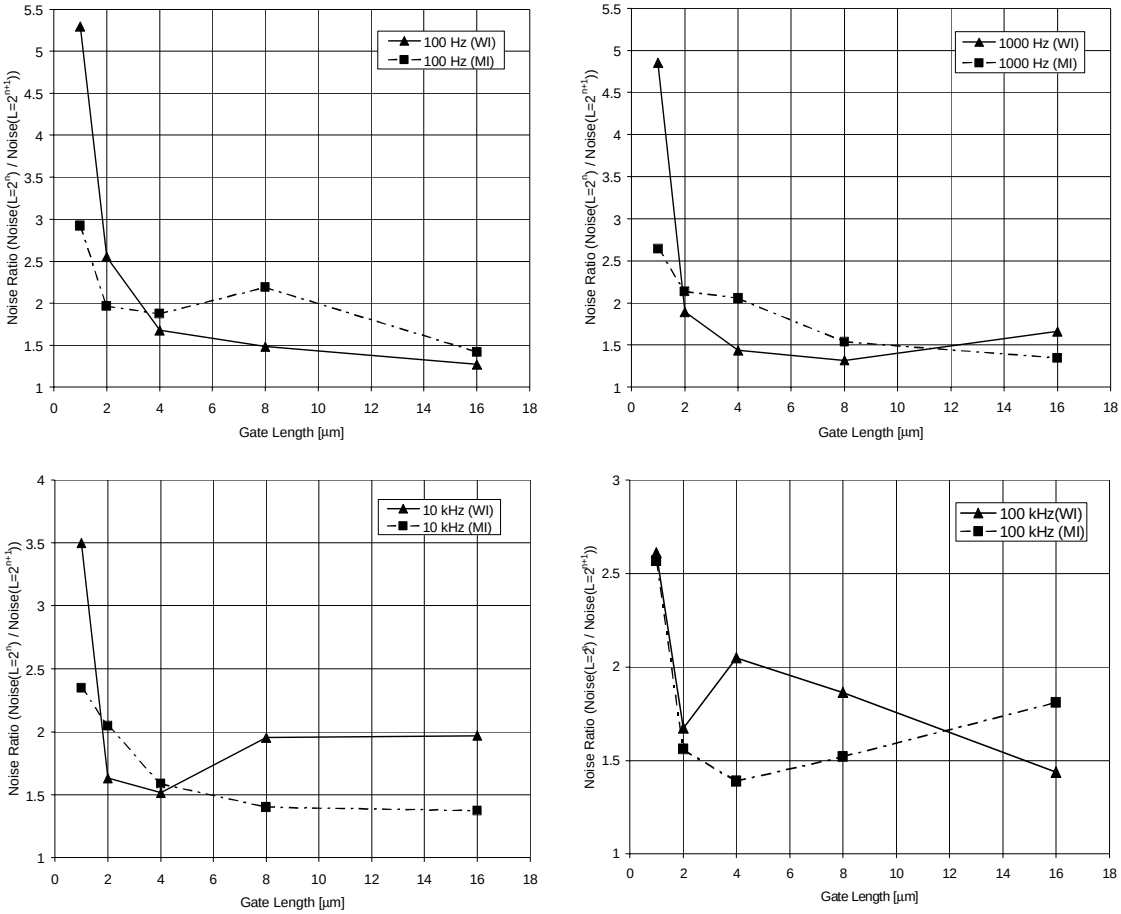


Figure 13 SOS low threshold NMOS noise ratio versus gate length calculated at 100 Hz, 1 kHz, 10 kHz, and 100 kHz for weak inversion (WI, IC~0.02) and moderate inversion (MI, IC~0.5).

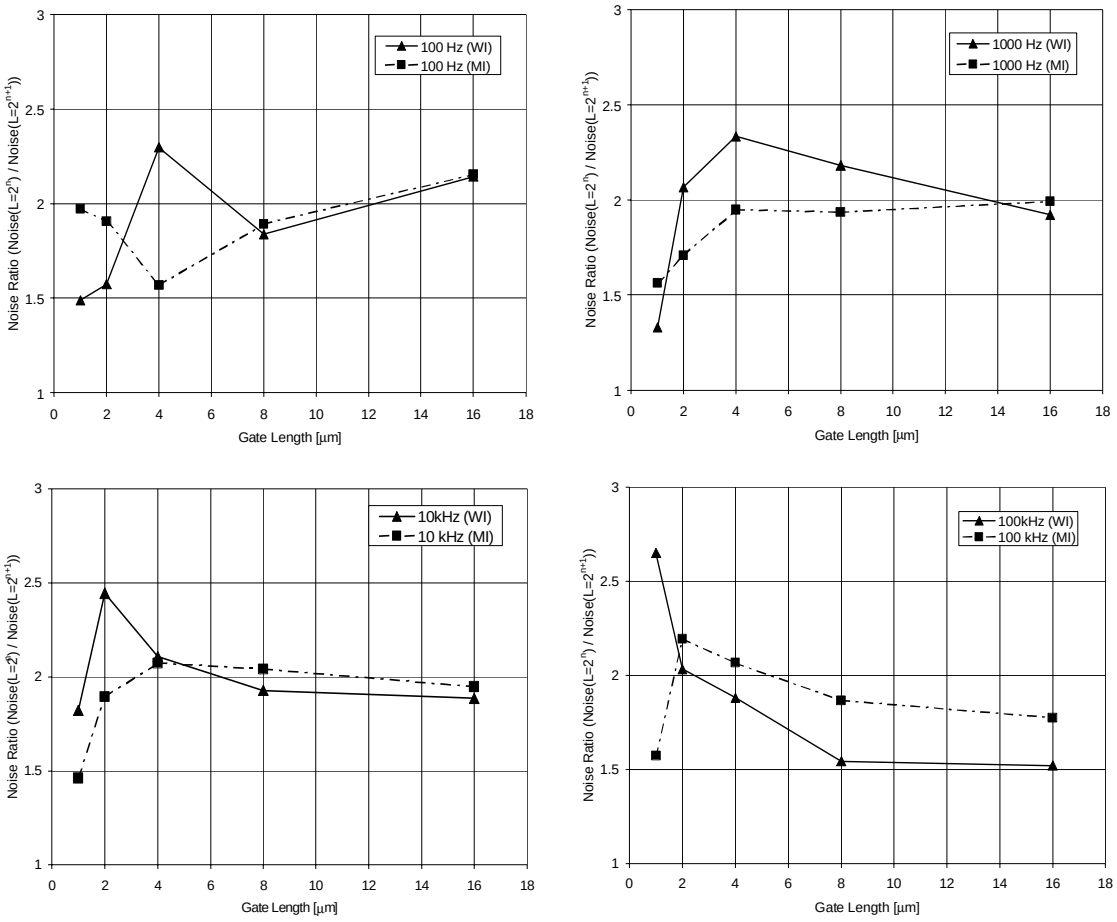


Figure 14 SOS low threshold PMOS noise ratio versus gate length calculated at 100 Hz, 1 kHz, 10 kHz, and 100 kHz for weak inversion (WI, IC~0.02) and moderate inversion (MI, IC~0.5).

Preliminary flicker noise simulations of the SOS devices using foundry supplied device models indicated poor agreement of the simulation results with measured data. In order to improve the model, measured device data was used to iteratively fit the simulation models to match measured data. The foundry supplied Level 49 BSIM model was modified by changing the flicker noise magnitude coefficient (K_a) and the flicker noise slope coefficient (E_f). The results of this fitting operation are shown for both the NMOS and PMOS devices in weak inversion in Figures 15 & 16, respectively. In cases where a dual slope flicker noise characteristic was measured, the low frequency decades where the noise magnitude is largest was used for the fitting operation. This will better model the in-band flicker noise of the experimental ΣΔ modulator that was shown to limit the measured dynamic range.

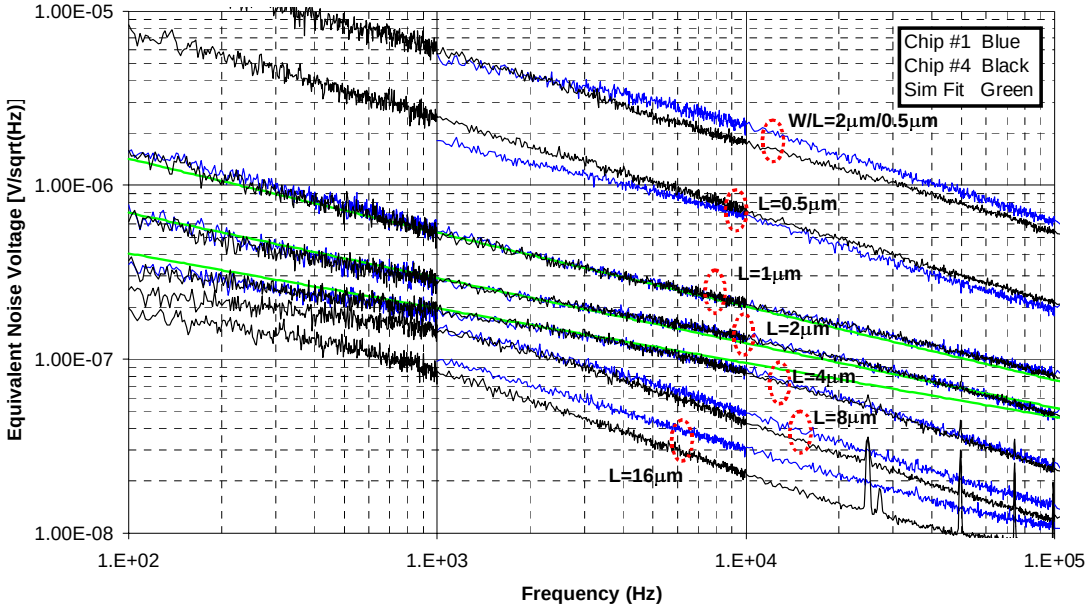


Figure 15 Measured SOS NMOS device eni (Chip 1, W/L_{drawn} = 50, I_D=8.2μA, V_{DS}=2.0V, T=25° C) and simulation results using improved models.

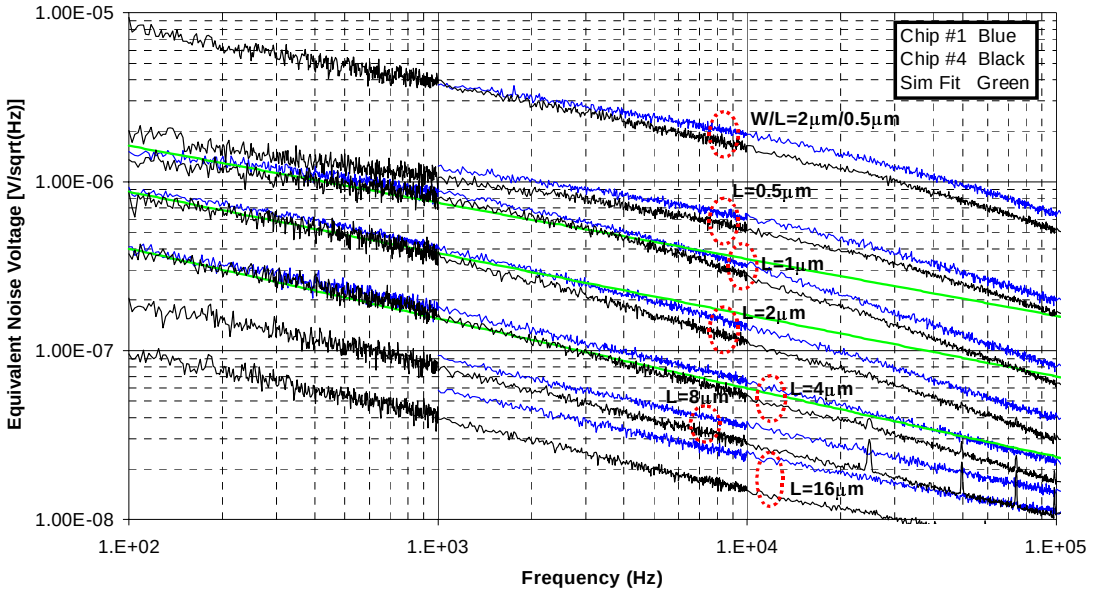


Figure 16 Measured SOS NMOS device eni (Chips 1&4, W/L_{drawn} = 50, I_D~-17μA, V_{DS}=-2.0V, T=25°C) and simulation results using improved models.

References

[1] D. M. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS of the Continuum of Inversion Level and Channel Length," Proc. 7th IEEE Int. Conf. On Electronics, Circuits & Systems ICECS'2k, Kaslik, Lebanon, Dec. 17-20, 2000, pp. 161-164.

[2] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications," Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, 1995, pp. 83-114.

APPENDIX B

ΣΔ MODULATOR TEST & ANALYSIS SYSTEM VERIFICATION

In order to verify proper functioning of the custom test system and to obtain valuable experience in making modulator measurements and performing the related performance calculations, a commercial ΣΔ ADC evaluation system was purchased for comparison with the custom test system. The evaluation system was based on the Analog Devices AD1555/AD1556 24-bit ADC chipset and incorporated a hardware board with a PC parallel port connection and a Windows-based executable for viewing the modulator output spectrum and performing a few dynamic parameter calculations. Initially, the commercial evaluation system was tested separately to collect and process the modulator data. The modulator output from the AD1555 modulator chip was then connected to the custom test system and data collected and processed for comparison of the spectral plots and dynamic calculations. This section will provide the details of the results of these tests including comparison of the results obtained using the custom test system with the specifications provided in the commercial ADC data sheet.

The AD1555 modulator output and associated clock were input directly to the custom data collection board. A limited set of performance tests was performed at each of the following temperatures: 27° C, 125° C, 140° C, and 160° C. The sampling rate on the evaluation board was set to 256 KHz. Depending on the digital filtering used, a number of different DORs and associated value of M can be implemented. The digital filtering used in these measurements was implemented as three separate FIR filters with interstage deci-

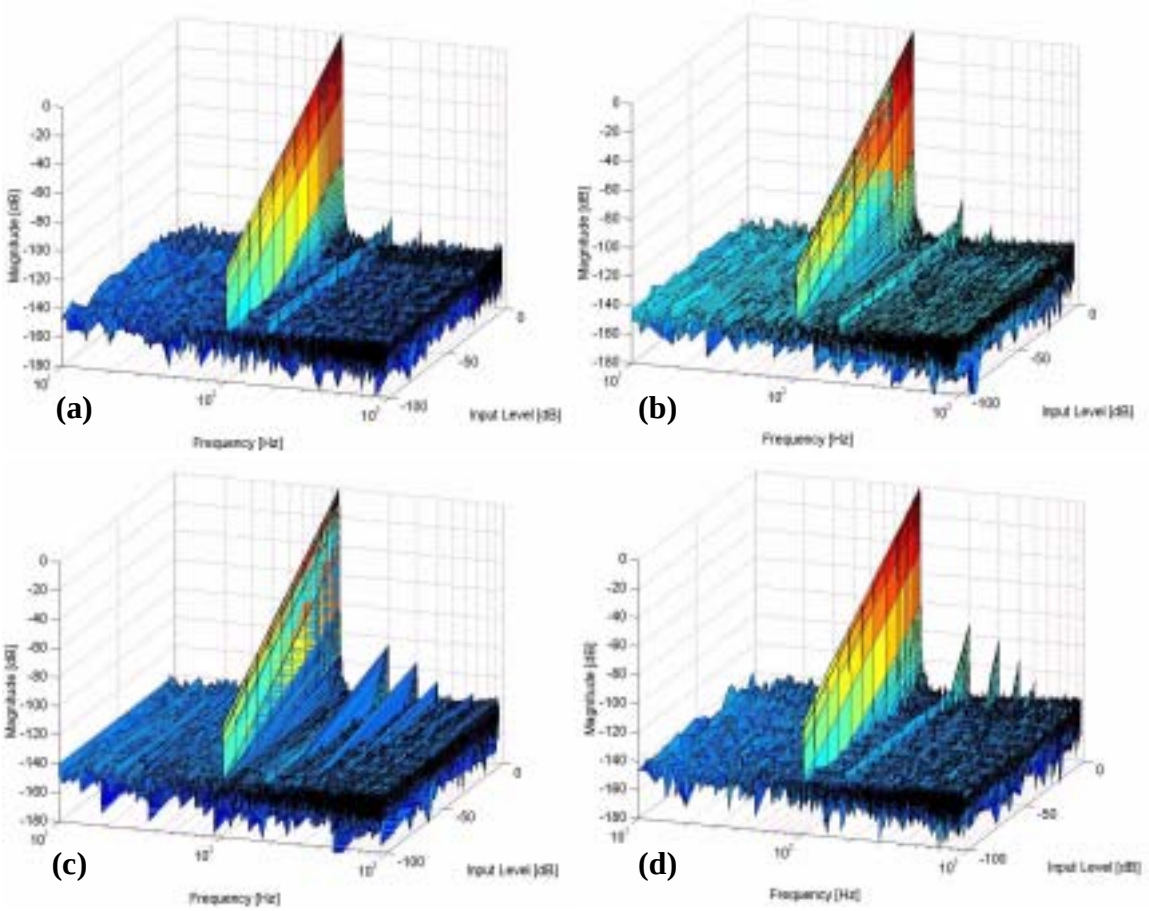
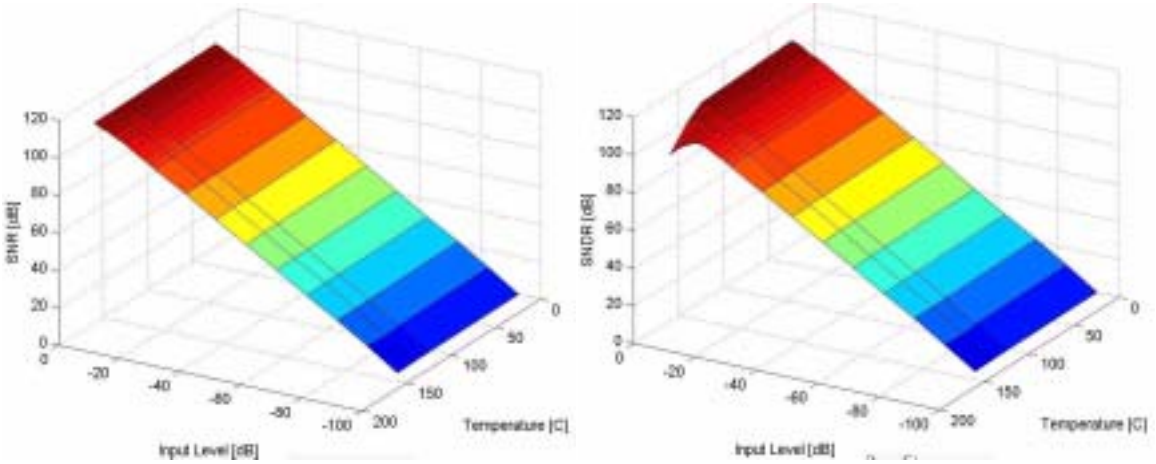


Figure 1 AD1555 modulator output spectrum. Figure 2(a) 27° C, (b) 125° C, (c) 140° C and (d) 160° C.

mation. The filter taps were designed using Matlab *sptool* and decimation ratios of 8, 4, and 4 were incorporated following each of the FIR filters. All calculations were performed using a signal bandwidth of 1kHz (M=128, DOR=2kHz).

Fig. 1 shows the modulator output spectrum obtained at 27° C, 125° C, 140° C, and 160° C using an ~8000-point FFT with a stepped input ranging from full scale (0 dB) to -100 dB of full scale. Note the increase in harmonic distortion and spreading about the fundamental at elevated temperatures.

Plots of SNR and SNDR as a function of input level and temperature are shown in Fig. . Fig. shows the calculated THD as a function of temperature and input level. Note that all performance measurements were calculated using a 1000-Hz signal bandwidth.



(a) **(b)**

Figure 2 AD1555 measurements Vs. input level & temperature: (a) SNR and (b) SNDR.

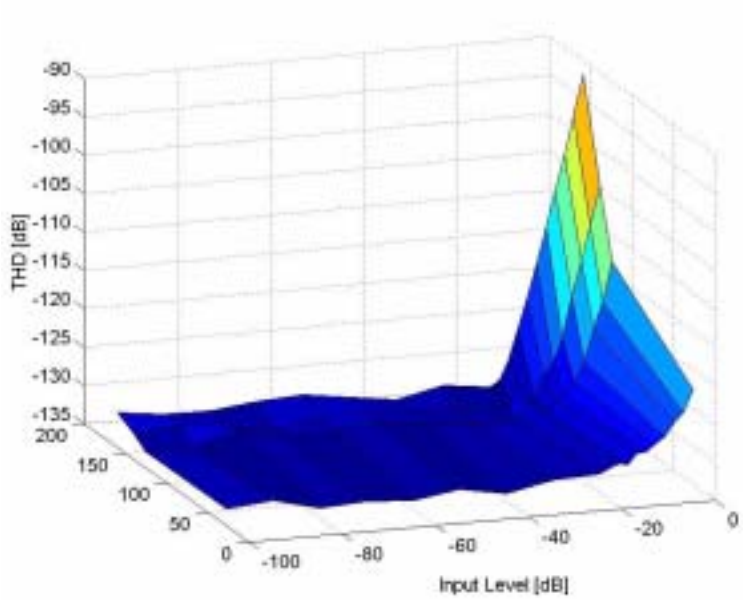


Figure 3 AD1555 THD vs. input level and temperature.

Table 1 and Table 2 show a summary of measured performance parameters and provide corresponding AD1555 specifications, when available. The data was calculated from 1,048,576 modulator samples using a 1-kHz bandwidth. Overall, the AD1555 performed very well in these tests. The room temperature measured data agrees well with the AD1555 data sheet information. Some discrepancies are seen in the DR measurement. The improved performance published by Analog Devices (116dB minimum, 120dB typical in 1-kHz bandwidth) is measured with shorted inputs. In these tests, the data were taken with a very small input signal (SNR ~ 1) which conforms to audio testing standards. Under this measurement condition, a very small 60-Hz signal was coupled into the input that degraded the DR. Performing this measurement again with shorted inputs should provide better agreement.

Table 1: Comparison of DR and THD data.

Dynamic Range Measured (bits / dB)	Dynamic Range AD1555 Data Sheet (bits / dB)	Total Harmonic Dist. Measured @ -6dB (dB)	Total Harmonic Dist. AD1555 Data Sheet (dB)
18.17 / 111.16 (27° C)	18.97 / 116 Minimum 19.64 / 120 Typical (0-85° C)	-128.4 (27° C)	-120.6 (0-85° C)
18.01 / 110.19 (125° C)		-126.2 (125° C)	
17.96 / 109.87 (140° C)		-118.9 (140° C)	
17.93 / 109.70 (160° C)		-106.6 (160° C)	

Table 2: Summary of Measured SNR and SNDR data.

SNR Measured with 0dB Input (dB)	SNR AD1555 Data Sheet (dB)	Measured Peak SNDR (dB)
108.7 (27° C)	116.7 (0-85° C)	108.3 (27° C)
107.5 (125° C)		105.4 (125° C)
106.9 (140° C)		102.3 (140° C)
106.8 (160° C)		97.3 (160° C)

In addition, the measured SNR was smaller than that specified by Analog Devices. This discrepancy can be attributed to the non-trivial issue of filtering out the fundamental frequency from the FFT data in the SNR calculation. This filter was applied by removing a number of FFT bins on either side of the fundamental and replacing these bins with an average value obtained from adjacent bins. In this work, the number of bins replaced was determined by simulating the spreading of the fundamental due to the Nuttall window, and determining the number of bins where the spreading was above the noise floor. In both the measured modulator spectrum and the published AD1555 modulator spectrum it is apparent that some spreading (or skirting) of the fundamental occurs for large input signals (see Fig. 4). This phenomenon is real and contributes a significant amount of noise power that degrades both the SNR and SNDR. It appears that this spreading phenomenon was not fully included in the calculations performed by Analog Devices. The measured decrease in SNDR with temperature is expected given the increase in the harmonic tones with increasing temperature demonstrated in Fig. 1.

Overall, the AD1555 modulator performed well over the range of temperatures tested, with some performance degradation. Careful attention to the setup and testing method was given to ensure valid results, including the use of an Analog Devices evaluation board and measurement comparisons performed using the complete Analog Devices evaluation system and processing software. The modulator output spectrum and performance calculations agreed nicely between the two systems and the data sheet validating the custom testing system. Though this device does operate at 160° C, long-term reliable performance and survivability is unlikely since the part was not specified, designed or packaged for use at temperatures exceeding commercial temperature range (0 - 85° C).

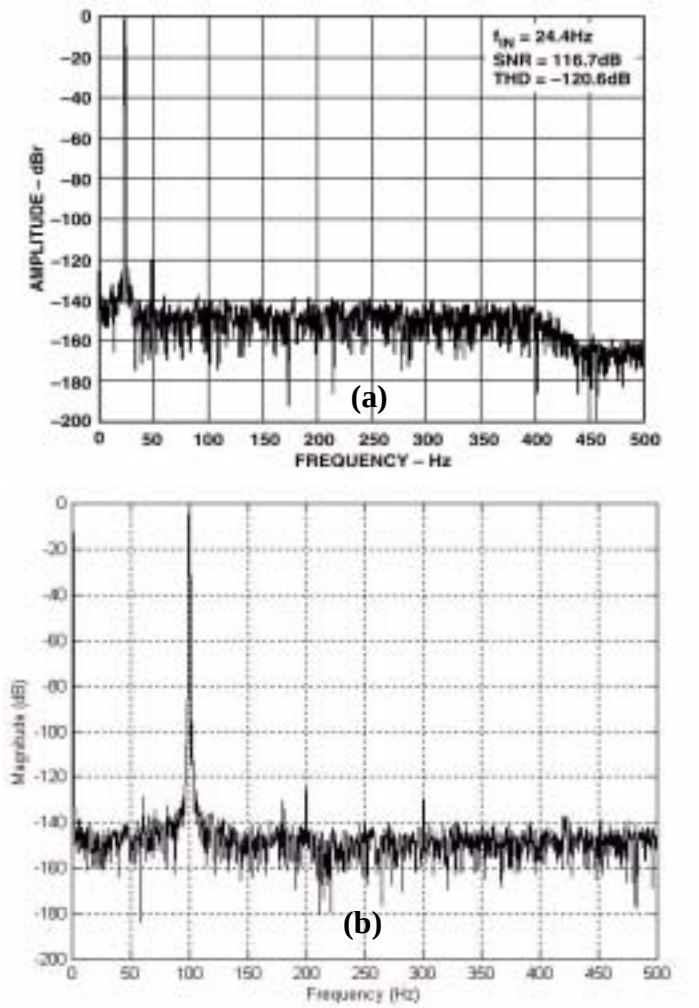


Figure 4 Comparison of AD1555 modulator output spectrum. (a) provided by AD1555 data sheet and (b) measured using custom measurement systen

The results of this characterization exercise indicate reasonable acceptable performance of the custom test system since agreement between measured performance and the device specifications was demonstrated (see Table 1 and Table 2). Several key issues associated with performance calculations, device fixturing, supply filtering, and shielding were also addressed in this exercise making it very valuable to the overall objectives of both validating the custom test system and obtaining experience in making modulator measurements.

APPENDIX C

RELATED PAPER SUBMISSIONS

Three paper summaries related to this work have been submitted to engineering conferences. The paper titles and associated conferences are listed below. Each of the paper submissions are included in the remainder of this appendix.

Comparison of 2nd- and 4th-Order ΣΔ Modulators Fabricated in 3.3V 0.5μm SOS-CMOS for High-Temperature Applications

M.N. Ericson[1], J.M. Rochelle[2], M. Bobrek[1], C.L. Britton[1], A. Bobrek[1], B.J. Blalock[2], R. Schultz[3], and J.A. Moore[1]

[1]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006
[2]The University of Tennessee, Knoxville, TN 37996
[3]Halliburton Energy Services, Inc., Carrollton, TX 75006

(submitted to IEEE 2002 SOI Technology Conference)

A Fully Differential Folded-Cascode Amplifier in 0.5μm Silicon-On-Sapphire for High-Temperature Applications

M.N. Ericson[1], J.M. Rochelle[2], C.L. Britton, Jr.[1], B.J. Blalock[2], and R. Schultz[3]

[1]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006
[2]The University of Tennessee, Knoxville, TN 37996
[3]Halliburton Energy Services, Inc., Carrollton, TX 75006

(submitted to IEEE 2002 SOI Technology Conference)

Noise Behavior of MOSFETs Fabricated in 0.5μm Fully-Depleted (FD) Silicon-on-Sapphire (SOS) CMOS In Weak, Moderate, and Strong Inversion

M. N. Ericson[1], C. L. Britton, Jr.[1], A. L. Wintenberg[1], J. M. Rochelle[2], B. J. Blalock[3], and D. M. Binkley[4]

[1]*Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006*
[2]*Concorde Microsystems, Inc., Knoxville, TN 37932*
[3]*The University of Tennessee, Knoxville, TN 37996*
[4]*The University of North Carolina, Charlotte, NC 28223-0001*

(submitted to IEEE 2002 Nuclear Science Symposium & Medical Imaging Conference)

Comparison of 2nd- and 4th-Order ΣΔ Modulators Fabricated in 3.3V 0.5μm SOS-CMOS for High-Temperature Applications

M.N. Ericson[1], J.M. Rochelle[2], M. Bobrek[1], C.L. Britton[1], A. Bobrek[1],
B.J. Blalock[2], R. Schultz[3], and J.A. Moore[1]

[1]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006
[2]The University of Tennessee, Knoxville, TN 37996
[3]Halliburton Energy Services, Inc., Carrollton, TX 75006
Email: ericsonmn@ornl.gov, Tel: (865) 574-5637

ABSTRACT

A ΣΔ modulator fabricated in 0.5μm SOS-CMOS is reported. The design incorporates two 2nd-order loops allowing reconfigurability as either a 2nd-order single loop or a 4th-order 2-2 cascade. Test results of the both modulator configurations over a temperature range of 25°C-200°C are presented for a range of input signal bandwidths and oversampling ratios. The modulator achieves an effective resolution of 14.4 bits resolution at 2 KSPS at room temperature. Design details pertaining to topological selection and device sizing is presented with an emphasis on temperature tolerance. Results of modulator noise analysis is presented along with techniques for improving the modulator noise performance. This paper represents the first reported 4th-order ΣΔ modulator fabricated in an SOI/SOS process.

INTRODUCTION

Improvements in high-temperature analog-to-digital conversion are needed for application to extreme temperature environments including geothermal, automotive, space flight, and reactor monitoring. ΣΔ methods incorporating oversampling and noise shaping provide improved resolution over Nyquist-rate conversion methods by trading component accuracy for time. This property of oversampled converters makes them ideal for high-temperature applications since component errors and drifts associated with elevated temperature are well tolerated compared to other analog-to-digital conversion (ADC) techniques.

Several papers have been published on ΣΔ modulators implemented in SOS/SOI for high-temperature or radiation environments [1-3]. Though significant, these reported designs implement 2nd-order noise shaping and produce at best 13 bits of resolution. This research addresses the need to extent the obtainable resolution of ΣΔ ADCs fabricated in SOI/SOS for high-temperature applications and reports the first 4th-order modulator architecture fabricated in SOS/SOI.

SUMMARY

The modulator reported was designed with special consideration for high-temperature operation. Though cascade topologies do present some disadvantages when compared to single-loop structures, namely reduced input dynamic range and matching errors, the topology composed of two 2nd-order loops is inherently stable. High-order single-loop modulator architectures offer slightly improved dynamic range and allow for more straight-forward implementation of the digital decimation filters, but require proper initialization, monitoring and compensation to ensure robust stability. For these reasons, a 2-2c cascaded architecture was selected. The classical integrator gain was implemented since it has been shown to be less sensitive to matching errors as compared to alternative gain selections that minimize the required integrator output swing [4]. The 2-2c modulator architecture is shown in Figure 1.

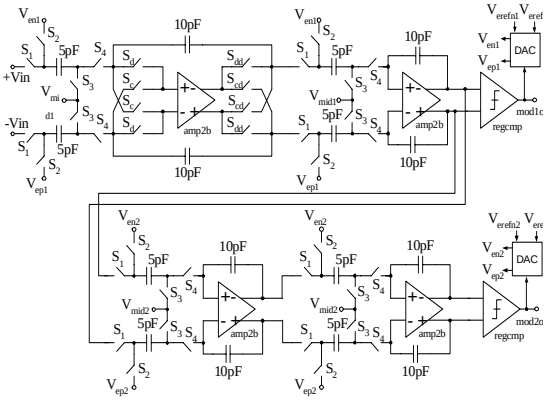


Figure 1. 2-2c cascade modulator architecture with 1st-stage chopper integrator.

The modulator was fabricated in 0.5μm SOS and tested using a custom-designed test system with LabView-based data acquisition and analysis software. A sample measured output spectrum as a function of input amplitude is shown in Figure 2 for a 144 Hz sine input. Each FFT size is ~1M points. The chips were

tested from 25°C to 200°C in 25°C steps. At each temperature step the SNR, SNDR, and THD were calculated as a function of input amplitude. Test results indicate decreased peak SNR with temperature as expected. However, this is believed to be the result of increased electronic noise and not quantization noise shaping as demonstrated by both the measured dc gain of the integrator amplifier and observed slope of the shaped quantization noise at high temperature.

For comparison, the peak SNR was calculated from measured data for both the 2^{nd}-order and 4^{th}-order modulators for a number of oversampling ratios and is presented in Figure 3. At higher oversampling ratios, the 2^{nd}-order outperforms the 4^{th}-order due to the reduced input dynamic range for the 4^{th}-order. However, at lower oversampling ratios (~100) the 4^{th} order produces better SNR due to the improved quantization noise shaping. Thus, the design is electronic noise limited and not quantization noise shaping limited. As a result, reduction of the input-referred integrator amplifier noise will result in improved dynamic range. A summary of test data is shown in Tables 1 & 2.

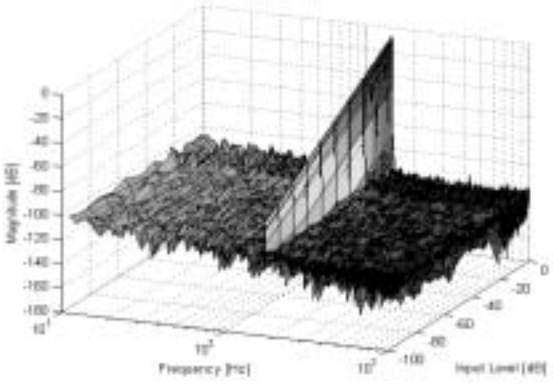


Figure 2. Measured modulator output spectrum vs input fundamental amplitude (f_{in}=144 Hz, T=25C).

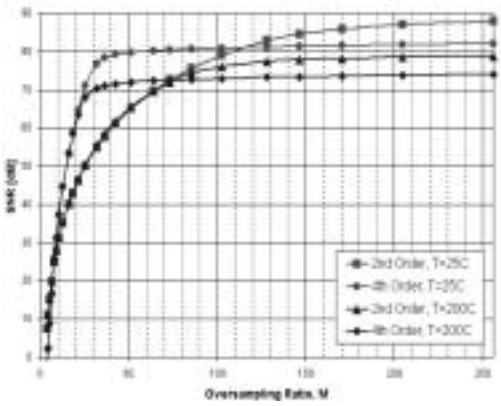


Figure 3. Measured SNR vs OSR for 2^{nd}- and 4^{th}-order modulators.

Testing demonstrates low-frequency noise reduction by the chopper circuit at low frequencies but the introduction of spurious tones due to chopper clock coupling and folding into the baseband produces a zero net improvement in modulator performance.

Table 1. Measured modulator performance (DOR=2KSPS)

Parameter	**T=25°C (2^{nd} / 4^{th})**	**T=150°C (2^{nd} / 4^{th})**	**T=200°C (2^{nd} / 4^{th})**
SNR [dB]	87.9 / 82.0	83.6 / 78.0	78.8 / 74.0
Res. [bits]	14.2 / 13.1	13.5 / 12.4	12.8 / 11.8
SNDR [dB]	87.9 / 81.9	83.6 / 78.0	78.8 / 74.0
THD [dB]	-110.1/ -99.2	-101.9 / -96.61	-90.1 / -88.5

Table 2. Measured modulator performance (DOR=16KSPS)

Parameter	**T=25°C (2^{nd} / 4^{th})**	**T=150°C (2^{nd} / 4^{th})**	**T=200°C (2^{nd} / 4^{th})**
SNR [dB]	54.9 / 76.7	55.3 / 74.3	55.5 / 70.5
Res. [bits]	9.0 / 12.3	9.0 / 11.9	9.0 / 11.9
SNDR [dB]	54.9 / 76.7	55.3 / 74.3	55.5 / 70.5
THD [dB]	-110.2 / -99.2	-101.9 / -96.6	-90.1 / -88.5

This work represents the first presentation of a 4^{th}-order ΣΔ modulator in SOI/SOS and demonstrates the feasibility of high-resolution data conversion in SOS using ΣΔ techniques at elevated temperatures. Over the entire temperature range, the measured modulator performance indicates that the design is input-noise limited and not quantization noise limited. Therefore, improved performance can be obtained with better noise management. In particular, noise reduction techniques such as input chopping or correlated double sampling (CDS) must be used to avoid audio frequency dynamic range degradation due to high MOS transistor flicker noise. An improved design implementing both an improved low-noise integrator amplifier and 1^{st}-stage CDS for low-frequency noise reduction is scheduled for June 2002 submission. Additional information on low-noise amplifier design, noise measurement, and candidate noise reduction techniques including correlated double sampling and chopping will be discussed. In addition, a more thorough presentation of the measured modulator results versus temperature will be provided.

REFERENCES

[1] A.Viviani, D. Flandre, and P. Jespers, "High-temperature sigma-delta modulator in thin-film fully-depleted SOI technology," *Electronics Letters*, vol. 35, no. 9, April 29, 1999, pp. 749-751.

[2] C.F. Edwards et al., "A multibit Sigma Delta modulator in floating-body SOS/SOI CMOS for extreme radiation Environments," *IEEE J. Solid-State Circuits*, vol. 34 no. 7, July 1999, pp. 937 -948.

[3] A. Swaminathan et al., "A low power Sigma Delta analog-to-digital modulator with 50 MHz sampling rate in a 0.25 mm SOI CMOS technology," 1999 IEEE International SOI Conference Proceedings, pp. 14 -15.

[4] F. Medeiro et al., Top-Down Design of High-Performance Sigma-Delta Modulators, Kluwer Academic Publishers, Boston, 1999, ISBN 0-7923-8352-4.

A Fully Differential Folded-Cascode Amplifier in 0.5μm Silicon-On-Sapphire for High-Temperature Applications

M.N. Ericson[1], J.M. Rochelle[2], C.L. Britton, Jr.[1], B.J. Blalock[2], and R. Schultz[3]

[1]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006
[2]The University of Tennessee, Knoxville, TN 37996
[3]Halliburton Energy Services, Inc., Carrollton, TX 75006
Email: ericsonmn@ornl.gov, Tel: (865) 574-5637

ABSTRACT

A fully differential, folded cascode opamp fabricated in 3.3V 0.5μm SOS-CMOS is reported. The design is intended for use in data acquisition systems operating at temperatures up to 200°C. The amplifier topology is a folded cascode with continuous-time common-mode feedback allowing use in either sampled- or continuous-time applications. Results of the amplifier characterization performed over a temperature range of 25°C-200°C are presented including loop gain, bandwidth, stability, settling and noise. Design details pertaining to topological selection, amplifier biasing, and device sizing are presented with an emphasis on temperature tolerance and noise performance. In addition, a thorough noise analysis is presented along with comparison of simulated and measured noise for both individual SOS MOSFETs and the fabricated amplifier.

INTRODUCTION

Operational amplifiers play a crucial role in the development of many data acquisition systems. The ideal operational amplifier is characterized by infinite gain and bandwidth, zero noise, and has infinite input impedance and zero output impedance. However, the realization of opamp structures imposes significant limits on these performance parameters due to practical design and implementation issues such as device limitations, power and size constraints, and parasitics. The addition of temperature effects further restricts the performance of integrated circuits and introduces temperature-dependent errors that diminish the efficacy of many designs in high-temperature applications [1].

In any feedback amplifier the open loop characteristics of the opamp impact the accuracy of the desired circuit transfer function. The primary open loop parameters of interest include the low-frequency or dc gain, and the location of the poles that in conjunction with the external components determine the frequency response and stability of the circuit. In ΣΔ modulators, the open loop gain is a critical parameter as non-infinite gains produce some level of quantization noise leakage into the baseband. Other parameters of interest for ΣΔ applications include settling, slew rate, output swing, and noise bandwidth. For any sampled-time system the settling time determines the level of error at the end of the sampling period and is considered a linear error. The slew rate is a nonlinear error and can be a significant source of distortion. The output swing and the noise bandwidth both contribute to the overall dynamic range of the circuit, particularly in sampled-time systems where undersampling of the noise causes folding of noise into the baseband. Clearly, these parameters vary with temperature and must be carefully considered in the opamp design so that some minimum performance is maintained over the entire temperature range. In this paper an opamp is presented that addresses the primary design issues associated with designing an opamp for high temperature applications.

SUMMARY

A folded cascode amplifier was designed for use in a harsh environment ΣΔ modulator as well as other high temperature applications. A fully differential architecture was implemented for rejection of common-mode noise and offsets. Preliminary simulations and SOS MOSFET device measurements indicate that either a multi-stage topology or cascoded topology is required to obtain open loop dc gains on the order of 2000. Multi-stage topologies require more than one common-mode feedback loop (CMFB) and are typically more difficult to compensate than single-stage structures [2]. Conversely, a folded cascode topology produces high loop gain, requires a single CMFB loop, and is more easily compensated. Disadvantages of this architecture include increased input-referred noise and limited output swing due to the cascode devices. However, the stability advantages of the folded cascode over multi-stage topologies make it more desirable for wide temperature application.

The amplifier was fabricated in a 0.5μm SOS-CMOS process (see Figure 1). Continuous-time CMFB was incorporated to allow use in both sampled- and continuous-time applications. The output of the amplifier is buffered using source followers made of

intrinsic devices (~zero threshold voltage) and the common-mode voltage determined using a resistance divider. The CMFB loop compares this voltage to a CMFB reference and controls the load devices M9 & M10 to maintain the output at the desired common-mode level. Low voltage cascode biasing is used throughout to provide maximized output swing and precise bias setting [3,4]. The bias circuit for the amplifier is shown in Figure 2.

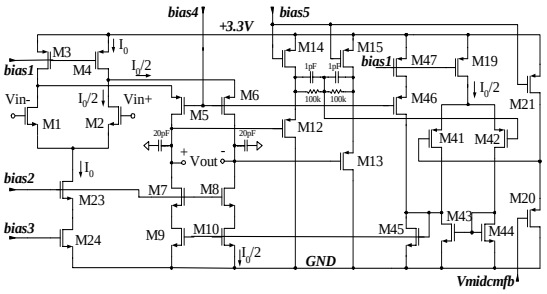


Figure 1. Folded cascode opamp with common-mode feedback.

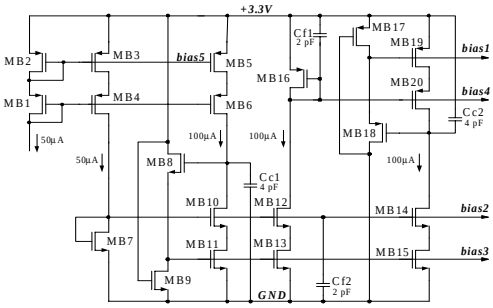


Figure 2. Opamp bias circuitry incorporating low-voltage cascodes

A number of measurements were performed on the amplifier from 25°C to 200°C. Figure 3 shows the open loop response of the amplifier as a function of temperature with 20pF load capacitance. Table 1 summarizes the preliminary results of the testing.

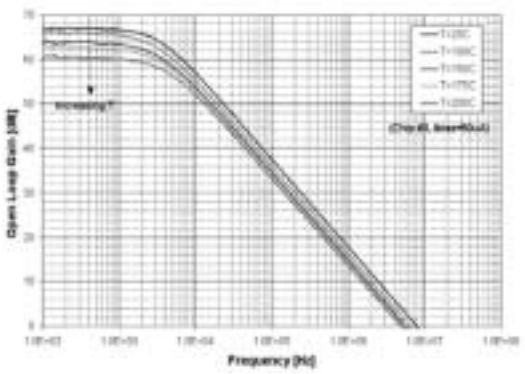


Figure 3. Measured DC open loop gain vs. temperature.

Table 1. Opamp Measured Performance Summary

Parameter	T=25°C	T=150°C	T=200°C
A_{ol} [V/V]	2298	1611	1117
GBW	7.85MHz	5.60 MHz	4.99 MHz

Figure 4 shows the measured equivalent input noise of the amplifier. The illustrated high flicker noise limits front-end audio frequency applications to those that employ chopper or CDS for flicker noise reduction.

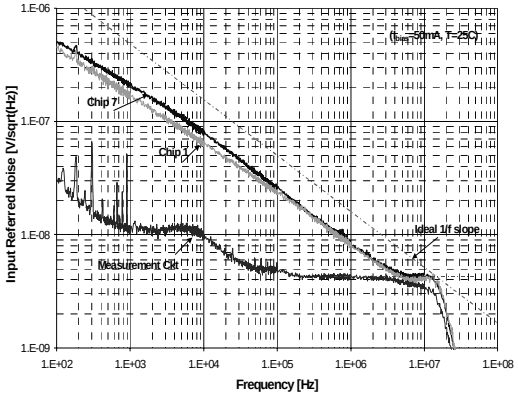


Figure 4. Measured equivalent input noise.

Specifics of the design including topology selection, low-voltage cascode biasing for maximizing output swing, common-mode feedback control, device sizing, and related noise issues will be presented in detail and supported by actual measurements where appropriate. Measurements presented will include open loop characteristics, slew rate, power dissipation, and input-referred noise. In addition, simulation results using models fitted to match actual device noise measurements will be presented and compared with measured opamp noise data.

REFERENCES

[1] Jean-Paul Eggermont, Denis De Cuester, Denis Flandre, Bernard Gentinne, Paul G. A. Jespers, Jean-Pierre Colinge, "Design of SOI CMOS Operational Amplifiers for Applications up to 300°C," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, February 1996, pp 179-186.

[2] F. Medeiro, Angel Perez-Verdu, and Angel Rodriguez-Vazquez, Top-Down Design of High-Performance Sigma-Delta Modulators, Kluwer Academic Publishers, Boston, 1999, ISBN 0-7923-8352-4.

[3] D. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, New York, 1997, ISBN 0-471-14448-7.

[4] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, New York, 2001, ISBN 0-471-32168-0.

Noise Behavior of MOSFETs Fabricated in 0.5μm Fully-Depleted (FD) Silicon-on-Sapphire (SOS) CMOS In Weak, Moderate, and Strong Inversion

M. N. Ericson[1], C. L. Britton, Jr.[1], A. L. Wintenberg[1], J. M. Rochelle[2], B. M. Blalock[3], and D. M. Binkley[4]

[1]*Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006*
[2]*Concorde Microsystems, Inc., Knoxville, TN 37932*
[3]*The University of Tennessee, Knoxville, TN 37996*
[4]*The University of North Carolina, Charlotte, NC 28223-0001*

ABSTRACT

This paper presents a summary of the measured noise behavior of CMOS MOSFETs fabricated in a fully depleted (FD) silicon-on-sapphire (SOS) 0.5μm process. SOS CMOS technology provides an alternative to standard bulk CMOS processes for high-density detector front-end electronics due to its inherent radiation tolerance. In this paper, the noise behavior of SOS devices will be presented and discussed with reference to device inversion coefficient. The concept of inversion coefficient will be introduced and the results of SOS device noise measurements in weak, moderate, and strong inversion will be presented and compared for devices with gate lengths of 0.5μm to 16μm. Details of the noise measurement system will be provided including specifics of the measurement approach and custom circuits used for device biasing. This work will provide a thorough presentation of measured SOS device noise as a function of inversion coefficient. In addition, strategies for device biasing and sizing to obtain optimum noise performance will be presented encouraging more widespread use of SOS integrated circuits in high-density detector applications.

Abstract Submission for IEEE 2002 Nuclear Science Symposium

Corresponding author: M. Nance Ericson
Oak Ridge National Laboratory
P.O. Box 2008, MS 6006
Oak Ridge, TN 37831-6006
Phone: (615)574-5637
FAX: (615)576-2813
E-mail address: ericsonmn@ornl.gov

Suggested Topic Area: Analog and Digital Circuits

Authors would prefer an oral presentation if possible.

SUMMARY

Bulk CMOS has remained the dominant technology for implementing high-density detector front-end electronics due to the widespread availability of fabrication processes. The continual migration of fabrication technologies to deeper submicron structures is driven primarily by the demand for high-speed, low-power, and low-cost digital integrated circuits. This trend has allowed designers to meet the demanding front-end requirements of many physics applications where high channel count and small size and mass are essential [1-3]. However, as device feature sizes decrease, short channel effects particularly bothersome in low-noise analog design become more prominent, reducing the utility of smaller feature sizes for improved radiation resistance.

Historically, devices fabricated in SOS have demonstrated improved radiation tolerance over circuits fabricated in bulk CMOS [4,5]. The primary mechanisms responsible for bulk CMOS radiation susceptibility are gate oxide and field oxide charge trapping resulting in threshold voltage shifts and increased leakage currents. Recent literature reports improved radiation resistance of bulk CMOS by the use of submicron process having thinner oxides and reduced area, and by the incorporation of layout techniques that reduce the radiation-induced leakage currents [1,6]. However, SOS fabrication technology is becoming more generally available for both high volume production and prototyping and continues to follow trends in feature size reduction, making it a suitable candidate for many detector front-end applications.

Presentation of MOSFET device parameters in terms of the inversion coefficient (IC) was introduced by Vittoz and provides a measure of the inversion level of a MOSFET [7]. From this foundation a design methodology emphasizing this parameter was recently developed by Binkley [8] that allows the designer to simplify the design process by exploiting the known advantages offered by operating a device at a specific inversion coefficient. Using this methodology, the designer specifies only the device inversion coefficient and gate length – all other design parameters are then calculated directly. The advantages offered by this new approach include device biasing to minimize the noise contribution.

In this paper MOSFET noise in general will be discussed and related expressions given with an emphasis on $1/f$ and white noise and associated dependencies on inversion level, i.e. weak or strong inversion. An overview of inversion coefficient analysis will be given and the associated utility for these strategies in low-noise analog design will be discussed. The results of an extensive noise study of devices fabricated in 0.5µm SOS CMOS will be presented in which both NMOS and PMOS devices were fabricated with a fixed drawn W/L ratio of 50 for gate lengths of 0.5µm, 1µm, 2µm, 4µm, 8µm, and 16µm. These devices were biased in weak inversion, moderate inversion, and strong inversion and noise data was acquired using a custom device biasing electronics module and data acquisition system (see Figure 1). Details of the noise measurement system will be provided. Noise data as a function of gate length and inversion coefficient will be presented and compared for all device types biased at the three inversion levels (see Figure 2 for a sample of measured noise data). The experimentally determined effect of the inversion coefficient and gate L on MOSFET noise will be summarized and compared to expected theoretical performance. The results of this work will aid the proliferation of SOS integrated circuits for application to low-noise detector front-end electronics where radiation resistance is an essential design requirement.

REFERENCES

[1] D.C. Christian, J.A. Appel, G. Cancelo, J. Hoff, S. Kwan, A, Mekkaoui, R. Yarema, W. Wester, and S. Zimmerman, "FPIX2: a radiation-hard pixel readout chip for BteV," *Nuclear Instruments and Methods in Physics Research A*, 473, 2001, pp. 152-1656.

[2] C. L. Britton, Jr., M. N. Ericson, S. S. Frank, J. A. Moore, M. L. Simpson, G. R. Young, R. S. Smith, L. G. Clonts, J. Boissevain, S. Hahn, J. S. Kapustinsky, J. Simon-Gillo, J. P. Sullivan, H. van Hecke "A 32-Channel Preamplifier Chip for the Multiplicity Vertex Detector at PHENIX *", Review of Scientific Instruments*, vol. 70, no. 3, March 1999, pp. 1684-1687.

[3] A. Kandasamy, E. O'Brien, P. O'Connor, and W. Von Achen, "A monolithic preamplifier-shaper for measurement of energy loss and transition radiation," *IEEE Trans Nucl Sci*, vol. 46, no. 3, part 1, June 1999, pp. 150-155.

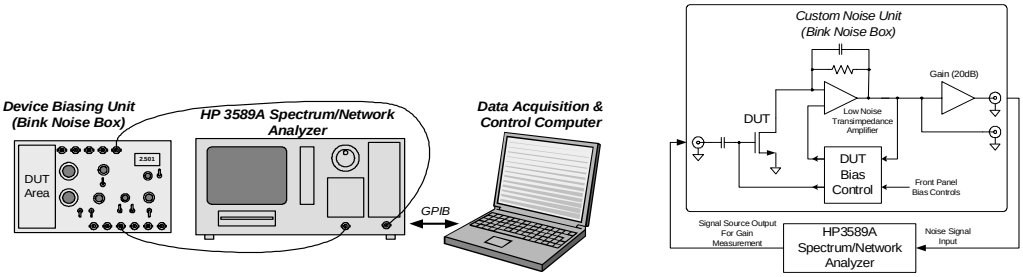
[4] R.A. Kjar and G. Kinoshita, "Transient Photocurrent in SOS Structures," *IEEE Trans Nucl Sci*, vol. 20, 1973, pp. 315-318.

[5] D.H. Phillips, "Silicon-on-Sapphire Device Photoconduction Predictions," *IEEE Trans Nucl Sci*, vol. 21, 1974, pp. 217-220.

[6] A. Vandooren, J.P. Colinge, and D. Flandre, "Gate-All-Around OTA's for Rad-Hard and High-Temperature Analog Applications," *IEEE Trans Nucl Sci*, Vol. 46, No. 4, August 1999, pp. 1242-1249.

[7] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications," Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, 1995, pp. 83-114.

[8] D. M. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS of the Continuum of Inversion Level and Channel Length," Proc. 7th IEEE Int. Conf. On Electronics, Circuits & Systems ICECS'2k, Kaslik, Lebanon, Dec. 17-20, 2000, pp. 161-164.



(a) **(b)**

Figure 1: a) Noise measurement system, and b) custom noise unit used to bias MOSFET devices.

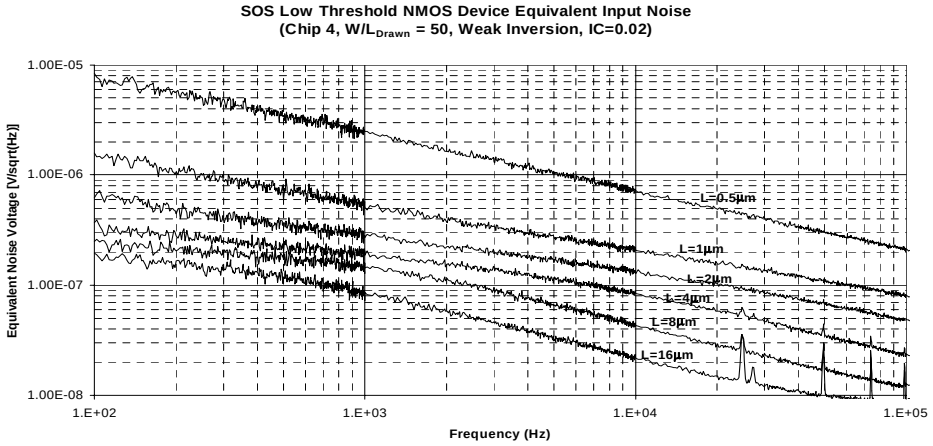


Figure 2. Measured NMOS SOS Device Input-Referred Noise In Weak Inversion.

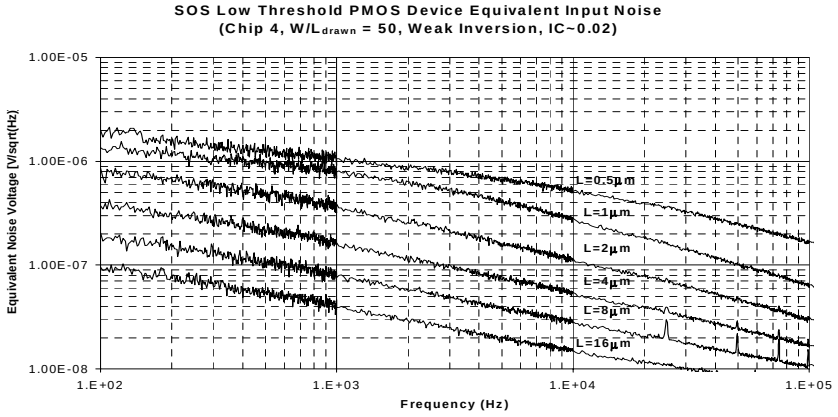


Figure 3. Measured PMOS SOS Device Input-Referred Noise In Weak Inversion.

VITA

M. Nance Ericson born in Memphis, TN in 1965. He received the B.Sc. degree in electrical engineering from Christian Brothers University, Memphis, TN in 1987, and the M.S. degree from the University of Tennessee, Knoxville, in 1993.

In 1987, he joined Oak Ridge National Laboratory, Oak Ridge, TN as a Research and Development Engineer in the Monolithic Systems Development Group. In this capacity, he has been involved in a variety of development projects with focus on the design of mixed-signal CMOS integrated circuits and integrated sensors. His research interests include physiological/biological sensing, wireless, silicon-based optical detectors, high-resolution data converters, and high-temperature CMOS. He has authored or coauthored over 35 technical publications. He holds four patents in the area of high-temperature measurement and integrated photo-spectrometers.

Mr. Ericson is a member of IEEE and Tau Beta Pi. He was the recipient of the IEEE Nuclear and Plasma Sciences Society Early Achievement Award in 1997.