# GAN-BASED POINT-OF-LOAD CONVERTERS FOR DATA CENTER APPLICATIONS

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*"In normal life we hardly realize how much more we receive than we give, and life cannot be rich without such gratitude. It is so easy to overestimate the importance of our own achievements compared with what we owe to the help of others." – Dietrich Bonhoeffer*

# Abstract

The growth of the information technology sector has increased demand for high-density, high-efficiency point-of-load (POL) converters. As industry continues to demand an increase in server processing power, high-current operation presents challenges to designing high-efficiency POL converters. Increased conduction and overlap losses induce significant power losses in high-power modes. The introduction of Gallium-Nitride (GaN) switching devices and the implementation of zero-current-switching (ZCS) topologies for POL applications have the potential to improve converter efficiency while maintaining or surpassing the industrial power density standard. This thesis addresses the challenges presented by high-current operation by demonstrating an accurate power loss model of the quasi-resonant zero-current-switching (QR-ZCS) buck converter and presents a comparison between the synchronous buck and QR-ZCS buck in a 5-1.8 V POL application.

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# Chapter 1 Introduction

Data centers are an integral part of the global energy economy. In 2014, 1.8% of all energy generated by the United States was consumed by data centers [1]. Social media, streaming services, and online retail services continue to increase demand for processing, storing, and sharing user data, further contributing to the growth of the data center industry. The adoption of the internet in the early 2000's produced a rapid growth of data centers, increasing data center energy usage by 90% from 2000-2005 [1]. From 2005-2010, this trend continued, and data center energy consumption rose by another 24% [1]. Predictions made in 2010 suggested a further increase in data center energy usage, prompting the Department of Energy (DOE) to demand improvements in data center efficiency [2]. One response to the DOE's request is the hyperscale data center. The rise of hyperscale data centers and improvements in server utilization have reduced the predicted energy usage trend to a growth of only 4% as opposed to the projected 200% increase as shown in Figure 1.1 [1]. Recent innovations in Wide Bandgap (WBG) materials, especially Gallium-Nitride (GaN), have presented an opportunity for high-efficiency and high-power density servers by reducing switching losses and allowing for high frequency operation.

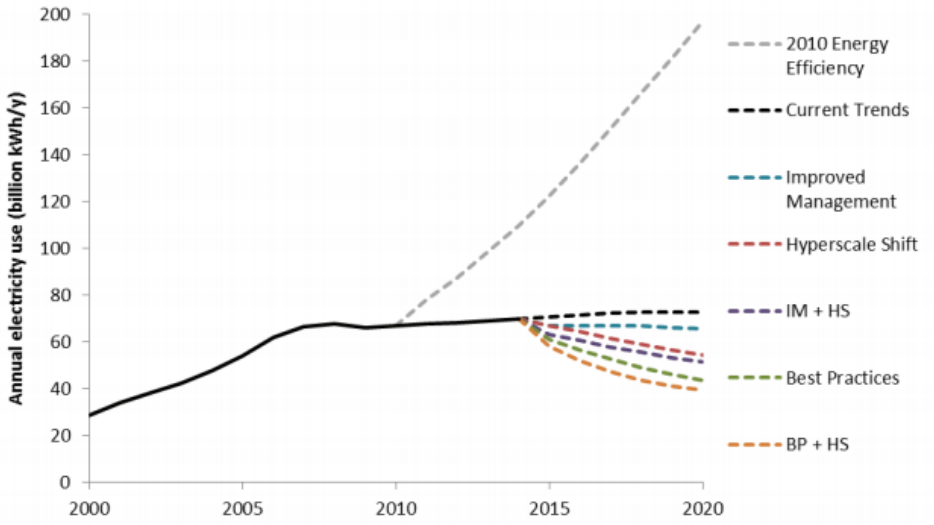


Figure 1.1 Predicted data center total energy use [1]

## 1.1 Data Center Power Consumption

Definitions surrounding the power efficiency of data centers vary, but are typically measured as a ratio between the input power to the data center and the power used by the Information Technology (IT) equipment. One of the more common standards of measurement is known as a data center's Power Usage Effectiveness (PUE) [3]. In 2014, the average data center PUE was estimated as 2.0. Ideally, PUE is 1, and all the input power goes directly to the IT processors. PUE includes all the inefficiencies within a data center including the power loss in the power converters, auxiliary equipment, and cooling systems. Small-scale data centers are measured to be less efficient than their large-scale counterparts and on average have PUE's around 2.0 [4]. In contrast, hyperscale data centers have PUE as low as 1.02 [5]. A survey of state-of-the-art data centers and the progression of data center PUE is shown in Figure 1.2 [6-11].

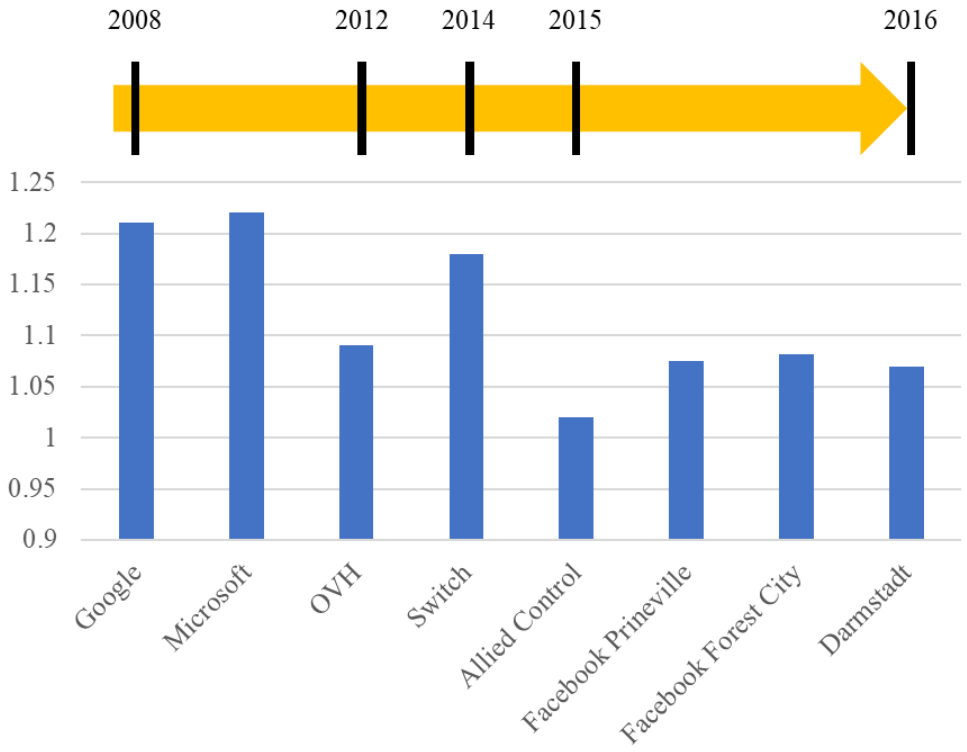


Figure 1.2 Example data center PUEs

Inefficiencies within server power converters not only increase the energy demanded from the grid, but also increase the energy consumed by the data center cooling system. Therefore, efficiency improvements to power converters decrease the need for cooling infrastructure and converter heatsinks while improving the efficiency of the previously cascaded converters. Because higher efficiency facilitates a reduction in cooling infrastructure, system power density is increased, further enabling the escalation of processing power demanded by an information-driven economy.

Research conducted on legacy data centers shows that approximately one-third of the energy consumed by these data centers was used by the cooling infrastructure to cool the power

electronics and servers [12]. Furthermore, a survey of current data center technologies showed that between 30% and 55% of all data center input power is consumed by the cooling system [13]. Figure 1.3 shows a breakdown of legacy data center power usage.

Improvements and innovations in server efficiency and power handling, as well as the deployment of new cooling technologies has drastically improved the average PUE of U.S. data centers. In 2008, Google achieved a PUE of 1.21 across all six of its data centers, and at the time it was considered to be as close as possible to a perfect PUE. In 2017, Supermicro announced that an unnamed company had utilized its disaggregated MicroBlade system in a new data center and achieved a PUE of 1.06. In October of 2015, Allied Controls boasted a PUE of 1.02 using a special 3M cooling fluid [5].

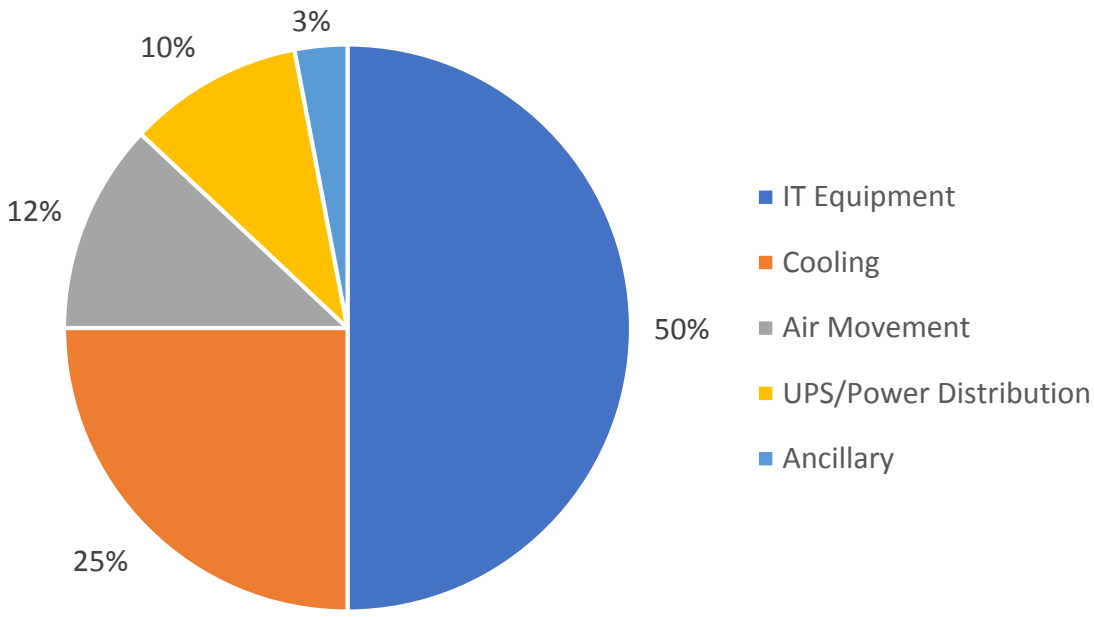


Figure 1.3 Legacy data center power usage distribution

Research has shown that initial investment in efficiency measures can yield large operational savings and result in a higher data center PUE over time [14, 15]. However, these investments require significant financial expenditure, and can only be made my large technology companies planning to create large scale data centers known as hyperscale data centers. These data centers contain a minimum of five thousand servers and are over 10,000 $ft^2$. The growth of virtual computing has increased the number of hyperscale data centers from 259 at the end of 2015 to 390 by the end of 2017 and one hundred more are expected to be built by the end of 2019 [16]. The expansion of hyperscale data centers has vastly increased the demand for high power density IT equipment as floor space for IT equipment is extremely valuable and much effort is given to optimizing server rack placement and cooling infrastructure.

## 1.2 Data Center Architecture Considerations

Many data center power distribution architectures have been implemented and analyzed. In some cases, AC power is distributed to a server rack or tower, the voltage is reduced through one or a series of power conversion stages, and power is then distributed at the blade and board level. A survey of common power distribution architectures is shown in Figure 1.4. Depending on the data center power distribution system, up to four conversion stages may occur before power reaches the Point-of-Load (POL) converter. A POL converter is used to step down a voltage to below 5 Volts. These converters are used to supply power to many auxiliary server components and processors. Voltage-Regulation-Modules (VRMs) are synonymous with POL converters. The simplification of these stages, especially the Intermediate Bus Converter (IBC) and POL converter, has become a substantial research focus.

Recent studies have shown that an increase in the motherboard distribution voltage from 12 V to 48 V has benefits to increasing efficiency due to the reduction of conduction losses inherited from bus wiring [14, 17, 18]. Figure 1.5 shows a comparison between different power distribution implementations and the financial impact of each architecture's energy savings. Figure 1.4(a) shows a common power distribution architecture which allows for AC-12V conversion at the rack level and 12-1V conversion on the blade. According to [18], the most efficient architectures have either AC-48V or AC-384V conversion at the rack level, and all other conversion stages at the blade level. According to this survey, there are significant annual savings by using a 48-1V conversion at the POL rather than the common 12-1V. By reducing the number of cascaded converter stages, the system efficiency is slightly increased.

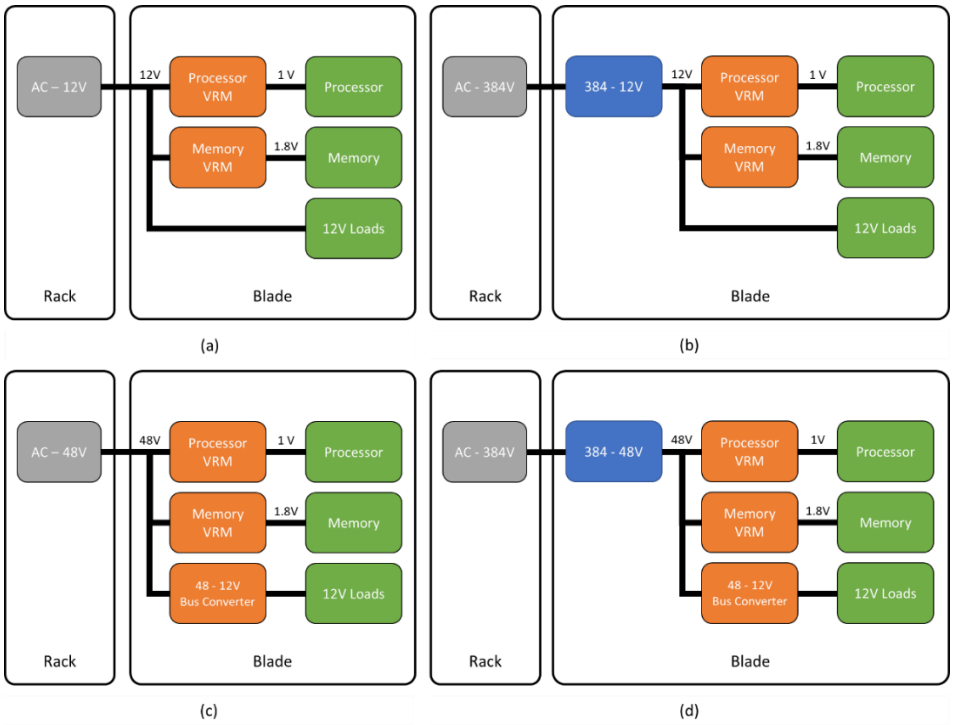


Figure 1.4 Comparison of data center architectures: (a) AC-12-1V, (b) AC-384-12-1V, (c) AC-48-1V, and (d) AC-384-48-1V

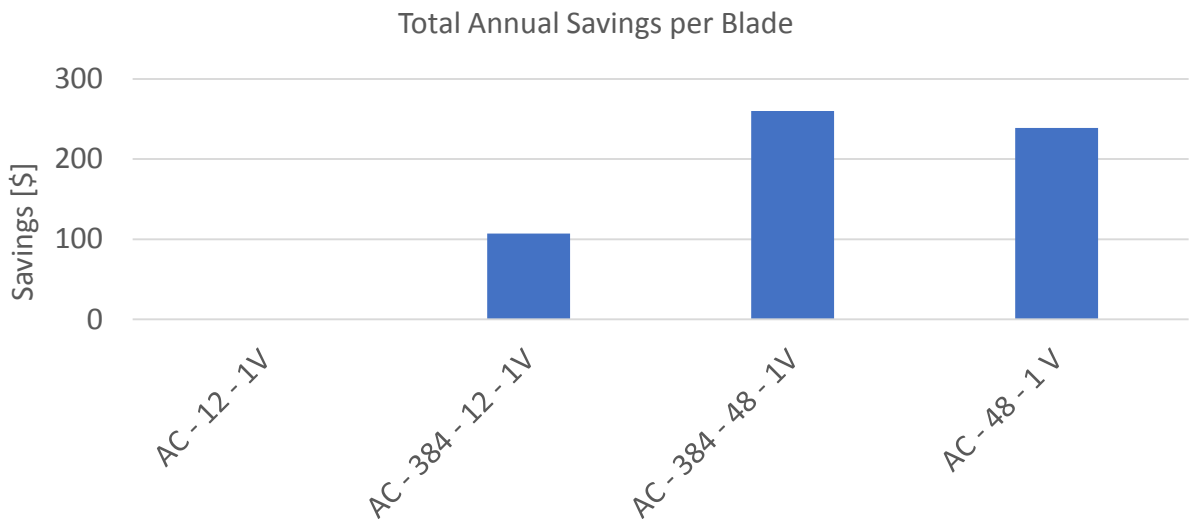


Figure 1.5 Annual Blade Savings Summary

However, a major disadvantage of 48-1V converters is the use of large magnetics in high step-down converters [19-21]. When adding a 48-1V POL converter to a blade, the volume of the blade will increase significantly when compared to a 12-1V POL converter. Although Figure 1.5 shows that the AC-12-1V architecture is the least efficient, it likely has the highest blade power density.

## 1.3 Point-of-Load Conversion

The term Point-of-Load converter is used to refer to a power converter used in low-voltage applications, often supplying power to computer processors. POL converters, also known as Voltage Regulation Modules (VRMs) are most often used in 12-to-1 V conversion to supply power to a CPU on a motherboard. A bus voltage of 12 V is convenient for transitioning to 5 V and 3.3 V auxiliary circuitry while maintaining relatively low current across the motherboard.

Figure 1.6 shows a desktop computer motherboard with VRMs highlighted. A 12 V connection from the Power Supply Unit (PSU) supplies power to several components across the motherboard including the Central Processing Unit (CPU), Random Access Memory (RAM), and auxiliary components. Voltage is regulated from the 12 V input to 5 V, 3.3 V, and 1 V through various VRM stages. As is shown, VRMs occupy a significant portion of the available motherboard real-estate, with power devices and passive components dominating the VRM footprint. As VRM efficiency improves, the size of on-board heatsinks used to extract heat from the VRM converters can likely be reduced, improving system power density.

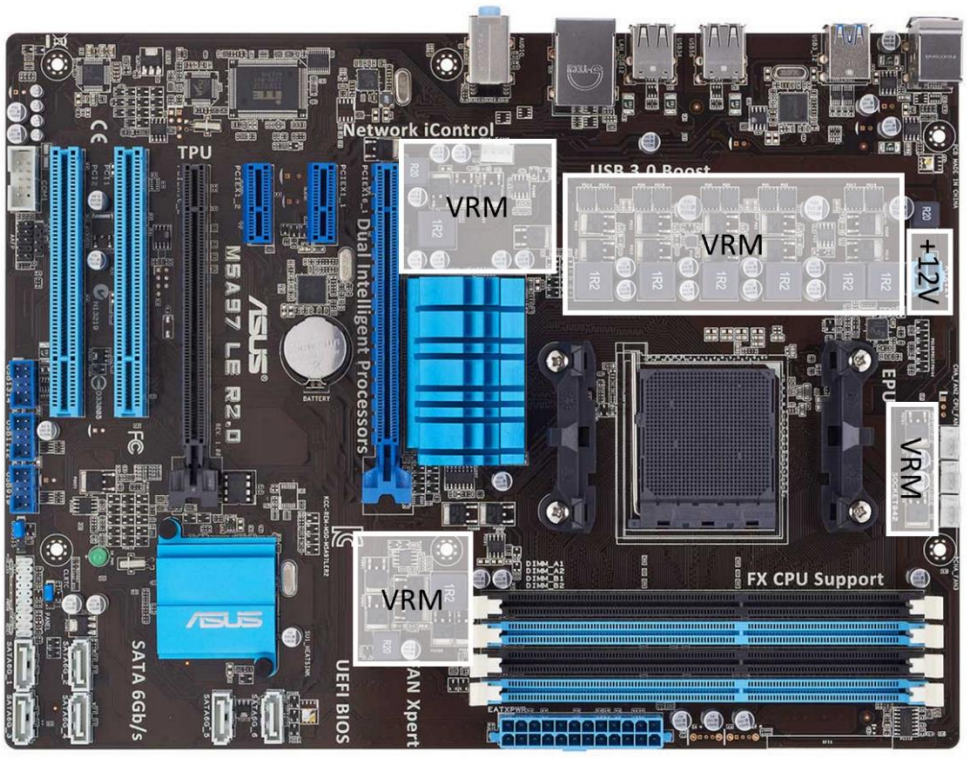


Figure 1.6 Motherboard with highlighted components [22]

The efficiency of the POL conversion stage influences overall system efficiency because of the cascading effect of power loss. A reduction in power loss consequently produces a reduction in cooling infrastructure, yielding higher power density converters and enabling more compact data center layout. Research shows that a savings of 1 W at the POL will save a total of 2.84 W at the facility scale [23]. With tens of thousands of POL converters throughout a single hyperscale data center, a sub-Watt power loss savings could equate to thousands of dollars saved annually.

A challenge to increasing server power density is the volume reduction of magnetic components used by power converters at the POL. One approach to decreasing the footprint of magnetic components is to increase converter switching frequency. For a buck converter with a fixed output inductor, increasing the switching frequency yields a lower current ripple, reducing conduction losses. By proportionally decreasing the output inductance, the current ripple can be maintained while the volume of the inductor decreases.

The benefits gained by increased switching frequency are joined with the challenge of increased power loss from frequency-dependent switching losses. In the synchronous buck, a topology commonly used in POL applications, parasitic capacitances and inductances in the power loop cause ringing and an extended overlap time during the switching transitions. As the device transitions from an on-state to an off-state, the voltage across the device decreases while current through the device decreases, this overlap of current and voltage results in power loss. As frequency increases, these “overlap” losses become more significant and eventually become the dominant form of power loss.

To mitigate these switching losses in POL converters, several methods are considered. Minimization of the power loop and gate loop inductances has shown to reduce switching losses

marginally [24]. Low-voltage Gallium-Nitride (GaN) FETs have reduced parasitic capacitance and gate charge when compared to similarly sized Silicon FETs. The lateral geometry of EPC eGaN FETs has low inductance Ball Grid Array (BGA) and Land Grid Array (LGA) packages, further decreasing overlap losses [25]. To illustrate the importance of low-inductance packaging and layout, Figure 1.7 shows a comparison between different packaging schemes and their impact on power losses [26]. Additionally, Figure 1.8 and Figure 1.9 show that minimizing common source inductance and loop inductance greatly benefit converter efficiency [27]. While the FET packaging impacts the common source inductance, the power loop inductance is reduced by circuit board layout.

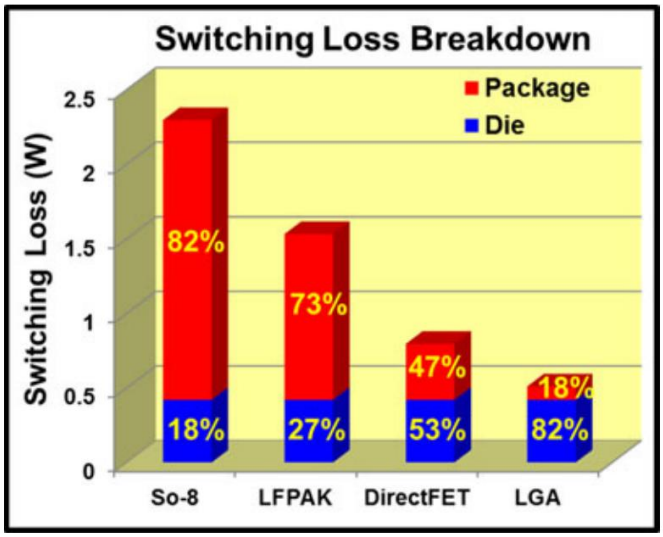


Figure 1.7 Power loss breakdown of various packaging methods [25]

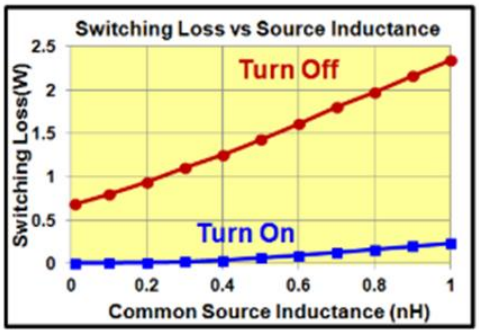


Figure 1.8 Switching loss as a function of common source inductance [26]

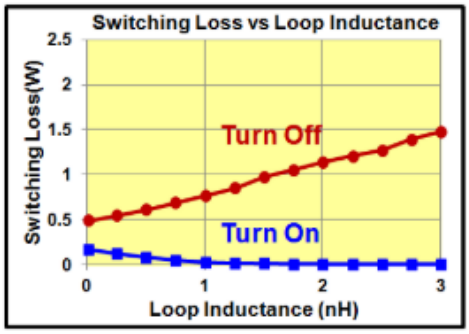


Figure 1.9 Switching loss as a function of loop inductance [26]

## 1.4 Summary

Growth of the information industry is spurring the creation of data centers around the world, and especially in the United States. U.S.-based companies such as Facebook, Amazon, Apple, and Google continue to expand their virtual and physical domain, requiring an increase in data centers. Current trends suggest that data center PUE is improving, but further improvement to POL converters is necessary to maintain power architecture efficiency while increasing output power capabilities. Research shows that slight efficiency improvements at the POL stage can

generate noteworthy power savings at the facility level by reducing the cascading effect of power loss while decreasing the demand on cooling infrastructure.

Data center power distribution architectures and cooling systems vary widely, but recent research has shown that increasing the motherboard distribution voltage has the potential to increase facility efficiency and significantly reduce cost. Current 48-1 V converter topologies by themselves have not demonstrated high efficiency but have the potential to increase the cascaded system efficiency between the IBC and POL converters.

As output power from data centers continues to increase, there is a need for high power density POL converters. Increasing the switching frequency of power converters produces an opportunity for decreased output inductance and reduces the magnetics footprint. Implementing high switching frequency generates power losses and must be mitigated if high efficiency is to be maintained. In the case of POL applications, ZCS has the potential to reduce significant overlap losses. Parasitic capacitances and inductances from PCB layout and device packaging also greatly impact POL efficiency. EPC eGaN FETs with LGA and BGA packaging are useful for diminishing switching losses, further facilitating increased switching frequency. The material benefits of GaN will be further explored in the literature review. Chapter 2 is the literature review, Chapter 3 discusses the modeling two topologies considered for the POL converter, Chapter 4 describes the implementation and testing of the two POL converter topologies, and Chapter 5 discusses conclusions and future work.

# Chapter 2 Literature Review

## 2.1 Point-of-Load Implementation

Figure 2.1 shows a survey of power density and efficiency of POL converters used in commercial applications compared to academic research. A comparison of 5-1 V, 12-1 V, and 48-1 V POL converters is shown. At the POL level, 48-1 V power conversion presents a difficult challenge. The high step-down ratio prohibits simplistic, conventional topologies, such as the synchronous buck, due to the extreme duty cycle. In a synchronous buck with a 48 – 1 V conversion ratio, nearly all current stress exists on the low-side device. For a 48-1 V synchronous buck converter, the low-side device is on for $(1 - D) \cdot T_s$ of the period, where $D = \frac{1}{48}$. This creates a condition in which the low-side device is conducting for the majority of the period and must be designed with a lower $R_{on}$. Unique solutions such as the coupled-inductor buck or tapped-inductor buck have been demonstrated with efficiencies nearing 90% [21, 28]. A new converter architecture based on the switched-capacitor topology with a 48 V input was shown to achieve high efficiency with a relatively high power density and a 6:1 voltage ratio [29]. The advantage of this topology is the distributed stress across the devices and capacitors. In a synchronous buck converter with a similar duty cycle, the current stress is mostly though the low-side device and the high-side device must block 48 V. In the switched-capacitor topology, the voltage and current stress is distributed equally across each device in the circuit. Even more extreme voltage ratios have been considered, such as a 400-1 V power converter [30, 31]. By using an input-series-output-parallel topology, an efficiency of 90% was achieved at an output power of 30 W.

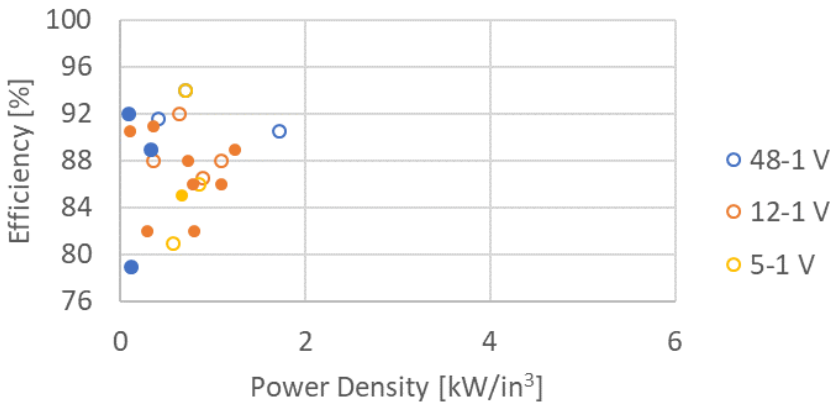


Figure 2.1 Survey of commercial and academic research POL converters

To increase power density and decrease current ripple, the switching frequency of a converter can be increased. However, the switching losses associated with device turn-on and turn-off increase proportionally to switching frequency. One significant switching power loss mechanism is overlap loss. Overlap losses occur when a device is either conducting while a voltage is applied across the drain and source terminals or a device has a voltage applied across the drain and source when it begins conducting. To reduce or prohibit this "overlap loss", resonant components are used to create Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) transitions. Resonance is generated from a combination of inductors and capacitors, either from a discrete circuit element or an existing parasitic inductance or capacitance. This resonance occurs between the turn-on and turn-off transitions to reduce the current through or voltage across a device to zero before the switching action occurs.

ZVS converters are commonly used in IBC converters due to the benefit of eliminating power losses caused by high-voltage turn-on and turn-off transitions [21, 31-33]. In the case of low-voltage, high current applications such as in POL converters, the benefit of ZVS transitions

is negligible. ZVS benefits high-voltage converters because the energy lost in the device output capacitance during the turn-on transition is proportional to $V^2$. For the interleaved buck converter, research reveals that the high-side turn-off transition is the primary source of switching loss [27]. Therefore, a ZCS topology may benefit POL applications by reducing the overlap losses at the high-side turn-off transition.

As mentioned previously, a primary difficulty to improving the power density of POL converters is the reduction of inductor volume.

Figure 2.2 shows a survey of commercial inductors fitting for POL applications. The two most significant metrics used in evaluating the relative merit of the inductors are its volume and DCR. Assuming the designed converter efficiency is 97% and the peak current is 500 A, the minimum number of inductors, $n_{min}$, is derived by calculating the number of parallel inductors,

$$n_1 = \frac{500\ A}{I_{sat}} \tag{1}$$

necessary to prevent saturation. The minimum DCR,

$$DCR_{min} = \frac{(500\ A \cdot 1.8\ V) \cdot (1 - 0.97)}{500\ A^2}, \tag{2}$$

is used to calculate the minimum number of parallel inductors,

$$n_2 = \frac{DCR}{DCR_{min}}, \tag{3}$$

to achieve an efficiency of 97%. The minimum number of inductors that will satisfy both the saturation and efficiency requirement is

$$n_{min} = \max(n_1, n_2)\,. \tag{4}$$

The total inductor power density,

$$\alpha_L = n_{min} \cdot \frac{P_{out}}{V_L}\ , \tag{5}$$

is used to compare between discrete inductor current capacity and power density.

The commercial inductor survey reveals that an inductor power density above 30 kW/in$^3$ is achievable at an output current below 20 A. Often, low-current POL modules are paralleled to achieve higher output current capabilities. It is important to note that this survey assumes a DC current and neglects inductor current ripple and the associated conduction losses. At low current, this assumption may create a significant discrepancy between the survey results and predicted power losses. At high current, a comparable current ripple has a reduced impact on RMS currents. At an output current of 1 A, 500 inductors must be paralleled to achieve the output power specification. With an inductance of 60 nH, the effective inductance is 0.12 nH. At a switching frequency of 2 MHz, the current ripple is 480% of the DC-current, resulting in large RMS currents, dropping the efficiency of the inductor from 97% to 60%. At an inductor power density of 30 kW/in$^3$ and a current of 60 A per inductor, low inductor ripple is achieved, but inductor has a height of 3 mm. After including device area, power density greatly decreases and is below the 6 kW/in$^3$ design target.

Furthermore, this survey does not include conduction losses due to the switching devices, other passive components, inductor core losses, or gate drive losses. An power loss model including these loss components is necessary to for an accurate converter design and optimization.

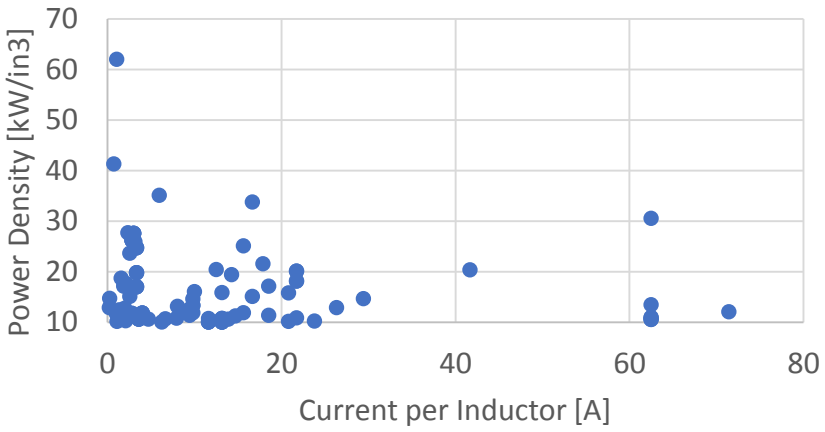


Figure 2.2 Commercial inductor survey

## 2.2 Gallium-Nitride (GaN)

As data center efficiency improvement has been a necessary focus in the industry over the past decade, new technologies and materials are enabling the further improvement of converter efficiency and power density. Gallium-Nitride (GaN) is a Wide-Bandgap (WBG) semiconductor material with properties that enable higher blocking voltages than that of Silicon. A bandgap is a material property corresponding to the amount of energy necessary for an electron to move from the conduction band to the valence band. The larger the bandgap, the more energy required for a device to experience voltage breakdown. For the same device structure and geometry, GaN devices are theoretically able to block the same drain-source voltage at a fraction of the device channel length. This material attribute, along with a much higher carrier velocity, means that the proportional device resistance of equal voltage-rated GaN is much lower than a Silicon device of the same geometry and area. Figure 2.3 shows a comparison between low voltage Silicon and EPC GaN devices. The lateral device structure of

low-voltage GaN devices facilitates a much lower gate charge ($Q_g$) and therefore has a reduced gate drive loss when compared to similarly sized silicon devices. GaN also has an increased electron mobility when compared to Silicon, reducing the resistance per device area.

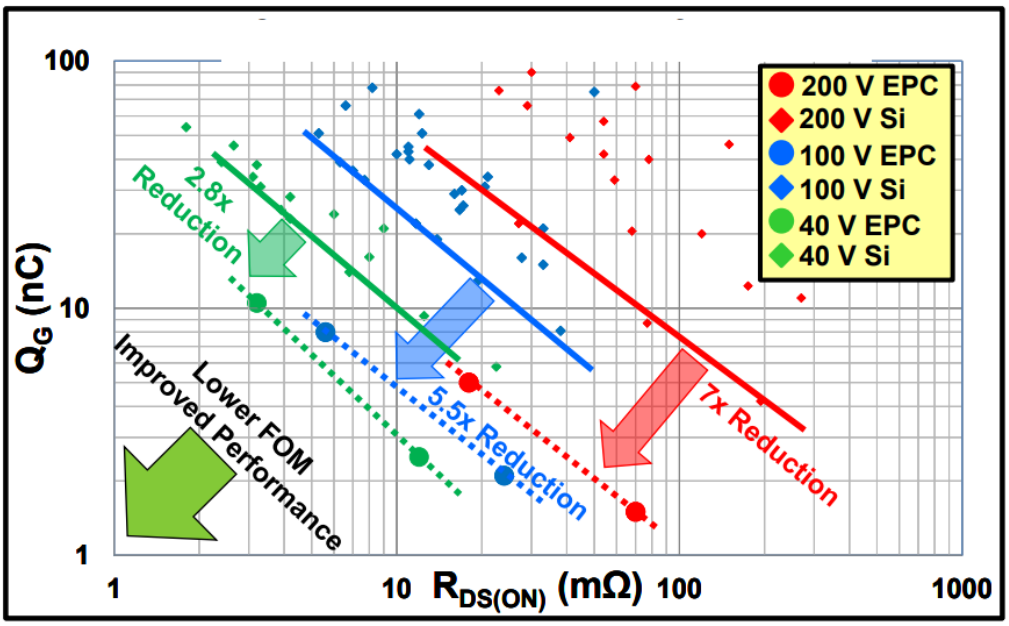


Figure 2.3 Comparison of low-voltage GaN and Silicon devices [34]

A lateral device structure is leveraged for low-voltage GaN to leverage the high mobility associated with a 2-dimensional electron gas (2DEG) conduction channel formed by an AlGaN layer above the channel [35]. The AlGaN layer is also used to deplete the 2DEG channel and create an enhancement-mode device [36]. An example of a lateral GaN device is shown in Figure 2.4. As the device is laterally structured, the conduction path is different than that of a vertical Silicon device. For one, the conduction channel is a high mobility 2DEG channel formed between the AlGaN and GaN layers. Secondly, because of the 2DEG lateral device structure,

there are no p-n junctions, meaning that there is no diode structure as with Silicon devices. However, reverse conduction is present [37]. The lateral structure of GaN devices also allows for lower parasitic output and input capacitances, reducing switching losses and increasing device switching speeds.

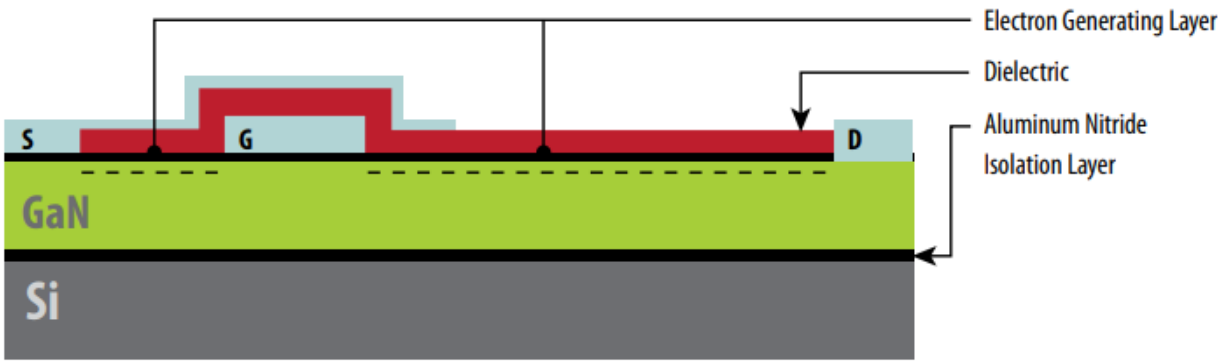


Figure 2.4 EPC GaN power transistor lateral structure [34]

GaN power devices have been applied to a wide variety of applications including low-power wireless power transfer [38] and medium-power electric vehicle inverters [39]. In the realm of data center applications, GaN devices have been utilized in nearly every power conversion stage. In POL converters, low-voltage GaN devices have shown marked improvement over similarly sized Silicon devices [40-42]. The high frequency switching enabled by GaN devices has further improved power density in POL converters while also increasing POL efficiency.

## 2.3 Topology Survey

In low-voltage, high-current applications, conduction losses often dominate the total power loss. In the synchronous buck converter, low on-resistance FETs and low-DCR inductors can be utilized to decrease conduction losses at the expense of power density. To decrease conduction losses, the device channel area is increased, effectively decreasing the FET on-resistance and consequently increasing the parasitic capacitance of the device. This trade-off yields lower conduction losses at the expense of higher overlap losses and larger device area. Rather than selecting larger devices, RMS currents can be reduced by either increasing output inductance or increasing the switching frequency, but these design trade-offs come with negative repercussions: large inductance can be designed at the expense of an increased DCR for the same volume and a higher switching frequency increases device overlap and gate drive loss. Converter topologies such as the coupled-inductor buck aim to reduce conduction losses by inversely coupling the inductors of interleaved synchronous buck phases, reducing RMS currents. The Quasi-Resonant Zero-Current Switching (QR-ZCS) buck uses soft-switching to reduce overlap losses. This topology enables higher switching frequency which yields the benefit of a reduced output inductance and RMS currents without the detriment of increased overlap losses.

### 2.3.1 Synchronous Buck Converter

The most widely used topology for commercial POL converters is the interleaved synchronous buck converter. The buck converter is a relatively simple topology, only requiring a single inductor and two transistors. Figure 2.5 shows a synchronous buck converter schematic and Figure 2.6 shows the corresponding waveforms. Buck converter operation is as follows: for time $DT_s$, $Q_1$ turns on; next, $Q_1$ turns off, $Q_2$ turns on for $(1 - D) \cdot T_s$.

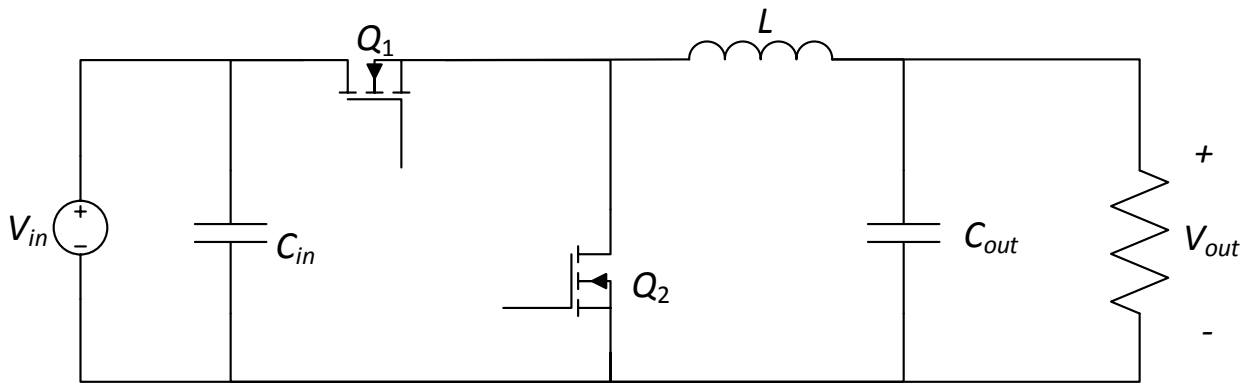


Figure 2.5 Synchronous buck converter schematic

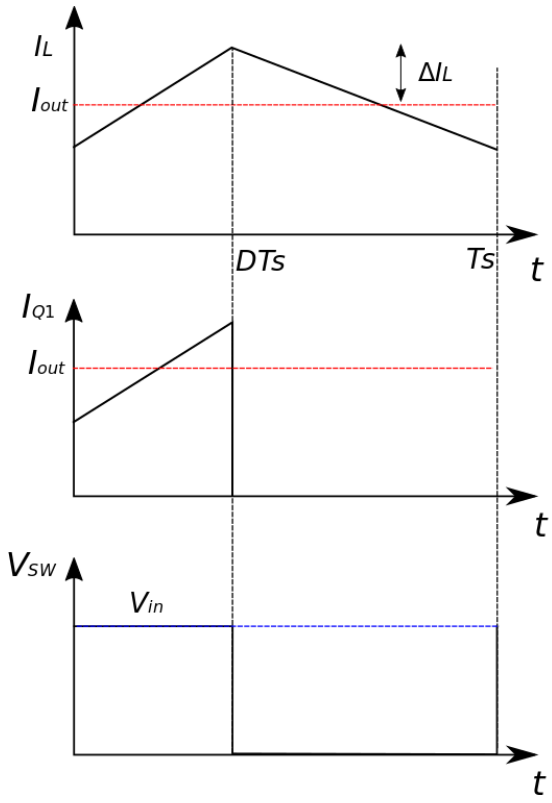


Figure 2.6 Synchronous buck converter waveforms

While the advantage of the buck converter is its simplicity and low-volume, a major disadvantage is the overlap power losses associated with hard-switching due to $Q_1$ turning off at peak current. These power losses are often a significant portion of the overall power loss, preventing high current and high frequency operation [25, 27]. Figure 2.7 shows an example of the $Q_1$ turn-on switching transition. During time $t_1$, the gate voltage of the high-side device, $Q_1$, begins to decrease. At the Miller voltage of the device, the device current, $I_D$, begins to rise. During $t_2$, the voltage across the device rises as $C_{gd}$ is charged by $I_D$. At time $t_3$, the current through the device decreases until the gate-source voltage reaches the threshold voltage and the device is completely off. The power loss is calculated by integrating the product of $I_D$ and $V_{DS}$.

Research exploring these switching transitions is used to estimate the lengths of the timing intervals and the slopes of the current and voltage [43, 44]. Device packaging and PCB layout can heavily influence the severity of these overlap losses by adding parasitic inductance and capacitance to the power loop. Higher parasitic loop inductance increases overlap losses and the mitigation of these overlap losses is a motivating factor in the design of a synchronous buck converter. Various power loop designs have been investigated in an effort to minimize loop inductance [24, 45]. The experimental results of these studies give insight into the layout of synchronous buck converters and help to guide the component selection and physical layout of synchronous buck converters.

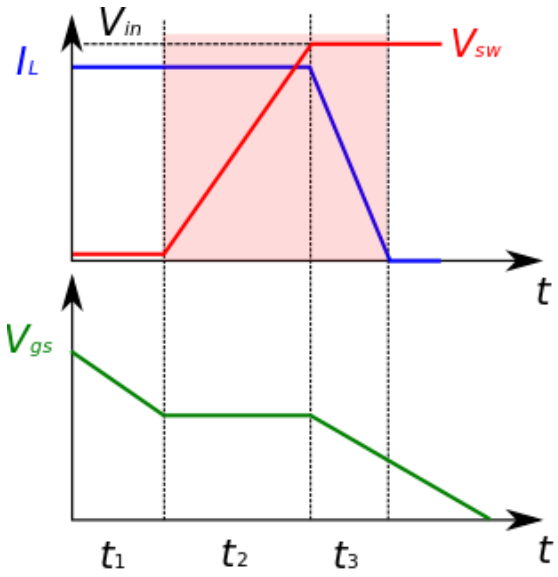


Figure 2.7 Diagram showing turn-off switching transition of $Q_1$

Many examples of the synchronous buck converter being used in POL applications exist. Using an integrated inductor and discrete GaN FETs, a two-phase interleaved synchronous buck converter converting 12-1 V achieves a power density of 790 W/in$^3$ and an efficiency of 86% with a full-load current of 20 A [26]. In another case, a 12-1 V GaN-based POL converter achieves a full-load efficiency of 100 W/in$^3$ and efficiency of 90.5% at an output current of 15 A [46]. A 12-1 V synchronous buck utilizing a planar inductor is constructed and tested up to 20 A of output current [47]. The maximum power density reaches 1.2 kW/in$^3$ and 89% efficiency, suggesting that planar inductors have the potential to enable high power density. A two-stage 48-12-1.8V POL converter demonstrates a full-load efficiency of 89% at 220 W [20]. The 48-12 V conversion stage has a power density of 870 W/in$^3$ and the overall system has an estimated power density of 330 kW/in$^3$.

The synchronous buck converter achieves a power density of 1.2 kW/in$^3$ at a relatively high output current of 20 A. The low component count of the synchronous buck enables high power density, and the utilization of planar magnetics is shown to further decrease converter volume. The minimization of loop and common source inductance are critical to the implementation of the synchronous buck. While the cascaded buck and multi-level buck decrease voltage stress across the devices, the power density of these topologies is much lower than the synchronous buck.

## 2.3.2 Coupled Inductor Buck

Interleaved buck converters are a common topology used in POL applications [48-52]. Using coupled-inductors allows for the reduction of RMS current per phase as well as using multi-phase currents to cancel flux in an inductor core, reducing both conduction and core losses. Figure 2.8 shows a two-phase coupled inductor buck and its corresponding waveforms are shown in Figure 2.9. An interleaved buck topology using coupled inductors was introduced in 2000 and leveraged to increase the self-inductance of the output inductors, effectively decreasing the output ripple [53]. When compared to a similarly designed uncoupled buck converter, the efficiency of the coupled inductor shows marked improvement. As a result, the core temperature rise was reduced. Depending on the duty cycle and coupling coefficient, inductor current ripple is significantly reduced and the transient response of a closed-loop system can be improved [54]. A 4.5 W converter demonstrates an efficiency of 90% using an integrated high coupling coefficient coupled inductor [55]. In this example, the volume of the inductor is only 7.77 mm$^3$.

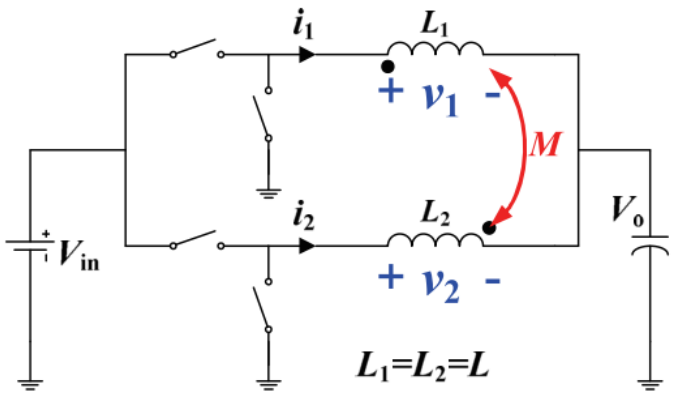


Figure 2.8 Schematic of 2-phase coupled inductor buck [54]

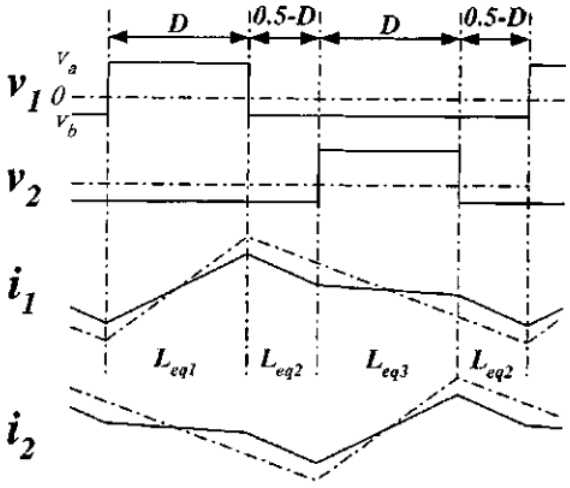


Figure 2.9 2-phase coupled inductor buck waveforms [53]

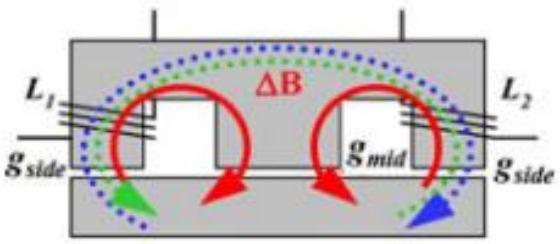


Figure 2.10 E-I coupled inductor implementation [56]

Figure 2.10 shows a common core geometry used in the coupled-inductor buck topology. Two windings, denoted by $L_1$ and $L_2$, are wound in such a way as to generate flux that oppose each other. The AC flux is partially cancelled, and the DC flux generated by the two windings is summed. For high current ripple designs, this AC flux cancellation has the potential to greatly reduce core losses.

Low-profile coupled inductors require precise fabrication, and therefore the manufacturing process is more complicated than that of a standard planar inductor. In some examples, commercially available E-I ferrite core shapes, such as the geometry shown in Figure 2.10, are utilized in coupled inductor POL converters [56]. More complex structures using low-temperature co-fired ceramics (LTCC) technology can be used to integrate these inductors into a PCB [54, 57].

Many implementations of the coupled inductor buck have been explored and their advantages and disadvantages discussed in detail. A custom, integrated LTCC coupled-inductor is designed, fabricated, and compared to a discrete inductor in [58]. The 12-1.2 V converter achieves a power density of 800 W/in$^3$ and efficiency of 82% at a full-load current of 15 A. Another example of an LTCC integrated inductor is a 5-1.2 V POL converter tested at 40 A

output current [56]. This coupled-inductor buck achieves a full-load efficiency of 85% and a maximum power density of 680 W/in$^3$. A 12-1 V discrete component prototype is implemented with a footprint area of 3355 mm$^2$ and an output current of 60 A [50]. The efficiency at maximum power is 82%. When compared to a conventional converter, the efficiency is increased by nearly 5% and only requires the addition of three capacitors. To achieve a single-stage POL converter, a 48-1 V switched-capacitor converter using interleaved coupled-inductors is designed and achieves a maximum efficiency of 79% at 30 W output power [49].

High current and efficiencies approaching 90% are achieved with the coupled-inductor buck. Power densities up to 800 W/in$^3$ are achieved with integrated inductors. Coupled-inductors are used in 48-1 V as well as 5-1.2 V applications. While this topology is versatile and demonstrates high current capabilities, fabrication of a coupled-inductor is expensive and the efficiency target is not met by any previous research.

### 2.3.3 Quasi-Resonant Zero-Current Switching Converter

Research has shown that overlap losses have a significant impact on POL converter performance [27, 40]. In low-voltage, high-current applications, conduction and overlap losses are typically the dominant power loss mechanisms. As frequency increases, the conduction losses decrease due to smaller current ripple and therefore RMS current decreases while the switching losses increase. The benefit of a ZCS converter topology is the reduction of the high-side turn-off overlap loss but is achieved at the expense of increased current ripple. The QR-ZCS buck converter utilizes a resonant capacitor and inductor to resonate the $Q_1$ channel current to zero before turning off the high-side device. Figure 2.11 shows the schematic of the QR-ZCS buck and Figure 2.12 shows the corresponding waveforms.

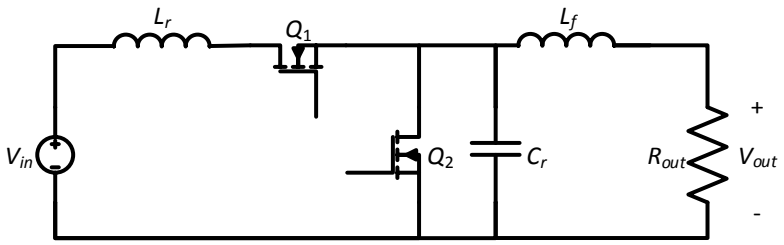


Figure 2.11 QR-ZCS buck converter schematic

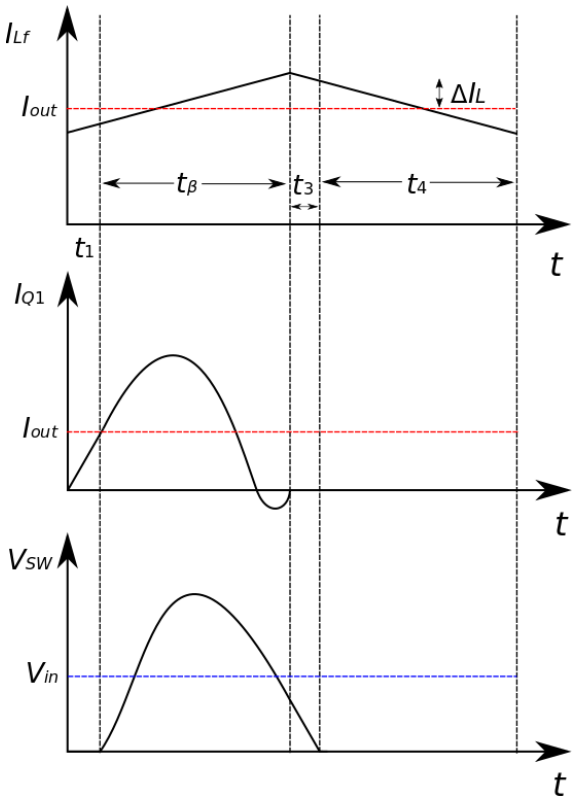


Figure 2.12 QR-ZCS buck converter waveforms

A brief description of the QR-ZCS buck converter operation is as follows: during $t_1$ $Q_1$ and $Q_2$ are on and the resonant inductor current, $I_{Lr,}$ increases until it reaches the average output current, $I_L$; during $t_{2,}$ $Q_2$ turns off and the resonant inductor ($L_r$) and resonant capacitor ($C_r$) resonate around the input voltage and output current until the current reaches zero, allowing Q1 to achieve zero-current switching; during $t_{3,}$ both $Q_1$ and $Q_2$ turn off and the voltage in $C_r$ is discharged by $I_L$ until $V_{cr}$ is zero; during $t_4$, $Q_2$ turns on and $I_L$ freewheels until the output inductor volt-second balance is achieved.

The QR-ZCS buck is often used in the application of bidirectional DC-DC conversion. In some cases, the QR-ZCS buck is coupled with a switched-capacitor circuit. In one such example, an interleaved Zero-Current-Switching Switched-Capacitor Quasi-Resonant converter is designed for use in battery management applications [59]. Using a custom magnetic design, this topology achieves an efficiency of 85% at 580 W output power and 36 A output current. Due to the integration of the switched-capacitor circuit, the voltage ratio is fixed. A low-power example of this circuit is given in [60]. This converter uses discrete components to regulate a nominal 3.7 V output with a 12 V input. A maximum efficiency of 87% is achieved with a power density of 3.7 kW/in$^3$. The maximum output current of this implementation is 1.3 A. The integration of this topology is beneficial to decreasing the converter volume but is only demonstrated with Silicon devices. GaN integrated circuits (ICs) may further increase the efficiency of this topology.

One disadvantage of the QR-ZCS buck is increased device voltage stress. Compared to the synchronous buck, the voltage stress is doubled. An increased voltage stress will influence FET selection and may require the selection of a device with increased on-resistance to prevent voltage breakdown. The current stress through $Q_1$ and $L_r$ is another area of concern and may limit high-current operation. For inductors with a magnetic core, operation is current-limited by

the saturation of the magnetic material. One method of preventing saturation is by using air-core inductors, which also have the added benefit of zero core losses. Depending on the air-core geometry and design, the inductor volume may prohibit high power density.

Another disadvantage of this topology is the increased volume gained by the addition of a resonant inductor and a resonant capacitor. If the same devices are used as with the synchronous buck, the total converter volume of the QR-ZCS buck is much larger. Along with increasing converter volume, conduction loss from AC-resistance (ACR) and equivalent series resistance (ESR) will impact efficiency. Though parallel resonant capacitors will occupy a similar footprint as the decoupling capacitors in a synchronous buck converter, a low-DCR resonant inductor will significantly increase converter volume. To be competitive with the synchronous buck and coupled-inductor buck in terms of power density, a higher output current is required for the same power density. Further analysis regarding the comparison of reduced switching losses and increased component count and volume is not investigated in the literature.

### 2.3.4 Other topologies

In an effort to reduce current ripple, a 12 – 3.3 V multi-level buck is investigated [61]. The schematic of this Asymmetrical Three-Level Buck converter is shown in Figure 2.13. The flying capacitor, $C_f$, is used to reduce the effective voltage across the output inductor, decreasing the current ripple. This capacitor also distributes the voltage stress across the devices, enabling the utilization of low-voltage devices. Assuming the same operating conditions and current ripple, the output inductance is reduced by 23% when compared to the synchronous buck.

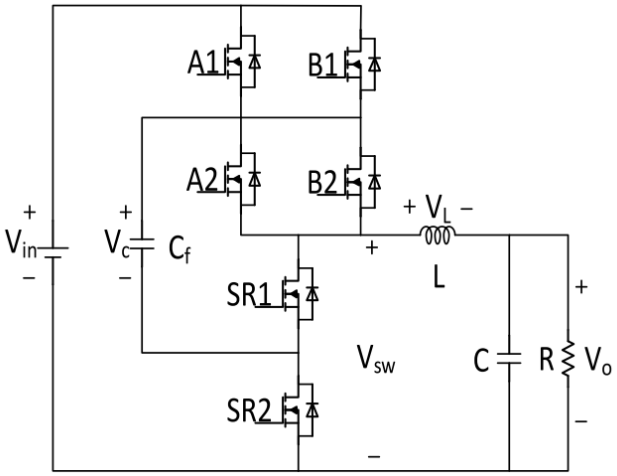


Figure 2.13 Schematic of Asymmetrical Three-Level Buck converter [61]

A cascaded, multi-phase buck POL converter is developed for single-stage 54-1 V conversion. A full-load efficiency of 89% is achieved at 150 W output power [28]. A schematic of the cascaded, multi-phase buck is shown by Figure 2.14. The multi-level topology reduces voltage stress across the individual devices but requires a higher component count than a conventional synchronous buck. This simple input-series, output-parallel design allows for the reduction of voltage and current stress through the devices, but the large transistor count results in a large volume converter. The modularity of this topology allows for a flexible conversion scheme. More parallel legs will increase the output power, while more series connections decrease voltage stress across the devices and facilitates high input voltage operation.

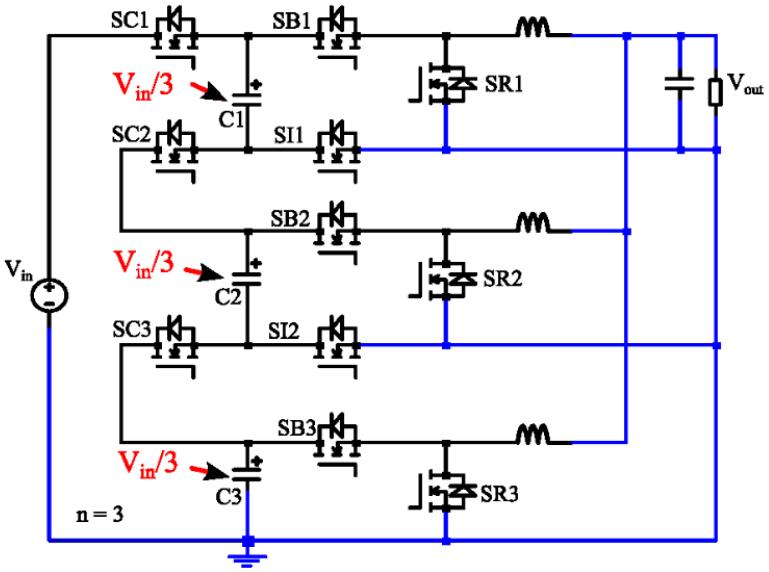


Figure 2.14 Schematic of a multi-phase cascaded buck converter [28]

## 2.4 Summary and Motivation

The physical and virtual expansion of technology companies has increased the demand for high-density, high-efficiency data center components. POL converters occupy a significant portion of the total motherboard footprint. By increasing POL converter power density, data centers can increase computing power and storage capabilities. This improvement in power density often comes at the expense of higher power losses.

As Silicon begins to reach its maximum potential as a semiconductor material, the recent development of wide bandgap materials such as Gallium-Nitride has facilitated both increased converter power density and efficiency due to its beneficial material properties. The characteristics of GaN yield smaller parasitic capacitances, decreasing frequency-dependent overlap losses and allowing for faster switching speeds and enabling increased operating

frequency. The low-inductance packaging of lateral GaN devices also allows for decreased parasitic loop inductance which is known to adversely affect switching transitions and lead to increased overlap losses and switch-node ringing.

Few converter topologies are suitable for low-voltage, high-current, and high-frequency operation. The synchronous buck converter is widely used in commercial applications due to its simplicity of control and its low component count. The efficiency of a hard-switching topology is often limited by overlap losses and prohibits high frequency and high current operation. One variant of the synchronous buck is the coupled-inductor buck converter, which utilizes coupling of parallel VRM inductors to increase the effective output inductance of these parallel VRM phases. The coupled-inductor buck converter allows for decreased current ripple and potentially improved power density over the conventional buck converter, but the complexities associated with designing and fabricating a custom inductor are a substantial impedance to its widespread use and commercialization. Many 48-1 V POL applications have benefited significantly from zero-voltage switching, but lower voltage applications do not receive a substantial improvement from ZVS. Therefore, the use of ZCS topologies may enable higher current or higher frequency operation prohibited by overlap losses in hard switching topologies such as the synchronous buck converter. The use of the zero-current switching has been considered in high-current topologies due to its reduction of overlap losses. However, no research has shown significant analysis regarding the merit of the QR-ZCS buck for POL applications.

# Chapter 3 Converter Power Loss Models and Optimization

The research presented by this thesis focuses on the comparison between the synchronous buck and QR-ZCS buck converters and explores the benefits and detriments of using this ZCS topology in a POL application. This chapter will focus on the design considerations of each converter, taking into account frequency-dependent power losses and presenting implementation challenges that will be further explored in Chapter 4. Along with the power loss model, a model for component volume will be constructed to estimate the relative merit of each grouping of discrete components as well as an estimated power density.

## 3.1 Synchronous Buck Converter Modeling

The synchronous buck converter offers two compelling advantages. First, this topology uses only two switches and a single inductor, allowing for high power density. Secondly, the simplicity of the device control allows for easy integration, further enabling high power density implementation. However, the disadvantage of this topology is limited high current operation due to overlap losses. The construction of a precise power loss model is paramount to the optimization of a high efficiency, high power density POL converter. While some loss mechanisms are more easily modeled, overlap losses are difficult to model because they are highly dependent on parasitic capacitances and inductances which may be difficult to quantify with precision. The synchronous buck converter waveforms and schematic are shown in Figure 3.1 and Figure 3.2. In the first period, $Q_1$ is conducting and the equivalent circuit is shown in Figure 3.3.

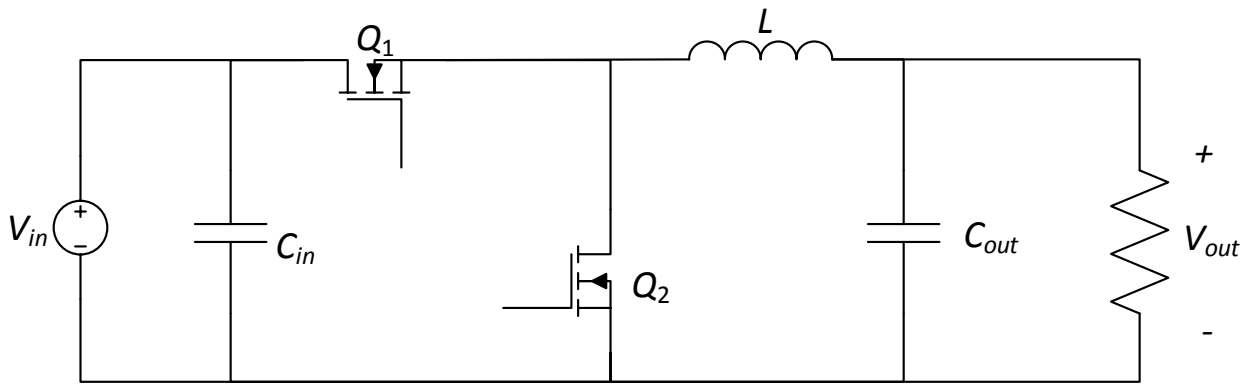


Figure 3.1 Synchronous buck converter schematic

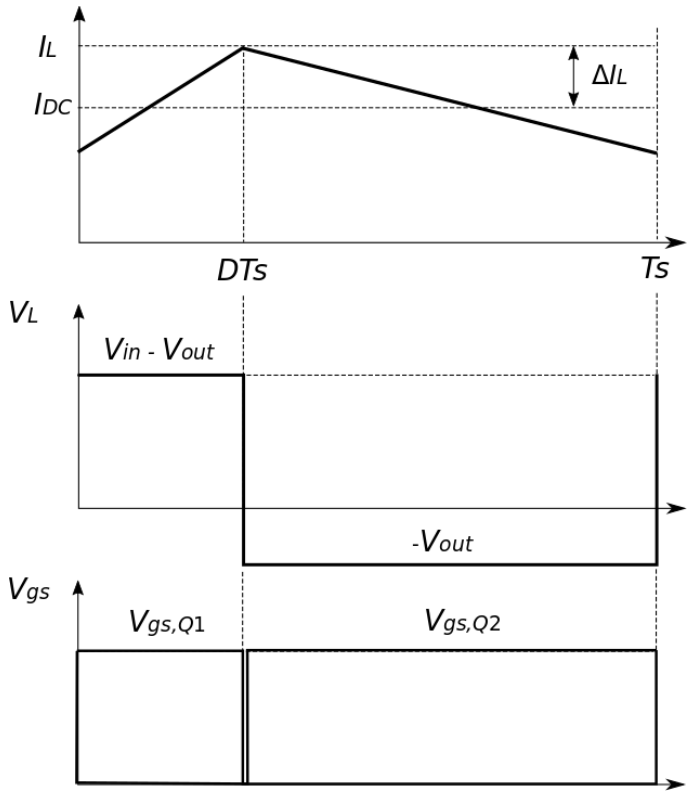


Figure 3.2 Synchronous buck converter waveforms

While $Q_1$ is on for time $DT_s$, the inductor current is shared by the high-side device. The current ripple,

$$\Delta I_L = \frac{V_{in}-V_{out}}{2 \cdot L} D \cdot T_s \,, \tag{6}$$

is used to calculate the RMS current through $Q_1$,

$$I_{Q1,rms} = I_{DC}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta \mathrm{I_L}}{I_{DC}}\right)^2}\,. \tag{7}$$

The conduction power loss for the high-side device over $DT_s$ is

$$P_{Q1,cond} = R_{on} \cdot I_{Q1,rms}^2. \tag{8}$$

During the next state, $Q_1$ turns off, $Q_2$ turns on, and the inductor current free-wheels through $Q_2$. This equivalent circuit is shown by Figure 3.4. The current through $Q_2$,

$$I_{Q2,rms} = I_{DC}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta \mathrm{I_L}}{I_{DC}}\right)^2}\,, \tag{9}$$

is used to calculate the conduction losses

$$P_{Q2,cond} = R_{on} \cdot I_{Q2,rms}^2. \tag{10}$$

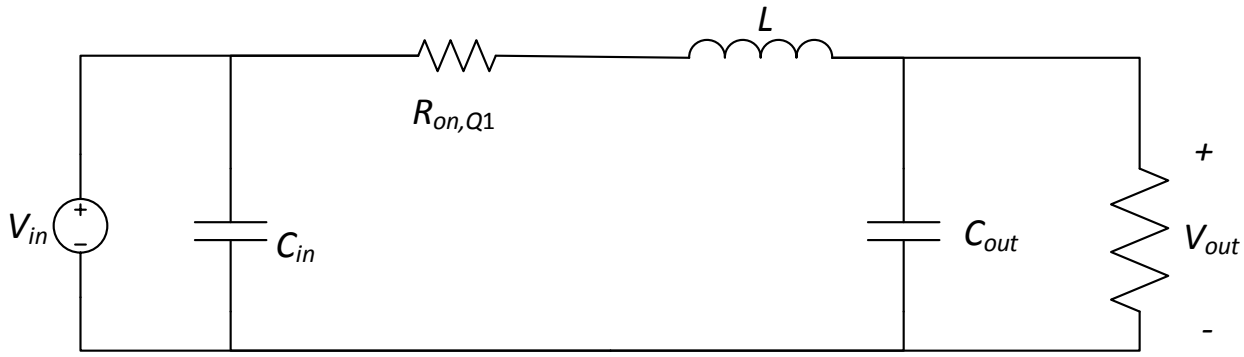


Figure 3.3 Equivalent circuit of the synchronous buck converter $0 < t < DT_s$

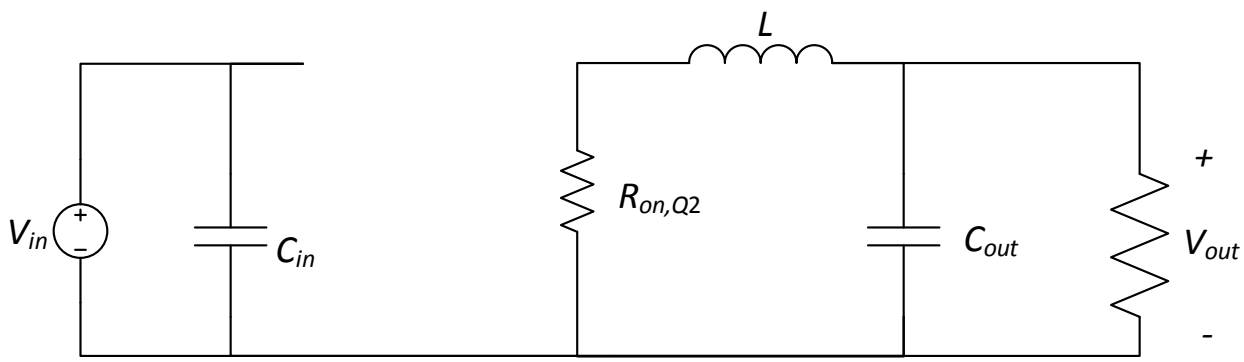


Figure 3.4 Equivalent circuit of the synchronous buck converter $DT_s < t < T_s$

At the beginning of the period, the voltage across $Q_1$ is $V_{in}$. This charge is stored in the output capacitance, $C_{oss}$, of $Q_1$. When $Q_1$ turns on again the charge is dissipated in the channel of $Q_1$,

$$P_{coss} = \frac{1}{2} V_{in}^2 \cdot C_{oss} \cdot f_s. \tag{11}$$

As the gate driver supplies and sinks current to and from the device input capacitance, the charge supplied by the gate driver to turn on the device is lost every period. This power loss,

$$P_{Qg} = \frac{1}{2} \cdot V_{dr} \cdot Q_g \cdot f_s, \tag{12}$$

increases with frequency and driving voltage.

The RMS current of the inductor is

$$I_{L,rms} = I_{DC} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta \mathrm{I_L}}{I_{DC}} \right)^2}, \tag{13}$$

and the conduction losses are

$$P_{L,cond} = R_L \cdot I_{L,rms}^2 . \tag{14}$$

### 3.1.1 Overlap Power Loss Model

Device overlap losses are a significant portion of the overall power loss, especially in high current applications. The overlap power loss model is described in detail by [44] and summarized in the following section. Figure 3.5 shows the $Q_1$ turn-off switching transition waveforms.

The peak current,

$$I_{L,pk} = I_L + \Delta I_L \,, \tag{15}$$

is used to calculate the overlap losses during the high-side device turn-off,

$$P_{ov} = \frac{1}{2}\left(V_{in} \cdot I_{L,pk}\right) \cdot (t_2 + t_3) \cdot f_s. \tag{16}$$

The length of $t_2$ and $t_3$ is determined by the amount of current that the gate driver can supply and the charge that it needs to supply to turn on the device.

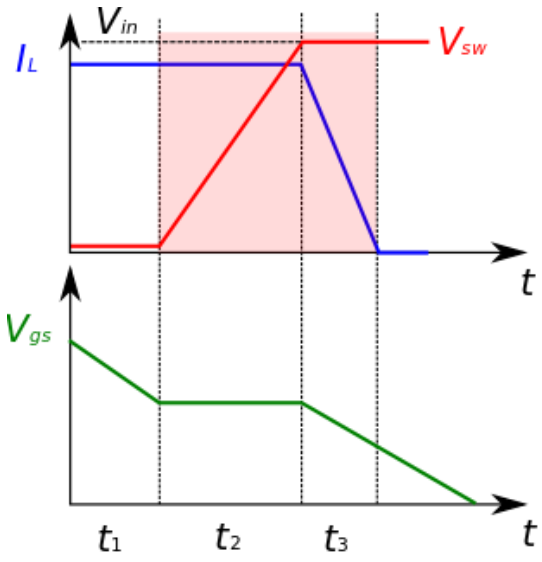


Figure 3.5 $Q_1$ turn-off waveforms

For the $Q_1$ turn-on and turn-off switching transitions, the current supplied by the driver during time $t_2$ is

$$I_{driver(L-H)} = \frac{V_{dr} - V_{sp}}{R_{driver(pull-up)} + R_{gate}} \tag{17}$$

$V_{sp}$ is the Miller voltage of the device during $t_3$ and is approximately

$$V_{sp} \approx V_{th} + \frac{I_{out}}{g_m}, \tag{18}$$

where $g_m$ is the device transconductance. Additionally, the current supplied by the gate driver during time $t_3$ is

$$I_{driver(H-L)} = \frac{V_{sp}}{R_{driver(pull-down)} + R_{gate}}. \tag{19}$$

By estimating that the total gate charge through the switching interval as

$$Q_{g(SW)} \approx Q_{gd} + \frac{Q_{gs}}{2}\ , \tag{20}$$

the switching times

$$t_2 = \ t_{s(L-H)} = \frac{Q_{g(SW)}}{I_{driver(L-H)}} \tag{21}$$

and

$$t_3 = t_{s(H-L)} = \frac{Q_{g(SW)}}{I_{driver(H-L)}} \tag{22}$$

are calculated.

The power loss through the low-side device is

$$P_{SW(LS)} = \left(t2_R \cdot V_f + t3_R \cdot \frac{V_f + I_{out} \cdot R_{on(0.9V_{dr})}}{2}\right) \cdot I_L \cdot f_{sw} \tag{23}$$

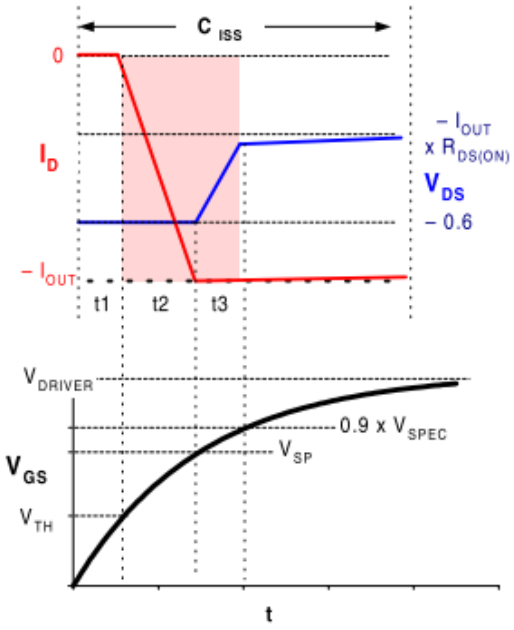


Figure 3.6 $Q_2$ turn-on switching transitions waveforms [44]

The time intervals are now calculated by using equations derived from a simplistic *R-C* circuit. Figure 3.6 shows the $Q_2$ turn-on switching transition waveforms. The ratio of $V_{dr}$, $V_{sp}$, and $V_{th}$ that describes time $t2_R$ is

$$K_{2R} = \ln\left(\frac{V_{dr}}{V_{drive}-V_{sp}}\right) - \ln\left(\frac{V_{dr}}{V_{drive}-V_{th}}\right) \tag{24}$$

and is used to describe the rise of the gate-source voltage to increase from $V_{th}$ to $V_{sp}$,

$$t2_R = K_{2R}\left(R_{driver} + R_{gate}\right) \cdot C_{iss}, \tag{25}$$

The ratio of $V_{dr}$ and $V_{sp}$ used to describe the rise time that it takes the gate voltage to increase from $V_{sp}$ to 90% of $V_{dr}$ is

$$K_{3R} = \ln\left(\frac{V_{dr}}{V_{dr} - 0.9 \cdot V_{dr}}\right) - \ln\left(\frac{V_{dr}}{V_{dr} - V_{sp}}\right) \tag{26}$$

and the time is

$$t3_R = K_{3R}\left(R_{driver} + R_{gate}\right)C_{iss} \tag{27}$$

The low-side turn-off power loss is calculated similarly. Figure 3.7 shows the $Q_2$ turn-off switching loss waveforms.

The ratio between $V_{dr}$ and $V_{sp}$,

$$K_{3F} = \ln\left(0.9 \cdot \frac{V_{dr}}{V_{sp}}\right), \tag{28}$$

is used to describe the period that the gate-source voltage decreases from $V_{dr}$ to $V_{sp}$,

$$t3_F = K_{3F} \cdot \left(R_{driver} + R_{gate}\right) \cdot \ C_{iss}. \tag{29}$$

The ratio between $V_{sp}$ and $V_{th}$,

$$K_{2F} = \ln\left(\frac{V_{sp}}{V_{th}}\right), \tag{30}$$

describes the period in which $V_{gs}$ decreases from $V_{sp}$ to the threshold voltage $V_{th,}$

$$t2_F = K_{2F} \cdot \left(R_{driver} + R_{gate}\right) \cdot C_{iss}. \tag{31}$$

As shown by the switching loss model, a larger $C_{iss}$ will result in a longer turn-on and turn-off times, yielding higher overlap losses. Device geometry and material have a significant impact on device input capacitance and gate resistance. Likewise, the gate driver resistance also influences the rise and fall times. By adding external resistance to the output of the gate driver, the switching transition times become longer, and the overlap losses increase.

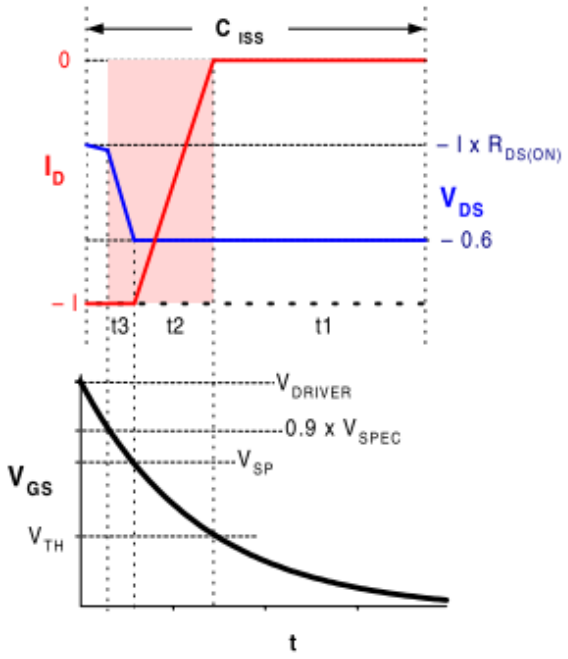


Figure 3.7 $Q_2$ turn-off switching loss waveforms [44]

## 3.1.2 ACR Power Loss Model

An ideal inductor has infinitely large inductance and acts as a current source, meaning only the DC-resistance affects power loss. If the inductance is not DC, the output inductor current looks like a triangle wave with a DC-bias. As the current ripple increases, the AC components of the inductor current begin to impact efficiency by introducing frequency-dependent power losses and the AC-resistance (ACR) begins to greatly impact efficiency. This impact is more influential in resonant topologies with large ripple currents such as the QR-ZCS buck. Nevertheless, the effect of ACR remains relevant to high current ripple synchronous bucks.

The Fourier series of the inductor waveform harmonics and fundamental switching frequency are

$$f(x) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} a_n \cos(\mathrm{nx}) + \sum_{n=1}^{\infty} b_n \sin(nx)\,. \tag{32}$$

Where

$$a_0 = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)dx \tag{33}$$

describes the mean of the waveform,

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\cos(nx)\,dx \tag{34}$$

and

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin(nx)\,dx \tag{35}$$

describe the magnitude of the waveform. The RMS of the $n^{th}$ harmonic component is

$$I_{n,rms} = \frac{\sqrt{a_n^2 + b_n^2}}{\sqrt{2}} \tag{36}$$

The AC-resistance of an inductor, $R_{AC}$, is measured by an impedance analyzer and the power loss is

$$P_{ACR} = \sum_{n=1}^{h} I_{n,rms}^2 \cdot R_{AC,n}\,. \tag{37}$$

In practice,

$$I_{rms,tri} \approx \frac{\sum_{n=1}^{h} \frac{\Delta I_L}{\pi^2 \cdot (q - 2q^2)} \cdot \frac{\sin(2 \cdot \pi \cdot n \cdot q)}{n^2}}{\sqrt{2}}, \tag{38}$$

where

$$q = \frac{D}{2 - D} \tag{39}$$

is utilized for reducing computational burden when calculating the ACR power loss of the output inductor. Two example circuits are described by Table 1. Circuit (1) has a large inductance and low current ripple. Conversely, circuit (2) has a relatively small inductance and a large current ripple. Equation $(38)$ shows that the magnitude of the harmonics is dictated by the duty cycle, *D*, and the current ripple, $\Delta I_L$. The respective output inductor current waveforms and FFTs are shown in

Figure 3.8 and Figure 3.9. Depending on the ACR of these inductors, this harmonic content may be significant and must be considered during the design phase.

Table 1 Example synchronous buck converter circuits

| Circuit examples | (1) | (2) |
|---|---|---|
| Switching frequency [MHz] | 2 | 2 |
| Filter Inductance [nH] | 330 | 50 |
| $\Delta I_L$ [ A] | 0.873 | 5.76 |
| *D* | 0.36 | 0.36 |

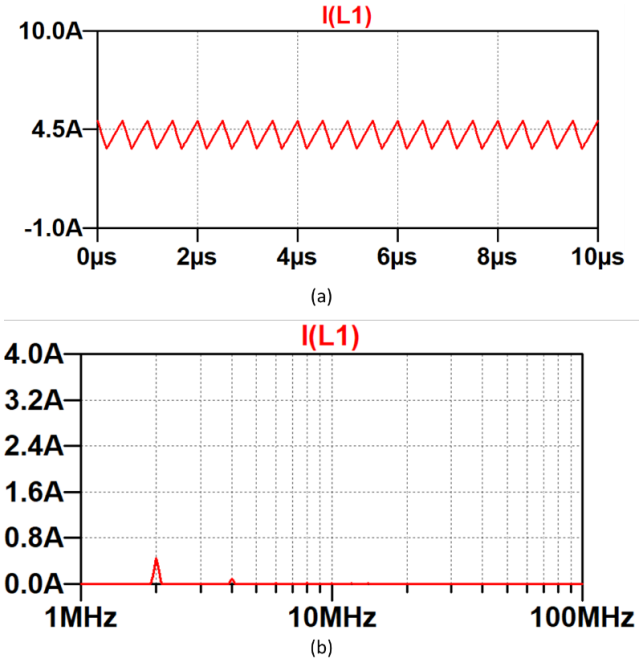


Figure 3.8 Filter inductor current waveform (a) and FFT (b) for Circuit Example (1)

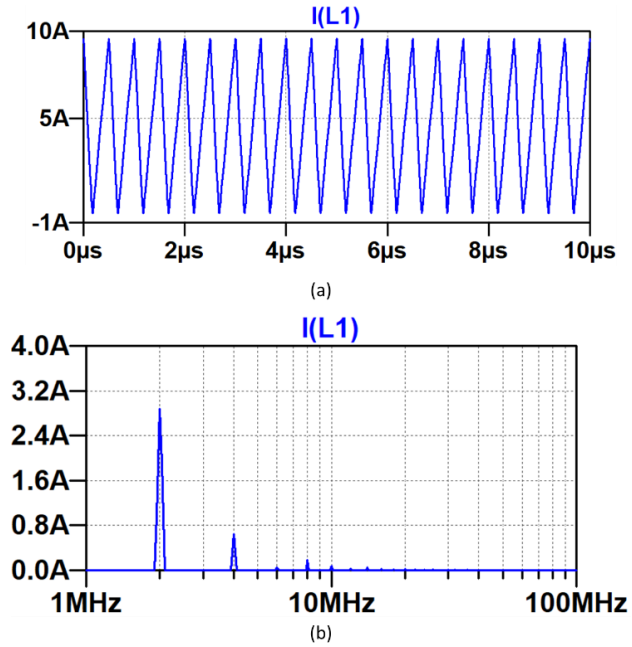


Figure 3.9 Filter inductor current waveform (a) and current FFT (b) for Circuit Example (2)

The power loss model can be further improved by calculating the RMS currents of the harmonics of the current through the input capacitor. By measuring the ESR of the input capacitors, the same method used with the output inductor is applied. The input current is a sawtooth wave with a DC-bias as shown by Figure 3.10. The RMS current,

$$I_{rms,Cin\_n} = \sum_{n=1}^{h} \frac{2\Delta I_L}{n \cdot \sqrt{2}}\,, \tag{40}$$

is used to calculate the power loss,.

$$P_{ESR,Cin} = \sum_{n=1}^{h} I_{rms,Cin\_n}^2 \cdot R_{ESR,n} \tag{41}$$

through the input capacitors.

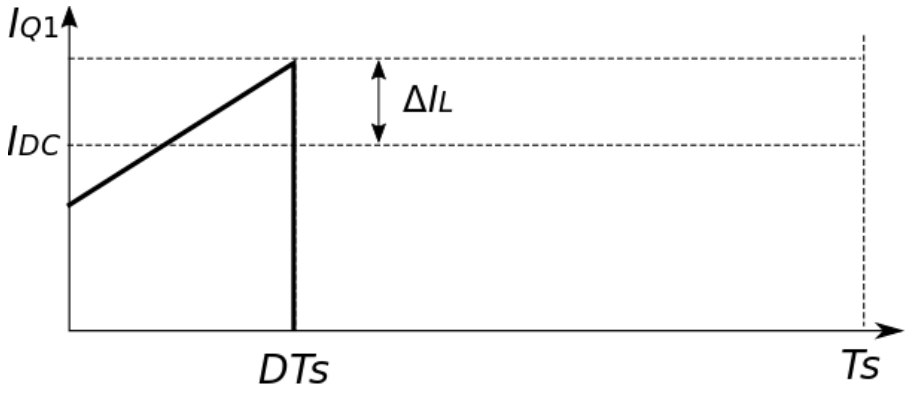


Figure 3.10 Input current waveform

## 3.1.3 Other power loss mechanisms

Another frequency-dependent loss is the power loss of the filter inductor core. These losses are a function of peak current and core material properties. Plots taken from a discrete inductor data sheet were used to calculate the core material Steinmetz parameters $\alpha, \beta,$ and $k$. Figure 3.11 shows a plot used to estimate core power loss from a discrete inductor. By creating a system of at least three equations, $\alpha, \beta,$ and $k$ are calculated. Using Steinmetz parameters gleaned from the material properties and

$$P_{core} = k \cdot B_{pk}^{\beta} \cdot f_s^{\alpha} \cdot V_{core}, \tag{42}$$

the core power loss, is calculated.

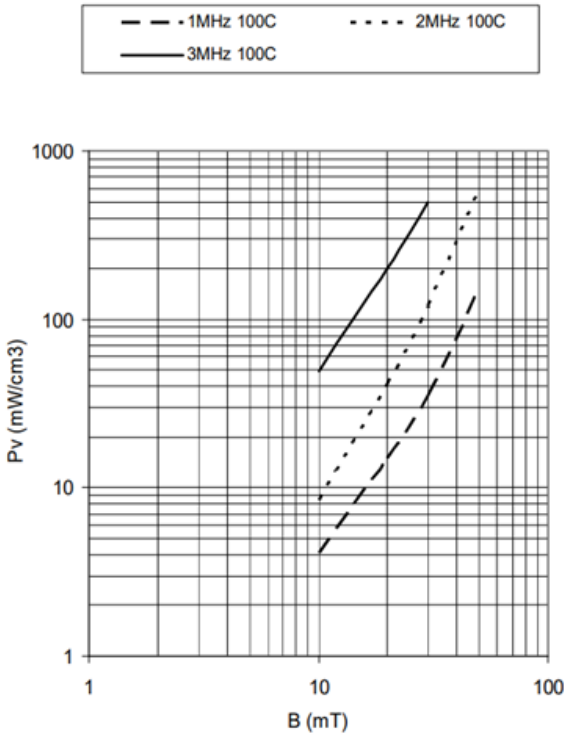


Figure 3.11 Core loss of 3F46 material [62]

Diode conduction loss occurs due to a non-ideal turn-on and turn-off timing of the high-side and low-side devices. As shown in the analysis of the switching losses, the time between turn-on and turn-off is not instantaneous, and one consequence of this discrete switching time is overlap loss. Likewise, this switching time can create a condition in which both switching devices are off and the body diode of a FET conducts the full output current. GaN HEMTs do not have the same p-n body diode structure as a Silicon FET, but there are losses associated with reverse conduction. The threshold voltage of the source-to-drain, $V_{SD}$ of a lateral GaN device is often much higher than the forward voltage of the body diode of a similarly-rated Silicon device. The power loss associated with reverse conduction,

$$P_{reverse} = V_{SD} \cdot I_{out} \cdot t_d \cdot f_s, \tag{43}$$

is used to determine the losses associated with reverse conduction during the dead-time, $t_d$. Turn-on and turn-off switching times are influenced by gate driver current dynamics and parasitic inductance. Without complex gate driver models and precisely measuring the parasitic loop and gate inductance, the switching transitions are difficult to accurately model. Therefore, it is assumed that the switching transition is infinitely fast and $\frac{di}{dt} = \infty$. An increase in either the dead-time or the switching frequency can negatively impact converter efficiency and much effort is given to minimizing the reverse conduction losses. Increasing or decreasing the gate driver resistance and adjusting the dead time manually are two common ways of reducing these losses.

## 3.1.4 Buck converter design

In implementing the optimization, the footprint and volume of devices must also be taken into account to optimize for both power density and efficiency. To effectively compare power density and efficiency, a component volume model must first be constructed, and an

optimization of frequency, output current, and combination of discrete components must be performed to compare relative performance. A component database of low-voltage EPC GaNFETs and low-DCR, low-profile inductors is assembled and used as data source for optimization. Using the power loss model described in this section and known device footprints and volumes, power density and efficiency are calculated and compared. In addition to the FET and inductor volume, the gate driver, external gate resistances, and decoupling capacitor volume are considered. To effectively compare all combinations of discrete inductors, GaN FETs, and operating points, these converter components and operating points are iterated and a design is selected. The PCB footprint, $A_{PCB}$, is the addition of all component footprints shown in Figure 3.12. The power density of the converter is

$$\alpha = \frac{P_{out}}{A_{PCB} \cdot h_L} \tag{44}$$

To choose an optimal design point, an integer number of parallel inductors per phase is selected. Secondly, a discrete inductor and FET are chosen from the constructed database. The switching frequency and output current are swept iteratively, and the power density and efficiency are calculated using component parameters and operating conditions. The discrete inductor and FET databases are also iterated so that every combination of components and operating conditions create an array of potential designs.

By sweeping across these components and operating conditions, an envelope of designs is generated. Based on the desired power density and efficiency, the necessary components are selected, an optimal design point is chosen, and the design is implemented.

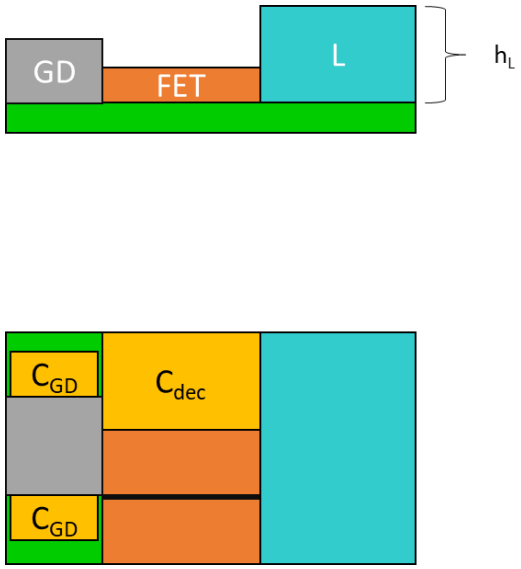


Figure 3.12 Diagram of the power density model

## 3.2 QR-ZCS buck power loss model

While current literature discusses the QR-ZCS switch timing model [63] and the estimation of operating modes [64], little research has investigated the predicted power losses of the QR-ZCS buck converter for a POL application. Initial discussion of switch timing and zero-current operation will be discussed briefly before moving on to a more comprehensive analysis of power loss mechanisms.

### 3.2.1 QR-ZCS switch timing model

Figure 2.11 and Figure 2.12 show the schematic and relevant waveforms of the QR-ZCS buck converter.

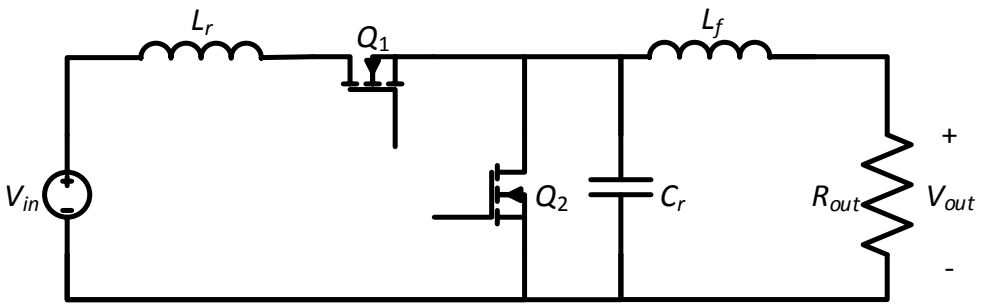


Figure 3.13 QR-ZCS buck converter schematic

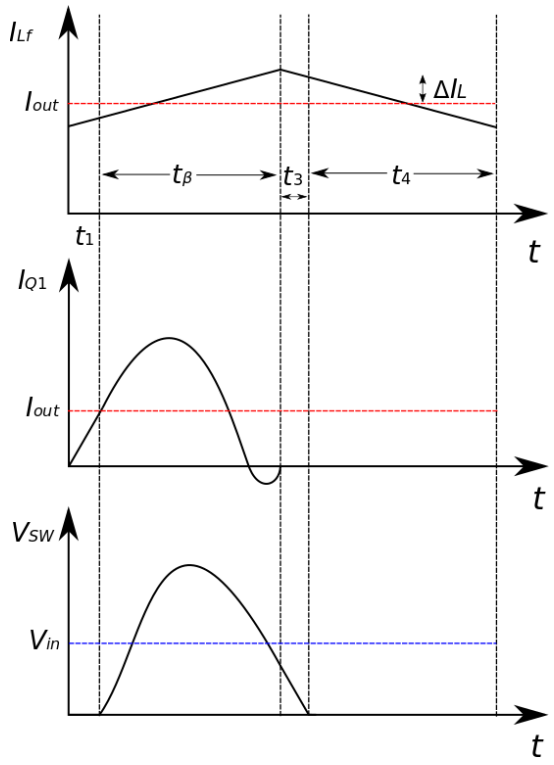


Figure 3.14 QR-ZCS buck converter waveforms

Operation is as follows: During $t_1$, $Q_1$ and $Q_2$ are on; the resonant inductor current increases. When the inductor current reaches the average output current, $I_L$, $Q_2$ turns off, and subinterval 2 begins for $t_\beta$. It is assumed that the output inductor, $L_f$, is large enough to be considered as a current source, therefore and the resonant inductor, $L_r$, and resonant capacitor, $C_r$, are decoupled from the converter output and are in series with the input voltage source. The filter inductor current and input voltage source act as DC biases around which the resonant components resonate. The resonant inductor crosses zero once, then at the second zero-crossing $Q_1$ turns off and the circuit operation enters subinterval 3 for time $t_3$. During this subinterval the output current discharges the resonant capacitor until the voltage across the capacitor is zero at which point $Q_2$ turns on again, entering subinterval 4. The output current freewheels through $Q_2$ until the volt-second balance across the output inductor is achieved after time $t_4$. To better describe the resonance of the circuit, state-plane analysis is used and shown by Figure 3.15. The state-plane model is previously developed in [63] and used in the switch timing calculations.

State-plane analysis is useful for better understanding the resonant operation of the converter and is used to calculate the precise timing needed for zero-current switching. The subintervals are again described using state-plane analysis and equations describing the waveforms are detailed.

First, the resonant capacitor voltage, $V_{cr}$, is normalized to the input voltage, where $V_{in} = V_{base}$

$$m_c = \frac{V_{cr}}{V_{base}}. \tag{45}$$

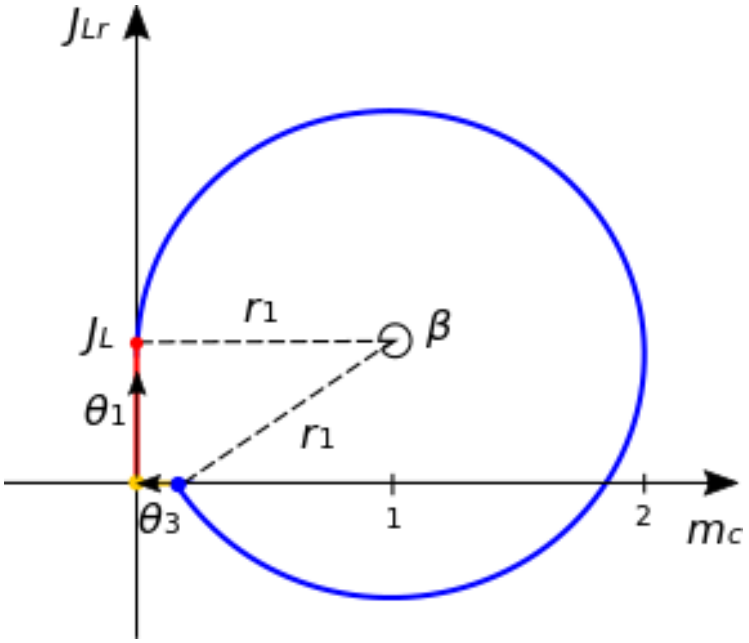


Figure 3.15 State-plane diagram describing QR-ZCS buck

The average resonant inductor current, $I_{Lr}$, is normalized to

$$J_{Lr} = \frac{I_{Lr}}{I_{base}}, \tag{46}$$

where

$$I_{base} = \frac{V_{base}}{R_o} \tag{47}$$

and

$$R_o = \sqrt{\frac{L_r}{C_r}}. \tag{48}$$

State-plane analysis describes the relationship between $V_{cr}$ and $I_{Lr}$ and is useful for illustrating resonant voltage and current. Analysis is first performed in the normalized state plane and is later de-normalized into the time domain using the resonant frequency,

$$\omega_r = \frac{1}{\sqrt{L_r \cdot C_r}}. \tag{49}$$

*Subinterval 1:*

Figure 3.16 shows the equivalent circuit of subinterval 1. The change in resonant inductor current is

$$\frac{di_L}{dt_1} = \frac{V_L}{L_r}. \tag{50}$$

The time for the resonant inductor current to reach $I_{Lr}$ is

$$t_1 = \frac{L_r}{V_L} \cdot I_{Lr}. \tag{51}$$

Equations (47) and (48) are used to transform $t_1$ into the normalized state plane where

$$\theta_1 = J_L. \tag{52}$$

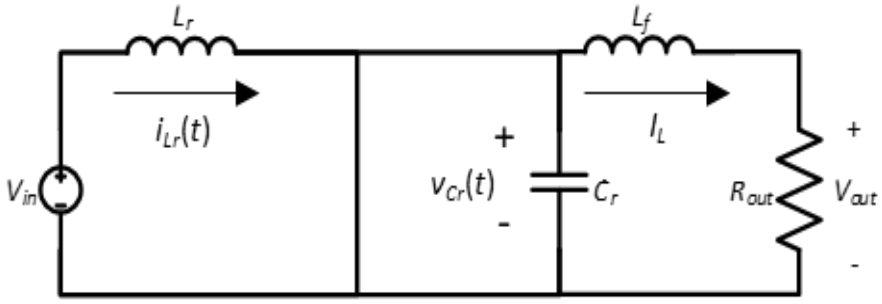


Figure 3.16 Equivalent circuit of Subinterval 1

*Subinterval 2:*

Figure 3.17 shows the equivalent circuit of subinterval 2. The angle,

$$\beta = 2 \cdot \pi - \sin^{-1}(J_L)\,, \tag{53}$$

is used to describe the length of the second subinterval. The radius of the circle,

$$r_1 = \begin{cases} 1, \\ \sqrt{M_1^2 + J_L^2}\,, \end{cases} \tag{54}$$

is used to calculate $v_{cr}$ at the end of the subinterval:

$$\frac{v_{Cr}(t_1 + t_\beta)}{V_{base}} = M_1 = \sqrt{1 - J_L^2}\,. \tag{55}$$

ZCS is achieved at the end of this subinterval. When $J_L > 1$, $M_1$ is negative. This negative voltage results in reverse conduction through $Q_2$, resulting in power loss.

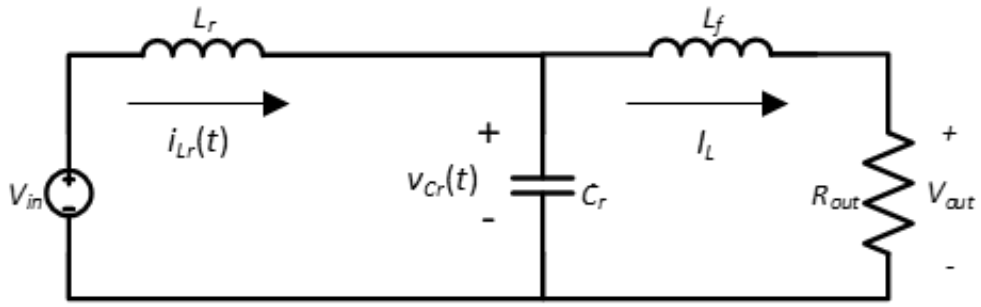


Figure 3.17 Equivalent circuit of Subinterval 2

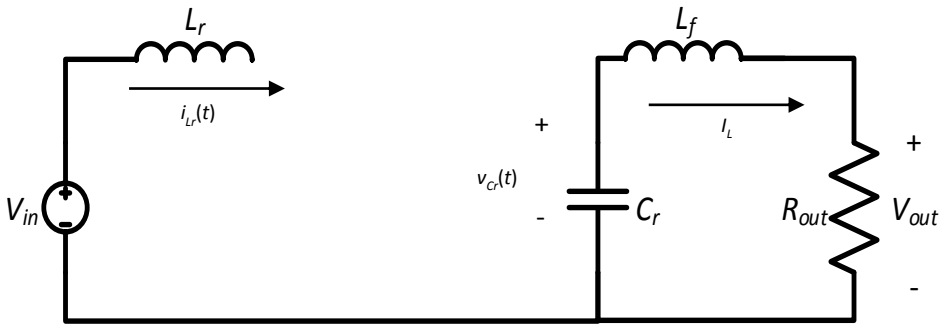


Figure 3.18 Equivalent circuit of Subinterval 3

*Subinterval 3:*

Figure 3.18 shows the equivalent circuit of subinterval 3. This subinterval is defined by the time necessary to completely discharge $C_r$,

$$t_3 = \frac{C_r \cdot M_1 \cdot V_{base}}{I_{Lf}}. \tag{56}$$

By transforming $t_3$ into the normalized state plane,

$$\theta_3 = J_L \cdot M_1, \tag{57}$$

*Subinterval 4:*

Figure 3.19 shows the equivalent circuit of subinterval 4. During this subinterval, $I_L$ is flowing through $Q_2$ and none of the resonant components are utilized. The length of this subinterval is determined by the desired voltage ratio,

$$M = \frac{V_{out}}{V_{in}}. \tag{58}$$

An approximation given by [65] shows that the voltage ratio is determined purely by the ratio of the resonant frequency, $f_r$, and the switching frequency, $f_s$:

$$F = M = \frac{V_{out}}{V_{in}} \cong \frac{f_s}{f_r}. \tag{59}$$

This subinterval angle,

$$\theta_4 = F - \theta_1 - \beta - \theta_3\ , \tag{60}$$

is the remainder of the switching period.

The subinterval times

$$t_1 = \frac{\theta_1}{\omega_r}, \tag{61}$$

$$t_\beta = \frac{\beta}{\omega_r}, \tag{62}$$

$$t_3 = \frac{\theta_3}{\omega_r}, \tag{63}$$

and

$$t_4 = \frac{\theta_4}{\omega_r} \tag{64}$$

are then de-normalized into the time domain by dividing the angles by $\omega_r$.

When designing the QR-ZCS buck, $M$ and $f_s$ are selected and $\omega_r$ is calculated by (49) Because $J_{Lr}$ is limited to less than 1, $I_{L,}$ should be less than $I_{base}$ at the full-load condition. The peak current of the resonant current is

$$I_{pk} = I_L + I_{base}. \tag{65}$$

. When $J_L > 1$, reverse conduction occurs during $t_3$, causing significant reverse conduction losses. If $J_L < 1$ at the full-load current, $I_L < I_{base}$, and the resonant peak current, $I_{pk}$, results in high conduction losses. If the resonant components are designed so that $I_L = I_{base}$ at full-load, the resonant current peaks are lower across the load range, reducing conduction losses.

If the converter is designed with a large $I_{base}$ is, then the peak current will be large regardless of the output current. After selecting $I_{base}$, the resonant component values are

$$L_r = \frac{R_o}{\omega_r} \tag{66}$$

and

$$C_r = \left(\frac{1}{L_r}\right) \cdot \left(\frac{1}{\omega_r}\right)^2 . \tag{67}$$

The calculated values are then implemented with discrete passives.

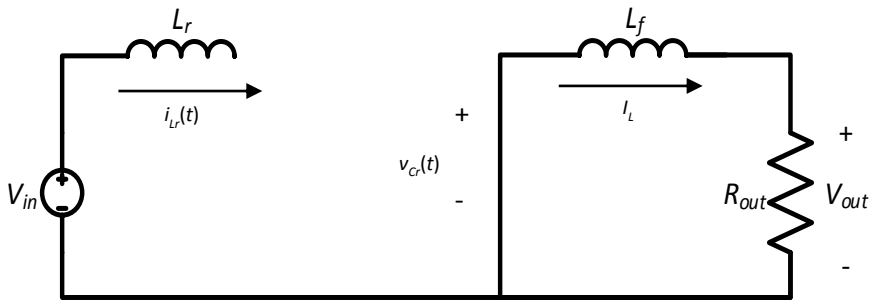


Figure 3.19 Equivalent circuit of Subinterval 4

## 3.2.2 QR-ZCS Power Loss Model

Unlike the synchronous buck topology, overlap losses are assumed to be negligible. However, the high peak resonant currents through the resonant components are shown to be a significant mechanism of this topology's power loss. To perform an effective comparison between the QR-ZCS buck and synchronous buck, an accurate power loss model is constructed. While the effect of ACR loss is discussed with regards to the synchronous buck, the frequency-dependent losses associated with resonant components are much more significant due to the magnitude of the resonant current

During subinterval 1, $L_r$, $Q_1$, and $Q_2$ are conducting. The RMS current through these components is

$$I_{rms,1} = \frac{V_g - V_o}{\sqrt{3} \cdot 2 \cdot L} \cdot t_1. \tag{68}$$

The current through the output inductor, $I_{out}$, though considered constant during the state-space analysis, has a current ripple,

$$\Delta I_{Lf} = \frac{V_{out}}{2 \cdot L_f} \cdot t_4. \tag{69}$$

The RMS current is

$$I_{rms,Lf} = I_{out} \cdot \sqrt{1 + \frac{1}{3}\left(\frac{\Delta I_{Lf}}{I_{out}}\right)}, \tag{70}$$

and the conduction power loss is

$$P_{cond,Lf} = R_{Lf} \cdot I_{rms,Lf}^2. \tag{71}$$

During subinterval 2, $L_r$, $C_r$, and $Q_1$ are conducting. The RMS current is

$$I_{rms,\beta} = \sqrt{f_s \cdot \left( t_\beta \cdot I_{out}^2 - \frac{(2 \cdot (I_{base}) \cdot I_{out} \cdot \cos(\beta) - 1)}{\omega_r} + (I_{base})^2 \cdot \left( \frac{t_\beta}{2} - \frac{\sin(2 \cdot \beta)}{4 \cdot \omega_r} \right) \right)}. \tag{72}$$

During subinterval 3, $C_r$ is discharged by the output current. Time interval $t_3$ is typically very short relative to the overall period, so the losses in the resonant capacitor during this interval are negligible. Though the losses due to the ESR of the capacitor are not considered here, the current is included during the analysis of the frequency-dependent losses.

During subinterval 4, the output current conducts through $Q_2$. As the power loss due to the DC-resistance of $L_f$ is already taken into account by (71), the power loss through $Q_2$ is separately. The RMS current through subinterval 4 is

$$I_{rms,4} = I_{out} \cdot \sqrt{\frac{t_4}{T_s}} \cdot \sqrt{1 + \frac{1}{3}\left(\frac{\Delta I_L}{I_{out}}\right)} \tag{73}$$

The total RMS current for $Q_1$ is

$$I_{rms,Q1} = \sqrt{I_{rms,1}^2 + I_{rms,\beta}^2}, \tag{74}$$

and the RMS current for $Q_2$ is

$$I_{rms,Q2} = \sqrt{I_{rms,1}^2 + I_{rms,4}^2}. \tag{75}$$

While the DC conduction losses of the QR-ZCS buck converter are a significant power loss mechanism, the frequency related losses are non-negligible and are considered using the same methodology as with the synchronous buck. During subinterval 2, the resonant inductor

and capacitor induce a resonant current that has a peak current $I_{pk} = I_{base} + I_{L.}$ Although the resonant current peaks change based on the output current, the AC portion of the current is heavily reliant on the parameter $I_{base}$ which is set by the converter full-load operation and resonant component implementation. Table 2 details two distinct operating points of the same converter and Figure 3.20 shows the schematic of the circuit simulation. Due to the high current operation of the circuit, two devices are paralleled to distribute the current stress. Figure 3.21 and Figure 3.22 show these two respective operating point waveforms and highlight the differences and similarities in RMS current through $L_r$.

Table 2 QR-ZCS buck converter example circuits

| Circuit examples | A | B |
|---|---|---|
| Switching frequency [MHz] | 1 | 1 |
| Resonant Inductance [nH] | 22 | 22 |
| Resonant Capacitance [nF] | 188 | 188 |
| Input Voltage [V] | 5 | 5 |
| Output Voltage [V] | 1.8 | 1.8 |
| Output Current [A] | 1 | 10 |

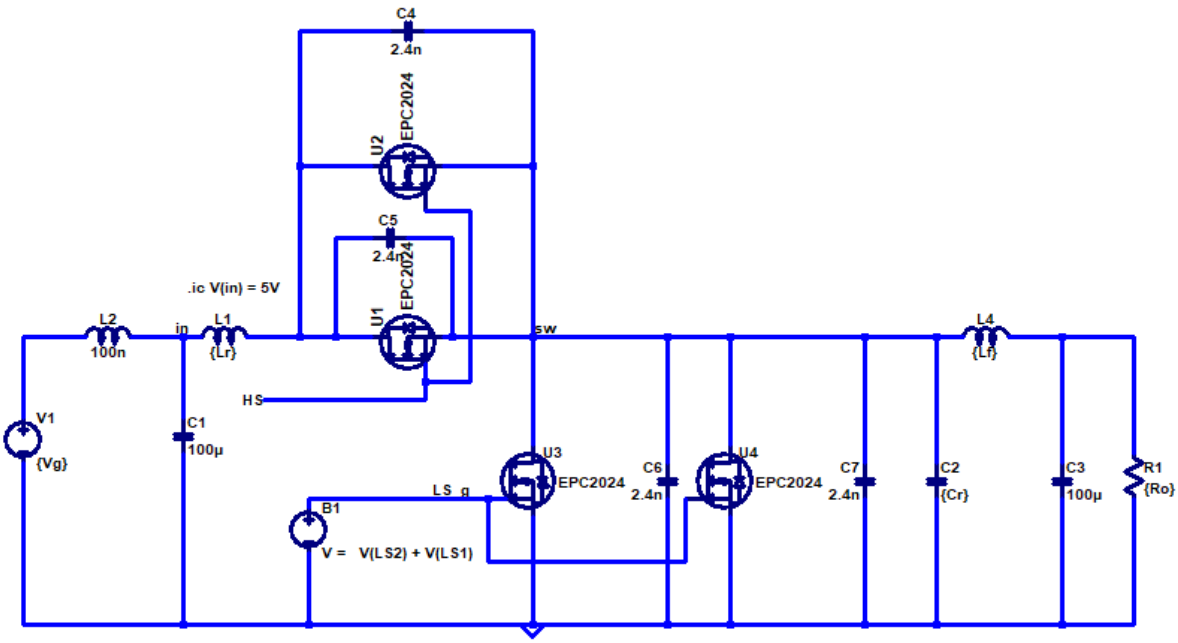


Figure 3.20 Schematic of QR-ZCS buck converter circuit simulation

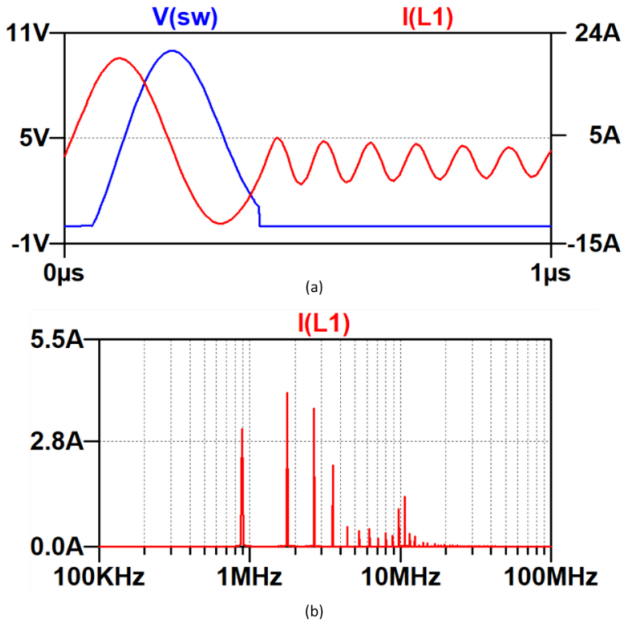


Figure 3.21 Circuit A QR-ZCS buck waveforms (a) and resonant inductor current FFT (b) operating at 1 A output current

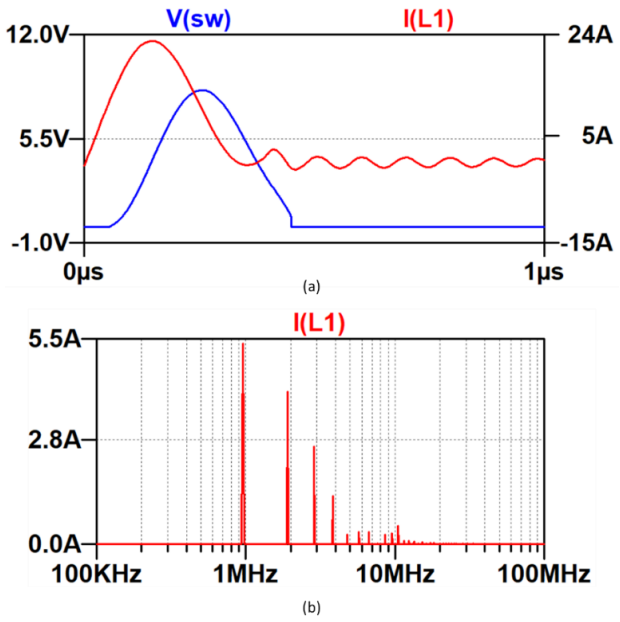


Figure 3.22 Circuit B QR-ZCS buck waveforms (a) and resonant inductor current FFT (b) operating at 10 A output current

As shown by the figures, the magnitude of the AC-components of the resonant inductor current changes as a function of output current. The magnitudes of the harmonics remain the same over the operating range, but the magnitude of the fundamental frequency is determined by the DC operating point. For the sake of modeling expediency, the resonant inductor waveforms are constructed in MATLAB and the resonant inductor harmonic components are calculated by evaluation of the Fourier series harmonic magnitudes. Figure 3.23 shows the QR-ZCS buck converter waveforms reconstructed using MATLAB. (32) is used to calculate the RMS of the resonant current harmonics. Table 3 compares the results from the time-domain analysis simulation and the MATLAB simulation. The results agree and show less than 10% error across the first four harmonics.

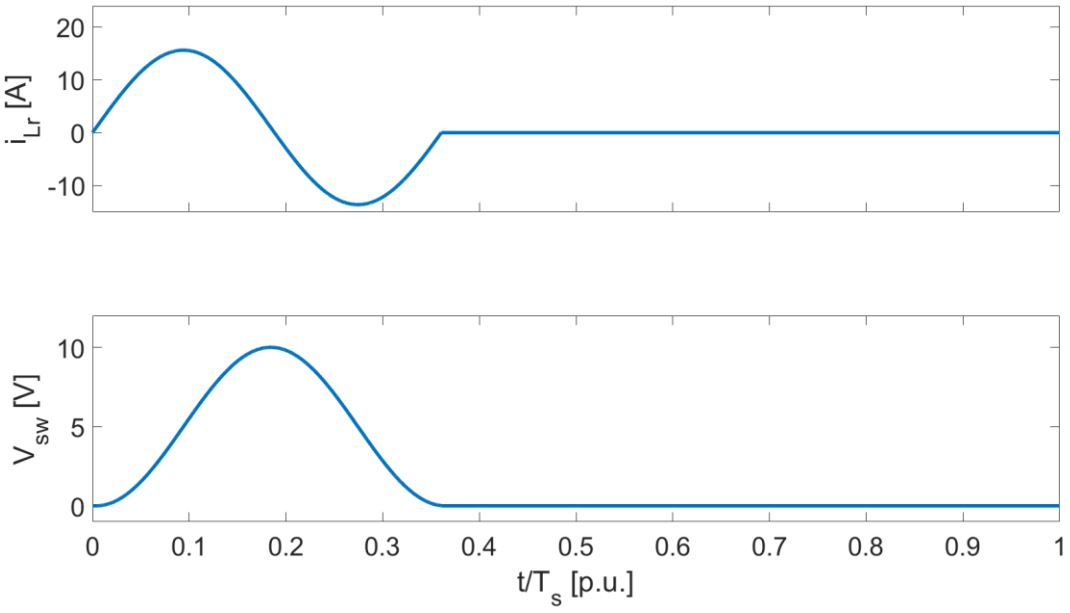


Figure 3.23 QR-ZCS buck converter MATLAB simulation waveforms

Table 3 Comparison of MATLAB and LTSPICE FFT results at 1 A output current and 1 MHz

| Switching frequency [MHz] | MATLAB | LTSPICE |
|---|---|---|
| 1 | 2.5 | 2.48 |
| 2 | 3.80 | 3.65 |
| 3 | 3.54 | 3.33 |
| 4 | 2.17 | 1.96 |

Like the synchronous buck converter, a component volume model is created to estimate the converter power density. The database of discrete output inductors and FETs used in the synchronous buck design is utilized to calculate the power density and efficiency. The resonant inductor and resonant capacitors are not initially included in this power loss model.

## 3.3 Synchronous Buck and QR-ZCS Buck Comparison

Because of the difficulties of modeling inductor ACR and core losses without access to extensive manufacturer data, attention will be devoted to comparing the synchronous buck and QR-ZCS buck in terms of conduction and overlap losses. For this analysis, it is assumed that the total converter loss is generated by the FETs and that the output inductance is infinitely large and lossless. In this survey, the maximum converter efficiency and the power density are considered. Three devices, the EPC2023, EPC2015C, and EPC2045 are chosen due to the range of $R_{on}$, $C_{iss}$, and footprint areas represented. These device parameters are shown in Table 4. The EPC2015C has a slightly higher on-resistance than the EPC2023 and a lower $C_{iss}$. In the synchronous buck topology, (7), (9), (11), (12), and (16) are used to estimate the total FET power loss. The output current is swept to estimate the converter efficiency. Figure 3.25 shows the results of the sweep. While the conduction losses at high current are non-negligible, the switching losses constitute the majority of the power loss in the switching devices, as shown by Figure 3.24.

Table 4 Survey of EPC FETs

| Devices | $R_{on}$ [mΩ] | $C_{iss}$ [nF] | Footprint [mm$^2$] |
|---|---|---|---|
| EPC2023 | 1.3 | 2300 | 13.915 |
| EPC2015C | 3.26 | 1050 | 6.56 |
| EPC2045 | 7 | 575 | 3.75 |

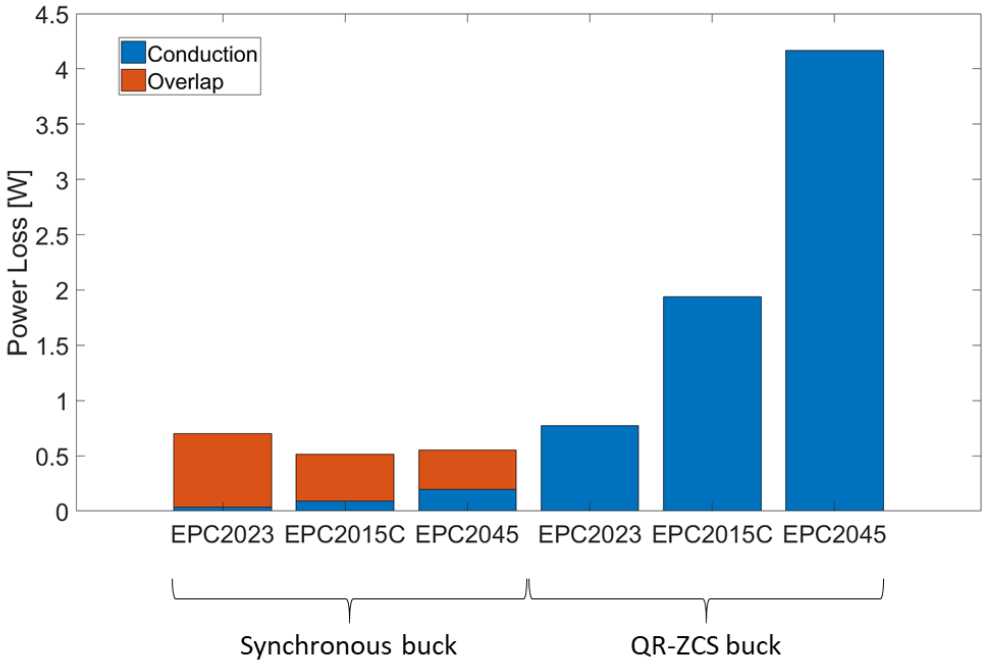


Figure 3.24 Comparison of overlap and switching losses between the synchronous buck and QR-ZCS buck

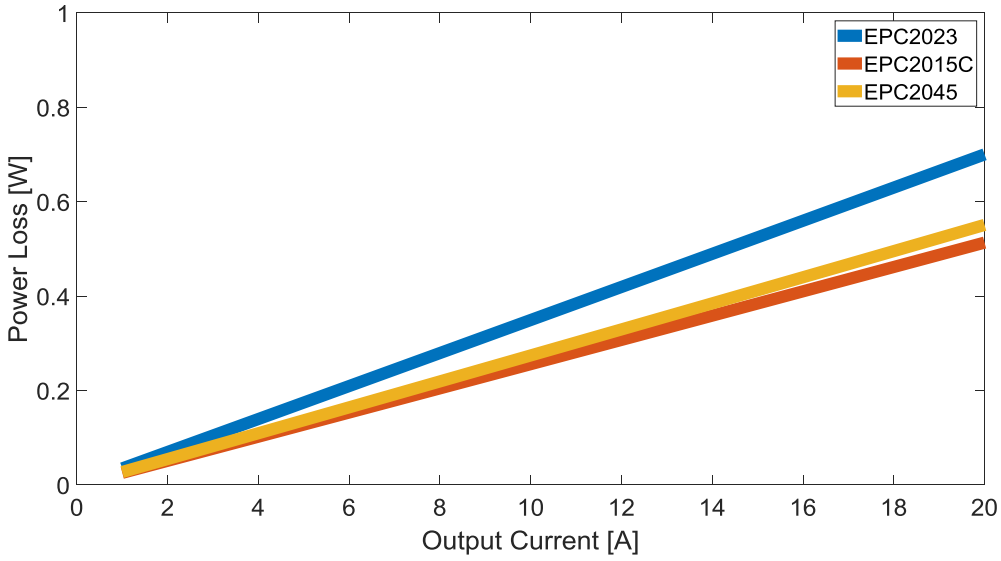


Figure 3.25 FET power loss of the synchronous buck

Though the EPC2015C has a higher on-resistance, its power loss is lower than the EPC2023. This trend suggests that switching losses dominate the power losses in the FETs. One seeming advantage to this trend is that the EPC2015C has a much smaller footprint than the EPC2023. However, as shown, this trend does not continue as the on-resistance increases in the EPC2045. At this point, current ripple is not considered, so this survey is only used to show the comparison and relationship between switching losses and on-resistance.

In the QR-ZCS buck topology the overlap losses are assumed negligible due to the zero-current switching operation. Therefore, the only power losses considered are the conduction losses. Again, the EPC2023, EPC2015C, and EPC2045 are chosen to compare to the synchronous buck. Figure 3.26 shows the FET power loss of the QR-ZCS.

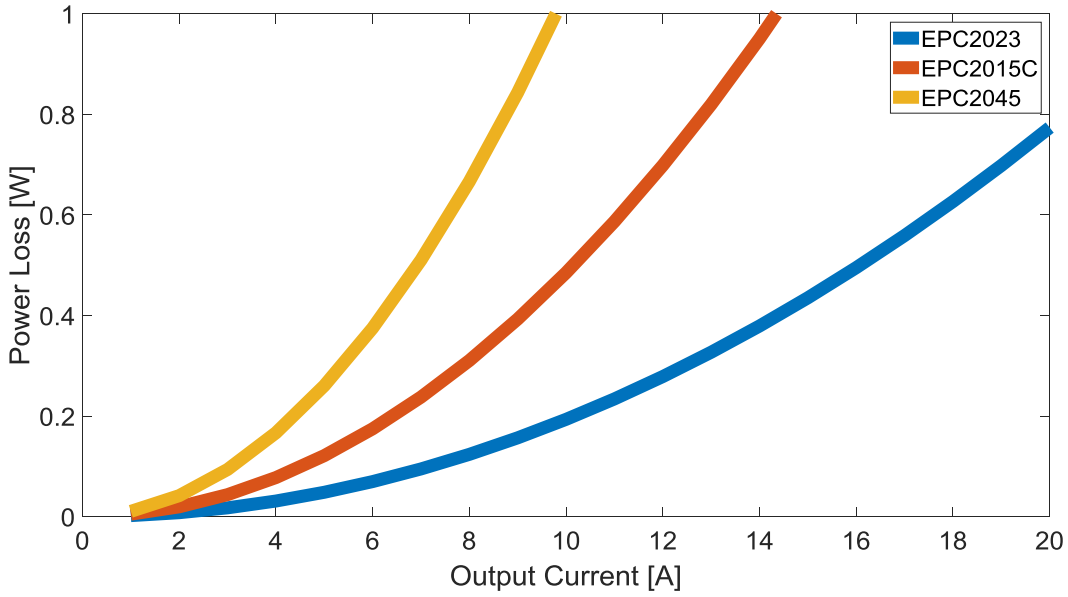


Figure 3.26 FET power loss of the QR-ZCS buck

The EPC2023 power loss is naturally the lowest as the conduction losses are the only power losses considered. As the on-resistance increases, the power loss increases dramatically. When using the EPC2023, the synchronous buck converter FET loss is 15% higher than the QR-ZCS case, suggesting that the two topologies may be competitive in terms of efficiency. This survey also suggests that the synchronous buck converter efficiency is limited by overlap losses, rather than conduction losses. As the device footprint decreases, the on-resistance increases, and the parasitic capacitance typically decreases, demonstrating the trade-offs between power density and efficiency. This review suggests that a combination of switching and conduction losses drives the design rather than a single loss mechanism. While the plots suggest that the QR-ZCS buck has the potential to be a more efficient topology, in practice the QR-ZCS buck will have

two inductors compared to the single output inductor of the synchronous buck topology, decreasing both efficiency and power density.

## 3.4 Summary

The power loss and power density models of the synchronous buck and QR-ZCS buck topologies are discussed in detail. In-depth exposition of the synchronous buck switching loss model is performed and analyzed in the context of the power loss model. An analysis of the harmonic content due to inductor current ripple is discussed and a brief analysis of the significance of inductor ACR and capacitor ESR is presented. The QR-ZCS buck operation and power loss model are discussed and the effect of ACR and ESR on the efficiency of this topology are considered.

A survey using a variety of GaN FETs is performed in an effort to compare the conduction losses between the two topologies. This examination reveals that the QR-ZCS topology has a similar estimated power loss in cases where the switching power losses dominate in the synchronous buck. This condition is dependent on the device size and output current. The power loss of the synchronous buck is shown to be less reactive to changes in on-resistance, while the efficiency of the QR-ZCS buck is heavily dependent on the on-resistance of the FETs. Because of the comparative efficiencies presented by preliminary analysis, both converter topologies will be designed by an iterative analysis and implemented using discrete components. After selecting components, a printed circuit board (PCB) is designed and both topologies are evaluated through experimentation.

# Chapter 4 Converter Implementation

A design methodology is established in Chapter 3, and converter implementation will be discussed in this chapter. Beginning with the iterative design of the converter, the power loss and power density models are analyzed and applied to selecting discrete components and implementing a converter design. Passive component selection is discussed and a more precise power loss model is developed based on measurements taken of discrete components. A printed circuit board (PCB) is designed, fabricated, and populated. Non-idealities and parasitic elements of the PCB are simulated and verified to further increase the precision of the power loss model.

## 4.1 Synchronous Buck Component Selection

Once the synchronous buck power loss and volume models are generated and a discrete inductor and FET database is constructed, a simple iterative design method is used to find an optimal design. For this design technique, each FET selection constitutes the selection of both devices in the half-bridge. The specifications given by an “optimal” design is based on application need, customer specifications, or both. The design specifications for this POL prototype converter are outlined by Table 5.

Table 5 POL converter specifications

| | |
|---|---|
| Input Voltage | 5 V |
| Output Voltage | 1.8 V |
| Power Density | > 6 kW/in$^3$ |
| Switching Frequency | > 2 MHz |
| Efficiency | > 97 % |

The power loss model and discrete device database described in Chapter 3 are used to design the synchronous buck converter. Table 6 shows a summary of the design boundary conditions. Because the output power scales linearly with the number of parallel POL modules, the optimization requires that only a single POL module be designed. PCB routing constraints are not included in the power density model and it is assumed that there is a single, complementary half-bridge gate driver per half-bridge. By paralleling several half-bridges per gate driver, the power density is increased, and the efficiency will likely decrease due to an increased overlap time. Therefore, the power density calculated in this design method is only an estimation and may not accurately describe the physical implementation of the POL converter.

First, the number of parallel inductors is selected. A discrete inductor and FET pair are chosen, and the device parameters are used to calculate the power density and efficiency over a range of output currents and switching frequency. At this point in the design, inductor core loss and power loss due to ACR are difficult to estimate. Unless the inductor data sheet includes detailed ACR and core loss data, an accurate estimation of the corresponding power losses is unlikely without measured data from an impedance analyzer and extensive core loss experimental data.

Table 6 Synchronous buck optimization boundaries and operating conditions

| | |
|---|---|
| Number of parallel inductors | 1 - 10 |
| Switching frequency | 2 - 4 MHz |
| Output current | 1-30 A |
| $R_{HS,pull-up}$ | 0 Ω |
| $R_{HS,pull-down}$ | 0 Ω |
| $R_{LS,pull-up}$ | 0 Ω |
| $R_{LS,pull-down}$ | 0 Ω |

Figure 4.1 shows the results of the optimization constrained by the operating conditions outlined in Table 6. Each dot represents a different potential design with an output current, switching frequency, number of parallel inductors, and discrete components. At first glance, it appears that the maximum efficiency of the synchronous buck approaches 97% efficiency. However, given the limited data regarding inductor ACR and quality factor, this power loss is not included, making for an inaccurate estimate of the total converter power losses. Further investigation into the discrete inductor parameters is necessary to create an accurate representation of the power losses in the inductor. It is noted that the synchronous buck converter maintains a relatively high efficiency at high power density. The component volume model, while not considering PCB routing or heat sink volume, is a relative metric, but a design with a power density larger than the specification is chosen to compensate for these unknowns.

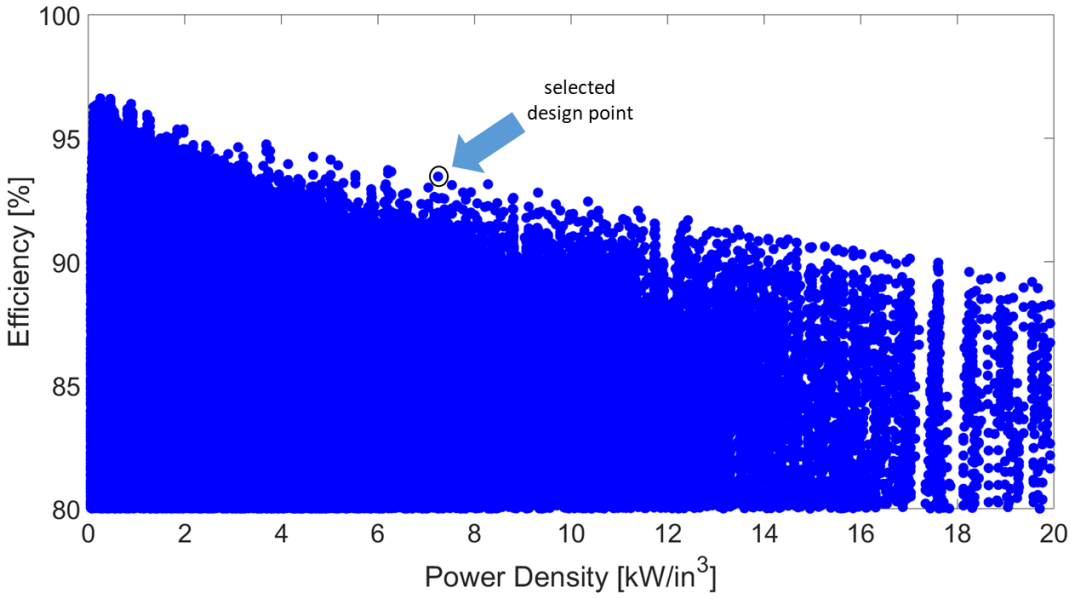


Figure 4.1 Results of synchronous buck optimization

The initial optimization shows that the Vishay IHLP-series inductors provide both high efficiency and power density. Therefore, further analysis is performed on these components to more accurately estimate the power losses. Firstly, plots from the component data sheet are used to estimate the ACR and core loss of the inductor [66]. Figure 4.2 shows the quality factor of the inductor, $Q$, as a function of frequency. Knowing the quality factor of an inductor allows for the calculation of the inductor ACR,

$$ACR_n = \frac{\omega_n \cdot L_n}{Q_n} \,. \tag{76}$$

The ACR is calculated at each harmonic as both the inductance and quality factor of the inductor change as a function of frequency.

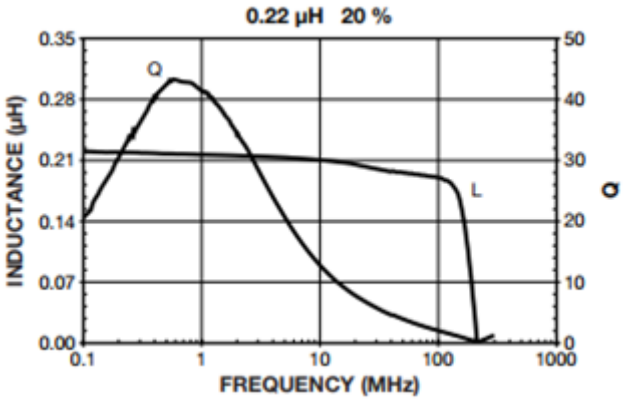


Figure 4.2 IHLP-1616AB 220 nH inductor quality factor and inductance [66]

The core loss is calculated using data provided by the Vishay website [67]. Figure 4.3 shows the core power losses as a function of peak flux density, $B_{pk}$. Knowing the flux density, the estimated core loss, and frequency, the Steinmetz parameters are calculated using the Vishay core loss calculator by a set of linear equations,

$$0.087 = k \cdot 2000000^{\alpha} \cdot 321.4^{\beta}, \tag{77}$$

$$0.282 = k \cdot 2000000^{\alpha} \cdot 571.4^{\beta}, \tag{78}$$

and

$$0.185 = k \cdot 3000000^{\alpha} \cdot 381^{\beta}. \tag{79}$$

The core loss calculator displays the $ET_{100}$ parameter which refers to the amount of energy that the inductor contains corresponding to 100 Gauss. First, the volt-second product, $ET$, is

$$ET = \frac{V_{in} - V_{out}}{f_s} \cdot D \tag{80}$$

The peak flux density,

$$B_{pk} = 100 \cdot \frac{ET}{ET_{100}}, \tag{81}$$

is then calculated using this parameter by (81) and the power loss of the core can then be calculated using (42).

Using the information given by the inductor data sheet, another optimization was performed only considering the IHLP1616AB 220nH inductor. The ACR and core loss of the output inductor are modeled and included in the iterative design approach. The results are shown in Figure 4.4. As shown, the maximum efficiency is slightly above 90%. The peak efficiency occurs around 5 kW/in$^3$ and the maximum power density approaches 25 kW/in$^3$. According to the results of the design method, a single inductor and the EPC2015C device will yield an efficiency greater than 90% with a power density nearing 6 kW/in$^3$. Alternative low-profile, low-DCR inductors are also selected and are listed in Table 7. These inductor data sheets do not provide core loss or ACR information and are not simulated.

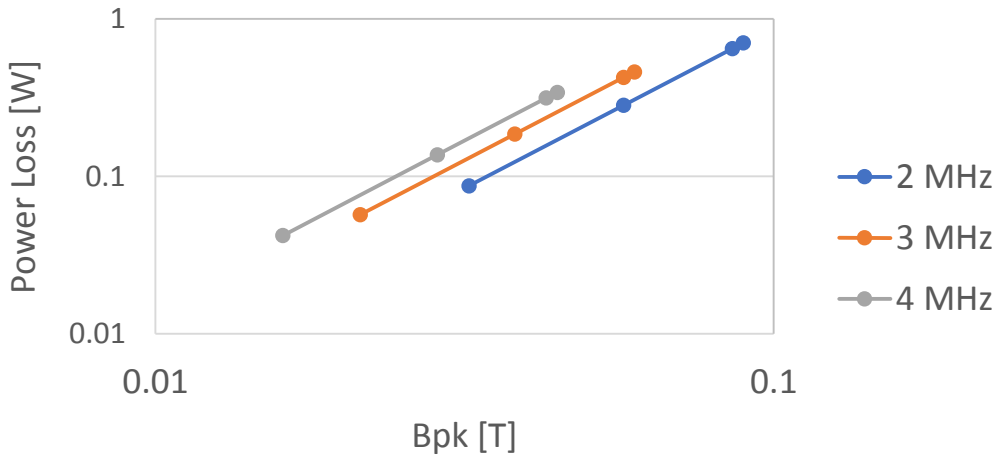


Figure 4.3 Graph of IHLP1616AB 220 nH inductor core loss

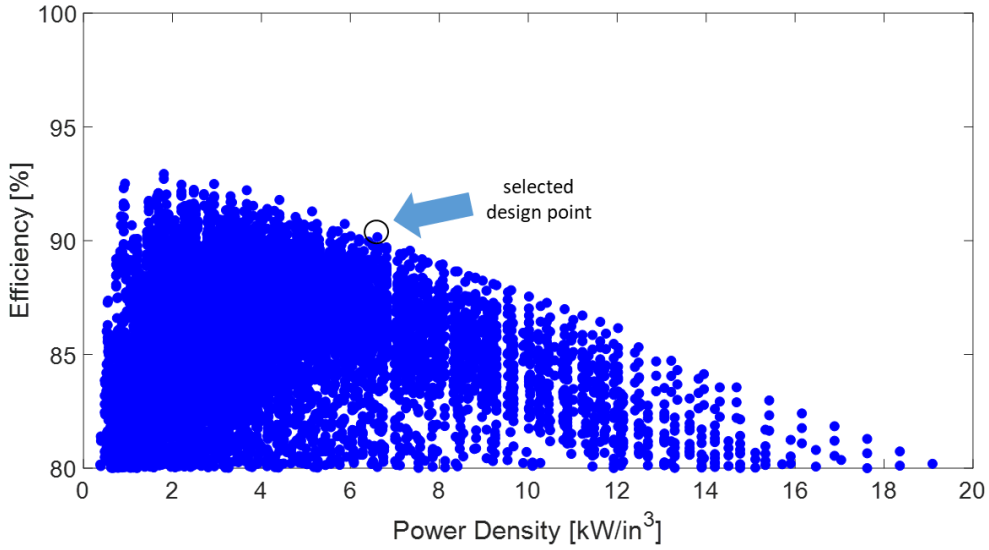


Figure 4.4 Results of synchronous buck optimization with ACR and core losses included

Table 7 Selected inductors for the synchronous buck converter

| Inductor Name | Inductance [nH] | DCR [mΩ] | Footprint [mm$^2$] | Height [mm] |
|---|---|---|---|---|
| IHLP-1616AB-01 | 220 | 9.5 | 19.78 | 1.2 |
| XEL3515-720MEB | 72 | 2.85 | 16.8 | 2 |
| XEL3520-700MEB | 70 | 2.45 | 22.4 | 1.5 |
| SRP4012TA-R10Y | 100 | 4.3 | 18.07 | 1 |
| SRP4012TA-R22M | 220 | 6.6 | 18.07 | 1 |

Table 8 Synchronous buck operating conditions and selected components

| | |
|---|---|
| Input Voltage | 5 V |
| Output Voltage | 1.8 V |
| Output Current | < 10 A |
| Switching Frequency | 2 MHz |
| FET | EPC2015C<br>$R_{on}$ = 3 mΩ |
| Inductor | IHLP1616AB-01<br>$L$ = 220 nH |
| $R_{g,HS\_pull\text{-}up}$ | 2 Ω |
| $R_{g,LS\_pull\text{-}up}$ | 2 Ω |
| $R_{g,LS\_pull\text{-}down}$ | 0 Ω |
| $R_{g,LS\_pull\text{-}up}$ | 0 Ω |

Table 8 describes the synchronous buck prototype operating conditions and the selected components. The power loss model is segmented into the various power loss mechanisms and is shown by Figure 4.5. Its efficiency and power density over an operating range is shown by Figure 4.6. The power loss distribution shows that the inductor contains the most power loss. At full-load operation, 50% of the converter loss is generated by the inductor and the overlap losses are estimated to be 20% of the total losses. At this operating point, an optimistic power density of 7.33 kW/in$^3$ is estimated before considering PCB routing and non-ideal positioning. The synchronous buck converter design is fabricated on a PCB and populated using the components described in Table 8.

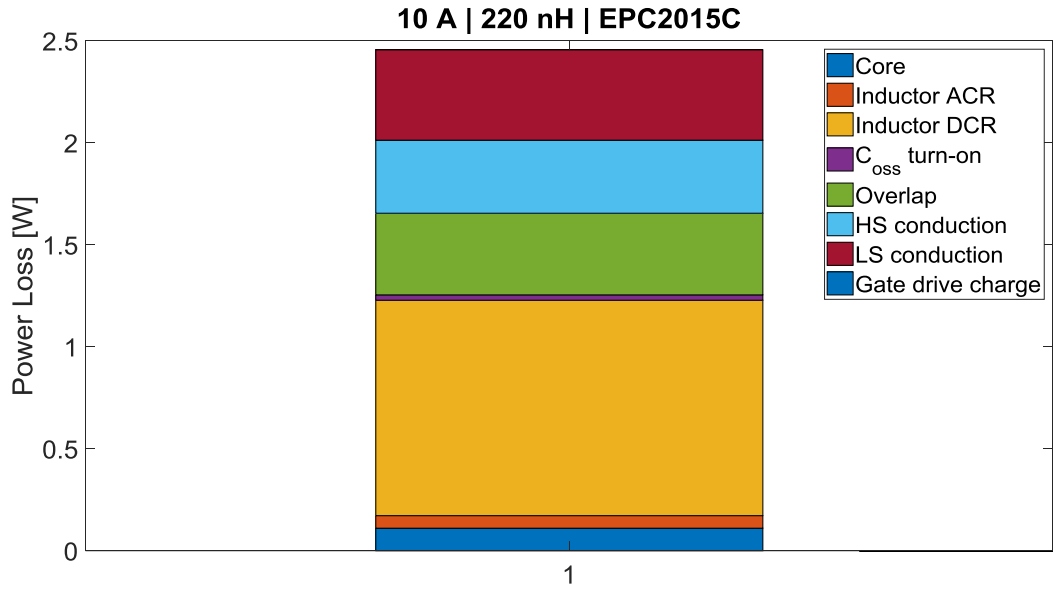


Figure 4.5 Power loss breakdown of synchronous buck design at 10 A output current

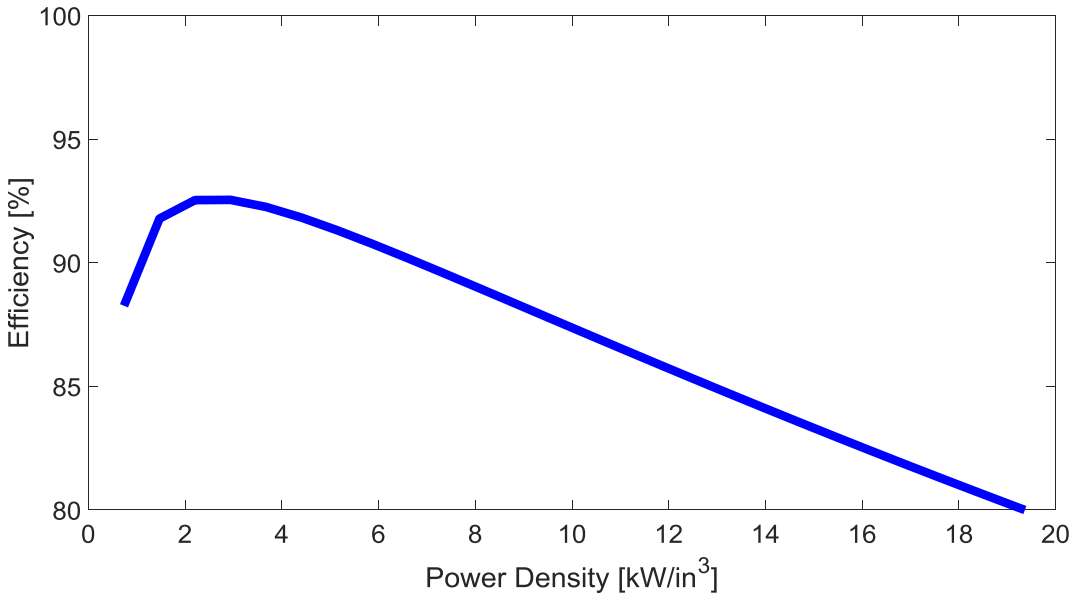


Figure 4.6 Synchronous buck converter simulated efficiency

# 4.2 Synchronous Buck Results

Figure 4.7 shows the prototype board and highlights the relevant components and the power stage dimensions. The total footprint of the power stage is 80.36 $mm^2$ and the inductor height is 1.2 mm. The predicted efficiency and power density is given in Table 9. An image detailing the experimental setup is shown by Figure 4.8. This experiment uses two power supplies, one to supply power to the input of the converter and another to supply power to the gate driver circuit. Two voltmeters are used for measuring the input and output voltage and two ammeters are used for measuring the input and output current. An oscilloscope is used to show the switch-node voltage and the gate drive waveforms.

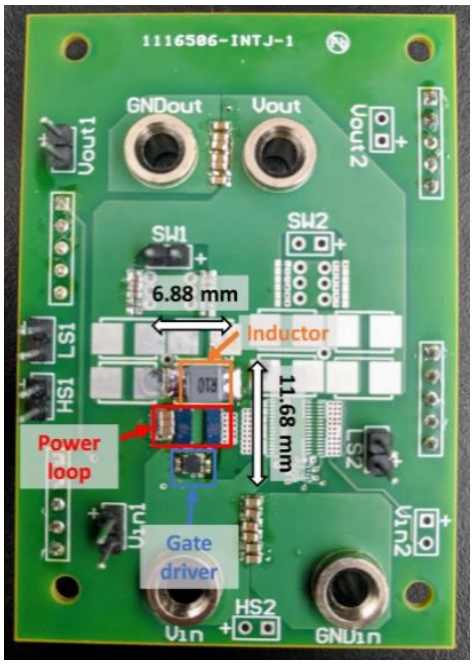


Figure 4.7 Prototype synchronous buck converter with highlighted components

Table 9 Predicted power density and efficiency of synchronous buck converter

| | |
|---|---|
| Efficiency | 89.3 % |
| Power Density | 3.06 kW/in$^3$ |

A Field Programmable Gate Array (FPGA) is used to generate gate drive signals for the switching devices. To compensate the power loss in the converter, the duty cycle is adjusted in open loop to keep the output voltage at 1.8 V as the output current is changed. The optimal dead time changes as a function of current and therefore the dead time is adjusted to maximize efficiency. To implement these adjustments, auxiliary buttons are used to change the duty cycle and dead times between the rising and falling edges of the gate signals, $t_{d1}$ and $t_{d2}$. A diagram demonstrating the FPGA waveforms is shown in Figure 4.9.

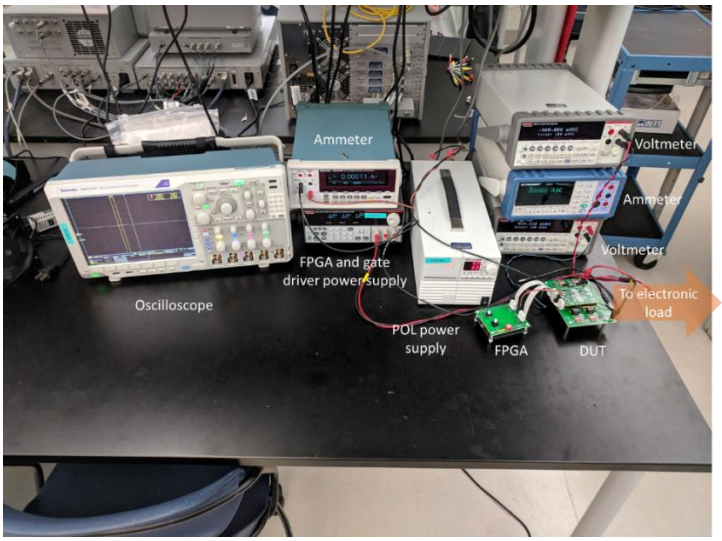


Figure 4.8 Picture of experimental setup

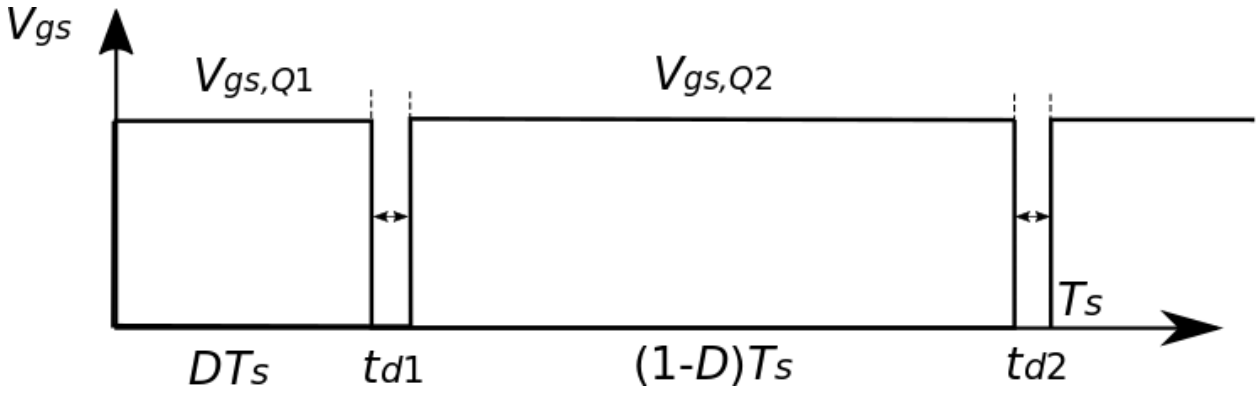


Figure 4.9 FPGA gate signal waveforms

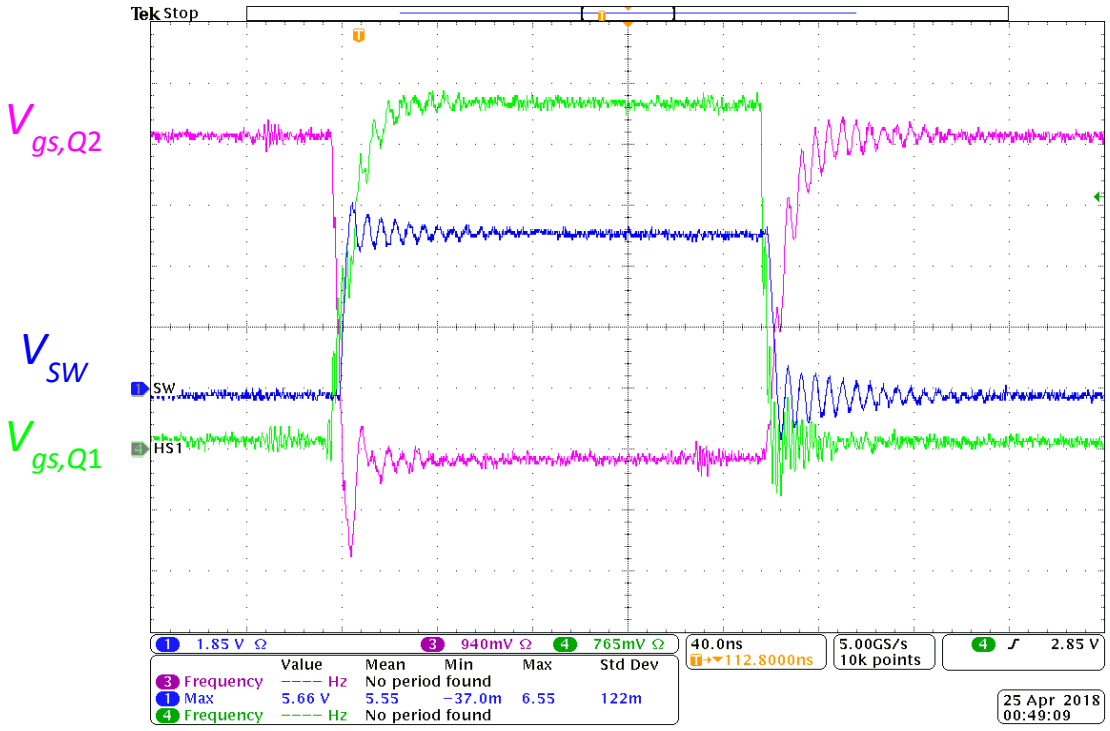


Figure 4.10 Synchronous buck $Q_1$ gate signal (green), $Q_2$ gate signal (pink), and switched-node voltage (blue)

Experimental waveforms of the synchronous buck operating with no load are shown in Figure 4.10. The dead time between the devices is adjusted to minimize reverse conduction losses. When optimizing the time between the gate signals, the external gate resistance can be adjusted, or the gate signals can be changed to increase or decrease the dead time to increase efficiency. Due to the finite resolution provided by the FPGA clock, there is a limited capacity to adjust the dead time. If the dead time decreases so that both devices are on at the same time, cross-conduction will reduce efficiency and potentially damage the circuit. Experimentally, the dead time is adjusted manually to determine the highest efficiency. Figure 4.11 shows the experimental difference between using a tuned dead time and using a fixed dead time. With an adjustable dead time, the converter power loss decreases by 200 mW at 10 A.

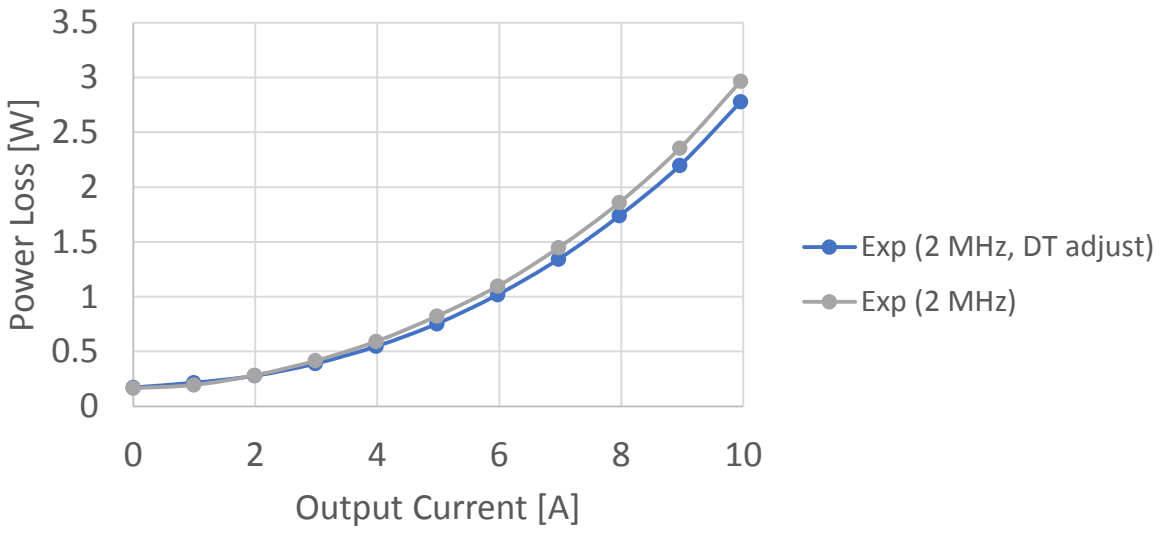


Figure 4.11 Comparison between experimental and simulation results

To improve the power loss model, the trace resistance is measured and added to the current power loss model. Figure 4.12 shows the equivalent circuits of the synchronous buck converter including the PCB trace resistance. A voltage source is connected to the input and a current source is connected to the output. By sending a constant ON signal to the high-side device and constant OFF signal to the low-side device, the total conduction path resistance is measured. Likewise, to measure the low-side conduction path resistance, a voltage source is connected to the output and the power supply current is limited. A constant ON signal is sent to the low-side device and a constant OFF signal is sent to the high-side device. The current through the conduction path and voltage across the inductor and device are used to calculate the total resistance. Table 10 shows the measured device, inductor, and trace resistance.

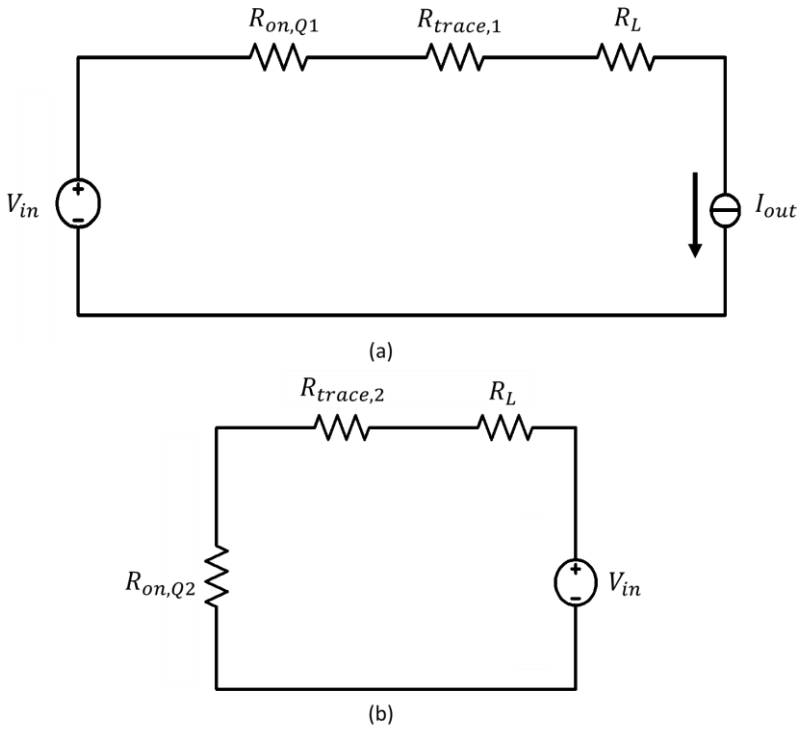


Figure 4.12 Equivalent synchronous buck circuits including trace resistance

Table 10 Measured component and PCB trace resistances

| | |
|---|---|
| $R_{on,Q1}$ | 3.06 $m\Omega$ |
| $R_{on,Q2}$ | 2.87 $m\Omega$ |
| $R_{trace,1}$ | 3 $m\Omega$ |
| $R_{trace,2}$ | 0.5 $m\Omega$ |
| $R_L$ | 5.5 $m\Omega$ |

Calculated results not including the PCB trace resistance predicted a full-load efficiency of 92.5% and a full-load efficiency of 89.3%. After including the measured trace resistance, the peak efficiency is predicted to be 91.2% and the full-load efficiency is estimated to be 87%. The synchronous buck converter is tested up to 10 A with a maximum efficiency of 91.5% and a full-load efficiency of 87%. The comparison of the circuit before and after adding trace resistance is shown in Figure 4.13. The experimental and calculated results are shown by Figure 4.14. The experimental power loss is lower than the calculated model at low current and higher than the calculated power loss at high current. According to the Vishay core loss calculator, the estimated core loss of the IHLP1616AB-01 220 nH inductor is 110 mW. According to the core loss model, these losses are considered to be constant across the operating region and do not account for DC-bias current, likely causing additional inaccuracy across the load range. An additional source of discrepancy is the diode conduction power loss due to the finite FPGA resolution. With increased current, $C_{gd}$ is discharged at a higher speed and the device is turned off more quickly than the 3.3 ns resolution, resulting in reverse conduction.

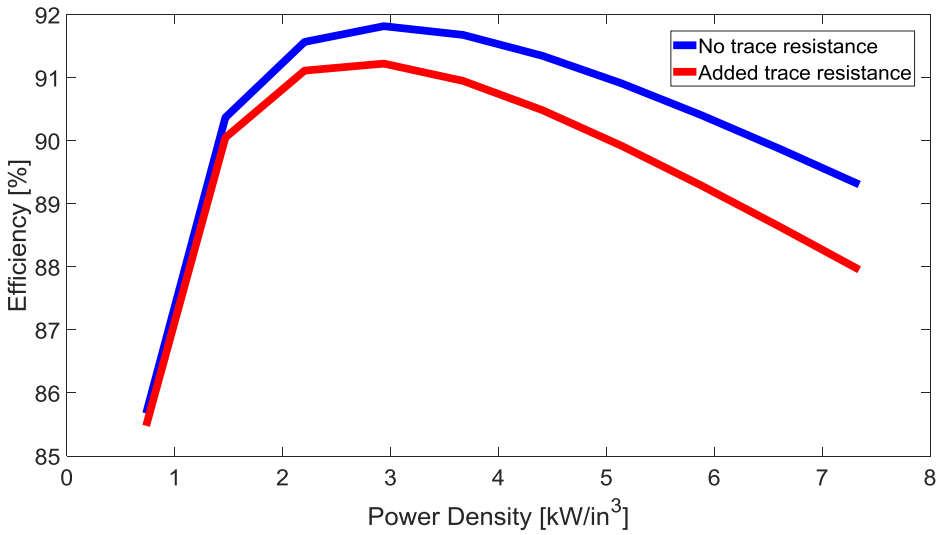


Figure 4.13 Comparison of power loss before and after adding trace resistance

The Vishay inductor is initially selected due to its predicted efficiency and power density as well the availability of a core loss model. The other inductors identified by Table 7 are also tested until converter efficiency drops below 87% and their power loss is shown in Figure 4.15. The XEL3520 has the lowest loss at 10 A, however, the height of this component is 50% greater than the SRP4012TA series. Therefore, the converter power density is greater with the SRP4012TA series as shown in Figure 4.16. Using the SRP4012TA-R10Y, a power density of 4.76 kW/in$^3$ is achieved with 87% efficiency at 23.4 W. The maximum efficiency measured experimentally was nearly 94% at 1 kW/in$^3$ with the SRP4012TA-R22M inductor.

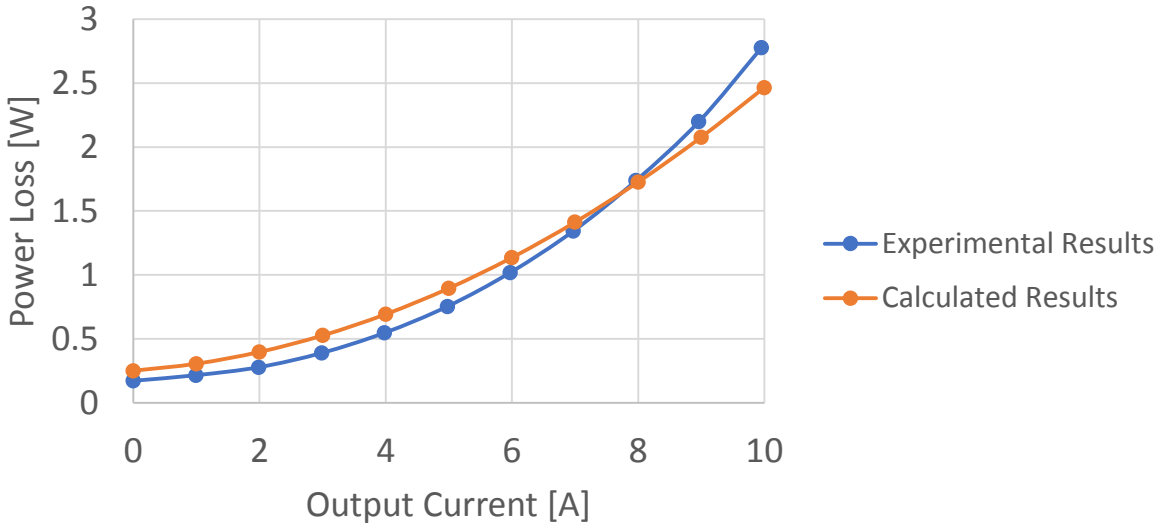


Figure 4.14 Comparison of simulated and experimental power loss using the IHLP-1616AB-01 220 nH inductor

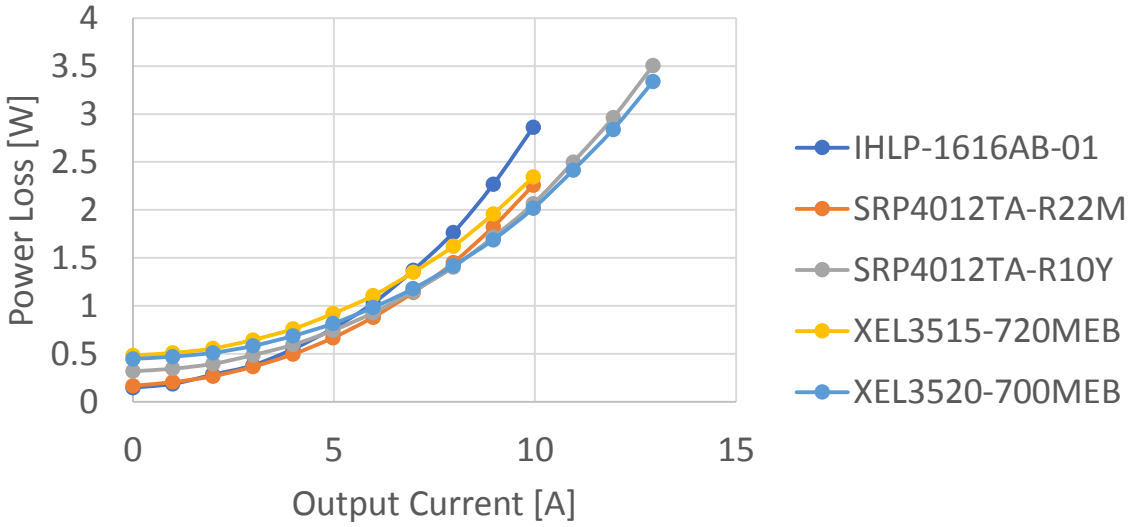


Figure 4.15 Synchronous buck power loss comparing different inductors

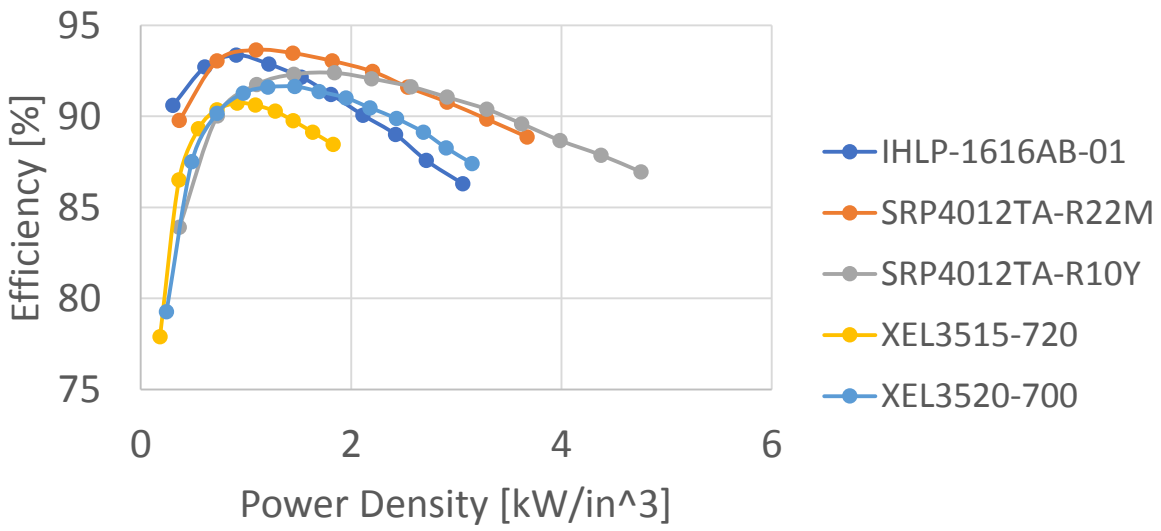


Figure 4.16 Synchronous buck power density vs. efficiency comparison for different inductors

## 4.3 QR-ZCS Buck Component Selection

Like the synchronous buck design, the QR-ZCS design is heavily dependent on the inductor selection. As shown by previous analysis, the efficiency of the QR-ZCS buck converter is greatly impacted by the device and inductor resistance as opposed to the overlap losses. Unlike the synchronous buck converter, the QR-ZCS buck has auxiliary passive components which must be designed for a specific operating point. The resonant component selection is dependent upon the switching frequency and the maximum output current, and therefore the resonant components change as the converter is optimized for different operating currents. At the maximum output power, $J_L$ is designed to be 1, as stated in Section 3.2.1.

In the optimization of the synchronous buck converter, iteration of the discrete filter inductor allows for the calculation of the converter efficiency and power density. Because the

resonant inductor is designed upon the selection of a switching frequency and output current, ACR and core loss from a discrete inductor cannot initially be used to describe the resonant inductor power loss until after the resonant inductor value is calculated and a discrete component is selected. The output inductor and switching devices are selected through this iterative design method, but selection of a discrete resonant inductor will occur after the operating point is chosen. As with the synchronous buck converter optimization, the output current, switching frequency, output inductor, and FETs are iterated, and the power density and efficiency are calculated.

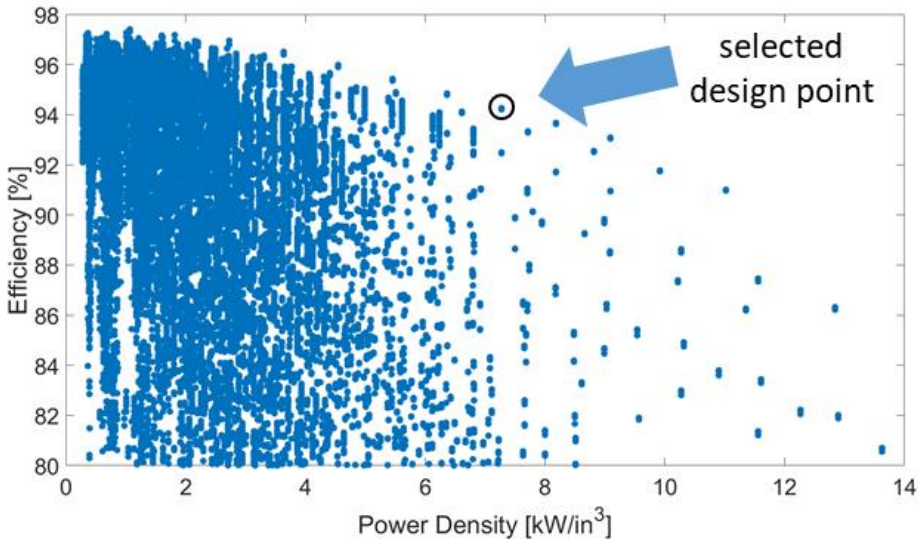


Figure 4.17 QR-ZCS buck optimization results

The same design boundaries are used as shown in Table 6. Figure 4.17 shows the results of the optimization. The EPC2023 device provides the highest efficiency design. While the predicted maximum efficiency is higher than the synchronous buck, the power density at the maximum efficiency is much lower than the synchronous buck converter. The power loss due to the resonant inductor ACR and resonant capacitor ESR are expected to be significant, but the implementation of the resonant components will determine the impact of the frequency-dependent losses. Table 11 shows the operating conditions and resonant component values chosen from the optimization.

Table 11 QR-ZCS operating conditions and components selected

| | |
|---|---|
| Input Voltage | 5 V |
| Output Voltage | 1.8 V |
| Output Current | < 30 A |
| Switching Frequency | 2 MHz |
| FET | EPC2023C<br>$R_{on}$ = 1.3 mΩ |
| Resonant Inductor<br>(3 in parallel) | FP0404<br>$L_r$ = 7.3 nH<br>$R_{Lr}$ = 0.1 $m\Omega$ |
| Resonant Capacitance | $C_r$ = 270 nF |
| Output Inductor | SLC7530<br>$L_f$ = 50 nH<br>$R_{Lf}$ = 0.123 $m\Omega$ |

To implement the 30 A design, a resonant inductance of 7.3 nH and resonant capacitance of 270 nF are needed. The desired inductance value is not readily available, so three parallel 22 nH discrete inductors are used to achieve a resonant inductance of 7.3 nH. The predicted efficiency at full load is near the 97% specification, but the inductor ACR and capacitor ESR are not yet considered. Measurement of the resonant inductor ACR is needed to accurately predict the converter efficiency. Figure 4.18 shows the measured inductance and ACR of a single FP0404 resonant inductor. With the assumption that the inductors are uncoupled and identical, the ACR of the parallel inductors is equivalent to one-third of the measured FP0404 ACR. Using the measured ACR and the resonant inductor current harmonics, the power loss of the inductor is calculated by (37) . Figure 4.19 shows the RMS currents of $C_r$ and $L_r$ at the harmonic frequencies when the converter is operating at full load.


Figure 4.18 Measured inductance and ACR of FP0404 resonant inductor

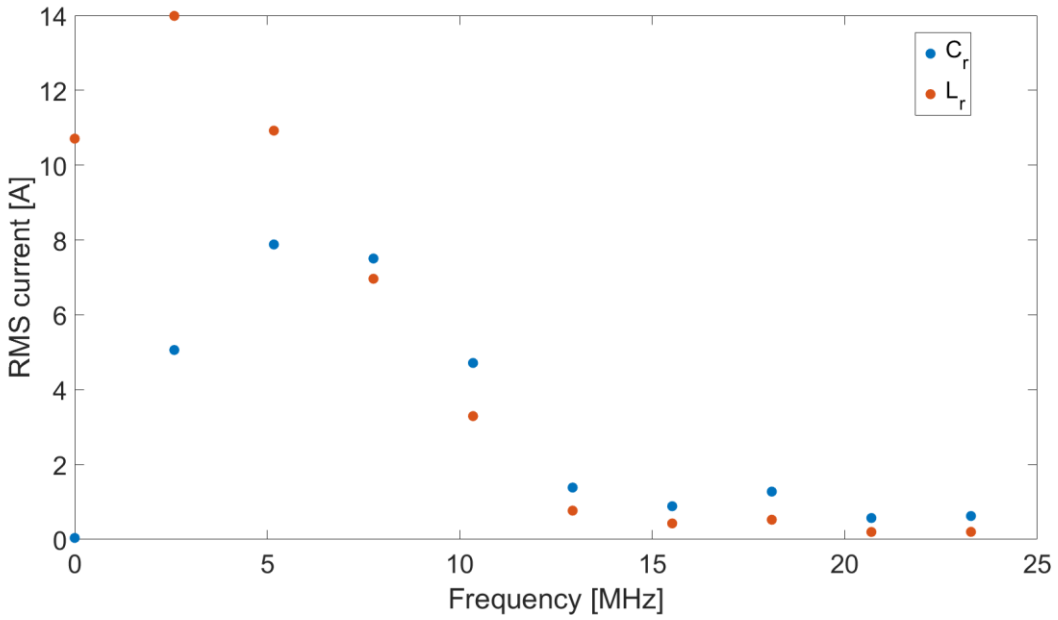


Figure 4.19 RMS of harmonics of $L_r$ and $C_r$ currents

Using this measured ACR, Figure 4.20 shows the power losses of the QR-ZCS buck including the first five harmonic components of the current through the 3 parallel FP0404 resonant inductors. The ACR power losses in the inductor constitute over half of the total power loss. Even without including the input capacitor and resonant capacitor ESR, the predicted efficiency is reduced from 97% to 91.5%.

To improve efficiency of the QR-ZCS buck, the ACR of $L_r$ must be decreased. An air-core inductor made of copper foil is designed with a resonant value of 6 nH using the simulation tool Q3D. Figure 4.21 shows a 3D model of the inductor simulated in finite element analysis (FEA) software and Figure 4.22 shows the results of the air core inductor simulation.

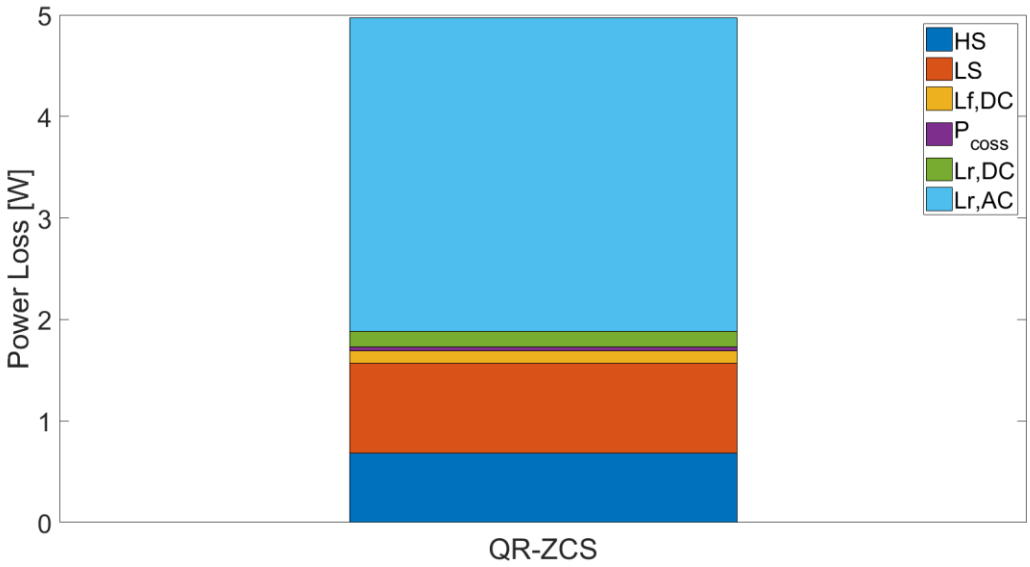


Figure 4.20 Power loss distribution of the QR-ZCS buck operating at 54 W output power

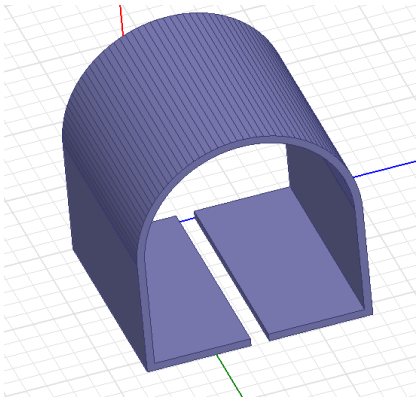

Figure 4.21 3D model of a 6 nH air core inductor from Q3D simulation

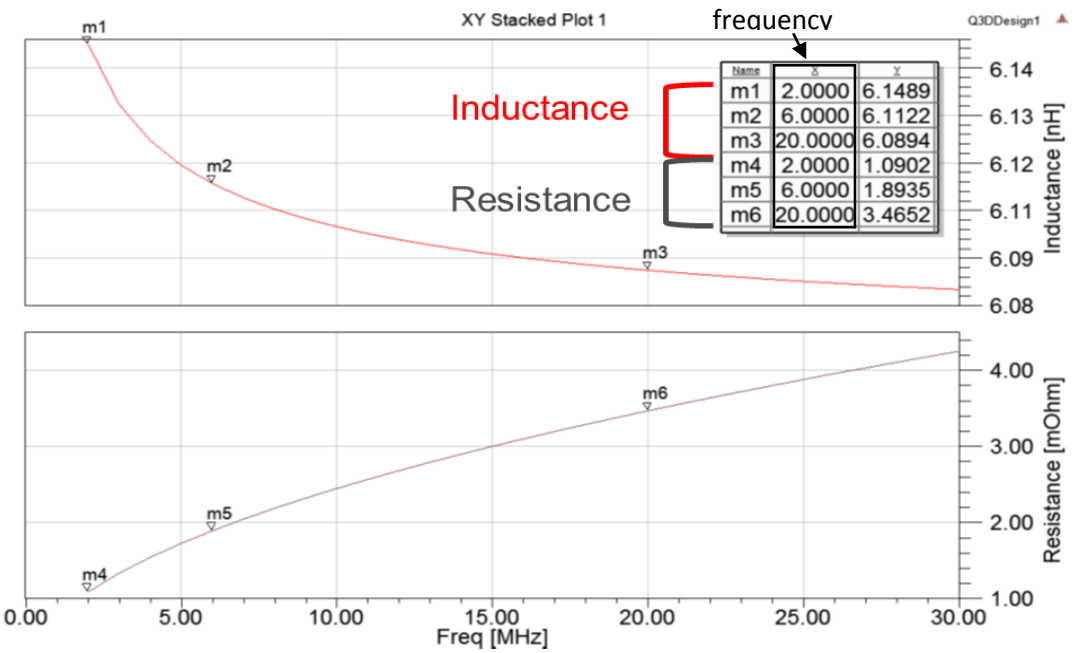


Figure 4.22 Simulation results of 15-mil air core inductor design

An inductance of 6 nH is achieved and the ACR of the resonant inductor is greatly reduced when compared to the discrete inductor. Table 12 shows a summary of the simulation results compared to experimental measurements. The ACR of the air core inductor is measured and shown by Figure 4.24. Significant ACR reduction is achieved at the expense of severely decreasing the converter power density. Figure 4.23 shows the implemented converter with the air-core inductor design.

Table 12 Simulation and measurement results of 6 nH copper foil inductor design

| | Custom inductor | | Discrete inductor |
|---|---|---|---|
| | Simulated | Measured | Measured |
| Inductance | 6 nH | 6.7 nH | 7.3 nH |
| DCR | 0.15 mΩ | 0.3 mΩ | 0.1 mΩ |
| ACR (@ 2 MHz) | 1.9 mΩ | 2 mΩ | 4 mΩ |

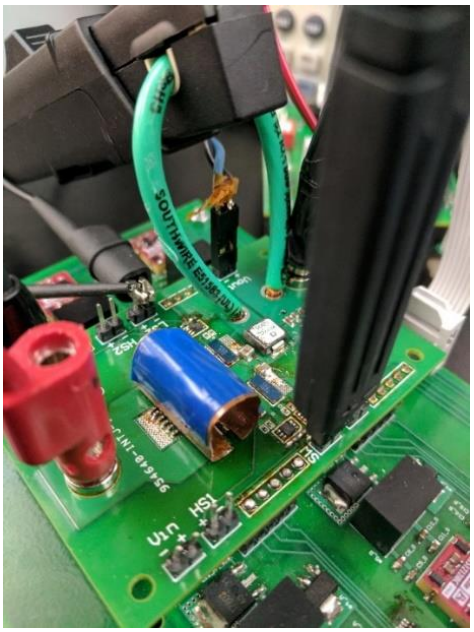

Figure 4.23 Prototype 15-mil, 6 nH air core inductor

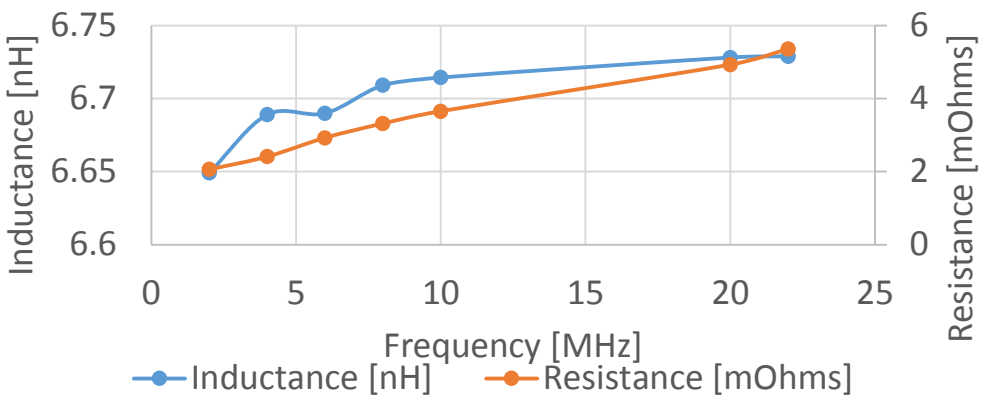


Figure 4.24 Measured inductance and ACR of 15-mil, 6 nH air core inductor prototype

The capacitor selection is non-trivial. In the original prototype, X7R capacitors are selected for the input capacitance and resonant capacitance. However, initial testing verified that the ESR of the capacitors was a significant source of power loss. Figure 4.25 shows a thermal image taken of the prototype QR-ZCS buck converter at no-load operation. In the image, the red reticle is fixated on the point of highest temperature, which in this case highlights the parallel resonant capacitors.

Figure 4.26 shows the ESR of a single 82 nF resonant capacitor. In the original design, a single 82 nF capacitor is in parallel with two 100 nF capacitors to give a total resonance capacitance value of 282 nF. The ESR of the resonant capacitance causes high conduction loss, even at no load, and therefore other dielectric material options are considered. The exploration of low-ESR capacitors introduced the U2J dielectric material. Figure 4.27 shows a comparison between two 100 nF capacitors of different dielectric materials, X7R and U2J. The U2J capacitor ESR is much lower than the X7R capacitor ESR and will have significantly reduced conduction losses.

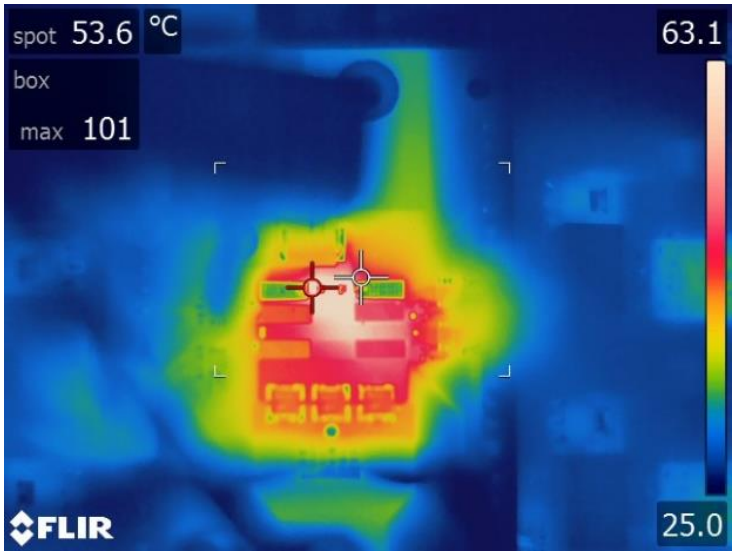


Figure 4.25 Thermal image of QR-ZCS buck converter taken at no-load operation (X7R)

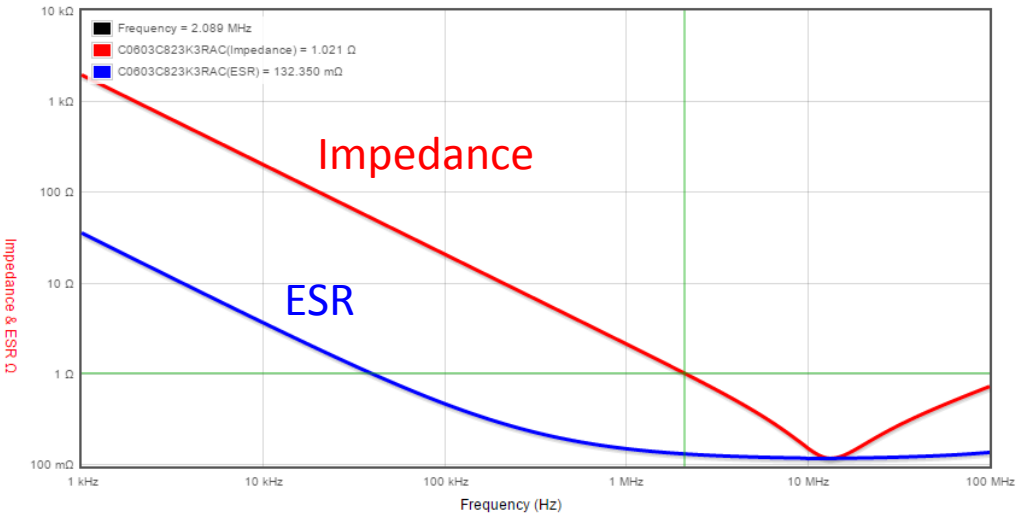


Figure 4.26 KEMET 82 nF X7R capacitor

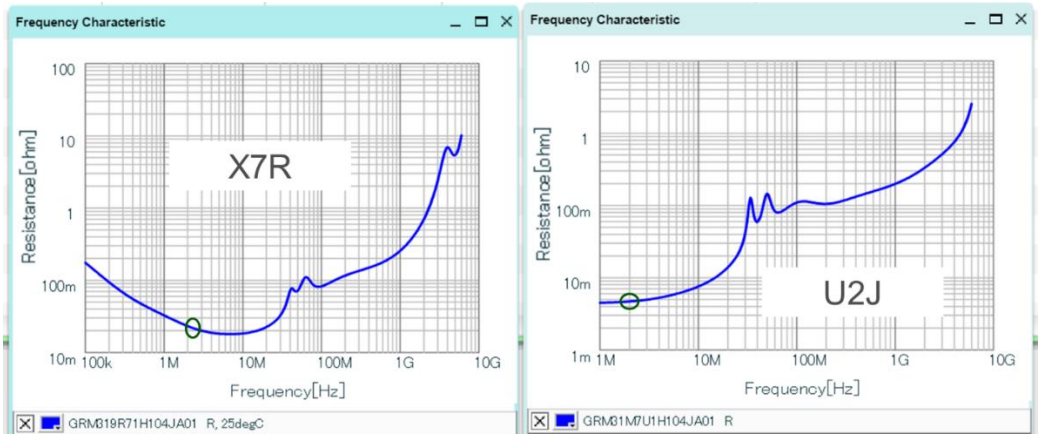


Figure 4.27 Comparison of X7R and U2J capacitor dielectric materials

The high frequency resonant inductor current is not supplied by the input power supply due to parasitic inductance impeding the current path. Instead the input capacitor, $C_{in}$, supplies the resonant current during $t_\beta$. The ESR of the input capacitance must also be taken into account to precisely predict the power losses in the resonant components. Not only does the ESR impact power losses, but the package inductance and ESR of the ceramic capacitors influences the way in which the equivalent value of the parallel capacitors is calculated. Figure 4.28 illustrates how the equivalent impedances of parallel capacitors can be combined into an equivalent impedance,

$$Z_{eq} = \sum_{i=1}^{n} \left( \frac{1}{Z_1} + \cdots \frac{1}{Z_n} \right)^{-1} \tag{82}$$

and equivalent ,capacitance

$$C_{eq} = -\frac{1}{imag(Z_{eq}) \cdot 2\pi \cdot f_s}. \tag{83}$$

The effective voltage ripple across the input capacitors is

$$\Delta v_{in} = \frac{I_{out} \cdot D}{C_{eq} \cdot f_s}. \tag{84}$$

The current through a single capacitor is

$$I_{Cr,1} = I_{Cr} \cdot abs\left( \frac{Z_{Cr,1}}{Z_{eq}} \right), \tag{85}$$

and the power loss is

$$P_{Cr,1} = I_{Cr,1}^2 \cdot real(Z_{Cr,1}). \tag{86}$$

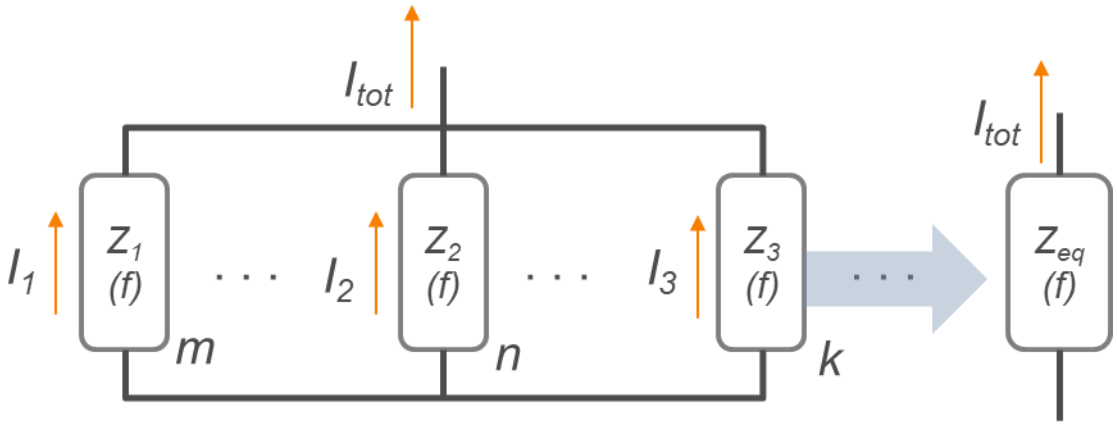


Figure 4.28 Diagram illustrating the equivalent impedance of parallel capacitors

Figure 4.29 shows an example of the power loss distribution between the four parallel capacitors and shows the equivalent resonant capacitance after including the ESR and package inductance. The model assumes two 33 nF U2J capacitors are in parallel with two 47 nF U2J capacitors. By recalculating the input and resonant capacitance and equivalent ESR, the power loss predicted.

Figure 4.30 shows a thermal image of the QR-ZCS buck converter prototype with two 100 nF U2J capacitors replacing the X7R resonant capacitors. The image shows that the reduced ESR results in much lower thermal stress on the resonant capacitors and much lower power loss. Figure 4.31 shows the predicted power loss distribution of the QR-ZCS buck after including the ESR of the two 100 nF and two 47 nF capacitors. Now that the resonant capacitor ESR and inductor ACR are considered and added to the power loss model, the QR-ZCS buck prototype is experimentally tested up to the full-load current.

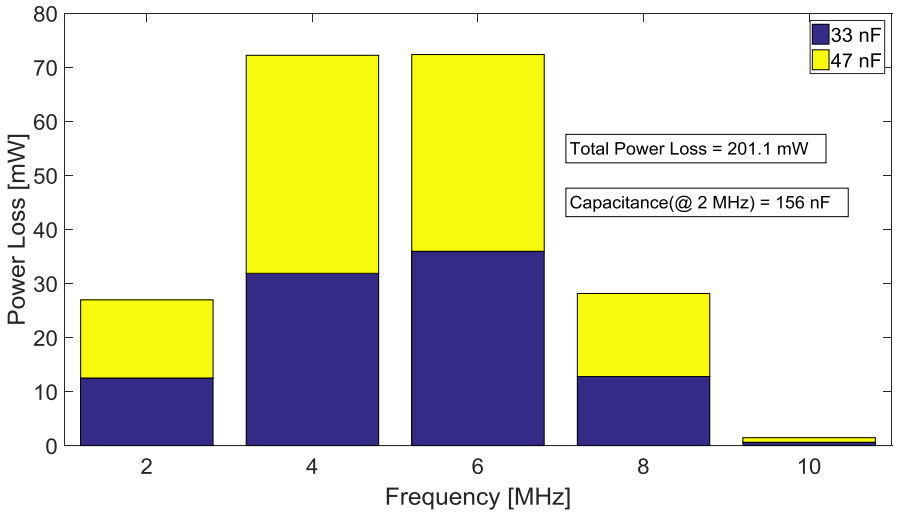


Figure 4.29 Results of the equivalent impedance calculations highlighting the power loss distribution in parallel resonant capacitors

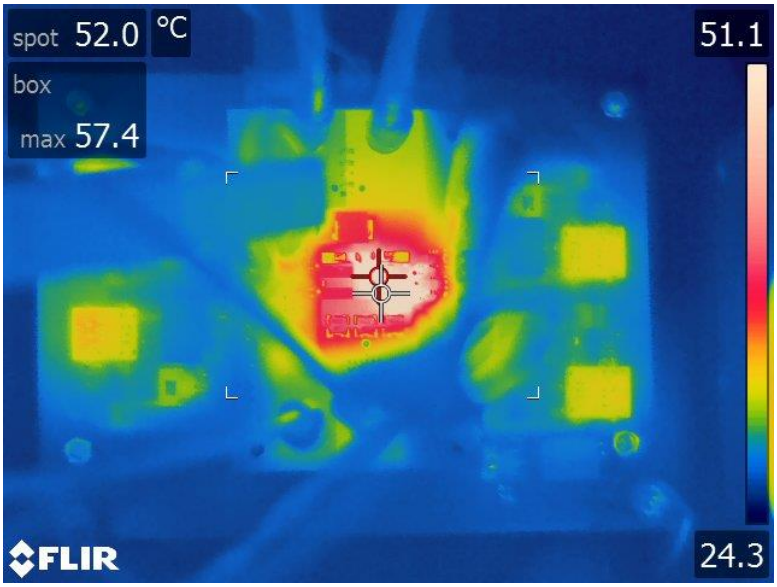


Figure 4.30 Thermal image of QR-ZCS buck converter taken at no-load operation (U2J)

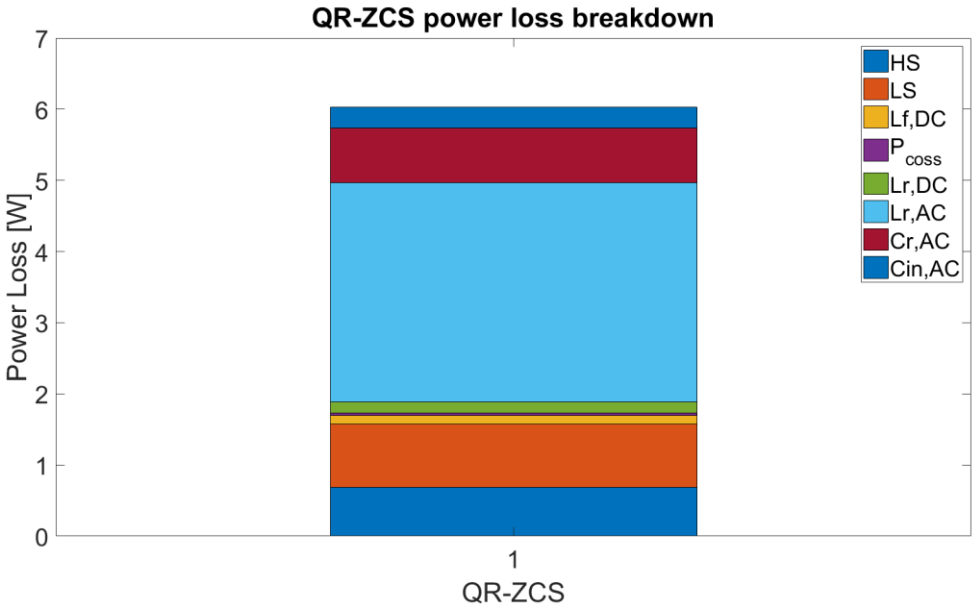


Figure 4.31 Power loss breakdown of the QR-ZCS buck operating at 54 W output power after including capacitor ESR

The power loss distribution illustrates that the AC-dependent losses are over two-thirds of the total power loss. The inclusion of the resonant capacitor and input capacitor ESR losses has increased the overall losses by 1 Watt. The predicted efficiency of the QR-ZCS buck operating at an output current of 30 A is 89.95% as compared to the previous estimation of 91.5%.

# 4.4 QR-ZCS Buck Experimental Results

The same experimental test setup is used as the synchronous buck and is shown in Figure 4.8. The timing signals provided by the FPGA are set initially, then the functional buttons adjust the timing intervals, $t_1, t_\beta, t_3$, and $t_4$ based on the calculated timing. The timing intervals $t_1, t_\beta$, and $t_3$ are adjusted according to the minimization of reverse conduction loss and overlap losses. Time $t_4$ is adjusted to compensate the power loss in the converter. If time $t_4$ is reduced, the volt-

second balance across the output inductor will increase the output voltage. Likewise, increasing time $t_4$ decreases the output voltage. In initial testing, the converter is evaluated up to 15 A until the power loss began to approach 4 W.

The resonant component power losses are included and the measured and simulated power losses are compared for the QR-ZCS buck. Figure 4.32 shows the waveforms of the QR-ZCS buck operating at no-load. Figure 4.33 shows that the simulated and measured efficiencies are similar across the tested range.

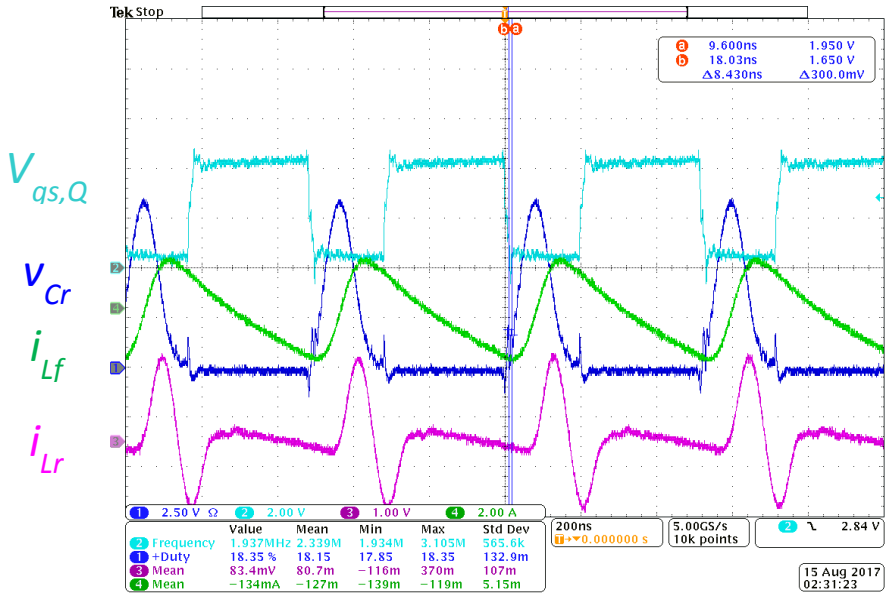


Figure 4.32 QR-ZCS buck converter operating at 2 MHz with no-load; $V_{gs,Q2}$ (cyan), $I_{Lf}$ (green), $V_{sw}$ (blue), and $I_{Lr}$ (pink)

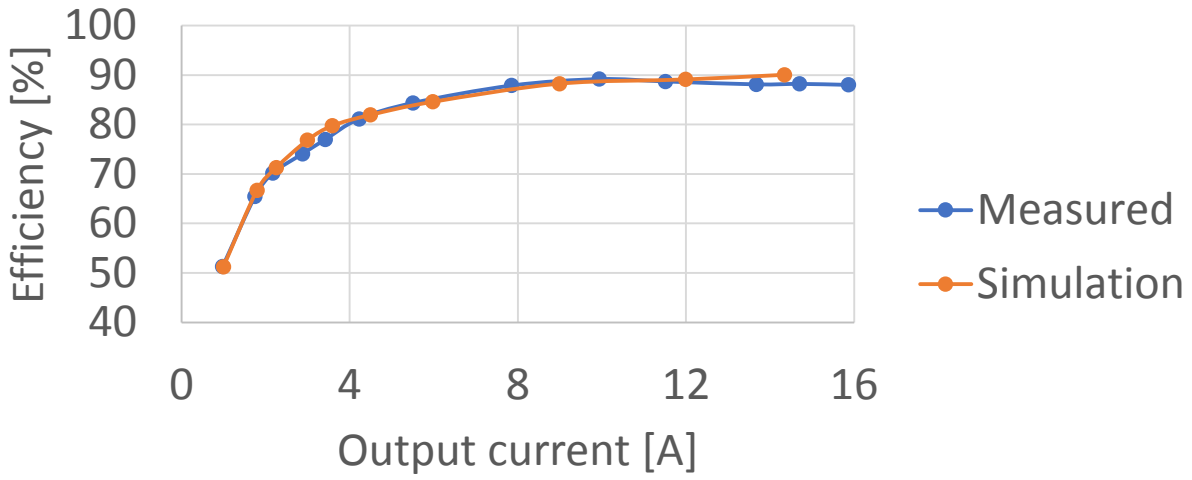


Figure 4.33 Comparison of measured and simulated power loss for the QR-ZCS buck

Although the efficiency does not satisfy the specification, the QR-ZCS buck is tested to the highest designed operating point as shown by Figure 4.34. The maximum efficiency reaches 90% at 25 W and the efficiency at maximum power is 86.4% at 54 W.

A comparison between the synchronous buck and the QR-ZCS buck is completed to evaluate the performance of each in a standardized environment. To investigate the relevant losses for each converter, the output inductance is kept constant for both topologies and the same PCB is used for each. An inductor with large inductance and low DCR is used to isolate loss mechanisms for comparison. The switching frequency is decreased to reduce the resonant component ACR and ESR losses. The switching losses in the synchronous buck are compared to the AC-losses in the QR-ZCS buck and discussed.

Table 13 describes the components used in the 1 MHz QR-ZCS and synchronous buck converters and the experimental operating conditions. For this comparison, the QR-ZCS buck is operating with a maximum current of 10 A, so $I_{base}$ is redesigned to be 13 A rather than 30 A to

reduce unnecessary peak currents. The calculated resonant inductance is 22 nH, and a previously characterized discrete inductor is selected.

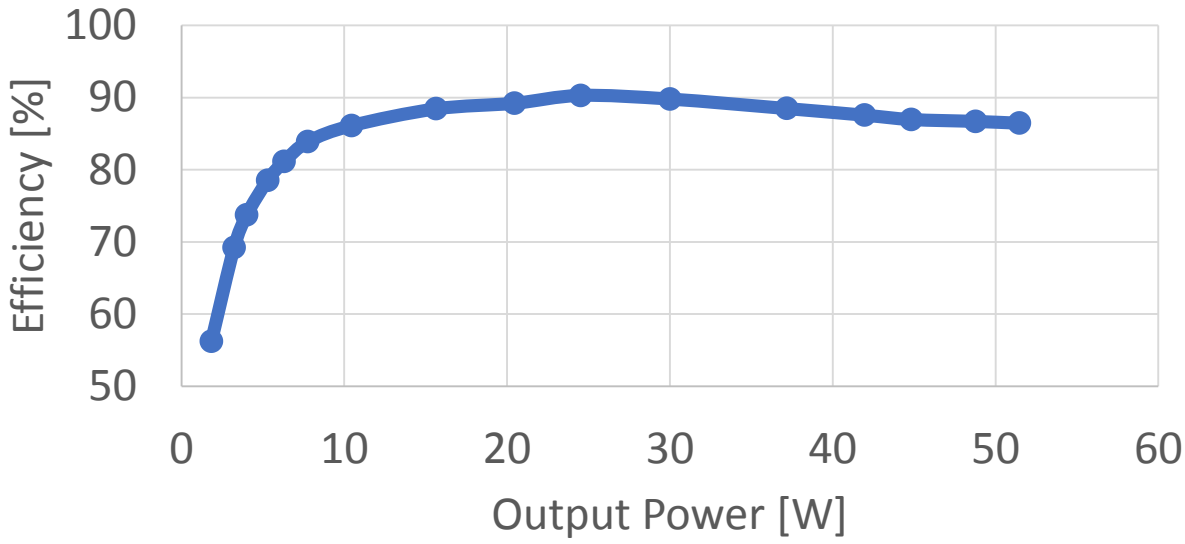


Figure 4.34 Measured efficiency of the QR-ZCS buck up to full-load operation

Table 13 Description of 1 MHz QR-ZCS and synchronous buck converter prototype

| | QR-ZCS buck | Synchronous Buck |
|---|---|---|
| Input Voltage | 5 V | 5 V |
| Output Voltage | 1.8 V | 1.8 V |
| Maximum Output Current | 10 A | 10 A |
| Switching Frequency | 1 MHz | 1 MHz |
| FET | EPC2031<br>$R_{on}$ = 2 mΩ | EPC2031<br>$R_{on}$ = 2 mΩ |
| Resonant Inductor | FP0404<br>$L_r$ = 22 nH<br>$R_{Lr}$ = 0.32 $m\Omega$ | - |
| Resonant Capacitance | $C_r$ = 188 nF | - |
| Output Inductor | Custom toroid<br>$L_f$ = 10 $\mu H$<br>$R_{Lf}$ = 22 $m\Omega$ | Custom toroid<br>$L_f$ = 10 $\mu H$<br>$R_{Lf}$ = 22 $m\Omega$ |

Figure 4.35 shows the QR-ZCS and synchronous buck 1 MHz prototype PCB. The same PCB is used for both topologies, but the trace connecting $V_{in}$ to the decoupling capacitors is cut and the resonant inductor is added to the input when testing the QR-ZCS. First, the synchronous buck converter is tested. The efficiency of the converter is given in Figure 4.36. The simulated losses match the measured efficiency.

New resonant component values are designed to compensate for the lower operating frequency and to decrease the resonant peaks, $I_{base}$ is designed to be 13 A rather than 30 A. The resonant inductor current is $2 \cdot I_{base}$, so by decreasing $I_{base}$, the current peak magnitudes will be smaller. The QR-ZCS buck is tested over the same operating range as the synchronous buck converter and the efficiency is shown in Figure 4.37. The simulated and experimental results

have very similar trends, suggesting that the power loss model is useful for predicting power loss in the QR-ZCS buck.

Figure 4.38 shows a comparison between the QR-ZCS and synchronous buck converters across the same operating range. As shown, the efficiency of the QR-ZCS buck is much lower at low current and remains at a lower efficiency than the synchronous buck throughout the operating range. While the QR-ZCS is shown to have high efficiency at high current operation, the resonant components utilized by the QR-ZCS buck prohibit comparable power density at low current operation. A lower ACR inductor is needed for higher efficiency.

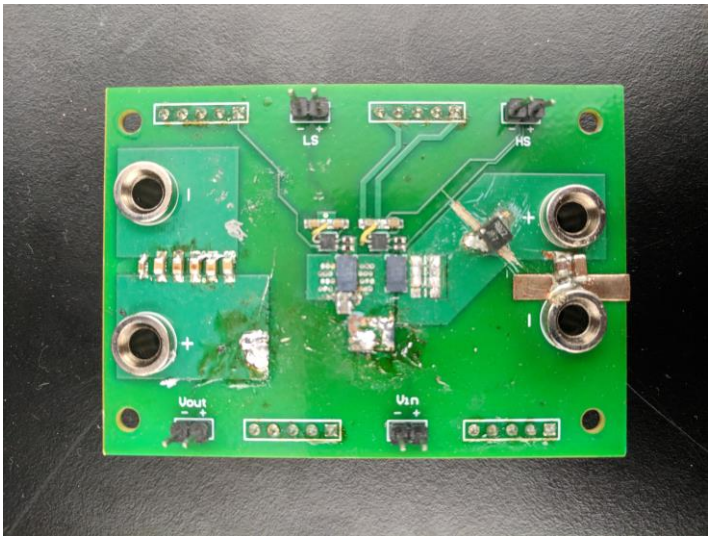


Figure 4.35 QR-ZCS and synchronous buck prototype board

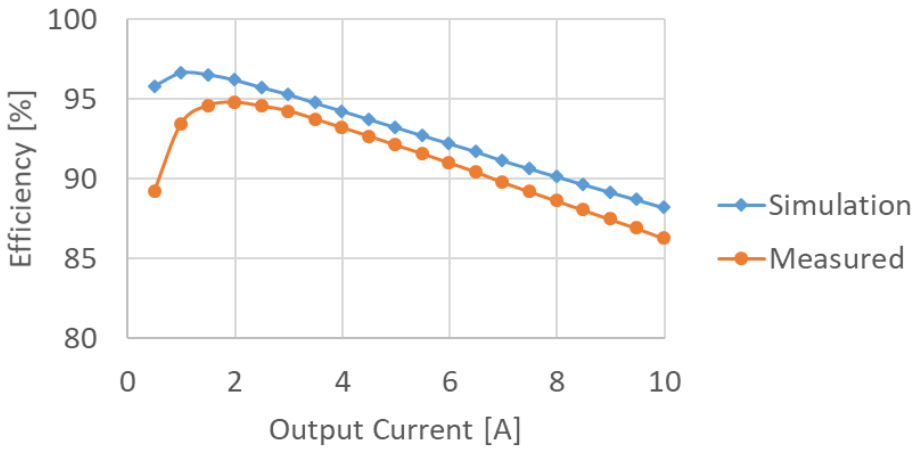


Figure 4.36 Comparison of measured and simulated efficiency of the synchronous buck operating at 1 MHz

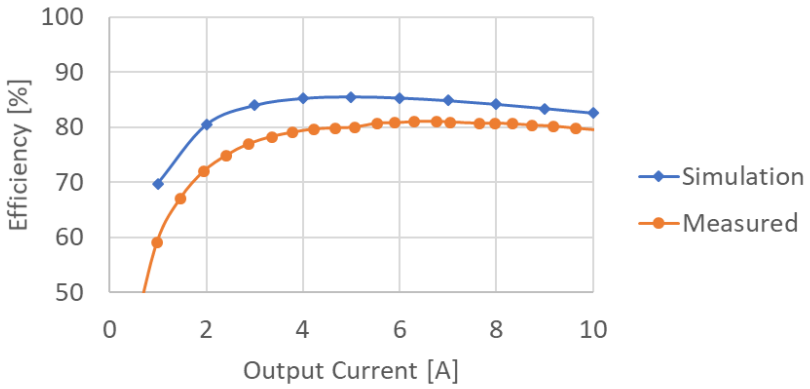


Figure 4.37 1 MHz QR-ZCS buck efficiency

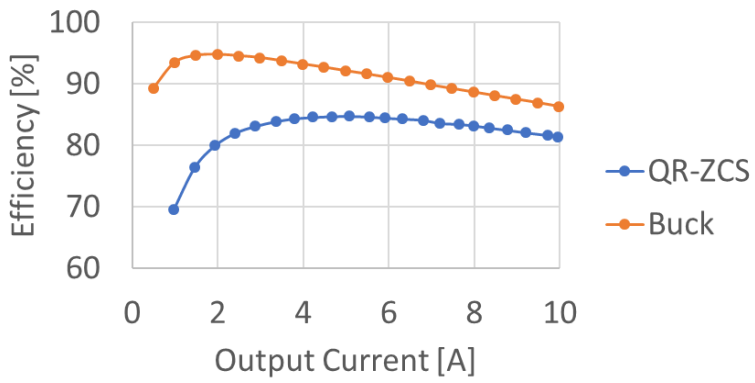


Figure 4.38 Comparison between measured power loss of the QR-ZCS and Synchronous buck converters at 1 MHz

The QR-ZCS buck has much lower efficiency than the synchronous buck across the load range. The power loss model shows that the resonant inductor ACR is a significant power loss mechanism that prohibits high efficiency. The resonant inductor is also increases the QR-ZCS buck volume over the synchronous buck. A custom inductor design may enable high efficiency and high power density. The requirements of the resonant inductor are discussed.

## 4.5 Analytical comparison of QR-ZCS and synchronous buck

An analytical comparison between the QR-ZCS buck and synchronous buck is performed to evaluate the trade-offs associated with each topology and to understand the operating conditions in which each topology excels. To compare the two topologies, the previously constructed power loss models are used to first predict the efficiency of each topology across a range of operating conditions. The power loss models are compared in Table 14.

Table 14 Comparison of the QR-ZCS and synchronous buck power loss models

| Synchronous buck | | QR-ZCS buck |
|---|---|---|
| $Q_1$ conduction | < | $Q_1$ conduction |
| $Q_2$ conduction | < | $Q_2$ conduction |
| $L_f$ conduction | = | $L_f$ conduction |
| $C_{oss}$ | = | $C_{oss}$ |
| $Q_g$ | = | $Q_g$ |
| Overlap | > | - |
| - | < | $L_r$ DCR conduction |
| - | < | $L_r$ ACR conduction |
| - | < | $C_r$ ESR |

Some losses are present in both topologies, such as $Q_1$ and $Q_2$ conduction losses. The current through these devices are different at the same operating point and therefore these power loss mechanisms will have different values. The $C_{oss}$ and $Q_g$ power losses are the same between the two topologies and so these losses are neglected in the efficiency comparison. The output inductor current is approximately the same between the two topologies and so the conduction loss and core losses of $L_f$ are also not included in the power loss calculations. The resonant capacitor ESR loss is much lower than the resonant inductor loss and is difficult to estimate without discrete devices. Therefore, it is neglected for this comparison.

The resonant inductor ACR and DCR conduction losses are not included in this power loss model because these power loss mechanisms are based on the component's physical implementation. The volume is also not considered. An efficiency target, $\eta_{set}$, is chosen, $I_L$ and $J_L$

are iterated, and the efficiency and power density for both topologies are calculated. This iteration assumes that the resonant inductor is a lossless component with zero-volume, allowing for all volume and power loss to be attributed to the resonant inductor. The topologies are compared at the target efficiency. By calculating the efficiency and power density for each topology under varying operating conditions, a resonant inductor design space describing the inductance, resistance, and volume of the resonant inductor is derived. The design parameters are shown in Table 15.

The results of this design iteration are shown in Figure 4.39. $I_{Buck}$ denotes the highest output current at which the synchronous buck converter can operate while meeting the efficiency specification, $\eta_{set}$. Likewise, $I_{QRZCS}$ denotes the highest operating current at which the QR-ZCS buck can operate while maintaining $\eta_{set}$. In this example, the QR-ZCS buck can operate at much higher current while maintaining the same efficiency. Using this information, a design space for the resonant inductor is constructed and utilized to describe the necessary resistance and volume to have a higher efficiency and power density than the synchronous buck.

Table 15 Circuit parameters and operating conditions used in comparative analysis

| | |
|---|---|
| $V_{in}$ | 5 V |
| $V_{out}$ | 1.8 V |
| $f_s$ | 5 MHz |
| $\eta_{set}$ | 92.5 % |
| $L_f$ | 100 nH |
| $I_{out}$ | 5 – 100 A |
| $J_L$ | 0.1 – 0.99 |
| $Q_1$ & $Q_2$ | EPC2023 |

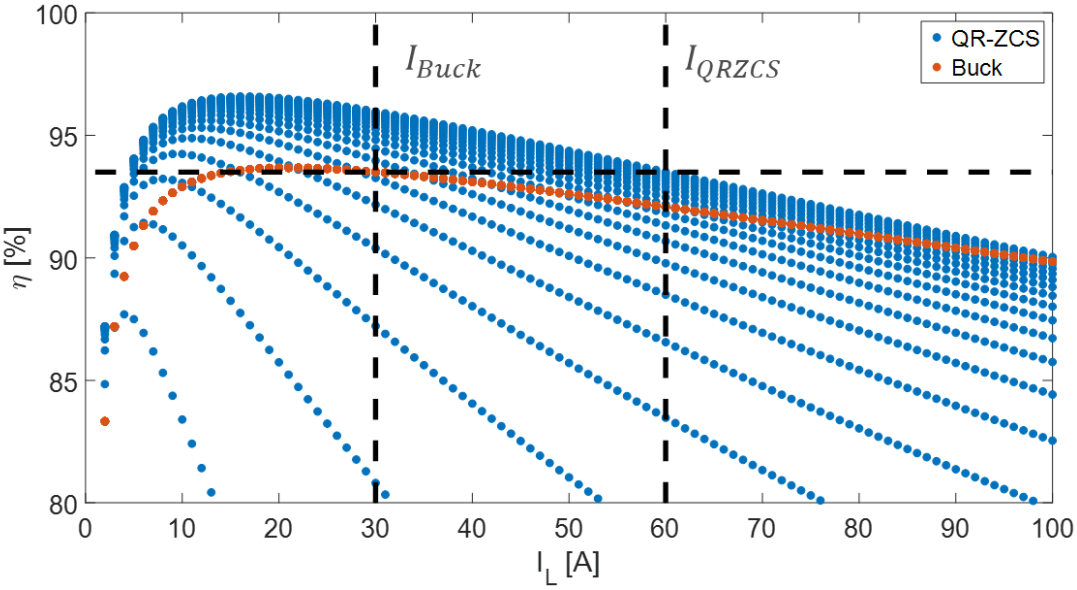


Figure 4.39 Efficiency comparison of the QR-ZCS buck and synchronous buck

The difference in power loss

$$P_{diff} = P_{sync} - P_{QRZCS}, \tag{87}$$

and resonant inductor current DC component and harmonics are used to calculate an equivalent resistance of the inductor,

$$R_{Lr,eq} = \frac{P_{diff}}{I_{rms,Lr}^2 + \left(I_{rms,Lr_{AC1}}^2 + \cdots I_{rms,Lr_{ACn}}^2\right)}. \tag{88}$$

The estimated volume of the synchronous buck, $V_{sync}$, is used to calculate the volume of the resonant inductor

$$V_{Lr} = \frac{I_{QRZCS}}{I_{buck}} \cdot V_{sync} - V_{sync}. \tag{89}$$

Figure 4.40 shows the constructed resonant inductor design space. After a resonant inductance value is chosen, a custom resonant inductor with an equivalent resistance and volume with the parameters shown will result in a QR-ZCS buck design with higher efficiency and power density than any synchronous buck designed at the chosen switching frequency and efficiency target. This methodology can be extended to any switching frequency or device for the construction of many resonant inductor design spaces.

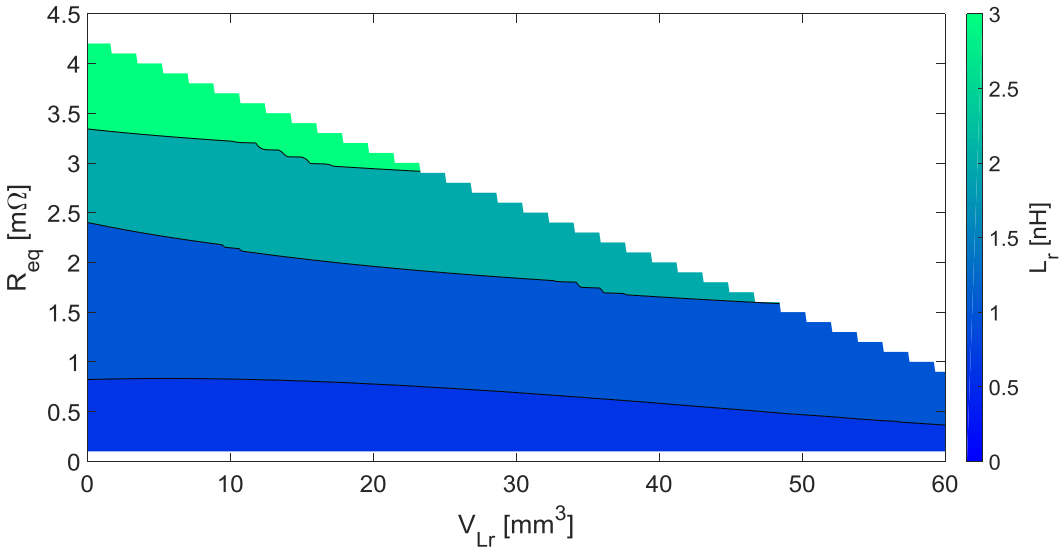


Figure 4.40 Contour plot of the resonant inductor design space

## 4.6 Summary

Design techniques for the synchronous buck and QR-ZCS buck are described and implemented using discrete components. A high-density synchronous buck converter is designed on a PCB and non-idealities such as trace resistance and dead-time losses are identified through experimentation. The trace resistance is measured and the respective conduction losses are added to the power loss model. The dead-time between FET switching transitions can be adjusted to maximize efficiency, allowing for improved accuracy of the power loss model. A maximum power density of 4.76 kW/in$^3$ is achieved with an efficiency of 87%. A peak efficiency of 94% is achieved at a power density of 1 kW/in$^3$, comparable to current high-efficiency POL designs.

A QR-ZCS buck converter is designed and a prototype is tested up to 54 W output power. A model describing the current harmonics through energy storage elements is constructed and verified through experimental results. In addition, the ACR of the resonant inductor is measured and the ESR of the resonant and input capacitors is taken from the data sheet and added to the power loss model. The trend of the simulated model correlates closely with the experimental results QR-ZCS buck at both 2 MHz and 1 MHz switching frequency. A maximum efficiency of 90% is achieved at 25 W and a full-load efficiency of 86.4% is attained at a switching frequency of 2 MHz.

The QR-ZCS buck and synchronous buck are compared using the same PCB layout, output inductor, and operating conditions. Across a low current operating range, the synchronous buck converter has lower power loss than the QR-ZCS buck converter. The passive components are shown to significantly impact the converter efficiency. The volume of the QR-ZCS buck is much larger than the synchronous buck due to inclusion of the resonant components and therefore the power density of the QR-ZCS buck is lower than that of the synchronous buck. To achieve a

comparable power density with the QR-ZCS buck, the output power must be greatly increased, and the resonant inductor must be designed to withstand the high resonant current peaks without saturating. Furthermore, the power losses associated with these high resonant currents will inhibit high-efficiency operation at high current. The design of a custom air-core inductor increases the efficiency of the QR-ZCS buck at the expense of increased volume. In both topologies, the discrete magnetic components produce the majority of the power loss.

A generalized analysis is performed to compare the two topologies across a wide range of operating conditions. By setting an efficiency target, a design space of resonant inductor requirements is constructed. Using this design space, the efficiency and power density of the QR-ZCS buck is evaluated and compared to the synchronous buck.

# Chapter 5 Conclusions and Future Work

## 5.1 Overview

POL converters are used to deliver high currents to server CPUs within a data center. These high currents are synonymous with high conduction losses and overlap losses, causing low efficiency in high power POL converters. New hyperscale data center architectures focus on the density of computing power, increasing the demand for high power density converters. To improve the power density, the discrete component size must be reduced and higher current operation made possible. In the case of POL converters, magnetic components occupy a substantial amount of space and often inhibit high efficiency. One way to reduce magnetic component volume is to increase switching frequency; for a given current ripple, an increase in switching frequency facilitates a proportional reduction in inductance. However, an increase in switching frequency is indicative of higher gate drive and switching power losses.

Recent developments in low-voltage GaN HEMTs leverage the material properties of GaN to reduce component volume while simultaneously decreasing device capacitances and channel resistance. The use of GaN in POL converters is demonstrated in previous work and is shown to improve efficiency and increase power density. Simply using GaN instead of Silicon has the potential to increase converter power density. However, research reveals that switching losses are still shown to be a noteworthy loss component at high current. If switching losses are indeed the most substantial loss mechanism, higher frequency operation is not suitable for use in the synchronous buck topology. Therefore, soft-switching topologies are utilized to reduce these power losses at the cost of conduction losses and power density. The introduction of soft-switching topologies is not new in POL applications, but the analysis of zero-current-switching

topologies and comparison to the synchronous buck topology is not explored in detail in literature. Low component count and high efficiency predicted warrants investigation into the QR-ZCS buck converter.

## 5.2 Conclusions

Analysis shown in this thesis reveals that the use of low-voltage GaN devices provides high efficiency and shows that overlap losses are much lower than the inductor conduction losses. High power density is achievable through the use of GaN HEMTs and low-profile inductors, but power loss in the filter inductor and resonant inductor far surpass the conduction losses and overlap losses in the switching devices. The optimization of the converter operating point and the selection of discrete components is a limited device characterization.

A high power density of 4.76 kW/in$^3$ is achieved with a synchronous buck converter using discrete components. Low-profile, low-DCR inductors are utilized to reduce the converter footprint and improve converter efficiency beyond some integrated inductor solutions. However, the power loss distribution shows that 50% of total loss is due to inductor core and conduction loss. The available pool of discrete inductors does not provide high efficiency at high current operating conditions.

In the QR-ZCS buck, overlap losses become negligible and the vast majority of power loss is generated by the AC-resistance of the resonant inductor. Through the design of a custom air-core inductor, the power loss in the resonant inductor is decreased substantially at the expense of increased converter volume. Still, the QR-ZCS buck is plagued by high peak currents, causing power losses in the resonant inductor ACR and capacitor ESR as well as current stress in the high-side FET. The work presented in this thesis demonstrates that the QR-ZCS buck is a viable

option for low-voltage, high-current converters if high *Q* inductors are available. Efficiency of 86.4% is shown at 30 A output current.

Generation of discrete waveforms in simulation software allows for precise signal timing and enables the evaluation of frequency-dependent losses. A model to describe the inductor ACR and capacitor ESR power losses is described in detail and is validated through comparison with experimental results. The effect of capacitor package inductance and ESR is included into the calculation of effective capacitance and capacitor voltage ripple. This model improves the accuracy of power losses due to input capacitor and resonant capacitor ESR and effectively predicts the equivalent impedance of paralleled capacitors.

A methodology is developed to compare the QR-ZCS buck and synchronous buck across a range of operating conditions. This analysis shows a design space in which the QR-ZCS buck has a competitive efficiency and power density to the synchronous buck.

## 5.3 Future Work

Improvements to the resonant and filter inductors are required for further increasing efficiency and power density. Therefore, custom magnetic designs and new topologies addressing these issues are suggested to be considered for future work.

### 5.3.1 Fully-Resonant Zero-Current-Switching (FR-ZCS) Buck Topology

The ACR of the resonant inductor and the high-frequency harmonics of the resonant inductor current generate the majority of the power loss in the QR-ZCS buck converter. Ideally, the ACR of the inductor could be reduced significantly and the high-frequency harmonics can be reduced or made negligible. A new topology which attempts to reduce the high-frequency

harmonic content is introduced. The topology, shown in Figure 5.1, aims to present a single resonant frequency to the resonant inductor by interleaving multiple phases of the QR-ZCS buck converter.

The advantages of the FR-ZCS are three-fold: (1) the utilization of a single resonant inductor for multiple phases of the QR-ZCS buck topology allows for an increased power density; (2) the near single-frequency current through the resonant inductor reduces the harmonic content and reduces power losses in the resonant inductor; and (3) the equivalent switching frequency of the topology is multiplied by the number of phases, reducing the switching frequency of each phase and increasing control bandwidth.

Figure 5.2 shows the equivalent circuit of the four sub-stages and Figure 5.3 shows the resonant component waveforms. To achieve a single-frequency current through the resonant inductor, the switch timing and input voltage are adjusted to compensate for the voltage conversion and number of phases.

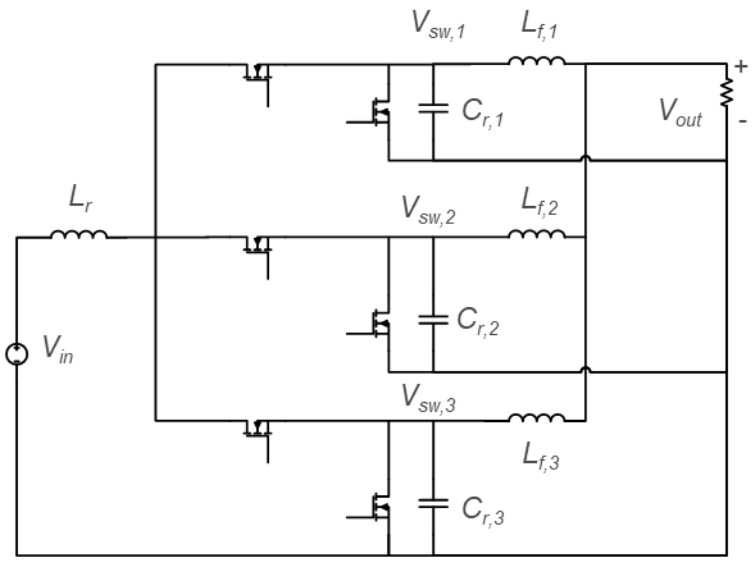


Figure 5.1 FR-ZCS buck converter schematic

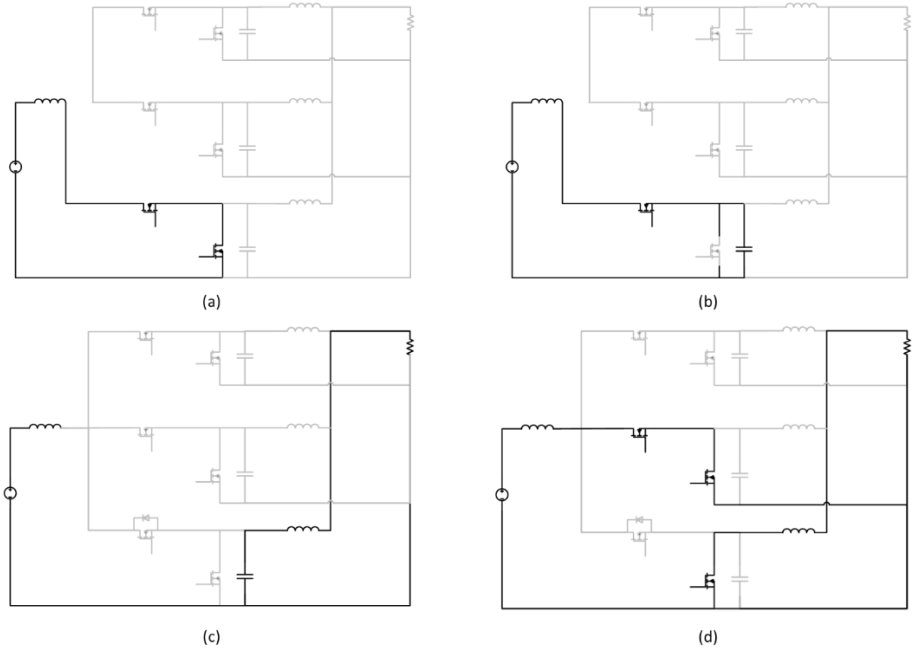


Figure 5.2 Equivalent circuit substages: substage 1(a), substage 2 (b), substage 3 (c), and substage 4 (d)

For a 5.4-1.8 *V* conversion ratio, three phases are needed. Using the equations outlined for the QR-ZCS buck, $t_1$, $t_2$, and $t_3$ are calculated and

$$T_s = t_1 + t_2 + t_3 + t_4. \tag{90}$$

The switching period also is also a function of the number of parallel phases *n*:

$$T_s = n \cdot (t_1 + t_2 + t_3) \tag{91}$$

$T_s$ is now in terms of $t_1$, $t_2$, and $t_3$:

$$T_s = t_1 + t_2 + t_3 + (n-1) \cdot t_1 + (n-1) \cdot t_2 + (n-1) \cdot t_3 \tag{92}$$

Simulation waveforms of the FR-ZCS converter operating at 48 A output current are shown in Figure 5.4. The FFT of the resonant current shows the near single-frequency operation desired. Note that each of the three phases has an output current of 16 A and a total output current of 48 A. For steep step-down conversion ratios, a resonant inductor with a small inductance and high quality factor would be required, but investigation into the benefit of this topology is needed to understand the design trade-offs at varying current levels and frequencies.

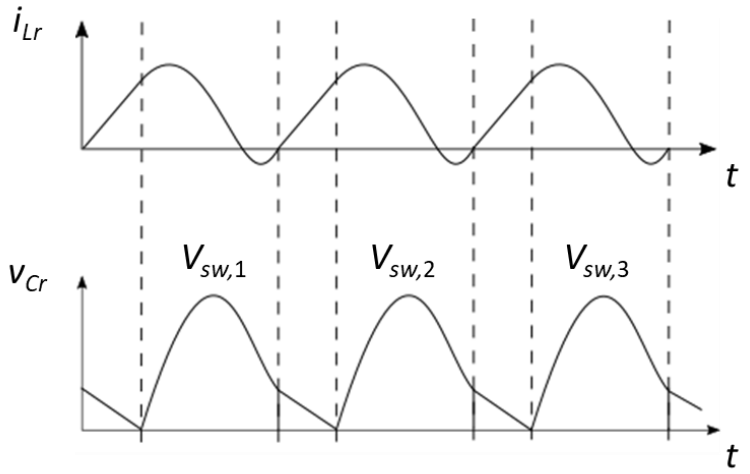


Figure 5.3 Diagram of FR-ZCS buck waveforms

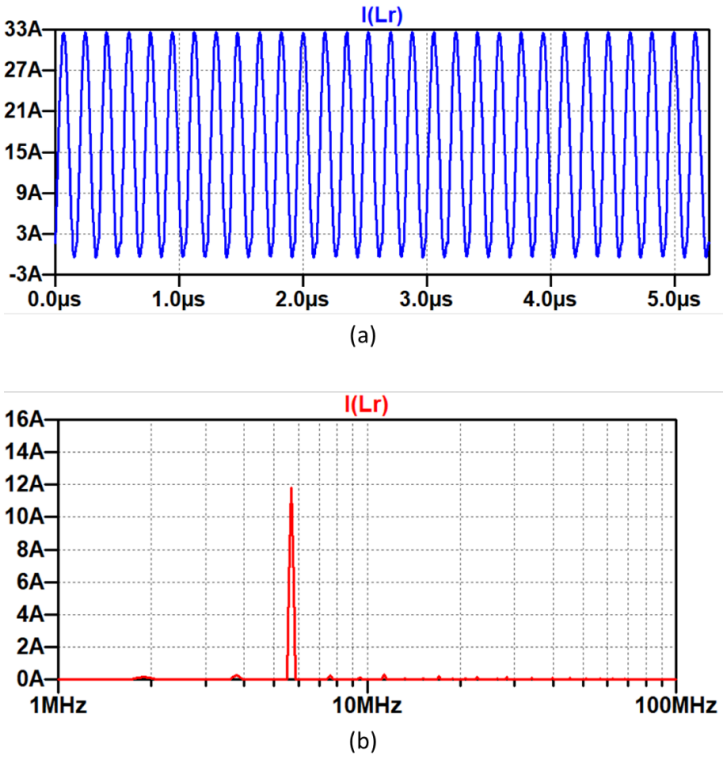


Figure 5.4 Resonant inductor current waveform (a) and FFT (b)

Analysis has been done to compare the FR-ZCS and QR-ZCS bucks and the power loss of three parallel phases of the QR-ZCS are compared to a single phase of the FR-ZCS. As with the previous analysis of the QR-ZCS buck, the power loss due to the resonant inductor ACR is not easily predicted without detailed measurements. For this analysis, the output inductance is the same for both topologies and a constant $Q = 31$ was chosen to compare the efficiency. Using this method, it is shown that the power losses in the FR-ZCS resonant inductor are nearly one-third of the losses in the QR-ZCS buck. For the same power level and conversion ratio, the FR-ZCS has a predicted efficiency of 96% while the QR-ZCS buck has a predicted efficiency of 92%. Further analysis of the details of the resonant inductor implementation will be useful in determining the feasibility of this topology in a POL converter application.

Table 16 Power loss comparison of FR-ZCS and QR-ZCS

| $J_L$ = 0.99, $I_{base}$ = 16 A | | |
|---|---|---|
| [W] | 2 MHz QR-ZCS (3 in parallel) | 2 MHz FR-ZCS |
| $P_{out}$ | 85.53 | 85.54 |
| $Q_1$ | 0.501 | 0.501 |
| $Q_2$ | 0.738 | 0.874 |
| $L_{f,DC}$ | 0.246 | 0.293 |
| $C_{oss}$ | 0.069 | 0.069 |
| $L_{r,DC}$ | 0.090 | 0.093 |
| $L_{r,AC}$ | 3.60 | 1.47 |
| $C_{r,AC}$ | 0.117 | 0.117 |
| $C_{in,AC}$ | 0.306 | 0.306 |
| $L_r$ [nH] | 9.03 | 28.3 |
| $C_r$ [nF] | 92.5 | 223 |
| $L_f$ [nH] | 100 | 100 |

## 5.3.2 Custom Magnetics Design

The analysis presented by this thesis details the impact of inductors on converter power density and efficiency. A survey of commercially available inductors shows a lack of low-volume, low-DCR possibilities. Of the inductors tested, high core losses and DCR dominate the total power loss and prohibit high efficiency at high currents. To reduce converter height and overall volume, a planar inductor design is considered. An investigation into available discrete cores reveals a limited selection of magnetic materials and few low-profile options. To reduce inductor power loss and achieve high power density, further research to design a planar inductor with a custom magnetic core is recommended.

An optimization method is proposed, accounting for the core volume and loss. Firstly, a generalized core model is proposed as shown in Figure 5.5. The geometric variables are labeled and equations for volume, inductance, and core loss are produced.

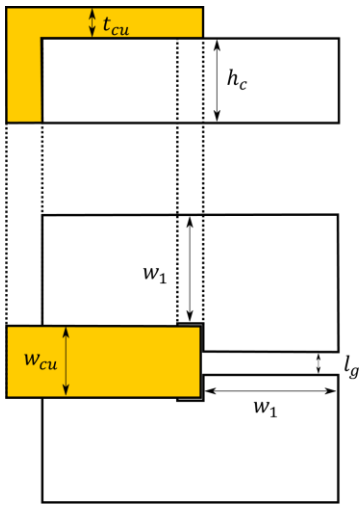


Figure 5.5 Magnetic core diagram highlighting geometric parameters

A DC output current is chosen and the inductance

$$L = \frac{n^2 \cdot \mu_r \cdot \mu_0 \cdot h_c \cdot w_1}{2 \cdot w_1 + w_{cu} + l_g \cdot (\mu_r - 1)}, \tag{93}$$

is used to calculate the current ripple $(6)$. The maximum current,

$$I_{max} = I_{DC} + \Delta i_L \tag{94}$$

and maximum flux density,

$$B_{max} = \frac{I_{max} \cdot \mu_0}{l_g} \tag{95}$$

determine the air gap of the core. The copper winding DCR is

$$DCR_{cu} = \rho \cdot \frac{2 \cdot h_c + w_1}{t_{cu} \cdot w_{cu}}, \tag{96}$$

and the respective copper conduction loss is

$$P_{cu} = DCR_{cu} \cdot I_{L,rms}^2. \tag{97}$$

The core volume is

$$V_{core} = (2 \cdot w_1 + w_{cu}) \cdot (2 \cdot w_1 + t_{cu}) \cdot h_c \tag{98}$$

and the corresponding core loss is estimated by $(42)$.

Optimization can be performed through numerical iteration or other optimization techniques and the core materials and geometry can be designed to minimize inductor power loss and maximize power density.

### 5.3.3 Interleaved Coupled-Inductor Buck

Another proposed avenue for investigation is the utilization of custom inductors in the coupled-inductor buck topology. The interleaved synchronous buck is a common topology used in commercial POL converters, and a natural progression of this topology is leveraging inductor

coupling to decrease RMS currents. The coupled-inductor buck topology is discussed in the literature review but is not explored in this research due to a lack of low-volume discrete prospects. The inductor modeling method discussed above is a possible method of optimizing the coupled inductor buck.

Figure 5.6 shows a diagram of a coupled-inductor buck. The inversely-coupled configuration is used to increase the effective inductance of the inductor, thereby decreasing the slope of the inductor current and reducing the RMS current.

A generalized, geometric model is necessary for optimizing the number of coupled-inductor phases, operating current, and volume of the inductor. Like the previously described method, the objective of this optimization is the maximization of efficiency and power density.

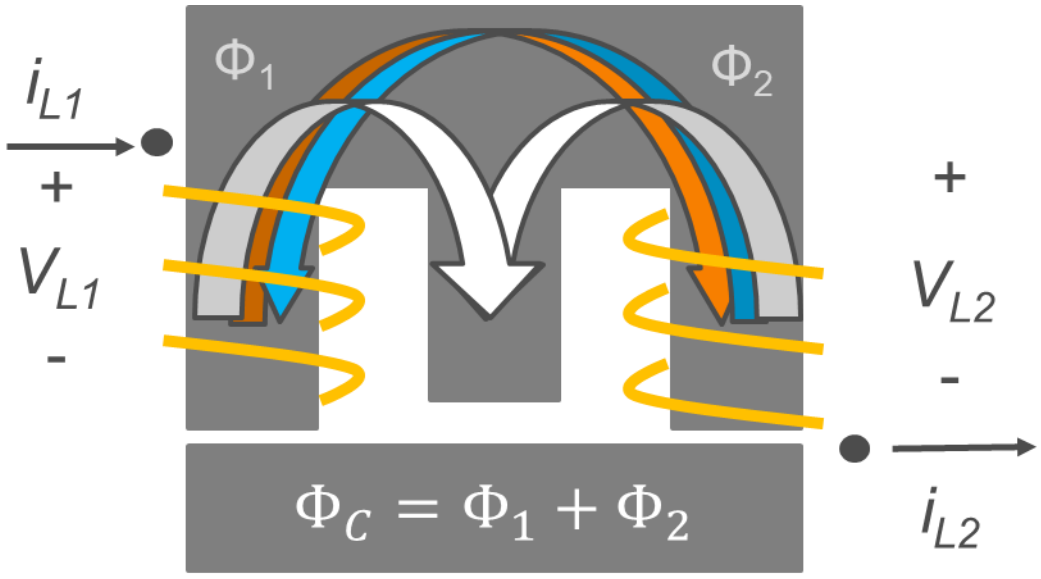


Figure 5.6 Diagram showing an example of a coupled-inductor buck

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# Vita

Douglas Bouler graduated from Munford High School in 2011. He came to the University of Tennessee, Knoxville as an undergraduate. He became heavily involved in his church, Calvary Baptist through leading worship and mentoring other undergraduate students. He became involved in the Montgomery Village Baptist Center in 2013 where he mentored teen boys until 2016. He researched the implementation of Gallium-Nitride switching devices in far-field energy harvesting and published his first paper in October 2015. He graduated cum laude with a bachelor's degree in Electrical Engineering in May 2016, and two days later, he was married to Christina Lulich.

Douglas was accepted into the Wide Bandgap Traineeship and accepted a position as a graduate research assistant under Dr. Daniel Costinett. He began his graduate career finishing his research in far-field energy harvesting before working on the development of a high-efficiency, high-density data center point-of-load converter. His future plans include staying in Knoxville and working as an Analog Layout Designer for Texas Instruments.