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Investigation of Various Shaping Methods for the Development of a Fully-Monolithic CMOS Constant-Fraction Discriminator

A Thesis
Presented for the
Master of Science
Degree
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Robert Gentry Jackson
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Dedication

I have dedicated this thesis to my parents

Mr. Wesley Jackson
and
Mrs. Linda Jackson

who have sacrificed much to give me unlimited educational opportunities,

and

to Amy

whose continual encouragement, support and patience helped see this thesis to completion.

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Abstract

In this work the design of a constant-fraction discriminator (CFD) fabricated in the Orbit Semiconductor 1.2-μ n-well CMOS process is presented. This timing pick-off circuit is designed for use in the readout electronics of the Lead-Scintillator subsystem of the Pioneering High Eenergy Nuclear Ion eXperiment (PHENIX) Electromagnetic Calorimeter at the Relativistic Heavy Ion Collider (RHIC). The design was driven by stringent requirements including low power consumption, small area, arrayable, low cost and a fully integratable shaping network. Various integratable CFD shaping methods are investigated, and the candidate methods chosen for fabrication were the distributed R-C delay-line shaping, lumped-element R-C shaping and Nowlin method shaping. An additional channel of ideal delay-line shaping, utilizing coaxial cable to generate delay, was fabricated and used for a reference in comparing methods. These shaping methods are compared on the basis of die area, time walk performance and timing jitter performance as implemented using the CMOS CFD presented.

Each shaping method investigated required no power from the dc supply. Die area for the distributed R-C delay-line, lumped-element R-C, Nowlin method and ideal delay-line (fraction circuit only) were 172 μ X 70 μ, 160 μ X 65 μ, 179 μ X 53 μ and 67 μ X 65 μ, respectively. Time walk over a 100:1 dynamic range (- 2 V_{peak} to -20 mV_{peak}) for these shaping methods in turn was found to be ± 175 ps, ± 150 ps , ± 150 ps and ± 185 ps, respectively. Timing jitter performance with a minimum input signal (- 20 mV_{peak}) in

rms units for the four methods in turn were 65 ps, 85 ps, 100 ps and 65 ps. The average power dissipated per CFD channel was found to be approximately 12 mW.

Table of Contents

Chapter Page

1. Colliders, Detectors and Calorimeter Systems 1
   1.1 Introduction to Colliders and Detectors 1
   1.2 Collider Experiments and Detectors 2
   1.3 Calorimetry and Calorimeters 3
      1.3.1 Calorimetry in High-Energy and Heavy-Ion Nuclear Experiments 3
      1.3.2 Types of Calorimeters 4
         1.3.2.1 Hadronic Calorimeters 4
         1.3.2.2 Electromagnetic Calorimeters 5
      1.3.3 Calorimeter Measurement Data 6
         1.3.3.1 Energy Measurements 6
         1.3.3.2 Trigger Formations 6
         1.3.3.3 Timing Information 7
   1.4 Readout Electronics for the PHENIX Electromagnetic Calorimeter 8
      1.4.1 Introduction 8
      1.4.2 EMCal PMT Passive Integrator Signal Processing 8
      1.4.3 PHENIX EMCal Integrated Circuit Electronics 9
   1.5 Present Technology in Integrated Timing Electronics 11
   1.6 Thesis Objective 11

2. The PHENIX Detector 13
   2.1 The RHIC Experiment 13
   2.2 The PHENIX Detector Theory and Mission 13
   2.3 PHENIX Detector Subsystems 14
      2.3.1 Introduction 14
      2.3.2 Inner Detectors 16
      2.3.3 Muon Arm 17
      2.3.4 Central Arms 19
         2.3.4.1 Tracking of Charged Particles and Measuring Momentum 19
         2.3.4.2 Particle Identification 19
         2.3.4.3 Electron and Photon Energy Measurements 21
   2.4 PHENIX EMCal Architecture 22
      2.4.1 The Lead-Glass Electromagnetic Calorimeter 22
      2.4.2 The Lead-Scintillator Electromagnetic Calorimeter 22

3. Constant-Fraction Discriminator Design 26
   3.1 Introduction 26
   3.2 Timing Measurement Uncertainties in the PHENIX EMCal 27
      3.2.1 Timing Uncertainties Inherent to the PHENIX Detector 27
      3.2.2 Uncertainties in a Timing Discriminator 27

Chapter Page

3.2.2.1 Time Walk 27
3.2.2.2 Timing Jitter 30
3.3 Timing Discriminator Circuits 32
3.3.1 Simple Leading-Edge Discriminator 32
3.3.2 Energy-Corrected Leading-Edge Discrimination 34
3.3.3 Constant-Fraction Discriminator 38
3.4 CFD Timing Methods 40
3.4.1 Introduction 40
3.4.2 True-Constant-Fraction Timing 41
3.4.3 Amplitude-Risetime-Compensated Timing 44
3.5 CFD Shaping Methods 44
3.5.1 Traditional CFD Shaping 44
3.5.2 C-R Differentiator Shaping Method 47
3.5.3 Binkley CFD Shaping Method 48
3.5.4 Distributed R-C Delay-Line Shaping Method 48
3.5.5 Lumped-Element R-C Lowpass Filter Shaping Method 52
3.5.6 Nowlin Shaping Method 54
3.6 CFD Shaping Method Analysis 56
3.7 PHENIX Lead-Scintillator CFD Circuit Designs 62
3.7.1 Architecture and Coincidence Gating 62
3.7.2 Zero-Crossing Comparator 68
3.7.3 Zero-Crossing Comparator dc Feedback Circuit 78
3.7.4 Arming Discriminator Design 85
3.7.5 Arming Discriminator dc Feedback Circuit 93
3.7.6 CFD Digital Output Circuits 95

4. Experimental Results 97
4.1 Introduction 97
4.2 Test Board Construction and Functionality 97
4.3 Time Walk Performance 102
4.4 Timing Jitter Performance 105
4.4.1 Introduction 105
4.4.2 Circuit Noise Induced Timing Jitter 107
4.4.3 Input Noise Induced Timing Jitter 107
4.5 Die Area and Power Consumption 118

5. Conclusions and Discussion of Future Work 122

List of References 125

Vita 129

List of Tables

Table		Page
3-1	Table showing the Orbit Semiconductor 1.2-μ n-well process parameters for the distributed R-C delay-line.	51
3-2	Lump element values for the 4.8 μm wide delay-line fabricated in the Orbit Semiconductor 1.2-μ n-well process in per length units.	51
4-1	Table of bias voltages for each IC tested.	101
4-2	Table of time walk measurements for each IC tested.	103
4-3	Table of time walk adjustment and threshold settings for each IC tested.	103
4-4	Table of rms timing jitter for - 20 mV peak inputs.	108
4-5	Table comparing simulation predictions to measured results for timing jitter due to an input noise source.	119
4-6	Comparison of die area required to realize each shaping method.	119
4-7	Comparison of the full CFD implementation for each shaping method.	119
4-8	Table of power dissipation per channel for ten ICs.	121

List of Figures

Figure		Page
1-1	Schematic of the passive integrator for PMT output signals.	10
1-2	Block diagram of PHENIX EMCal readout electronics.	10
2-1	A cutaway view of the PHENIX detector indicating various subsystems and their locations.	15
2-2	A cross-section view of the Muon Arm.	18
2-3	A cross-section view of PHENIX through the nominal collision point with subsystems labeled on the right central arm.	20
2-4	Diagrams and section views of the Lead-Scintillator module.	23
3-1	Illustration of timing discriminator time walk for input signals with equal peak times.	28
3-2	Illustration of timing jitter due to electronic noise.	31
3-3	Illustration of the threshold crossing time for a linear-edge input signal.	33
3-4	Illustration of crossing times in leading-edge discriminators as a function of input amplitude.	35
3-5	Illustration of crossing times in leading-edge discriminators as a function of input risetime.	35
3-6	Block diagram of the energy-corrected leading-edge discrimination technique.	37
3-7	Diagram of the constant-fraction discrimination shaping network.	39
3-8	Block diagram architecture of a constant-fraction discriminator.	39
3-9	Illustration of true-constant-fraction timing for equal risetime inputs.	42
3-10	Illustration of true-constant-fraction timing for equal amplitude inputs.	43

Figure Page

3-11 Illustration of amplitude-risetime-compensated timing for equal risetime inputs. 45

3-12 Illustration of amplitude-risetime-compensated timing for equal amplitude inputs. 46

3-13 Illustration of the distributed R-C delay-line shaping for constant-fraction discrimination. 49

3-14 Diagram of one lump in the HSPICE lossy transmission line Umodel. 51

3-15 Illustration of the lumped-element R-C lowpass filter shaping method for constant-fraction discrimination. 53

3-16 Illustration of the Nowlin shaping method for constant-fraction discrimination. 55

3-17 Plot of the pseudo-gaussian input used in simulation analysis. 57

3-18 Plot of signal peak position delay with increasing distributed R-C delay-line length. 57

3-19 Plot of signal degradation for the lumped-element R-C lowpass filter and the distributed R-C delay-line with increasing peak position delay times. 58

3-20 Plots of timing jitter components simulated in HSPICE for each shaping method investigated. 61

3-21 Time walk simulation results for the four shaping methods. 63

3-22 Time walk over a 100:1 input amplitude dynamic range in 5 dB steps for the zero-crossing time chosen for fabrication. 63

3-23 Three candidate shaping methods fabricated for the PHENIX PbSc CFD. 64

3-24 Block diagram of the PHENIX PbSc CFD with differential input from the passive integrator (PI). 65

3-25 Plot of the output voltages from the passive integrator for a pseudo-gaussian input. 67

Figure Page

3-26 Timing diagram indicating correct coincidence gating for the ZCC. 67

3-27 Circuit diagram of the ZCC shaping amplifier. 71

3-28 PMOS characteristic curves indicating various regions of operation. 73

3-29 Circuit diagram of the ZCC differential amplifiers following the shaping amplifier. 75

3-30 Circuit diagram of the ZCC differential to single-ended amplifier. 77

3-31 Circuit diagram of the ZCC dc feedback amplifier. 79

3-32 Circuit diagram to illustrate the ZCC dc feedback. 81

3-33 HSPICE plot showing ZCC output signal time spread variation along the zero-crossing edge. 83

3-34 Diagram of the first amplifier in the arming channel of the CFD. 86

3-35 Diagram of the cascaded differential input and output amplifiers preceding the threshold circuit. 90

3-36 Diagram of the arming discriminator threshold circuit amplifier performing differential input to single-ended output conversion. 90

3-37 Illustration of the effect of current limiting in the threshold circuit by M6 operating M4 in the ohmic region. 92

3-38 Circuit diagram of the arming discriminator dc feedback amplifier. 94

4-1 Illustration of IC testing configuration. 99

4-2 Illustration of the test board configurations used to generate the various CFD bias voltages. 100

4-3 Time walk curves for the four shaping methods investigated. 104

4-4 Plots of time walk for various input dc levels. 106

4-5 Plot of rms timing jitter with input amplitude for a typical channel from each shaping method. 108

Figure Page

4-6 Illustration of measured peak-to-peak timing jitter analysis. 112

4-7 Illustration of the summing network used to combine the input pulse with a sine wave. 115

4-8 Plot of the input sine wave induced timing jitter transfer function generated for each shaping method. 116

4-9 Plot of the input sine wave induced timing jitter transfer function showing relative values. 117

Acronyms

ADC	Analog-to-Digital Converter
ALICE	A Large Ion Collider Experiment
AMU	Analog Memory Unit
ARC	Amplitude-Risetime-Compensated
ATLAS	A Toroidal LHC ApparatuS
BB	Beam-Beam
BC	Beam-Clock
BGO	Bismuth Germanate
BNL	Brookhaven National Laboratory
BRAHAMS	Broad Range Hadron Magnetic Spectrometers
CERN	Centre European pour la Recherche Nucleaire (European Center for Nuclear Research)
CFD	Constant-Fraction Discriminator
CM	Central Magnet
CMOS	Complementary Metal-Oxide Semiconductor
CMS	Compact Muon Solenoid
C-R	Capacitor-Resistor
DC	Drift Chamber
EMCal (EM Cal)	Electromagnetic Calorimeter
GBW	Gain BandWidth product
HCAL	Hadronic Calorimeter
HVG	High-Voltage Generating
IC	Integrated Circuit
LED	Leading-Edge Discriminator
LHC	Large Hadron Collider
LHP	Left-Half-Plane
MM	Muon Magnet
MVD	Multiplicity Vertex Detector
NMOS	N-channel Metal Oxide Semiconductor
ORNL	Oak Ridge National Laboratory
Pb	Lead
PbGl	Lead-Glass
PbSc	Lead-Scintillator
$PbWO_4$	Lead Tungstate
PC	Pad Chamber
PCB	Printed Circuit Board
PHENIX	Pioneering High Energy Nuclear Ion eXperiment
PI	Passive Integrator
PIN	P-type Intrinsic N-type
PMOS	P-channel Metal Oxide Semiconductor
PMT	PhotoMultiplier Tube

QGP	Quark-Gluon Plasma
R-C	Resistor-Capacitor
RF	Radio Frequency
RHIC	Relativistic Heavy Ion Collider
RHP	Right-Half-Plane
RICH	Ring Imaging CHerenkov
SR	Slew-Rate
STAR	Solenoidal Tracker At RHIC
TAC	Time-to-Amplitude Converter
TCF	True-Constant-Fraction
TEC	Time-Expansion-Chamber
TOF	Time-Of-Flight
VGA	Variable Gain Amplifier
WLS	WaveLength Shifting
ZCC	Zero-Crossing Comparator

Chapter 1

Colliders, Detectors and Calorimeter Systems

1.1 Introduction to Colliders and Detectors

Due to the efforts of various organizations and collaborations between countries, much research has been accomplished through the experiments conducted with particle colliders. Science has made many advancements in the study of atomic and sub-atomic structure. The goal of a collider experiment is to produce high-energy collisions between particles resulting in the formation of undiscovered particles or phases of matter. When particles are accelerated to high velocities and collided with a target, a shower of particles with various energies will be emitted. These particles can exist in many different forms and can possess a variety of lifetimes. Thus far, the atom, its orbital components, the nucleus and sub-nuclear elements have been discovered.

In any experiment of this type, the atomic dimensions involved indicate the possibility of particles colliding without producing a "significant" event. A significant event would be one in which new and important physics can be studied. Statistical analysis for each experiment reveals indicators of how likely a significant event will occur in a given number of collisions (or luminosity). Accumulating sufficient data in a reasonable time requires a high rate of collisions. The frequency with which particles collide is a function of the probabilities involved, and it influences the detector designs.

For each collider, there is a theoretical point for collisions designated as the "nominal" collision point. This point could be a fixed target or the collision point between two particles traveling in opposing directions. In order to study these experiments, a main detector is constructed around this point. Each main detector contains many specialized subsystems (or detectors) for gathering information. The orientation of each subsystem and its distance from the collision point will vary as a function of its purpose. The types of measurements performed would include: resultant shower and particle identification, flight trajectory or vertices, energy, time-of-occurrence, lifetime, etc. With the use of large detectors in nuclear experiments, measurement data can be obtained, stored and analyzed at a later date. Various on-line and construction-phase particle colliders are in place around the world.

1.2 Collider Experiments and Detectors

The CERN laboratory in Switzerland is presently the home of several experiments either underway or under construction. WA98 is a currently on-line experiment in which lead (Pb) particles are accelerated into a target to study hadrons and photons [1]. The L3 experiment at CERN was designed to study the collisions of electrons and positrons. By limiting the range of particle detections, L3 has achieved better resolution in identification of electrons, muons and photons [2]. The Large Hadron Collider (LHC) experiment is presently under construction at CERN. This experiment will have at least three main detectors: the Compact Muon Solenoid (CMS) detector, A Toroidal LHC ApparatuS (ATLAS) detector and A Large Ion Collider Experiment (ALICE) detector.

Muon and hadron characteristics will be studied by the CMS and ATLAS detectors, respectively [3,4]. The ALICE detector will be dedicated to the study of high-energy interactions between hadrons [5].

In the United States, the Relativistic Heavy Ion Collider (RHIC) is under construction at the Brookhaven National Laboratory (BNL) in New York. The proposed experiments and their respective detectors at RHIC are the Solenoidal Tracker At RHIC (STAR) experiment, the Broad RAnge Hadron Magnetic Spectrometers (BRAHMS) experiment, the Pioneering High Energy Nuclear Ion eXperiment (PHENIX) and the Phobos experiment. The goal of the RHIC collider and its detectors is to study various aspects of the quark-gluon plasma (QGP) [6], a newly suspected phase of matter discussed in **Chapter 2**. Research and development of readout electronics associated with various subsystems for PHENIX is being conducted by the Monolithic Systems Development Group at the Oak Ridge National Laboratory (ORNL). This thesis is concerned with the development of timing measurement circuitry in the PHENIX electromagnetic calorimeter (EMCal). An introduction to calorimetry in collider experiments is presented in the following section.

1.3 Calorimetry and Calorimeters

1.3.1 Calorimetry in High-Energy and Heavy-Ion Nuclear Experiments

Calorimeter detectors are the devices or systems used to perform calorimetry measurements. Calorimetry, as related to high-energy nuclear experiments, is the acquiring of energy, trigger and timing data. A calorimeter acquires these forms of data

through the use of a scintillating material. Once a high-energy collision has occurred, some particles take the form of ionizing radiation. As ionizing radiation enters the dense scintillator medium, its velocity will decrease. The laws of conservation of energy state that a loss of kinetic energy must be converted into an equal amount of energy in another form. Inside a scintillator, this energy is released as light with a wavelength determined by the medium properties. Several devices are available to measure this light.

PIN photodiodes and photomultiplier tubes (PMTs) are two devices used to measure scintillation light. These devices produce an output electrical signal with an amplitude proportional to the intensity of the scintillation light. PIN photodoides possess an advantage over PMTs because they are not adversely effected inside a strong magnetic field. PMT outputs offer a feature of constant output rise- and falltimes independent of signal amplitude which is desirable in the acquiring of timing information. A scintillator and its PMT (referred to as a module) usually comprise a single channel in a calorimeter. In most multichannel calorimeters, the modules are placed in large arrays to form the walls of the calorimeter detector. Each scintillator would also be optically isolated from its surrounding modules to maintain channel integrity. The specific mediums and readout devices used depend on the type calorimeter and its environment.

1.3.2 Types of Calorimeters

1.3.2.1 Hadronic Calorimeters

Calorimeter classification is most often determined by which type of particle it detects. One type is the hadronic calorimeter (HCAL) designed to detect hadrons. A

hadron is the general classification of elements including the main particles found in the nucleus of an atom. Protons and neutrons are some of the more commonly recognized hadronic particles. The hadronic calorimeter in the CMS detector is designed to identify and to study the behavior of hadrons using plastic scintillator detector mediums. The L3 experiment's HCAL serves a slightly different purpose. This hadronic calorimeter uses uranium and bismuth germanate (BGO) crystals as detectors to study only hadron jets and to track muons [2]. The optimization of L3 allowed for the distinguishing of hadronic particles from the other particles without hadronic separation. Consequently, this HCAL will study shower characteristics, but it will not separate hadrons into their respective subset classifications.

1.3.2.2 Electromagnetic Calorimeters

Electromagnetic calorimeters provide identification of particles such as electrons and photons. The WA98 EMCal has approximately 10,000 channels equipped with lead-glass scintillators. Integrated readout electronics in this calorimeter system were developed by engineers at ORNL [7,8]. The L3 Electromagnetic Calorimeter has about 11,000 bismuth germanate (BGO) crystals for its detector medium. Since the L3 readout electronics reside in a high magnetic field, photodiode readout is used as opposed to photomultiplier tubes [2]. The ALICE Calorimeter for LHC will study photon generation from early interactions of heavy-ion particles using lead tungstate ($PbWO_4$) crystals and PIN photodiode readout [9]. The PHENIX experiment will implement two scintillator detector techniques, the Lead-Glass (PbGl) and Lead-Scintillator (PbSc) Calorimeters, to

study electron and photon generation [10]. These systems are detailed in the discussion of the PHENIX Electromagnetic Calorimeter in **Chapter 2**.

1.3.3 Calorimeter Measurement Data

1.3.3.1 Energy Measurements

Energy data is based on the total energy released inside the scintillating medium. For example, PMT devices output a current pulse in response to scintillation light. By integrating the current pulse over time, total output charge contained in the signal is acquired. The total charge collected is then proportional to the energy deposition in the scintillator. Since particles of interest in the experiment possess an expected dynamic range of light energy dissipation inside the scintillator, this information will assist in the separation and identification of particle types. The second kind of data is the trigger formation.

1.3.3.2 Trigger Formations

Trigger information is the indicator that a significant event has occurred. Depending on the trajectories, a particle shower can have particles release energy into more than one channel. Due to this phenomenon, any one channel and its surrounding channels must be considered individually and collectively. Neighboring channels can be summed together and compared against a threshold. These combinations are referred to as "trigger sums", and schemes for comparison are generally based on geometrical arrangement of the detector devices. If a sufficient energy level has been obtained, a

trigger is generated. This trigger, in conjunction with other subsystem triggers, contributes to the decision that a significant event was produced. When a significant event is detected, a central computing unit will collect and store all data relevant to that event for future analysis. A third data type acquired in an electromagnetic calorimeter is the timing information.

1.3.3.3 Timing Information

The time at which particle showers arrive at the detector is crucial in the identification and study of its components. Photons travel at the speed of light, while charged particles travel at velocities below the speed of light. Since photons are also neutral in charge, their flight path is not bent in a magnetic field like charged particles. These properties can be used to help separate particles based on their time-of-arrival.

In timing systems, the measurement is made with respect to a known reference. A common timing reference in nuclear collider experiments is the RF clock used to accelerate the beam. This beam clock (BC) represents the rate at which "packets" of pre-accelerated particles are introduced into the main collider. These packets are essentially a tightly packed cloud of particles traveling along opposing beam lines, and a collision between two packets is referred to as the "beam-crossing". A collider experiment can also be designed to allow for "empty" collisions by prohibiting the entrance of a packet into the main beam. Empty collisions effectively reduce the rate of collisions, and these empty crossings can be used to calibrate and diagnose the readout electronics. The rate of

collisions becomes significant in the design of timing readout electronics when the circuitry must be active for every beam-crossing.

1.4 Readout Electronics for the PHENIX Electromagnetic Calorimeter

1.4.1 Introduction

The readout electronics for the PHENIX EMCal detectors are based on the types of electrical signals produced by the PbGl and PbSc PMTs. Both PMT models will produce a negative going current pulse proportional to the intensity of the gathered scintillation light. The rise- and falltimes of the PMTs will be fairly constant independent of signal amplitude. PbGl PMTs are expected to produce nearly gaussian pulses with 10 ns rise- and falltimes, while the PbSc pulses are expected to produce 5 ns and 15 ns rise- and falltimes, respectively.

The PHENIX EMCal timing electronics must be active or "live" for each beam-crossing. The BC rate is expected to be approximately 9 MHz. This requires the timing discriminator to trigger on an event and return to its baseline in approximately 110 ns. In addition, timing resolutions of $\sigma_t \approx 300$ ps are required for proper separation of collision products [10]. Readout electronics for the PHENIX EMCal are to be realized in a CMOS integrated circuit technology.

1.4.2 EMCal PMT Passive Integrator Signal Processing

A passive integrator (PI) is to be implemented in the PHENIX EMCal circuitry to perform initial signal processing. The passive integrator contains a 50 Ω resistor, R_{dev},

serving a dual purpose. As shown in Figure 1-1, this resistor will terminate a length of 50 Ω coaxial cable from a PMT and also develop a voltage signal for the timing measurement circuitry. The 500 pF capacitor, C_{int}, integrates the current pulse and stores the charge for energy measurement purposes. The total charge expected from the PMT for a full-scale output is 500 pC. This translates into a 1 V peak signal developed across the integrating capacitor. The 100 kΩ resistor, R_{decay}, is connected between a voltage reference and the capacitor. This resistor sets a + 4 V dc level on the capacitor for processing of negative going signals. Since the energy channel outputs will be sampled at the beam-clock rate, the R_{decay}-C_{int} time constant will be much longer than the sampling frequency to ensure a small error in the energy measurement due to voltage decay.

1.4.3 PHENIX EMCal Integrated Circuit Electronics

The readout electronics under development at ORNL consists of a two-chip set of integrated CMOS circuits shown in Figure 1-2. This choice is preferable to classical CAMAC, FastBus or NIM-based discrete designs due to lower power, smaller area and reduced cost. Techniques available in integrated circuit technology possess attractive features that also aid in the elimination of external user adjustments and cabling. The main components of the first chip are timing discriminators, variable gain amplifiers (VGAs), time-to-amplitude converters (TACs) and trigger sum circuits. This chip will process a total of four channels. A chip containing analog-memory units (AMUs) and analog-to-digital converters (ADCs) along with buffer register circuits comprise the second chip. Although these circuits are not timing specific, they are a part of the overall

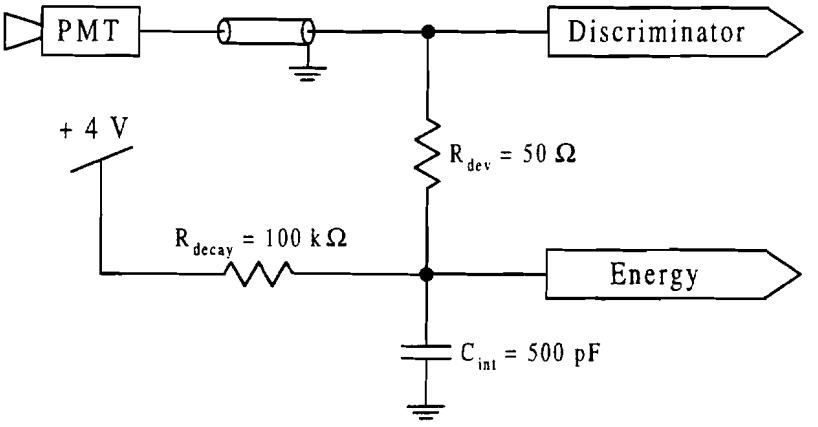


Figure 1-1. Schematic of the passive integrator for PMT output signals.

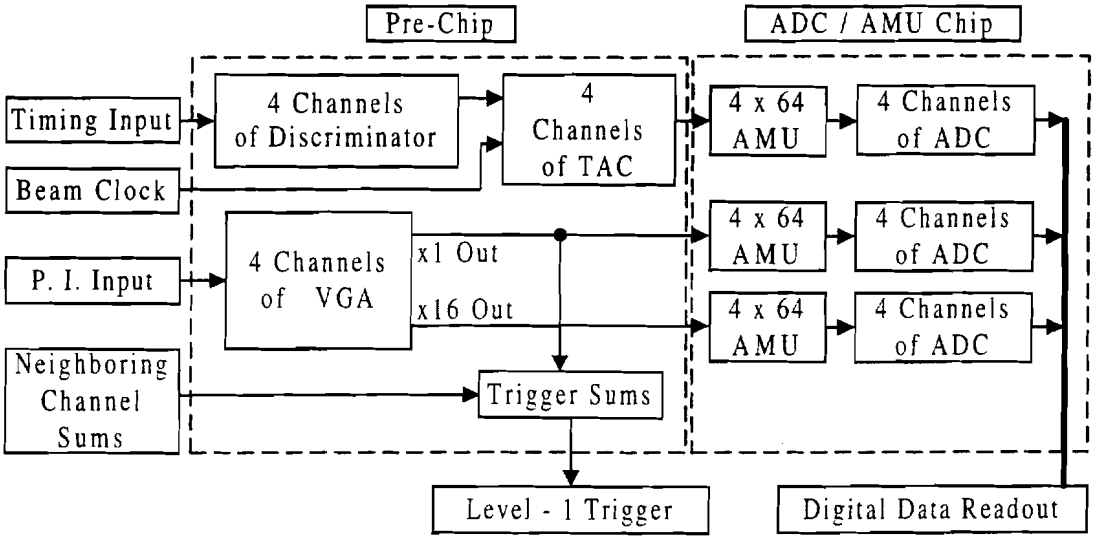


Figure 1-2. Block diagram of PHENIX EMCal readout electronics.

timing system. These circuits will be discussed in the context of the overall timing system design in **Chapter 3**. Both chips are to be designed for a single + 5 Vdc supply.

1.5 Present Technology in Integrated Timing Electronics

Much work has been accomplished in the integration of multichannel detector electronics using CMOS technology. CMOS constant-fraction discriminator (CFD) techniques were reported by Binkley, Simpson and Rochelle using external delay-line shaping [11]. Further work in the area of lumped-element signal shaping that can be integrated in CMOS technology has been reported by Nowlin [12,13], Turko and Smith [14] and Binkley [15]. Simpson, et al. [8] and Binkley [15] have reported fully integrated CMOS CFDs implementing these shaping techniques. Simpson, et al. [16] have also reported a fully integrated CMOS CFD using an on-chip distributed R-C delay-line.

1.6 Thesis Objective

In this work, a short description is provided concerning the PHENIX detector at RHIC and its various subsystems. The choice of a timing discriminator technique such as simple leading-edge discrimination, energy-corrected leading-edge discrimination and constant-fraction discrimination is discussed. An existing ORNL designed CMOS CFD was revised for the PHENIX Lead-Scintillator Electromagnetic Calorimeter readout electronics, and the analysis and design of the new CFD is presented in this work. Several shaping methods integratable in a standard CMOS process are investigated for use with the CMOS CFD. Distributed R-C delay-line shaping, lumped-element R-C

delay-line shaping and Nowlin method shaping are compared to an ideal delay-line version on the basis of timing jitter performance. Time walk performance for these shaping methods is evaluated for the CMOS CFD architecture presented herein. Experimental data for time walk and rms timing jitter will be presented and discussed for the CFD and shaping methods as implemented in the Orbit Semiconductor 1.2-μ n-well CMOS process.

Chapter 2

The PHENIX Detector

2.1 The RHIC Experiment

The Relativistic Heavy Ion Collider experiment will collide sub-atomic particles called heavy-ions with 100 GeV energies in each beam [6]. The beam clock will be generated from the 9 MHz RF frequency and other harmonics. With particles traveling in opposite directions, an extra energy component due to momentum will be introduced into the total energy of collision over fixed target experiments. This added energy contained in the collision will facilitate the generation of higher energy particles and phase transitions.

2.2 The PHENIX Detector Theory and Mission

Current theory states that the universe began as a "singularity" containing enormous pressure and minute size. In an event referred to as "The Big Bang", the singularity began rapidly expanding. Drastic increases in volume were met with drastic decreases in pressure and temperature. One implication of this idea is the study of the four known forces: gravity, strong-nuclear forces, weak-nuclear forces and electromagnetic fields. Physicists believe these forces existed as one within the singularity. Consequently, theories claim these four forces split apart, respectively,

during the first few microseconds after expansion began. Theory also claims the universe existed as a quark-gluon plasma a few microseconds after its beginning. Physicists feel the separation between weak-nuclear forces and electromagnetic forces occurred during the formation or existence of the QGP.

To study these theories, various types of high-energy particles and phases of matter must be documented and characterized with detectors such as the PHENIX detector. The PHENIX experiment is a global collaboration with scientists, engineers, and graduate students belonging to 10 countries and 43 institutions. The mission statement for the PHENIX detector reads [10]:

> "The primary goals of the PHENIX experiment are to detect the quark-gluon plasma (QGP) and to measure its properties. Many of the potential signatures for the QGP are measured as a function of a well-defined common variable to see if any or all of these signatures show a simultaneous anomaly due to the formation of the QGP. In addition, basic quantum chromodynamics phenomena, collision dynamics, and thermodynamic features of the initial states of the collision are studied."

Although the electromagnetic calorimeter detector will be the focus of this thesis, a general overview of the full detector is provided next. The PHENIX EMCal with its two main components are detailed at the end of the section.

2.3 PHENIX Detector Subsystems

2.3.1 Introduction

The PHENIX detector has been designed for future upgrades, however, the basic detector for Day-1 operation is referred to as the "Baseline" detector [10]. The cutaway view of PHENIX in Figure 2-1 indicates the various subsystems and their locations

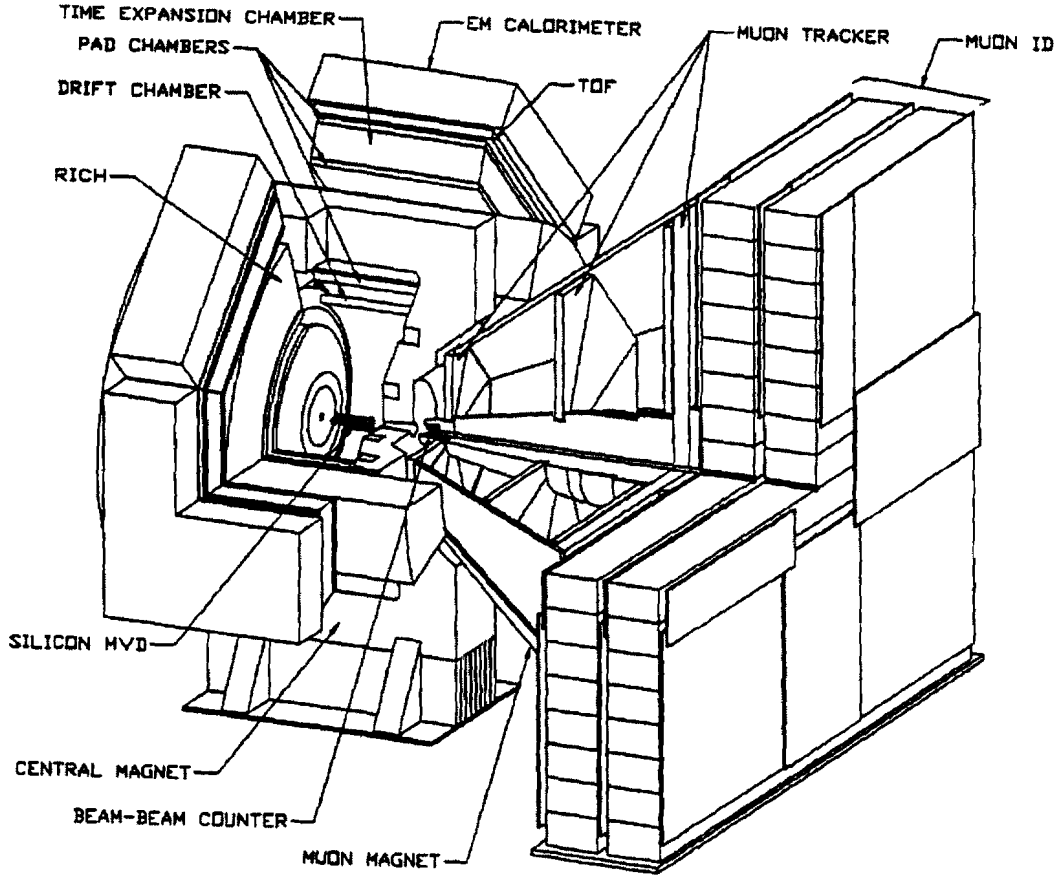


Figure 2-1. A cutaway view of the PHENIX detector indicating various subsystems and their locations.
Source: Kehoe, W. L., et al. PHENIX Conceptual Design Report. 29 January 1993, pg. 2-6.

relative to each other. Three spectrometers or "arms" makeup this basic detector along with a set of "inner detectors". Inner detectors are provided to distinguish the vertex location for an event, start time and multiplicity distribution. The Muon Arm is dedicated to the detection of muon particle products in the resultant showers and illustrated in Figure 2-1. Two other arms, the central arms, will face each other to detect electrons, photons and charged hadrons.

Among the different subsystems, similar measurements are taken to cover a specific area around the collision point and various points along the particle paths. Data collected from these systems must be considered together before forming conclusions. This approach is reflected in the design of each subsystem. The following sections will discuss the role and measurement of each PHENIX subsystem by topic.

2.3.2 Inner Detectors

Two main components acquire the data for this section of PHENIX. Two Beam-Beam (BB) Cherenkov counters are located at points before and after the collision point to makeup the first component. The BB counters lie just outside the central magnet pole tips and measure start times and fast vertices for particle showers. Using the two arrays in coincidence yields precise start time data ($\sigma_t < 100$ ps) and an approximate start vertex location in azimuth ($\sigma_z \approx 2$ cm).

The second component of this section is the silicon strip Multiplicity Vertex Detector (MVD). MVD surrounds the collision point and is shown in the cutaway view of PHENIX in Figure 2-1. Two layers referred to as a "barrel" and two one-layer

"endcaps" comprise MVD. Barrel pieces are made of 200 μm silicon strips, while the endcaps are equipped with pads. Total event multiplicity and the associated distribution are measured by MVD. Also, a more precise vertex location ($\sigma_z < 500$ μm) over the BB reading is acquired. MVD is the closest detector to the nominal collision point, and it requires special design for the expected radiation doses.

2.3.3 Muon Arm

The Muon Arm illustrated in the cross-section view of Figure 2-2 provides the momentum analysis, tracking of charged particles and muon detection. Full coverage can be obtained for a polar angle of $10° \leq \theta \leq 35°$, since particles with trajectories through this angle will pass through the pole tip of the Central Magnet in the central arms. If these particles emerge from the pole tip, they enter the Muon Arm.

A radial field produced by the Muon Magnet (MM) provides the medium for measuring charged particle momentums. Particle tracking, μT, will also use the MM with a three segment detector located at the entrance, middle and end of the muon magnetic field. The tracker segments are positioned perpendicular to the beam line for azimuthal coverage relative to the clockwise beam direction. Muon identification, μID, will be made at the end of the Muon Arm. A large concrete wall containing planes of sensor devices will distinguish the muon particles from other shower products based on particle propagation into the detector.

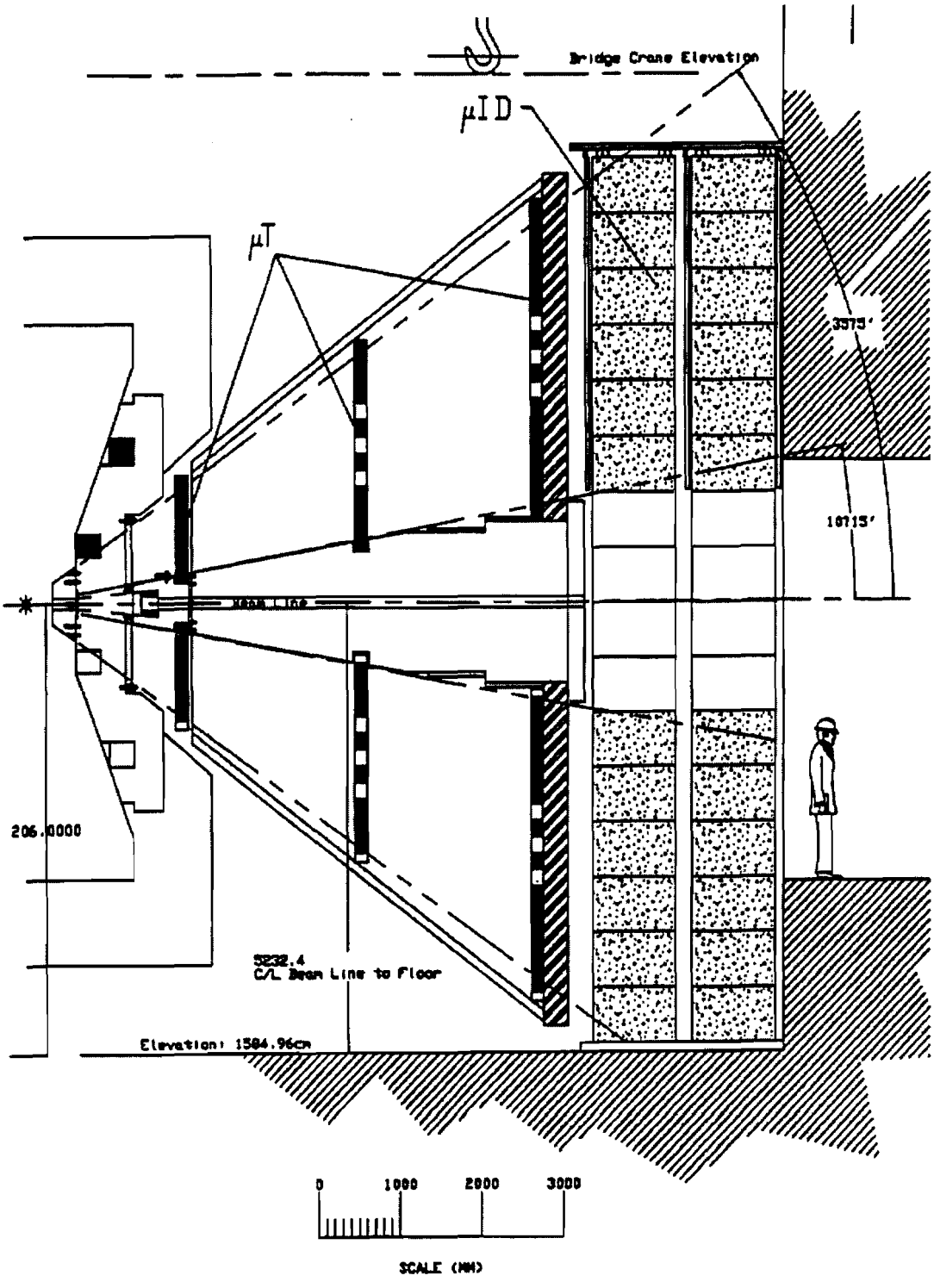


Figure 2-2. A cross-section view of the Muon Arm.
Source: Kehoe, W. L., et al. PHENIX Conceptual Design Report. 29 January 1993, pg. 2-6.

2.3.4 Central Arms

2.3.4.1 Tracking of Charged Particles and Measuring Momentum

Four systems are involved in this section. First, the Central Magnet (CM) for the Baseline detector will consist of an axial coil known as the outer coil surrounding the collision point. Future upgrades allow for a second coil to be added closer to the collision point. The other three types of systems in this section are a multilayer Drift Chamber (DC), a multilayer Time-Expansion-Chamber (TEC) and three Pad Chambers (PC) designated by PC1, PC2 and PC3.

The three remaining detectors in this section are placed in two groups and labeled in the right central arm of Figure 2-3. The first group is composed of the DC and an interpolating pad chamber, PC1. This group resides in the fringe field of the CM approximately two meters from the nominal collision point. The second group has the TEC surrounded by pad chambers PC2 and PC3 and is located about 4.5 meters from the nominal collision point.

2.3.4.2 Particle Identification

Electron and hadron identification are capabilities of several central arm detectors. The range of momenta to be studied at RHIC (0.2 - 5.0 GeV/c) require many different techniques to achieve good separation of electrons from hadrons. These various techniques provide for dynamic range and redundancy. The Time-Of-Flight (TOF) detector uses scintillators to acquire high resolution charged hadron momentum data and covers one-third of a central arm. With this system, separation of kaons and pions is

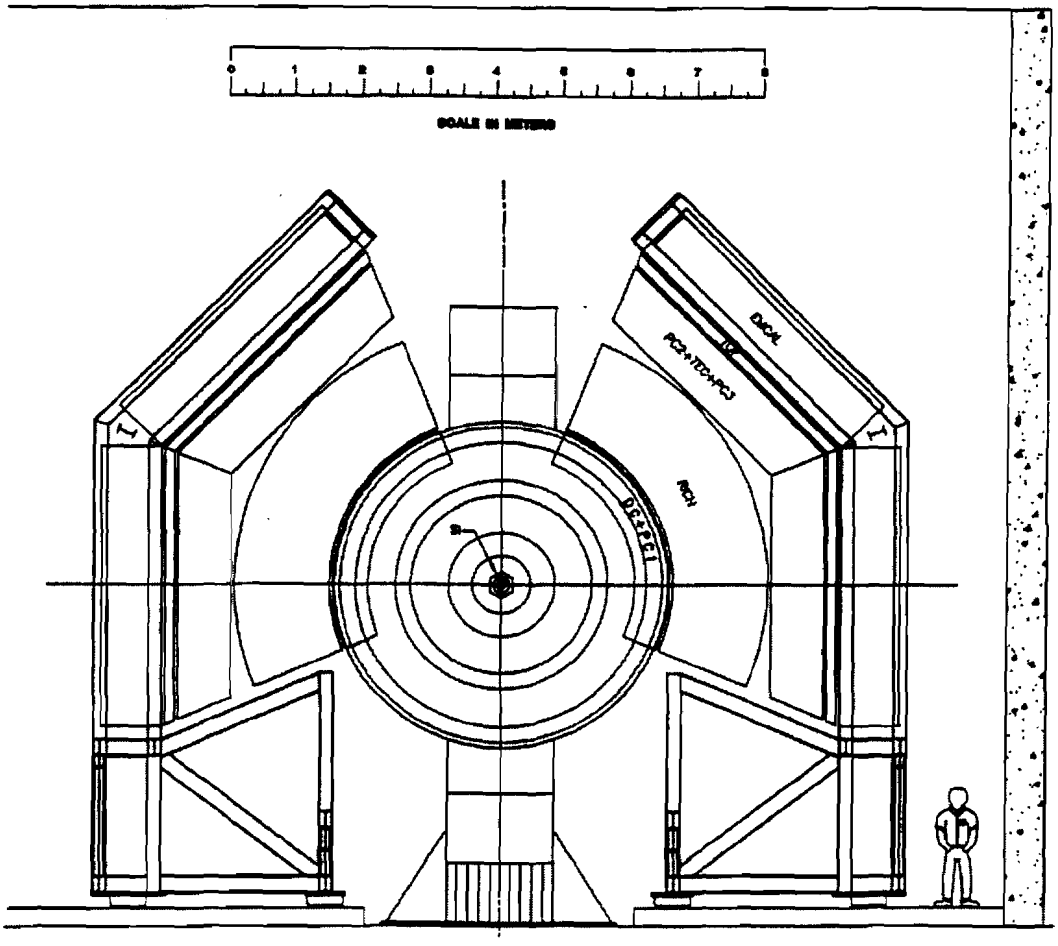


Figure 2-3. A cross-section view of PHENIX through the nominal collision point with subsystems labeled on the right central arm.
Source: Kehoe, W. L., et al. PHENIX Conceptual Design Report. 29 January 1993, pg. 2-3.

possible up to a momenta of 2.4 GeV/c. Next, the Ring-Imaging CHerenkov (RICH) detector is located between the two tracking detector groups. RICH is designed to provide electron identification up to approximately 3 GeV/c. A photomultiplier tube array will be used for readout if current research does not reveal a less expensive option. Finally, the TEC detector will provide identification of electrons with transverse momentums up to 2 GeV/c based on the derivative of the electric field, dE/dx. Comparison of dE/dx for electrons and pions is aided by EMCal measurements used to eliminate kaons up to 1 GeV/c.

2.3.4.3 Electron and Photon Energy Measurements

The PHENIX Electromagnetic Calorimeter is designed to separate photons and electrons, to measure energy and position, and to provide the ability to trigger when electrons and photons are produced with high transverse momentums. EMCal requirements for the Baseline detector call for two divisions: Lead-Glass (PbGl) counters and Lead-Scintillator (PbSc) sampling calorimeter units. Readout electronics with sub-nanosecond precision are required for the time-of-arrival of calorimeter pulses. One wall will contain the PbGl modules, while the PbSc will cover the remaining three walls. Since the timing electronics for PHENIX EMCal are the emphasis of this thesis, both subsystem types will be detailed in the next section.

2.4 PHENIX EMCal Architecture

2.4.1 The Lead-Glass Electromagnetic Calorimeter

The Lead-Glass system for the WA98 experiment in CERN is to be dismantled and reinstalled in the approximately 10,000 channel PHENIX PbGl detector. Each module in PbGl contains a 4 cm x 4 cm x 40 cm lead-doped glass beam or "tower", a model FEU84 Russian PMT with plastic housing and a high voltage-generating (HVG) base. After each PMT base is fixed to its beam, aluminized mylar is wrapped around the module and secured with shrink-wrap, providing optical isolation of each channel. In these experiments, the smallest discernible area in which a significant event occurred is referred to as segmentation. The cross-sectional area of each tower will limit the segmentation of PbGl to 4 x 4 cm^2.

Once a module is constructed, an array known as a supermodule is created. A supermodule is composed of 24 modules set in a 4 x 6 array. This array is wrapped with fiberglass cloth and epoxied. Oven curing at this point insures an even contact distribution along each module. If singular contact points exist between modules, stacking of supermodules could result in damage to a module. New HVG bases, readout electronics and trigger formations must be developed for implementation in the PHENIX detector.

2.4.2 The Lead-Scintillator Electromagnetic Calorimeter

The 15,552 channel Lead-Scintillator system for PHENIX will contain a sandwich or "shish-kebab" module configuration. The arrangement seen in Figure 2-4 consists of

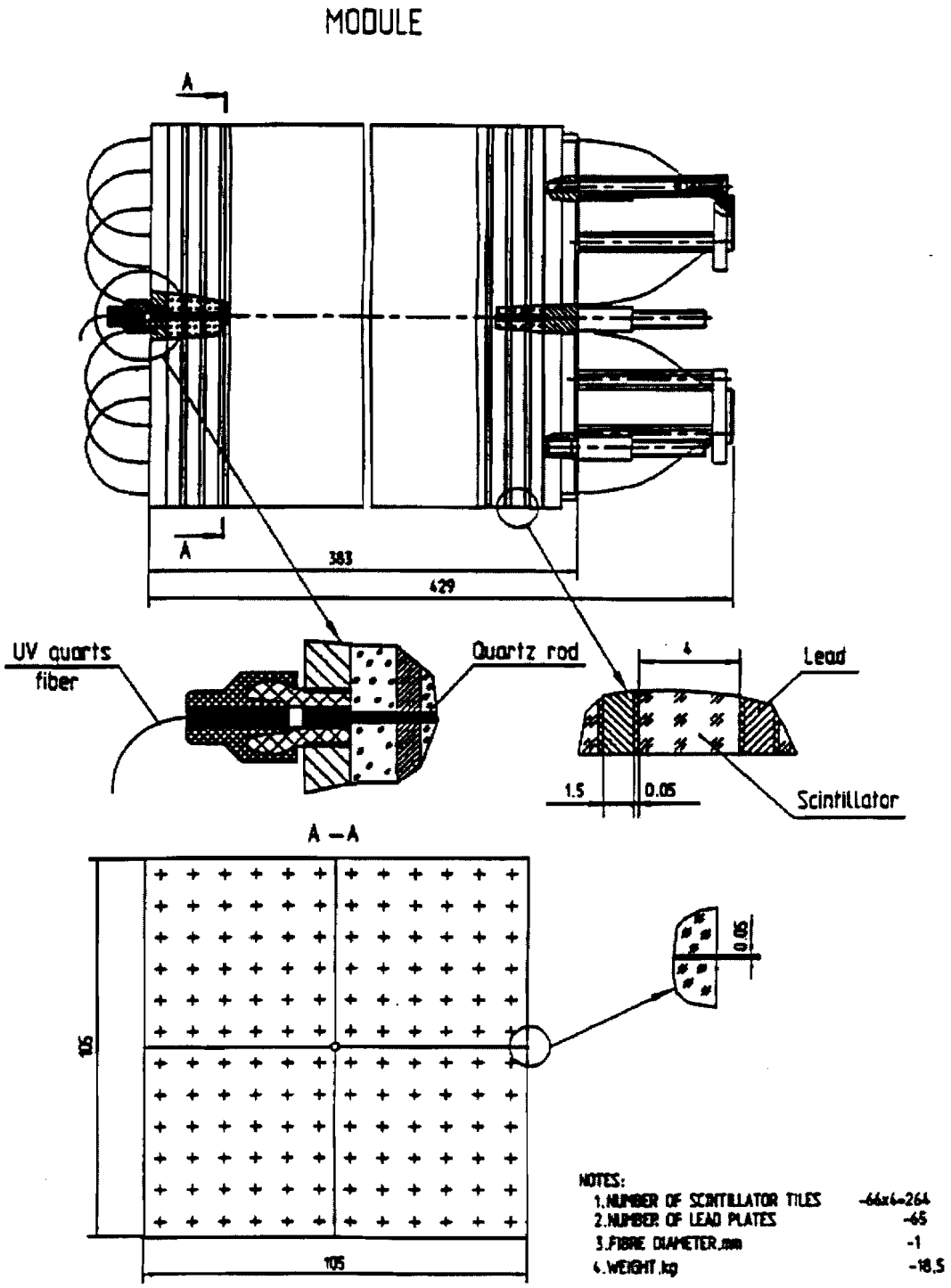


Figure 2-4. Diagrams and section views of the Lead-Scintillator module. Source: Kehoe, W. L., et al. PHENIX Conceptual Design Report. 29 January 1993, pg. 2-3.

66 alternating layers of lead and scintillating tiles. The 1.5 mm thick lead and a 4.0 mm thick polystyrene based scintillator sheets are separated by white reflecting paper for optical isolation. Light is contained in the tiles by coating each edge with reflective paint. Readout is to be achieved using Bicron's model BCF-99-29a wavelength shifting (WLS) fibers running the entire depth of the sandwich. A model FEU115M photomultiplier tube will be used to convert scintillation light to an electrical signal. Four shish-kebab towers placed in a 2 x 2 array comprise one module.

As seen in Figure 2-4, the each tower contains 5.25 cm x 5.25 cm tiles to produce a module measuring 10.5 cm x 10.5 cm. This configuration will give four channels for one module and a resulting segmentation capability of 5.25 x 5.25 cm^2. The section view A-A of Figure 2-4 indicates each tower has a 6 x 6 array of WLS fibers. The outer fibers of each tower are placed closer to the edges to compensate for light reflections. At each end of the tower, the fibers are grouped, epoxied, trimmed and polished. This bundle is held securely in a tube aligned on the tower axis for connection to its own PMT. An aligning rod is inserted into the common intersection point between the four towers during installation. Once installation is complete, a quartz rod illustrated in Figure 2-4 is inserted to send calibration light to each tower. The entire module is held together in compression with a stainless steel casing. As with the PbGl modules, the PbSc modules are arranged into a larger supermodule configuration.

The supermodule for PbSc will be an 8 x 8 array of individual modules attached to a 10 cm thick aluminum backplane. The backplane will be machined to accept the modules and provide access to the grouped fibers. Mounting hardware is provided to

secure each supermodule to the wall with space for mounting the PMTs. Once the supermodule is successfully installed, stainless steel is tack welded around the entire piece to create a dust-free and light-tight enclosure. Three walls of the PHENIX calorimeter will each contain about 25 PbSc supermodules.

Chapter 3

Constant-Fraction Discriminator Design

3.1 Introduction

In an effort to reduce size, power and cost in large, multichannel nuclear applications, integrated circuit technologies are currently being employed. Two common types of timing measurement circuitry are leading-edge discriminators (LEDs) and constant-fraction discriminators (CFDs). Ideally, the timing circuitry will introduce only a fixed delay into the measurement; however, variations in the detector and non-ideal properties of the timing circuits add some level of uncertainty in the measurement. After discussing the timing uncertainties involved in the timing measurement, the characteristics of leading-edge discriminators and energy-corrected leading-edge discrimination will be discussed. Several CFD shaping networks are presented, and a selected subset of these shaping methods are considered for the PHENIX PbSc CFD. The features of constant-fraction discrimination will be detailed, and the design of a monolithic CFD will be presented.

3.2 Timing Measurement Uncertainties in the PHENIX EMCal

3.2.1 Timing Uncertainties Inherent to the PHENIX Detector

Timing measurement uncertainties originate from several sources, and several basic unknowns are inherent to the PHENIX detector. Since the particles to be collided travel in a cloud as discussed before, there is uncertainty in the location of the collision defined by some volume. For discussion, assume the volume is a sphere and the detector is located some arbitrary distance away. Particles emitted on the detector side of the sphere travel a shorter distance to the detector than particles emitted on the side opposite the detector. The added travel distance through the sphere's diameter translates to a delayed arrival time at the detector. A second uncertainty in the timing is the energy deposition inside the detector. Ionizing radiation emitted from a collision can travel into the scintillating medium at various depths before depositing its energy, and the required time for scintillation light to propagate to the end of the detector will vary with this depth. Variations in the output signal response of the PMT readout devices will also add an uncertainty to the measurement.

3.2.2 Uncertainties in a Timing Discriminator

3.2.2.1 Time Walk

One source of error in a timing discriminator is time walk, the change in discriminator firing time as a function of input signal amplitude or risetime. Consider the two potential situations for linear-edge signals illustrated in Figure 3-1, and assume a logic pulse is generated when the input signal crosses a fixed threshold (i.e. neglect

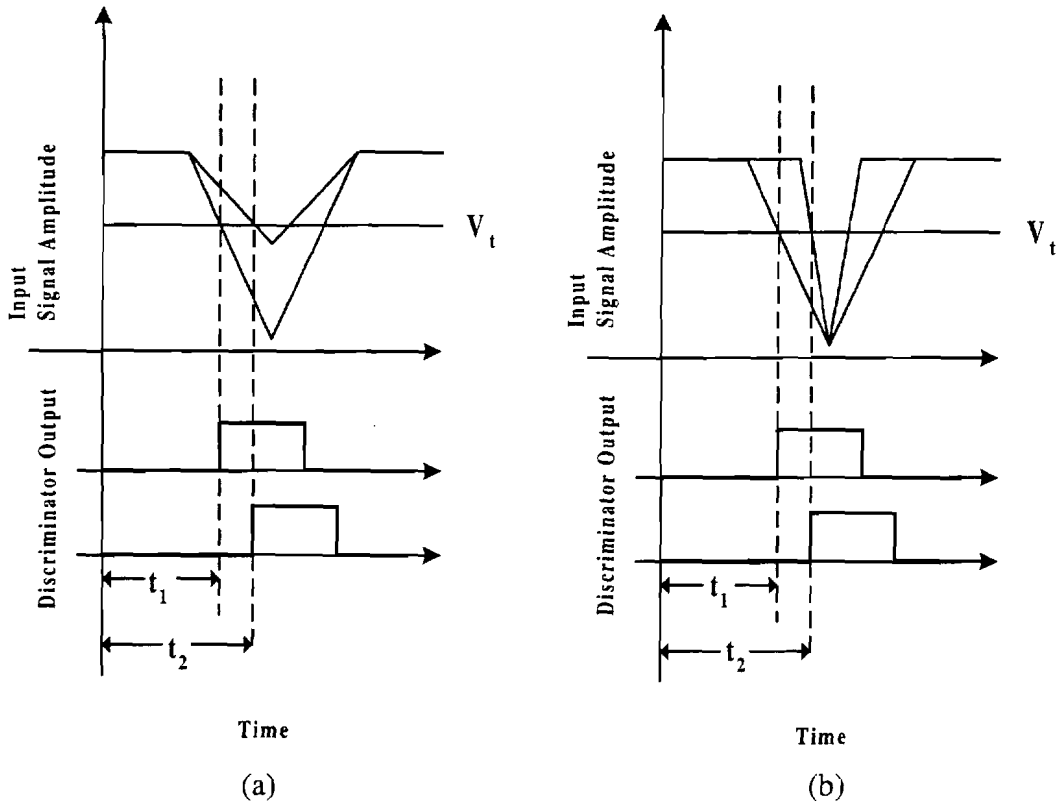


Figure 3-1. Illustration of timing discriminator time walk for input signals with equal peak times. (a) Amplitude-dependent time walk. (b) Risetime-dependent time walk.

comparator response time). Figure 3-1(a) illustrates amplitude-dependent time walk for two signals with equal peaking times. For signals with a larger amplitude, the threshold crossing, t_1, occurs before the smaller amplitude signal threshold crossing, t_2. This difference in time between t_1 and t_2 is the time walk. The timing diagram in Figure 3-1(b) depicts risetime-dependent time walk for two signals with equal amplitudes. The signal possessing the slower risetime crosses the threshold, V_T, before the signal with a faster risetime, where the risetime is defined here as the time required to reach the maximum amplitude. Once again, the difference in the threshold crossing times is the time walk, and this variation reduces the resolution of the system.

Another time walk phenomenon is referred to as comparator time walk. This time walk is due to the non-ideal properties of the timing discriminator. Comparator walk has been described using a charge-sensitivity model [18]. This model asserts that there is a required amount of charge to be deposited between the comparator inputs after a threshold crossing to trigger the comparator. A sufficient amount of charge to trigger the comparator may occur along an input signal leading-edge or after the signal has reached a maximum. Comparator time walk is greatly influenced by characteristics of the input signal. Input signal under-drive, over-drive and signal slope through the threshold crossing have been shown to influence timing error introduced by comparator walk [19, 20]. Furthermore, dc offset voltages at the comparator input influences the amount of charge in the charge-sensitivity model required to trigger the comparator. In practice, the elimination of the input dc offset voltage serves as a time walk adjustment.

3.2.2.2 Timing Jitter

Timing jitter is degradation in timing performance due to detector variations and the presence of electronic noise. The jitter due to electronic noise can be understood by considering a linear-edge signal passing through a comparator threshold. In Figure 3-2, a linear-edge signal passes through an uncertainty region, σ_v, around the average threshold voltage, Vt_{avg}. This region of uncertainty is representative of the electronic rms noise in the system referred to the threshold input. As the signal enters the rms noise region at time, t_1, until it leaves the noise region at time, t_2, there is an uncertainty, σ_t, as to when the threshold is crossed.

The full timing jitter expression is based on the triangle rule [21] as

$$\sigma_t = (\sigma_v / K) + \delta, \tag{3-1}$$

where σ_t is the rms timing jitter, σ_v is the rms noise voltage referred to the input, K is the slope of the input signal through the threshold and δ is an added jitter component introduced by signal-shape variations from the detector. To minimize timing jitter, the rms noise must be minimized while the signal slope through the threshold crossing must be maximized. The δ component in Equation 3-1 is minimized through the choice of an acceptable detector. For a fixed detector, the gain of the discriminator is set by the detector's dynamic range, and the first term in Equation 3-1 must be minimized through bandwidth considerations. Input referred rms noise in Equation 3-1 is related to bandwidth for a white noise source by

$$\sigma_v = \sqrt{S_i \cdot f_n}, \tag{3-2}$$

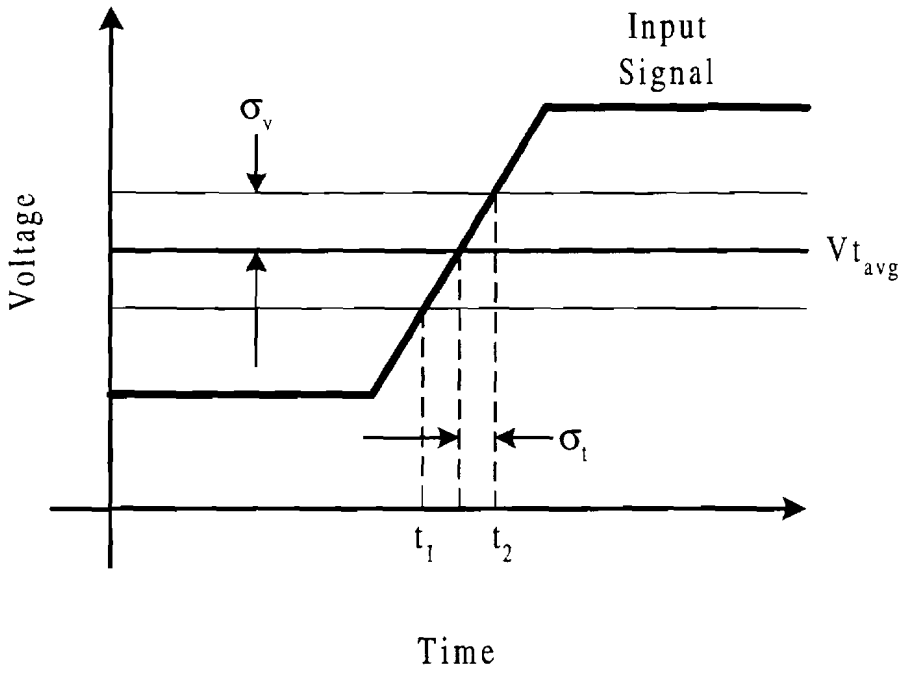


Figure 3-2. Illustration of timing jitter due to electronic noise.

where S_i is the input noise spectral density in V^2/Hz and f_n is the circuit noise bandwidth in Hz. Equation 3-2 indicates an increase in noise with increasing bandwidth. For input signals with a finite risetime (or finite slope), increasing the circuit bandwidth will increase the circuit's output signal slope up to that of the input slope. Once the circuit possesses enough bandwidth to preserve the input risetime, any additional bandwidth will only add noise in the timing jitter expression. This was the approach taken in the design of the CFD zero-crossing comparator discussed later.

3.3 Timing Discriminator Circuits

3.3.1 Simple Leading-Edge Discriminator

Leading-edge discrimination compares an input signal to a fixed reference and outputs a logic pulse when the input crosses that fixed threshold. Large input signals generate outputs close to the signal start time, but signal amplitudes close to the threshold generate outputs close to the peak time as seen previously in Figure 3-1(a). Leading-edge discrimination generates amplitude-dependent time walk sometimes referred to as leading-edge time walk. LEDs are also susceptible to the risetime-dependent time walk discussed in **Section 3.2.2.1**.

For a linearly increasing signal, the propagation time in an LED (or the time required to cross a fixed threshold) can be determined from Figure 3-3. By applying basic rules of similar right triangles, the propagation time is given by

$$\frac{t_c}{t_{rise}} = \frac{V_t}{V_{pk}}, \qquad \text{for } V_{pk} > V_t, \tag{3-3}$$

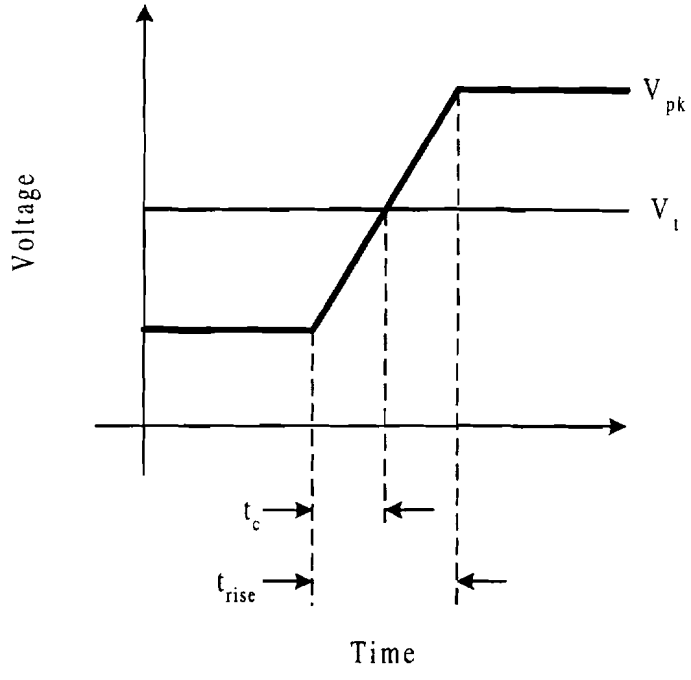


Figure 3-3. Illustration of the threshold crossing time for a linear-edge input signal.

where t_c is the crossing time, V_t is the fixed threshold, t_{rise} is the signal peaking time and V_{pk} is the signal peak amplitude. Equation 3-3 can be rearranged to become

$$t_c = \frac{V_t \cdot t_{rise}}{V_{pk}}, \qquad \text{for } V_{pk} > V_t . \tag{3-4}$$

Equations 3-3 and 3-4 are defined only when $V_{pk} > V_t$ because t_c is only defined for signal peak amplitudes above the threshold voltage. This requirement also indicates that the crossing time will always be less than the signal risetime. Figure 3-4 shows the relationship between propagation time and input amplitude for the expression in Equation 3-4. The upper limit for the crossing time, $tmax_a$, is set by the threshold setting, V_t. The minimum crossing time, $tmin_a$, is set by a maximum input signal, V_{limit}, from the detector. Crossing times are also related to variation in the input signal risetime for peak amplitudes above the threshold as seen in Figure 3-5. The minimum crossing time, $tmin_r$, is determined by the fastest input signal risetime while the maximum crossing time, $tmax_r$, is set by the slowest risetime signal. These relationships indicate that the variation in crossing time is actually the time walk introduced by the LED. Thus, simple leading-edge discriminators provide effective timing resolution only for applications with a small dynamic range of input amplitude and risetime or for signals with a very fast risetime.

3.3.2 Energy-Corrected Leading-Edge Discrimination

A common approach considered for implementation in some nuclear timing measurements is energy-corrected leading-edge discrimination. For example, particle physics experiments take corresponding energy and timing measurements. The timing

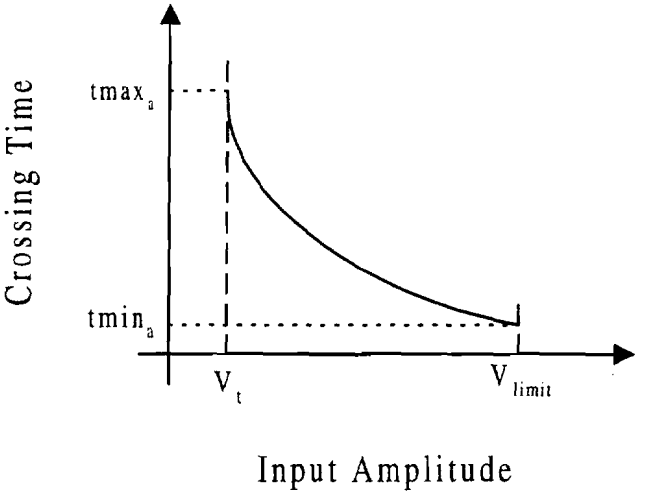


Figure 3-4. Illustration of crossing times in leading-edge discriminators as a function of input amplitude.

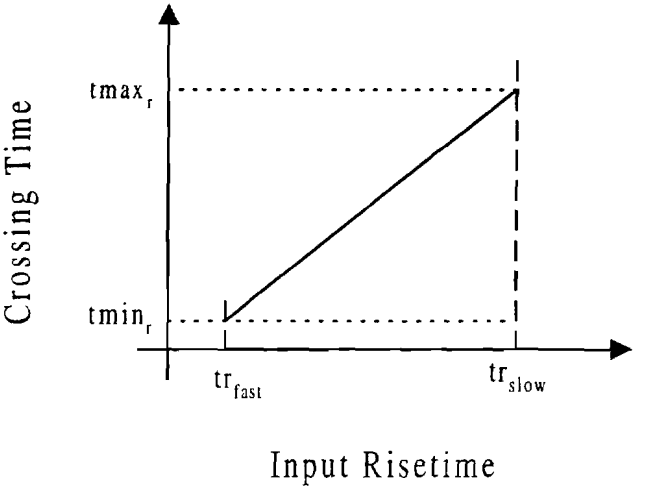


Figure 3-5. Illustration of crossing times in leading-edge discriminators as a function of input risetime.

measurement is made with a simple leading-edge discriminator circuit while a simultaneous energy measurement (related to input amplitude) is recorded. With a sufficient amount of test data, relationships derived between the measured energy and the corresponding LED time walk are used to perform off-line walk correction.

A block diagram in Figure 3-6 shows the energy-corrected leading-edge discrimination technique with the on-line and off-line processes delineated. In the processing of experimental data off-line, the variances in the different measurements and time walk correction function introduce variance components in the final timing measurement not seen in simple LED measurements. Although the specific processes involved in the combination of these variances is not presented, some representative quantities help convey the idea of added variance in the final energy-corrected leading-edge discriminator technique. Energy and timing measurement components of the block diagram have variances $(\sigma_E)^2$ and $(\sigma_{LED})^2$, respectively. A new energy related variance, $(\sigma_{OLP})^2$, is generated when the experimental time walk correction data is generated from experimental energy data and TW(E). The final off-line timing data variance is given by

$$(\sigma_T)^2 = (\sigma_{LED})^2 + (\sigma_{OLP})^2 + (\sigma_{LED\text{-}OLP})^2, \qquad (3\text{-}5)$$

where $(\sigma_T)^2$ is the final timing system variance and $(\sigma_{LED\text{-}OLP})^2$ is an additional variance due to correlation between $(\sigma_{LED})^2$ and $(\sigma_{OLP})^2$. The significance of the correlation component, $(\sigma_{LED\text{-}OLP})^2$, is determined by the time delay between the LED and energy measurement. If variance due to electronic noise is considered, a long delay will cause only the lowest frequency noise components common to both measurements to be

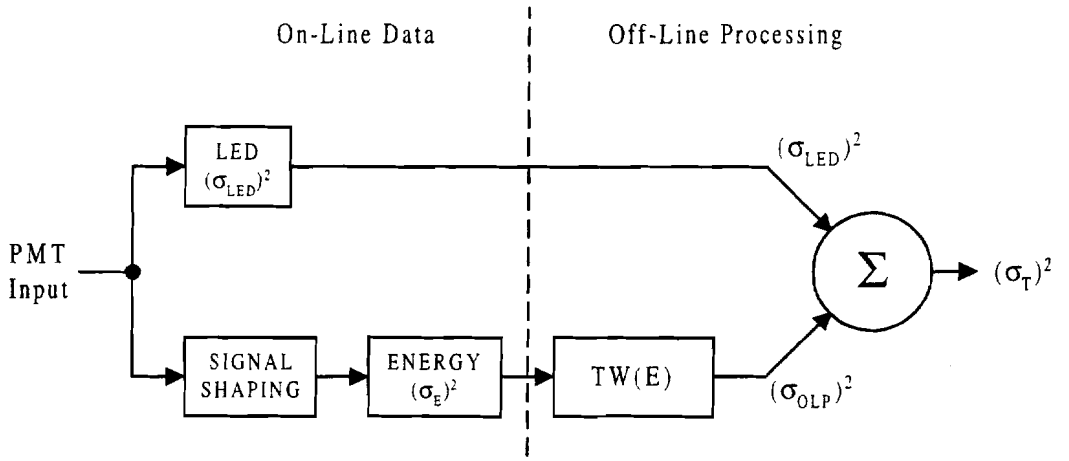


Figure 3-6. Block diagram of the energy-corrected leading-edge discrimination technique.

subtracted; however, shorter delays will selectively subtract out higher frequencies. Commonly in this type of correlated data, certain phase relationships between noise in the two measurements may also be such that the subtraction becomes additive (i.e. subtraction of a negative quantity). Delays in the timing and energy measurements are typically due to signal shaping in the energy channel. Signal shaping time in the energy channel for the PHENIX PbSc calorimeter is limited by the passive integrator introduced in **Chapter 1**.

In LED timing measurements covering a wide dynamic range of input signals, the time walk error is usually the largest source of timing error. The disadvantage of added timing variance with the energy-corrected leading-edge method is far outweighed by the advantages introduced by the time walk correction. The effectiveness of this method to improve timing resolution depends on the application and minimizing variances in the original test data.

3.3.3 Constant-Fraction Discriminator

The constant-fraction discriminator was first reported in the late 1960's by Gedcke and McDonald [22, 23]. Constant-fraction discrimination shaping illustrated in Figure 3-7 produces a bipolar output signal from a unipolar input signal with the zero-crossing providing a precise timing marker. A fraction, V_f, of the input signal is summed with a delayed copy, V_{td}, of the input signal to generate this bipolar signal. The zero-crossing in this method is invariant with input signal amplitude and risetime for a properly selected delay and fraction. Figure 3-8 shows a common architecture for a CFD

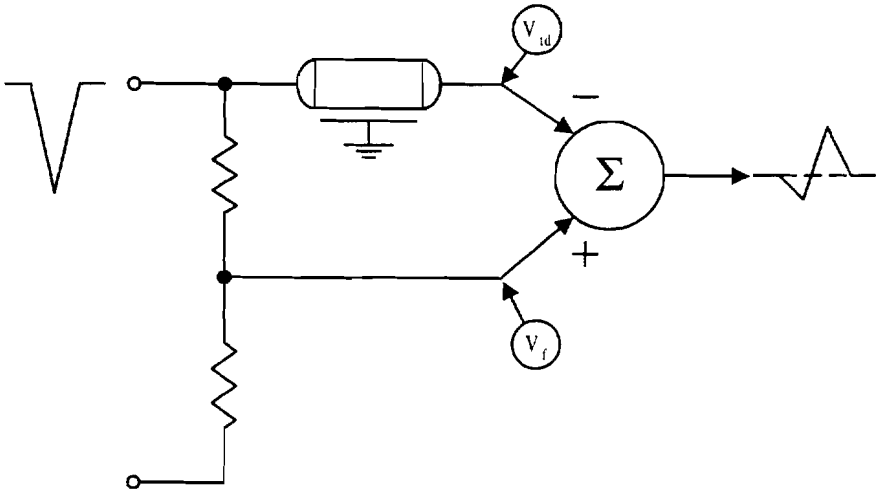


Figure 3-7. Diagram of the constant-fraction discrimination shaping network.

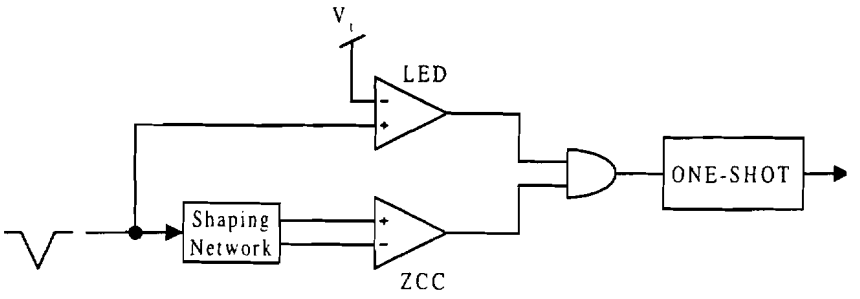


Figure 3-8. Block diagram architecture of a constant-fraction discriminator.

circuit. The shaped bipolar signal provides the input to a zero-crossing comparator (ZCC), while a leading-edge discriminator compares the input signal to an adjustable threshold. The output of the ZCC is gated with the output of the LED through a logical AND gate. When both inputs to the gate are a logic high, the gate will trigger. Typically, a one-shot multivibrator circuit is included to prevent multiple triggering on the same input pulse. The LED threshold adjustment prevents triggering on noise and provides settings for desired minimum amplitude inputs. Because the shaped signal generates the precise timing marker, the ZCC should control the AND gate triggering. If the LED arms the logic AND gate after the ZCC, the time walk will be determined by the LED.

3.4 CFD Timing Methods

3.4.1 Introduction

The constant-fraction discrimination shaping network can be realized in various manners. Differing combinations of fraction and signal delay time change the characteristics of the shaping network. For a properly chosen shaping network, CFD circuits can ideally provide zero-crossing times that are insensitive to input signal amplitude variations or insensitive to both input signal amplitude and risetime variations. The two types of CFD timing are true-constant-fraction (TCF) timing and amplitude-risetime-compensated (ARC) timing. After discussing the different types of ideal constant-fraction timing, practical shaping networks are discussed with emphasis placed on networks realizable in standard CMOS IC processes.

3.4.2 True-Constant-Fraction Timing

In TCF timing, the zero-crossing of the bipolar output signal occurs during or after the peak amplitude of the fraction signal. To ensure TCF timing, the delay and fraction circuit values are found using the relationship [21]

$$t_d > t_r (1 - f), \tag{3-6}$$

where t_d is the delay time, t_r is the input signal risetime and f is the fraction value. In many applications, the input signal has a short pulse width. For TCF timing to apply in these situations, the delay must be short enough to cause the zero-crossing to occur during the peak of the input fraction signal.

In the TCF shaping method, the zero-crossing time is invariant to input signal amplitude changes. Figure 3-9 illustrates TCF shaping for two linear-edge, flat-top pulses, V_1 and V_2, with equal risetime. Figure 3-9(b) shows the inverted fraction signals, V_{f1} and V_{f2}, and the original signals delayed in time, V_{d1} and V_{d2}. The summation of these two signals is shown in Figure 3-9(c). Both signals, V_{shape1} and V_{shape2}, cross zero at the same point in time, t_{zc}. TCF shaping for two equal amplitude inputs with different risetimes is illustrated in Figure 3-10. As the summation shows in Figure 3-10(c), the TCF shaping network zero-crossing time exhibits a dependence on input signal risetimes. As seen in the illustrations in Figures 3-9 and 3-10, the TCF shaping method can provide excellent timing resolution over a wide dynamic range of input signal amplitudes for a fixed risetime.

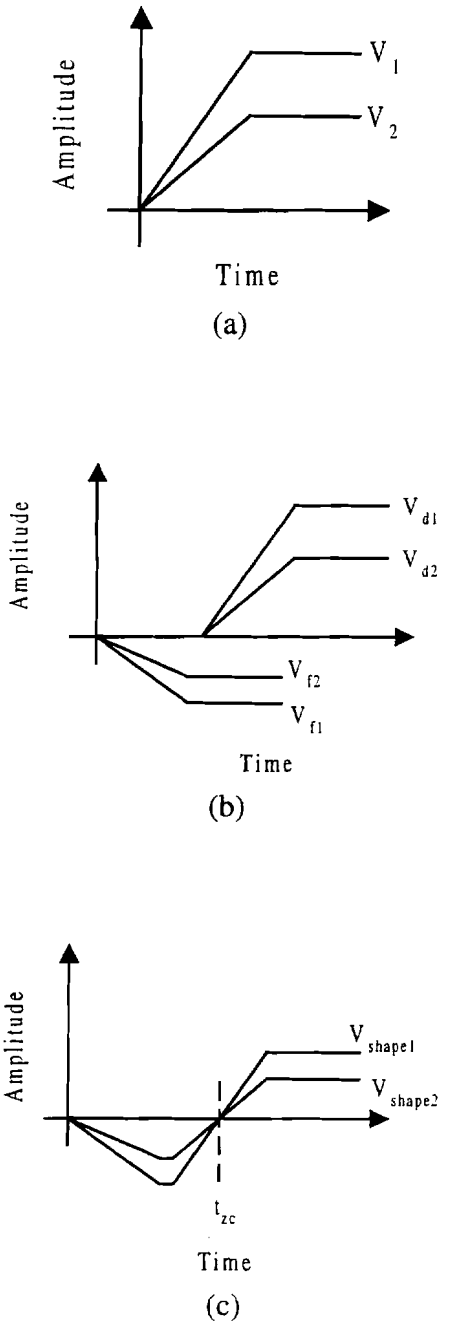
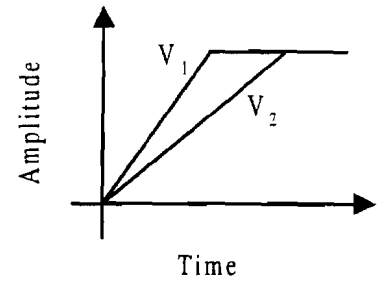
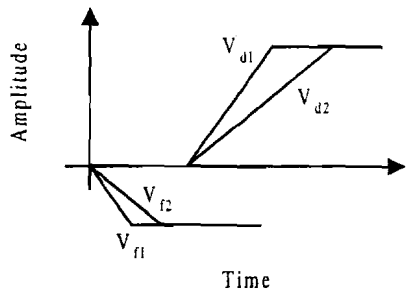


Figure 3-9. Illustration of true-constant-fraction timing for equal risetime inputs. (a) Inputs V_1 and V_2. (b) Attenuated, inverted copies and delayed copies. (c) Summed signals showing invariant zero-crossing with variations in input amplitude.



(a)



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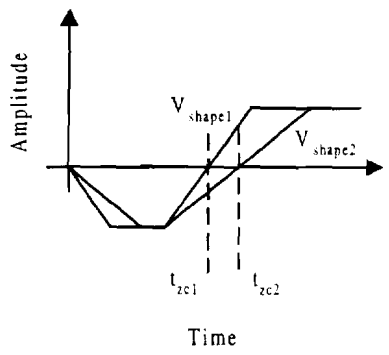


(c)

Figure 3-10. Illustration of true-constant-fraction timing for equal amplitude inputs. (a) Inputs V_1 and V_2. (b) Attenuated, inverted copies and delayed copies. (c) Summed signals showing variation in the zero-crossing with variation in input risetime.

3.4.3 Amplitude-Risetime-Compensated Timing

Constant-fraction discrimination shaping produces ARC timing when the zero-crossing is invariant with input signal amplitude or risetime variations. To guarantee ARC timing, the zero-crossing time must occur before the fraction signal has reached a maximum. The delay and fraction values required to achieve ARC timing are related by the equation [21]

$$t_d < t_{r(min)} (1 - f), \tag{3-7}$$

where t_d is the delay time, $t_{r(min)}$ is the smallest input signal risetime and f is the fraction value. Equation 3-7 applies to linear input pulses and ensures ARC timing for any input signal risetime greater than $t_{r(min)}$. An illustration of ARC signal formation for an ideal CFD is shown in Figures 3-11 and 3-12. The independence of zero-crossing times on input signal amplitude and risetime variations for flat-top, linear-edge pulses is shown in Figures 3-11 and 3-12, respectively.

3.5 CFD Shaping Methods

3.5.1 Traditional CFD Shaping

The constant-fraction shaping circuit introduced by Gedcke and McDonald used a coaxial cable to generate the delayed signal. This approach was utilized for many years due to its minimal signal degradation and excellent timing performance. Variable delays were easily realized in early instrumentation by changing the length of an externally connected cable. The corresponding fraction circuit could then be easily trimmed with external trim-pot adjustments as well.

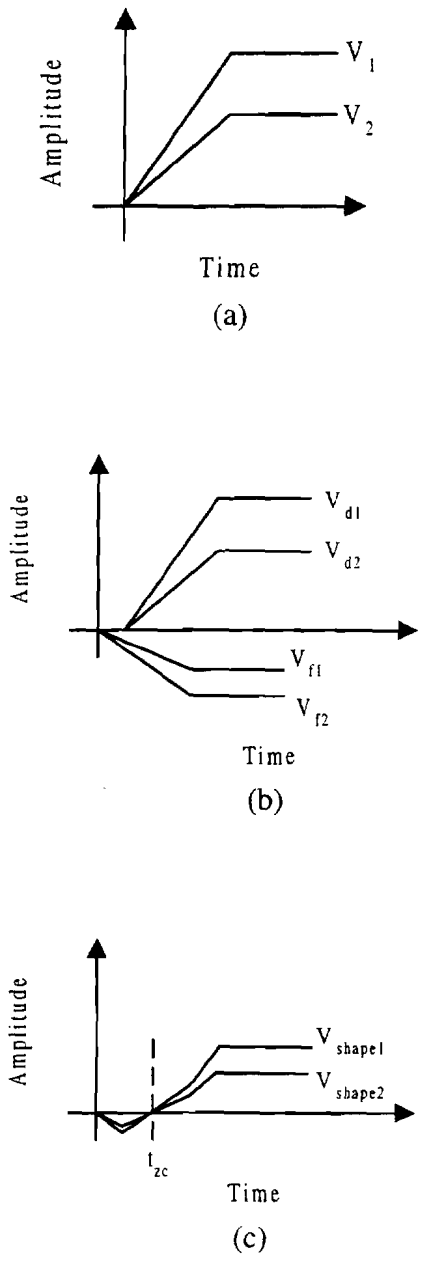


Figure 3-11. Illustration of amplitude-risetime-compensated timing for equal risetime inputs. (a) Inputs V_1 and V_2. (b) Attenuated, inverted copies and delayed copies. (c) Summed signals showing invariant zero-crossing with variations in input amplitude.

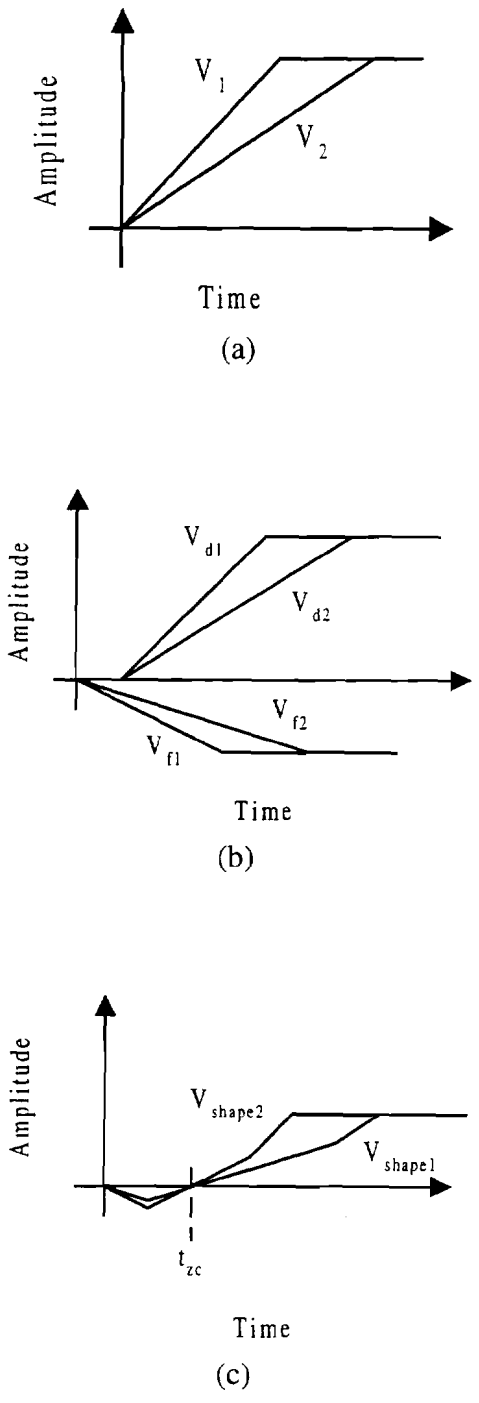


Figure 3-12. Illustration of amplitude-risetime-compensated timing for equal amplitude inputs. (a) Inputs V_1 and V_2. (b) Attenuated, inverted copies and delayed copies. (c) Summed signals showing invariant zero-crossing with variations in input risetimes.

With the advent of large nuclear physics experiments and other nuclear applications, a need arose for integrated electronics to reduce size, power consumption and overall costs. In spite of the savings from integrating the readout electronics, the number of extra connections and cumbersome cables required to implement coaxial cable delays for timing measurement was not feasible. This limitation has generated much interest in replacing the external delay-line with integrated CFD shaping methods. The major interests in the full integration of a signal shaping circuit are methods that require minimal die area and preferably consume no extra power from the supplies. Several integratable shaping methods are presented and evaluated based on their usefulness in the PHENIX EMCal readout electronics. Signal shaping using a delay cable was also investigated for comparison to the fully integratable methods.

3.5.2 C-R Differentiator Shaping Method

The C-R differentiation method [8] is one shaping method which does not require a fraction circuit. For unipolar input signals that possess a sign change in the derivative, an appropriate C-R differentiator time constant will produce a bipolar output signal with a zero-crossing near the input signal peak. This signal is then used as the input to the zero-crossing comparator. The amount of shaped signal over-drive and slope through the zero-crossing are determined by the trailing-edge of the input signal. This can introduce more timing jitter into the measurement in the presence of white noise and possibly increase time walk. However, the high-pass nature of the differentiation could provide lower timing jitter in the presence of high flicker noise. Due to the longer trailing-edge

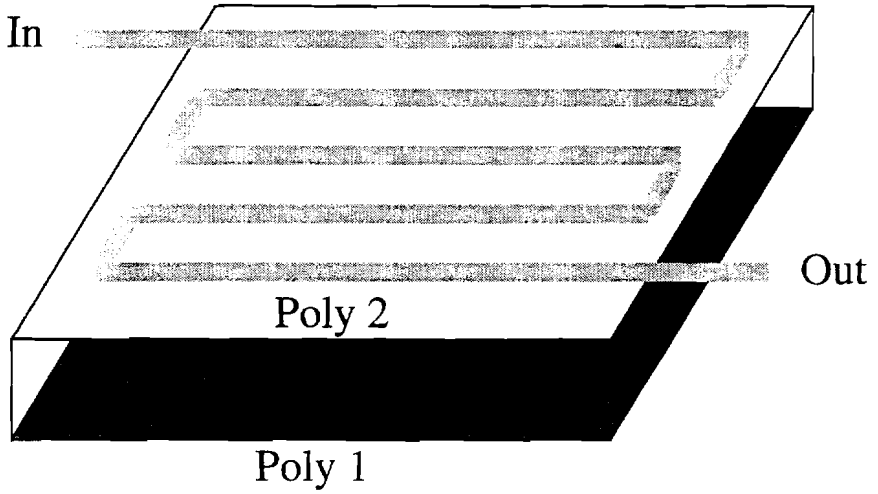
produced by the PHENIX PbSc PMTs (i.e. since timing measurements dependent on the faster leading-edge would be better), the C-R differentiation shaping is not considered further in this work.

3.5.3 Binkley CFD Shaping Method

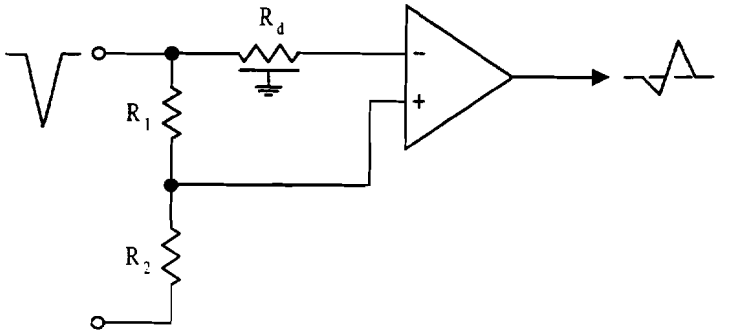
The Binkley CFD shaping method [15] utilizes a 4-stage Gaussian filter to realize the delay signal for traditional constant-fraction shaping. The input signal is delayed through the 4-pole network and summed with a fraction of the original signal. Although this approach seems attractive from performance perspectives, the area required to realize this 4-stage filter is relatively large. This size requirement is undesirable for the PHENIX readout electronics design; therefore, the Binkley method was not be pursued in this work.

3.5.4 Distributed R-C Delay-Line Shaping Method

The distributed R-C delay-line introduced by Simpson, et al, [16] is another easily realizable shaping technique for monolithic implementation. A diagram of the delay-line is shown in Figure 3-13(a), and an illustration of the shaping network is shown in Figure 3-13(b). This distributed R-C delay-line is realized as a serpentined layer of polysilicon above a second layer of grounded polysilicon producing a lossy transmission line. This lossy transmission line generates delay along with signal amplitude degradation and signal dispersion. These undesired characteristics affect the shaped signal as does the



(a)



(b)

Figure 3-13. Illustration of the distributed R-C delay-line shaping for constant-fraction discrimination. (a) Illustration of the serpentine polysilicon layers. (b) Circuit diagram of the shaping network.

lowpass filter. The distributed R-C delay-line shaping was chosen as a candidate for the PHENIX EMCal CFD implementation.

The distributed R-C delay-line was initially modeled with the lossy transmission line Umodel provided by HSPICE [24, 25]. This utility from HSPICE takes several forms of input data, and the model chosen in this work required geometrical input data. The delay-line was broken into several "lumps" in the HSPICE Umodel as shown in Figure 3-14. Line resistance, inductance, and capacitance were calculated along with reference plane resistance for the geometries and process charateristics given. In Table 3-1, the process parameters and dimensions are given for the polysilicon serpentine delay-line from the Orbit Semiconductor 1.2-μ n-well process. Umodel values for each lump parameter were calculated by HSPICE based on per unit line length. Table 3-2 gives the lump model values for the 4.8 μm wide delay-line calculated by HSPICE for the Orbit process. To calculate a single lump parameter, the values from Table 3-2 were multiplied by the line length and then divided by the number of desired lumps in the model.

Simulation data was based on a delay-line approximated with 20 lumps. An explicit 20-lump model for the HSPICE Umodel was originally generated for use in the noise analysis because the HSPICE Umodel utility models the line resistance as noiseless. Although the lump Umodel parameter values calculated by HSPICE in Table 3-2 were accurate, an ac analysis of the two models further showed up to a factor of 10 lower bandwidth in the explicit model versus the HSPICE Umodel data, suggesting a possible error in the HSPICE Umodel utility. HSPICE application notes for the lossy transmission line model [25] indicate a range of valid geometries for the lossy transmission line model

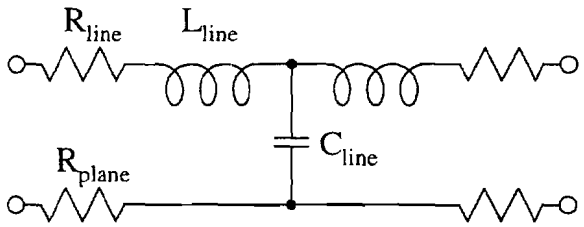


Figure 3-14. Diagram of one lump in the HSPICE lossy transmission line Umodel.

Table 3-1. Table showing the Orbit Semiconductor 1.2-μ n-well process parameters for the distributed R-C delay-line.
Adapted from: Simpson, M. L., G. R. Young, R. G. Jackson and M. Xu, "A Monolithic, Constant-Fraction Discriminator Using Distributed R-C Delay Line Shaping," *IEEE Transactions on Nuclear Science*, Vol. 43, No. 3, June 1996, pp. 1695-1699.

Parameter Name	Description	Value Used in Simulation
WD	R-C line width	4.8 μm
TH	R-C line thickness	400 nm
HT	R-C line height	70 nm
KD	Relative dielectric constant of SiO_2	4
RHO	Resistivity of R-C line	8 μΩ-m

Table 3-2. Lump element values for the 4.8 μm wide delay-line fabricated in the Orbit Semiconductor 1.2-μ n-well process in per length units.

Parameter	Description	Value
R_{line}	Resistance in delay-line	4.167 MΩ/m
R_{plane}	Resistance in reference plane	833.3 kΩ/m
C_{line}	Capacitance in delay-line	2.256 nF/m
L_{line}	Inductance in delay-line	17.27 nH/m

investigated. The geometries used in the Orbit process for this work fell outside these valid geometrical ranges; however, these two models exhibited similar transient response results for delay times and amplitude degradation. If the discrepancies in the ac response of the two models was due to skin effect considerations, the HSPICE Umodel should have produced a lower bandwidth response than the explicit model as opposed to the higher bandwidth results obtained. Simulation output data supplied warnings concerning the model values falling outside valid ranges, but the simulation was executed. Due to these discrepancies, the transient analysis and noise data for this work was determined using the explicit model.

3.5.5 Lumped-Element R-C Lowpass Filter Shaping Method

Turko and Smith [14] reported a shaping network for constant-fraction shaping using a single R-C lowpass filter to generate the delay signal. The lowpass filtered signal is summed with a fraction of the input signal as shown in Figure 3-15. This method is attractive for use in the PHENIX detector because it requires much less die area than the Binkley CFD 4-pole filter. The R-C lowpass filter shaping suffers from two disadvantages. First, the lowpass filter, while producing delay, also causes signal amplitude reduction due to integration. This feature results in a zero-crossing slope degradation in the shaped signal, but does provide for some filtering of higher frequency noise. This method was also chosen as a candidate shaping method.

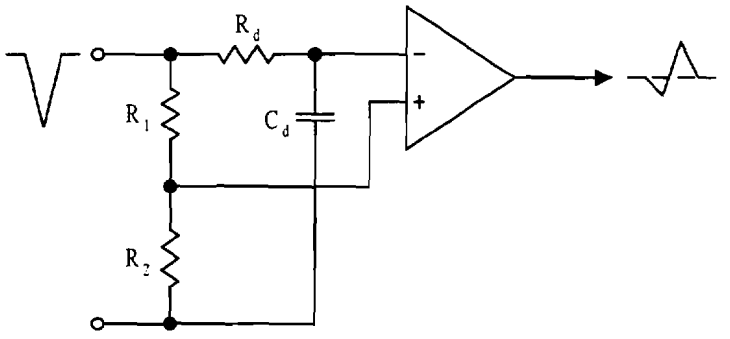


Figure 3-15. Illustration of the lumped-element R-C lowpass filter shaping method for constant-fraction discrimination.

3.5.6 Nowlin Shaping Method

The Nowlin shaping method [12, 13] was invented to produce an output signal optimized for low timing jitter. The Nowlin method illustrated in Figure 3-16 utilizes the lumped-element C-R differentiator along with a fraction circuit. A fraction of the original input signal is subtracted from the differentiated input signal. The extra lowpass filter at the output of the amplifier created by R_4C_2 represents the amplifier bandwidth. This approach produces a single real right-half-plane (RHP) zero with two left-half-plane (LHP) poles in the s-plane. Widder's theorem [26] states that the inverse Laplace transform of any Laplace transfer function will possess at least as many zero-crossing as there are real zeros to the right of the pole with the least negative real part (in response to a linearly increasing leading-edge input signal). Nowlin has provided an analysis and optimized design equations for his shaping network [12, 13]. The component values in Figure 3-16 to obtain minimum timing jitter are found as

$$R_1C_1 = R_4C_2 = (0.42)t_c \tag{3-8}$$

and

$$R_3 = (0.88)R_2, \tag{3-9}$$

where t_c is the zero-crossing time of the shaped output signal. Since the zero-crossing comparator in the final CFD was composed of more than one amplifier, results using these equations serve as an approximation to the ideal situation described by Nowlin. The Nowlin method was the last shaping method chosen as a candidate for the PHENIX EMCal constant-fraction discriminator shaping network.

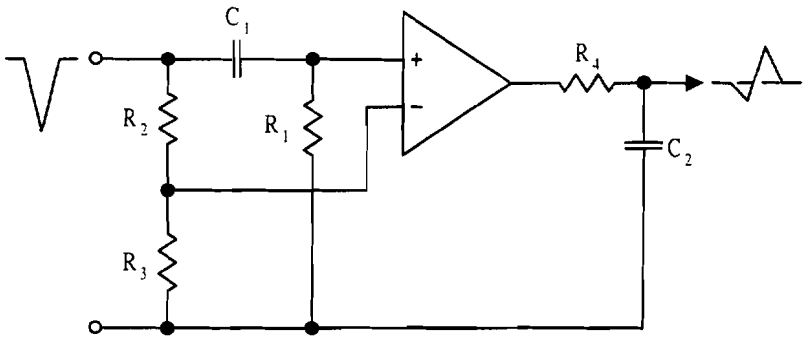


Figure 3-16. Illustration of the Nowlin shaping method for constant-fraction discrimination.

3.6 CFD Shaping Method Analysis

Several CFD shaping networks were considered as candidates for the PHENIX EMCal CFD timing circuit. The earliest work for this thesis involved comparisons between the lumped-element R-C shaping, the distributed R-C delay-line shaping and the ideal-delay line shaping networks. These shaping methods were analyzed using a - 20 mV pseudo-gaussian input signal approximating the PHENIX PbSc PMT signal and is shown in Figure 3-17. The zero-crossing comparator was approximated with cascaded stages of lowpass filtering (- 3 dB corner frequencies at 110 MHz) and gain. A white noise input source of ~ 400 nV/$\sqrt{\text{Hz}}$ at the shaping network input was used to perform timing jitter analysis. This large noise value at the input isolated the timing jitter due to the input noise source from timing jitter due to the inherent noise in the shaping network.

Since an explicit model for each length of the distributed R-C delay-line was required, simulation data was generated for delay-line lengths between 100 μm and 1000 μm in 100 μm increments. Figure 3-18 shows the delay associated with each line length based on the delayed signal's peak position time, and the same delay times were then determined for the lumped-element R-C shaping method. Initial comparisons were made between the lumped-element R-C lowpass filter and the distributed R-C delay-line. Figure 3-19 shows delayed signal amplitude degradation and delayed signal leading-edge slope degradation with increasing peak position delay. In both plots, the lumped-element R-C filter degradation was slightly more severe than the distributed R-C delay-line. After investigating these signal degradation characterisitcs, the fraction value, f, for the ideal

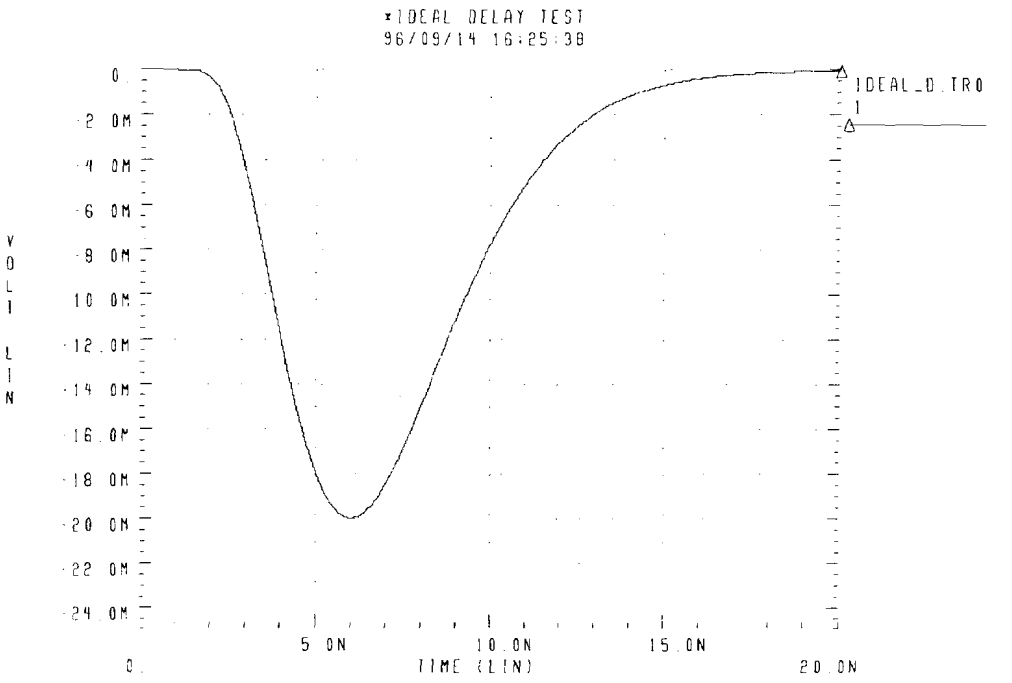


Figure 3-17. Plot of the pseudo-gaussian input used in simulation analysis.

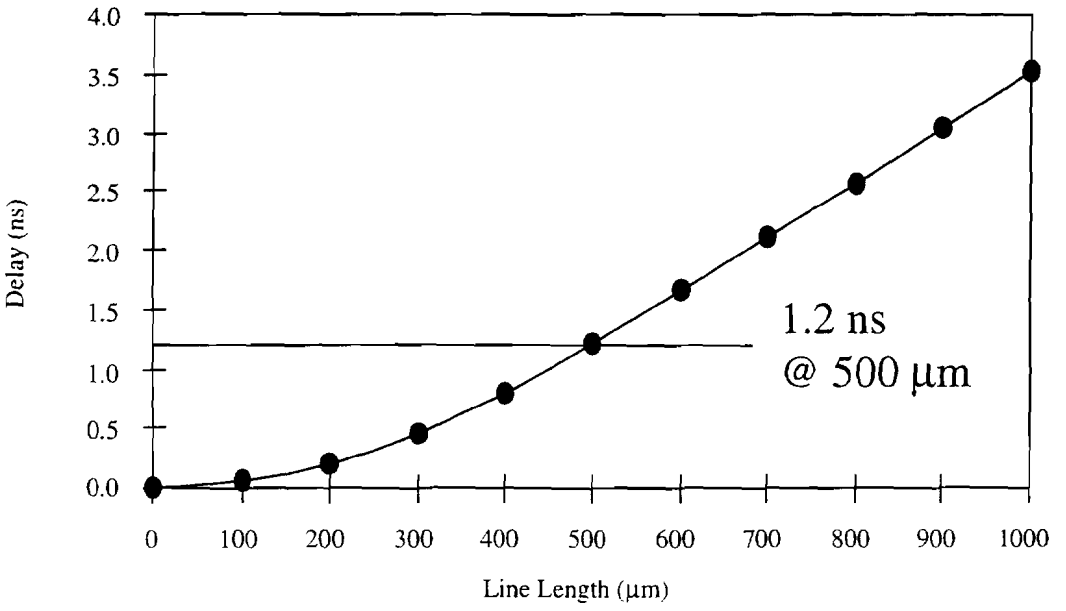


Figure 3-18. Plot of signal peak position delay with increasing distributed R-C delay-line length.

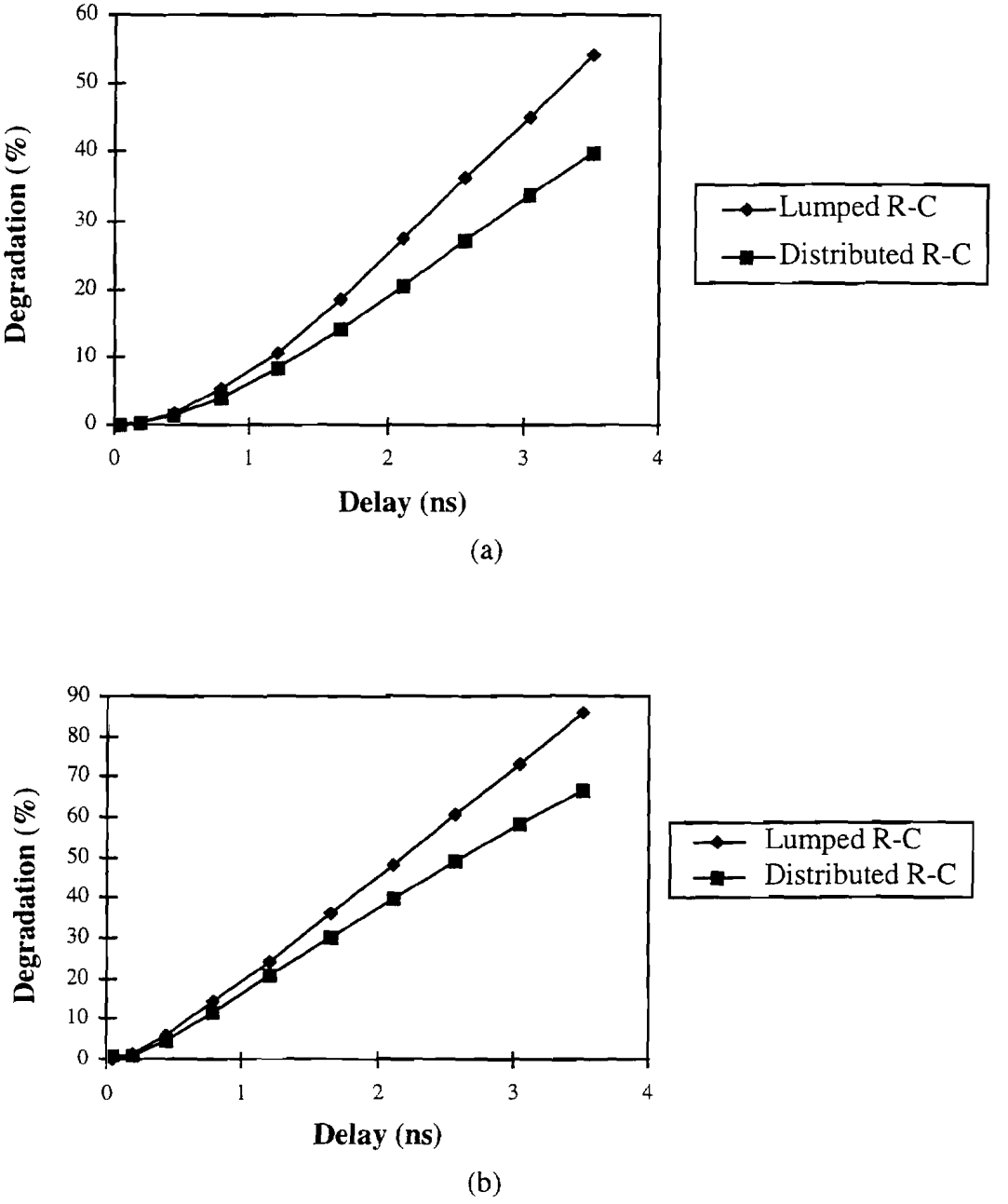


Figure 3-19. Plot of signal degradation for the lumped-element R-C lowpass filter and the distributed R-C delay-line with increasing peak position delay times. (a) Signal amplitude degradation. (b) Signal leading-edge slope degradation.

delay-line, the distributed R-C delay-line and the lumped-element R-C shaping methods were calculated using the relationship

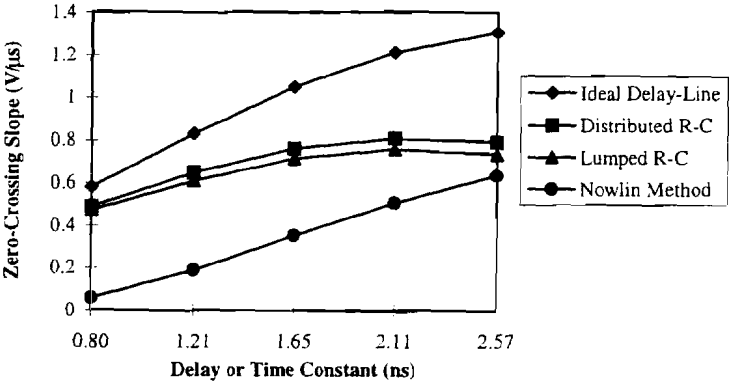
$$t_d = t_r(1 - f). \tag{3-10}$$

Shaped signal zero-crossing slope, total rms output noise and rms timing jitter were determined for these three methods with their comparison based on the delayed signal peak position time. Later in this work, the decision was made to include the Nowlin shaping method in the comparison. Since the Nowlin shaping method did not generate a delayed copy of the original input as the previous three methods, the comparison between all four methods was converted to delay times or time constants. Thus, the C-R differentiator time constant in the Nowlin method was set equal to the peak position delay times used in the other shaping methods investigated. The time x-axis used to compare methods in this work corresponds to a peak position delay time for the methods generating a delayed copy of the original. The time x-axis data points for the Nowlin method are the C-R differentiator time constants equal to these delay times.

As the delay time in the CFD shaping method was increased, the zero-crossing time of the shaped signal should have increased also. Because the distributed R-C delay-line and the lumped-element R-C shaping networks possessed severe attenuation and slope degradation for the longer delay-times, the zero-crossing times increased, reached a maximum and then began to decrease. This phenomenon introduced an undesireable charateristic in the comparisons desired for this work. For these reasons, the comparisons to be presented were based on the longest amount of delay where the zero-crossing time of the shaped-signal was still increasing.

Figure 3-20 shows the simulation data for the four shaping methods investigated. Each type of data was plotted versus increasing peak position delay or C-R time constant. Figure 3-20(a) shows the shaped signal slope through the zero-crossing for a - 20 mV peak pseudo-gaussian input. The ideal delay-line possessed the largest slope through the zero-crossing due to the pure delay with no attenuation. Lumped-element R-C and distributed R-C delay-line shaping exhibited zero-crossing slope rolloff at the longer delay times due to the amplitude and slope degradation in the delayed signal. Shorter C-R time constants severly attenuate the signal in the Nowlin method causing a small zero-crossing slope. Figure 3-20(b) shows the total rms noise at the output due to the ~ 400 $nV/\sqrt{Hz}$ white noise source. Nowlin shaping passed more noise to the output compared to the other shaping methods. Nowlin shaping also possessed a mostly flat output noise with C-R time constant due to the dominance of the amplifier bandwidths. Using the data taken in Figure 3-20(a) and 3-20(b), rms timing jitter was calculated by applying the triangle rule and plotted in Figure 3-20(c). Lower zero-crossing slope and higher output noise resulted in the Nowlin method possessing much higher timing jitter at shorter time constants. The ideal delay-line exhibited the optimum jitter performance. Lumped-element R-C shaping and the distributed R-C shaping methods were very close in timing jitter performance over the range of delay times shown. Distributed R-C delay-line shaping possessed slightly better jitter performance than the lumped-element R-C shaping.

Time walk introduced in the ZCC (the ZCC to be discussed later) for each method was also simulated. Each shaping method was analyzed for a 100:1 input signal



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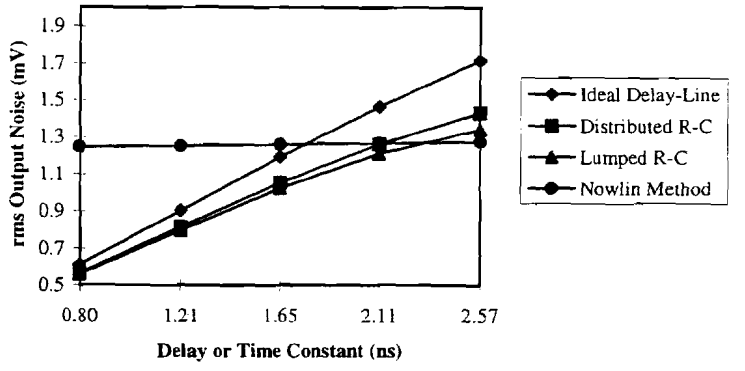

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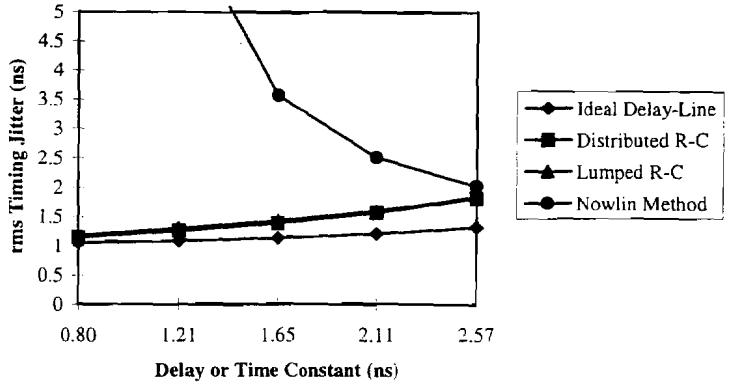


(c)

Figure 3-20. Plots of timing jitter components simulated in HSPICE for each shaping method investigated. (a) Shaped signal slope through the zero-crossing for - 20 mV input amplitude pulse. (b) Total rms output noise for ~ 400 nV/√Hz input white noise source. (c) The rms timing jitter applying the triangle rule.

amplitude dynamic range with a - 20 mV peak minimum signal. Figure 3-21 shows the time walk for each method with increasing delay times or C-R time constants. Each shaping method exhibited lower time walk with increasing delay time or C-R time constant. Since PMTs will be used in the PHENIX PbSc Electromagnetic Calorimeter, risetime induced variation was not considered here.

After reviewing rms timing jitter and time walk curves for each shaping method investigated, the shaping methods near to the peak position delay time of ~ 1.21 ns were chosen for development for the ideal delay-line, the distributed R-C delay-line and the lumped-element R-C shaping. The Nowlin shaping C-R time constant chosen for fabrication was ~ 2.3 ns. After selecting an appropriate set of shaping methods to have fabricated, time walk versus amplitude in 5 dB steps was determined for each of these methods and plotted in Figure 3-22. The time walk measurement was taken by determining some reference point in time along the ZCC output signal for a full-scale input (- 2 V peak). As the input amplitude was attenuated, the movement in time for each output relative to the full-scale input was recorded. The time walk curves were then plotted around a mean of zero and in 5 dB steps along the x-axis. Each shaping method fabricated with its component values are shown in Figure 3-23.

3.7 PHENIX Lead-Scintillator CFD Circuit Designs

3.7.1 Architecture and Coincidence Gating

The CFD architecture designed for implementation in the PHENIX EMCal PbSc readout electronics is shown in Figure 3-24. This circuit was closely related to the CFD

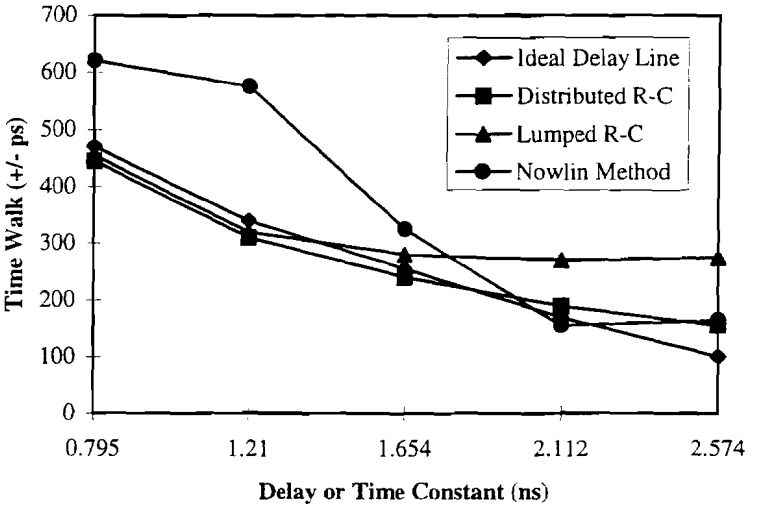


Figure 3-21. Time walk simulation results for the four shaping methods.

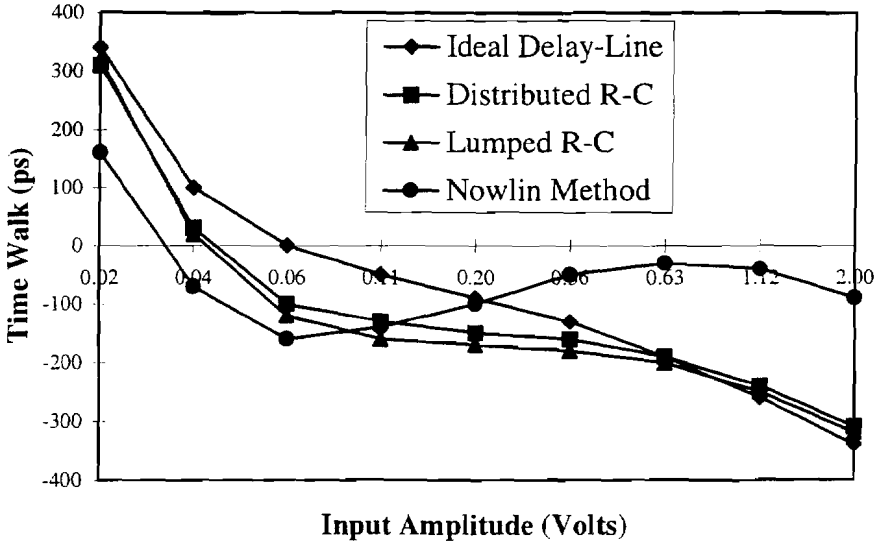
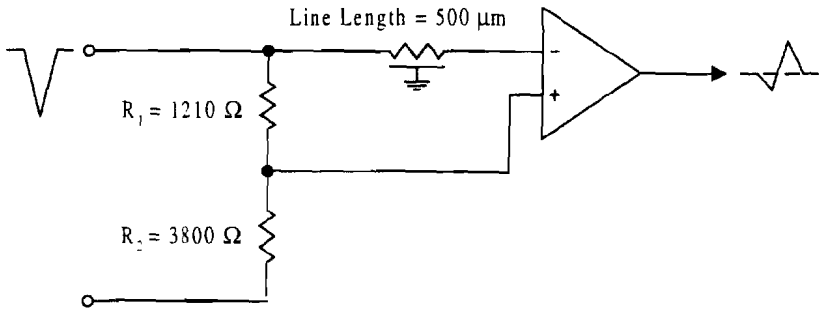
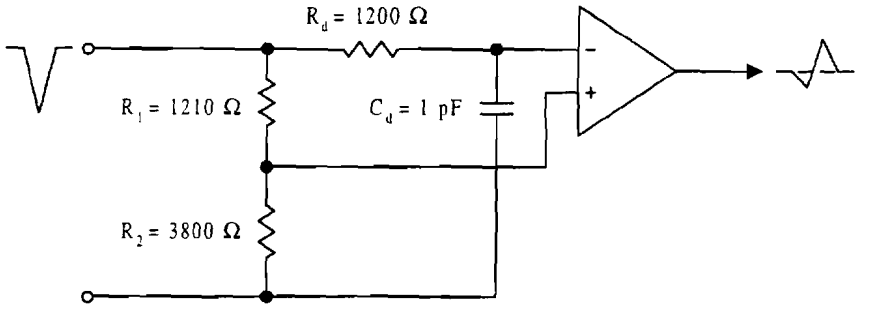


Figure 3-22. Time walk over a 100:1 input amplitude dynamic range in 5 dB steps for the zero-crossing time chosen for fabrication.



(a)



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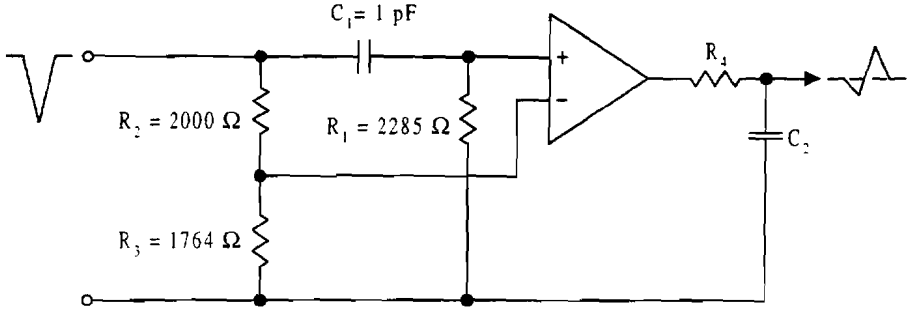


(c)

Figure 3-23. Three candidate shaping methods fabricated for the PHENIX PbSc CFD. (a) The distributed R-C delay-line. (b) The lumped-element R-C filter. (c) The Nowlin shaping circuit with R_4C_2 determined by the CFD.

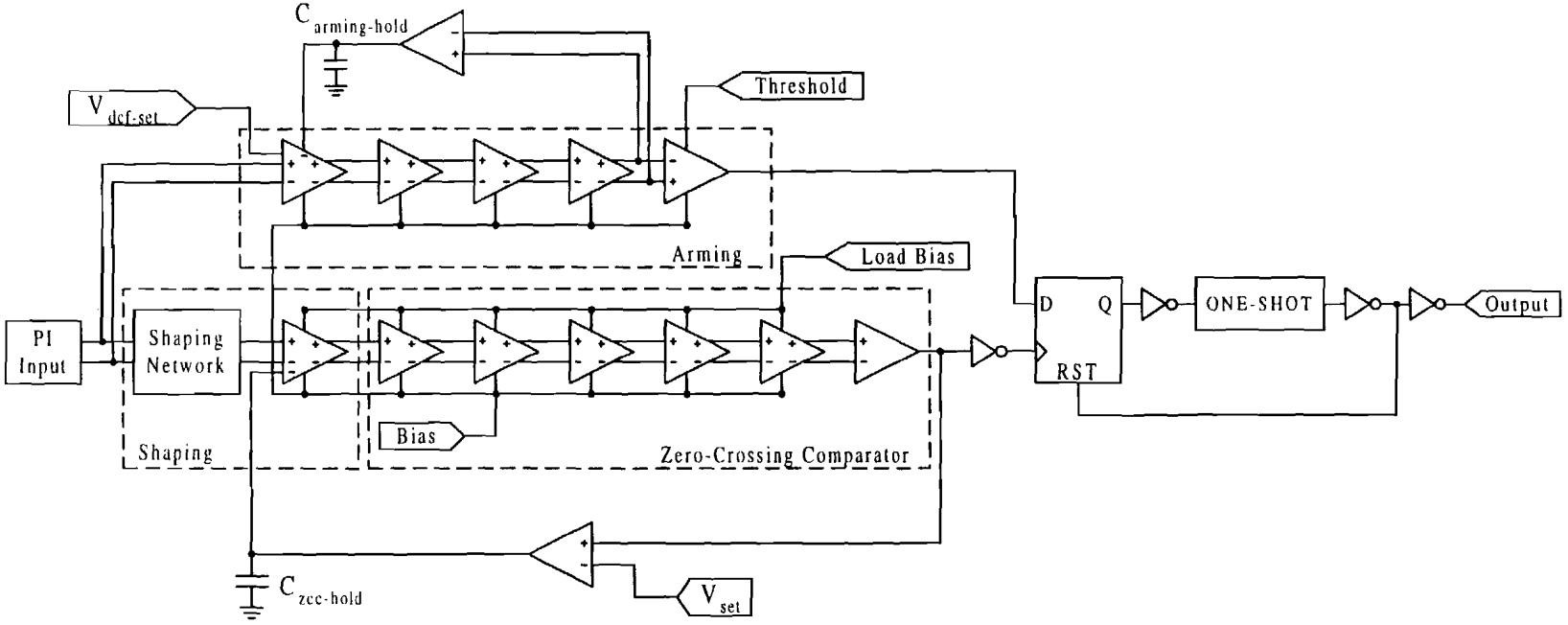


Figure 3-24. Block diagram of the PHENIX PbSc CFD with differential input from the passive integrator (PI).

architecture described earlier. The CFD consisted of a shaping network, a zero-crossing comparator, arming discriminator and coincidence gating logic. The labeled shaping network block shown in Figure 3-24 contained the respective shaping networks investigated in this thesis. A differential amplifier performed the subtraction of the shaping network signals. The ZCC had cascaded stages of differential input and differential output amplifiers, and a final amplifier performed differential to single-ended conversion. The arming discriminator was a simple leading-edge discriminator. A final amplifier with differential input and single-ended output possessed a threshold adjustment to determine the minimum input signal triggering level. Both the ZCC and the arming circuits contained dc feedback loops to adjust operating points. Figure 3-25 shows the passive integrator voltages (PI in Figure 1-1 page 10) developed at the timing and energy outputs. This plot shows the shift in the dc baseline level due to the shaping for the energy channel. A significant shift in the dc level prevented the CFD from returning to baseline before the next beam-crossing when taken single-ended (node 1 in Figure 3-25). To eliminate problems introduced by the dc baseline shift, the arming circuit and ZCC both picked-off the 50 Ω resistor (in the passive integrator) differentially, but this approach introduced common-mode signals on the input. The CFD possessed an acceptable amount of common-mode rejection to operate in this configuration.

Coincidence gating refers to the proper timing occurrence of the arming and ZCC output signals. Figure 3-26 gives a timing diagram indicating the proper timing for this CFD. The arming circuit went to a logic high before the ZCC to arm the D-input to the flip-flop. After the D-input transitioned to a logic high, the ZCC output clocked the flip-

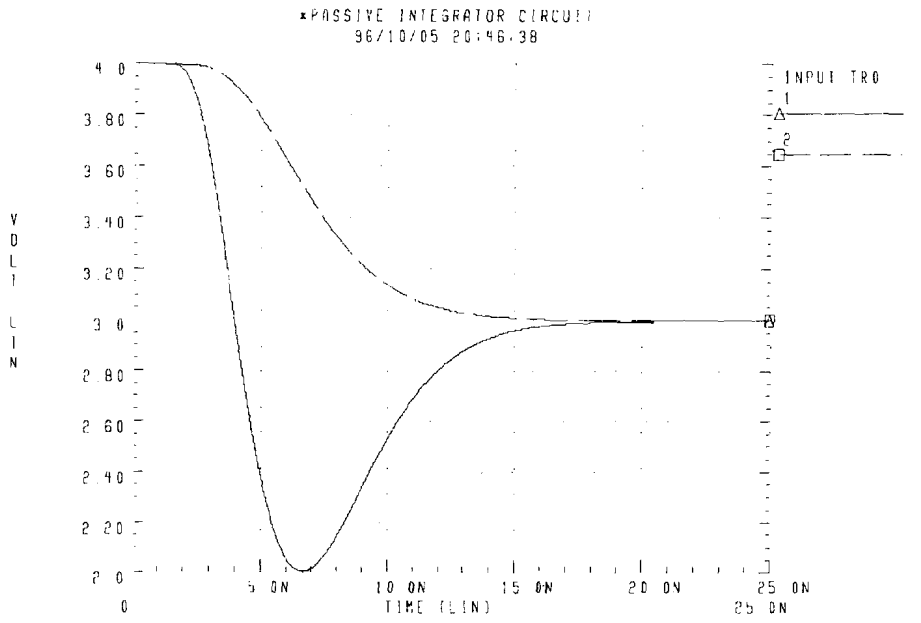


Figure 3-25. Plot of the output voltages from the passive integrator for a pseudo-gaussian input.

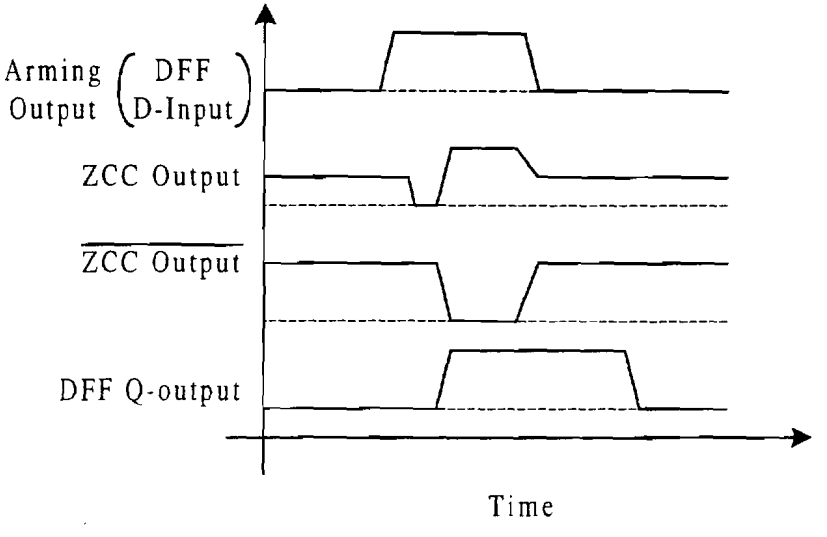


Figure 3-26. Timing diagram indicating correct coincidence gating for the ZCC.

flop and the Q-output went to a logic high. This order of operation was common to the architecture described earlier where a logical AND gate was used to perform the coincidence gating. Implementing the flip-flop structure ensured that the timing output was determined by the ZCC. If the ZCC clocked the flip-flop before the arming circuit provided a logic high to the flip-flop D-input, the flip-flop would not trigger. This approach was used to avoid the possibility of leading-edge walk present in coincidence gating schemes utilizing the logic AND gate. The remaining circuitry was provided to interface to the TAC and provided a reset to the D flip-flop. A one-shot provided width adjustment for the output logic pulse used to start the TAC measurement. The inverters included in the CFD supplied the correct polarity for a given output.

3.7.2 Zero-Crossing Comparator

The zero-crossing comparator was designed to produce a logic output pulse at the zero-crossing time of the shaped input signal. Ideally, the ZCC would be insensitive to input signal zero-crossing slope, under-drive (input drive below the threshold) and over-drive (input drive above the threshold). An ideal ZCC would also be perfectly linear and possess no dc offsets. If the ZCC possessed infinite bandwidth and slew-rate, the circuit would be insensitive to the zero-crossing crossing slope and possess no time walk. In practical applications, this requirement is non-realizable.

Area restrictions required certain trade-offs in the circuit topologies. Each circuit could not exceed some maximum pitch (height) and length to be implemented in the multichannel ICs. The circuit topology chosen for the PHENIX CFD ZCC contained

several stages of gain cascaded to produce a sufficient signal to clock the flip-flop. Distributing the gain and bandwidth between the circuits was determined by several factors affecting the time walk and timing jitter. Consider an amplifier with an open-loop, single-pole transfer function given by

$$\frac{A}{\left(1 + j\frac{f}{f_{p1}}\right)}, \tag{3-11}$$

where A is the gain, f is the frequency variable and f_{p1} is the -3 dB corner frequency. Increased gain in the PHENIX ZCC amplifier topology directly decreased the amplifier bandwidth (to first order) as described by the transfer function

$$\frac{2A}{\left(1 + j\frac{f}{(0.5)f_{p1}}\right)}. \tag{3-12}$$

On the other hand, a second identical amplifier cascaded with the first amplifier gave the transfer function

$$\frac{A^2}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p1}}\right)} = \frac{A^2}{\left(1 + j\frac{f}{f_{eq}}\right)}, \tag{3-13}$$

where f_{eq} was the new bandwidth. Equation 3-13 shows that the gain was squared and the new bandwidth was the combination of two identical corner frequencies, f_{p1}, given by,

$$f_{eq} = f_{p1}\sqrt{\left(2^{\frac{1}{n}} - 1\right)} = f_{p1}\sqrt{\left(2^{\frac{1}{2}} - 1\right)} \approx f_{p1}(0.64), \tag{3-14}$$

where n was the order of the frequency corner. By cascading two stages of gain, the new overall gain-bandwidth product (GBW) increased. The two stages resulted in twice the

area, but they both comfortably fit into the circuit pitch requirements setting side-by-side. Increasing the gain of a single stage would have possessed disadvantages in that more area or bias current would have been required. In the multichannel application for PHENIX, maintaining minimal bias current was a major concern, and some compromise between die area and power consumption was reached in the ZCC design. As more stages of gain were cascaded, the gain increased faster than the bandwidth decreased to continually increase the overall GBW. Differential input and output stages gave twice as much gain as a single-ended output which further maximized the circuit GBW.

Theoretically, cascading differential input and output stages of amplification would continually increase the gain-bandwidth product. Time walk for this circuit topology is always limited in practice by the non-ideal properties of the comparator. This condition prevails due to the non-linearity of the amplifiers as they are under-driven and over-driven. As mentioned earlier, the zero-crossing comparator should possess enough gain to just saturate the last amplifier stage, and any additional gain after these stages will only increase time walk. The number of amplifier stages implemented is commonly determined through simulations of the chosen topology and considering the general rules applying to time walk and jitter performance. The optimum number of stages of differential input differential output amplification was determined to be six including the shaping amplifier.

Figure 3-27 shows the topology for the ZCC differential shaping amplifier. This shaping amplifier utilized NMOS transistors as input devices connected in a differential pair configuration. The differential pair was biased with an NMOS current source M5,

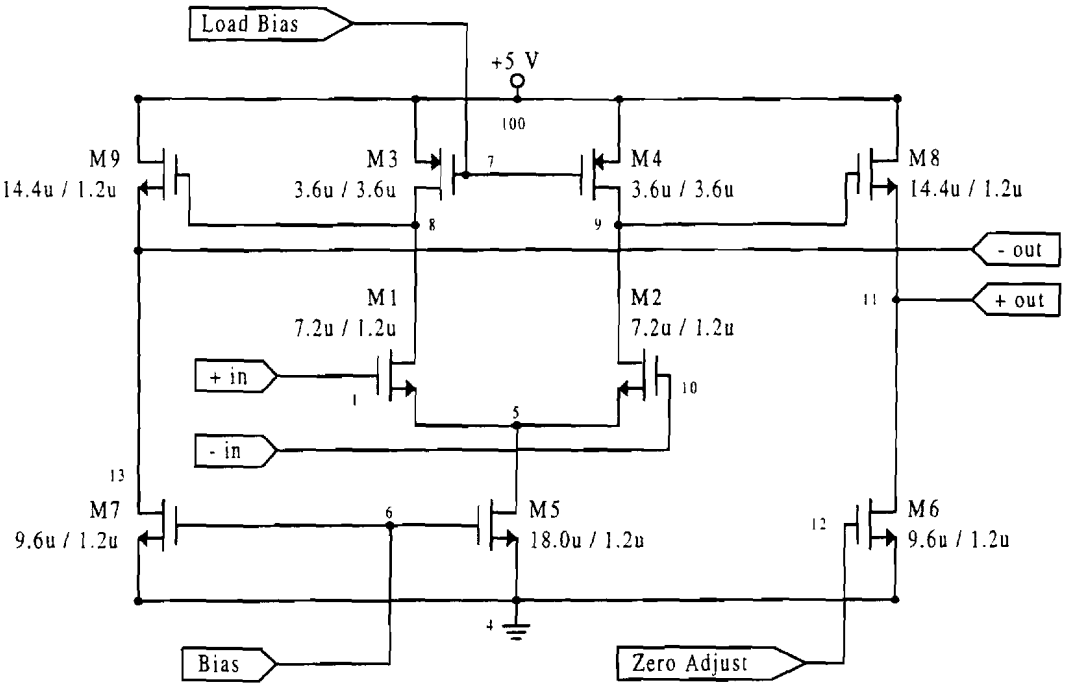


Figure 3-27. Circuit diagram of the ZCC shaping amplifier.

and this current source was biased with an external reference gate voltage. PMOS transistors M3 and M4 provided active loading to the differential pair drains, and the gate terminals were connected to an external bias voltage. This load bias voltage was set to operate the PMOS loads in the ohmic region indicated in Figure 3-28. For operation in the ohmic region, the impedance looking into the drain was approximately the reciprocal of the slope of the characteristic curve, V_{sd}/I_d, illustrated in Figure 3-28. Source-follower transistors M8 and M9 were connected to the drains in the differential pair to provide level shifting for the next differential input amplifier, and NMOS current sources M6 and M7 loaded the source-followers. M7 was biased with the same voltage as the current source in the differential pair. The gate of M6 provided an internal connection for dc feedback to be applied.

If identical devices were assumed and the body effect neglected, the differential gain, $A_{shaping}$, for the shaping amplifier shown in Figure 3-27 was approximately twice the single-ended gain given by

$$A_{shaping} \approx 2\left(\frac{g_{mM1}}{2} \cdot Ro_{M4} \| Ro_{M2}\right)\left(\frac{Ro_{M6}}{Ro_{M6} \cdot \frac{1}{g_{mM8}}}\right) \approx 2.8\,\frac{V}{V}, \qquad (3\text{-}15)$$

where g_{mM1} and g_{mM8} were the transconductances of M1 and M8, respectively; and Ro_{M2}, Ro_{M4} and Ro_{M6} were the output impedances of M2, M4 and M6, respectively. The output impedance of M2 for the chosen operating point was much less than M4 so that Ro_{M4} dominated the parallel combination with Ro_{M2}. The frequency response of this amplifier was determined by the dominant pole located at the drains of M2 and M4 and given by

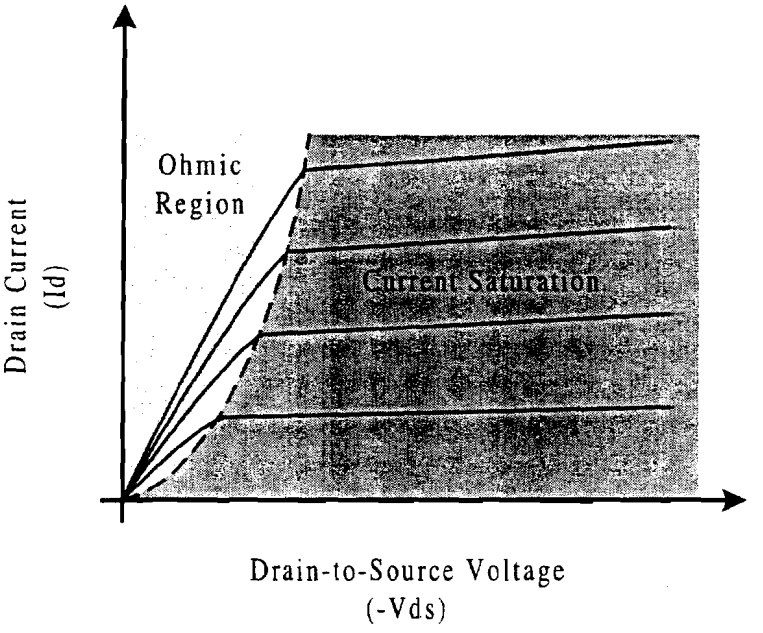


Figure 3-28. PMOS characteristic curves indicating various regions of operation.

$$f_{shaping(-3\,dB)} \approx \frac{0.159}{R_{eq} \cdot C_{eq}} \approx 110\,MHz, \qquad (3\text{-}16)$$

where R_{eq} was the parallel combination of drain looking in impedance for M2 and M4; and C_{eq} was the device and stray capacitances at the drains of M2 and M4. The frequency corner introduced at the output of the source-follower was much farther out in frequency space due to the lower output impedance of the source. Slew-rate for the shaping amplifier was given by

$$SR \approx \frac{I_{bias}}{C_{eq}} \approx \frac{107\,\mu A}{85\,fF} \approx 1.25\,\frac{V}{ns}, \qquad (3\text{-}17)$$

where SR was the slew-rate, I_{bias} was the bias current in the differential pair current source and C_{eq} was the capacitance from Equation 3-16. Figure 3-29 shows the differential input and output amplifier used in the remaining 5 differential amplifiers of the zero-crossing comparator. This second amplifier topology utilized the same topology as the shaping amplifier. The differential pairs in these amplifiers were biased with the same type current source as the shaping amplifier and shared the same gate voltage reference. PMOS load transistors in the differential pairs also shared the same load bias voltage for ohmic region operation. Gain, - 3 dB bandwidth and slew-rate were all calculated just as the shaping amplifier and found to be 2.4 V/V, 110 MHz and 0.71 V/ns, respectively.

The device sizes and bias current for the shaping amplifier were different from the remaining amplifiers for several reasons. The inverting input device, serving as the termination point (the line was not truly terminated) for the lossy transmission line formed by the distributed R-C delay-line, possessed a lower input capacitance at the end

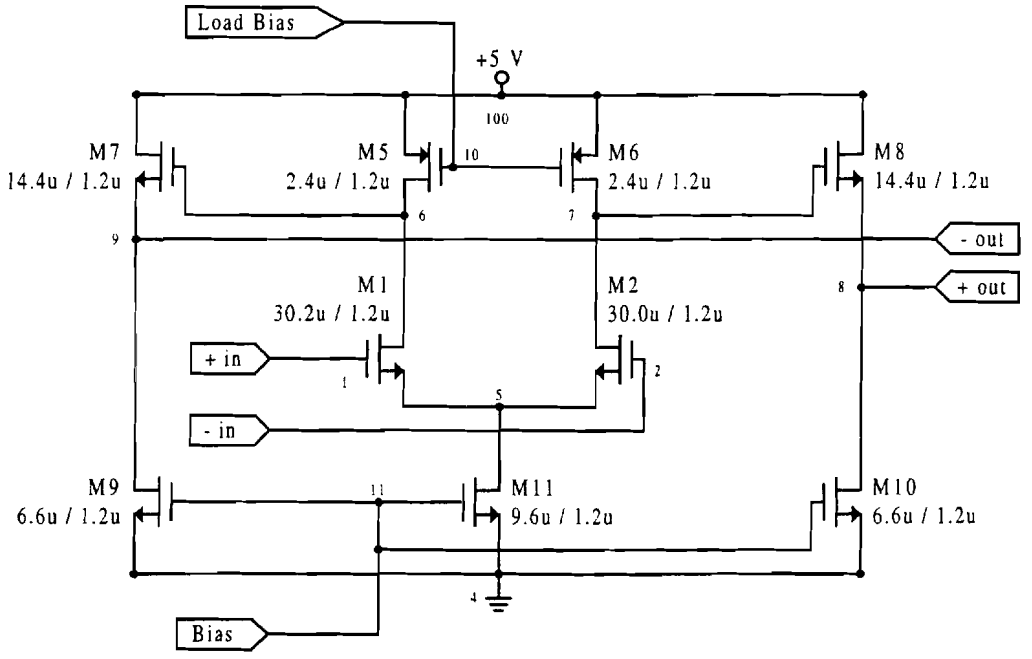


Figure 3-29. Circuit diagram of the ZCC differential amplifiers following the shaping amplifier.

of the delay-line. To maintain approximately the same gain and bandwidth as the other stages, the shaping amplifier was biased at a higher current which also provided a higher slew-rate. A significant common-mode voltage from the passive integrator was introduced at the inputs for a full-scale input as shown earlier in Figure 3-25. The shaping amplifier had to subtract two signals with varying input dc levels while the remaining amplifier inputs essentially operated around a constant dc level. PMOS load transistors in the differential pair were sized to result in a drain voltage of greater than + 4 Vdc on the input differential pair devices. Maintaining a positive voltage from the drain-to-gate for the input differential pair devices ensured operation in the current saturation region and preserved amplifier linearity.

A differential to single-ended amplifier shown in Figure 3-30 provided the output signal to the inverter used to clock the D flip-flop. This topology consisted of a PMOS input pair with active loads. Transistor M3 was diode connected and mirrored by the load transistor M4. This amplifier had a single-ended gain, A_{seout}, approximated by

$$A_{seout} \approx g_{mM2} \cdot \left(Ro_{M2} \| Ro_{M4}\right) \approx 23 \frac{V}{V}, \tag{3-18}$$

where g_{mM2} was the transconductane of M2; and Ro_{M2} and Ro_{M4} were the output impedances of M2 and M4, respectively. The - 3 dB frequency corner was established at the output node described by

$$f_{-3\,dB} \approx \frac{0.159}{\left(Ro_{M2} \| Ro_{M4}\right) \cdot C_{out}} \approx 60\,MHz, \tag{3-19}$$

where C_{out} is the equivalent capacitance at the output node. This amplifier did not possess a current source in the input device sources as is commonly used in differential

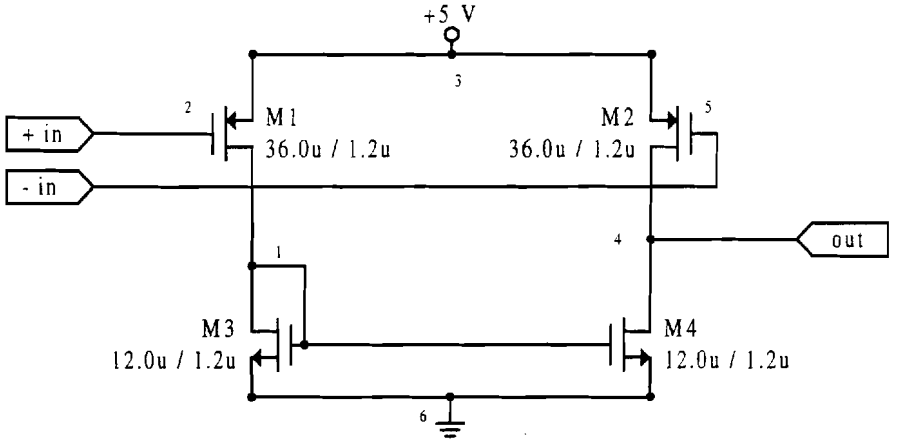


Figure 3-30. Circuit diagram of the ZCC differential to single-ended amplifier.

pair topologies. The dc levels on the input PMOS gates were set by the output dc levels of the last differential ouput amplifier, and these voltages set the dc bias currents in the input devices.

3.7.3 Zero-Crossing Comparator dc Feedback Circuit

The zero-crossing comparator possessed a dc feedback loop which provided a time walk adjustment. This approach included a feedback amplifier with an output hold capacitor in the feedback loop. Figure 3-31 shows the topology for the ZCC feedback amplifier. The devices M1 and M2 served as the inputs to a differential pair amplifier. M9 provided a current source for the pair while M3 and M4 were diode connected active loads. Differential to single-ended conversion was achieved with M6 connected in a common-source topology with M8 providing NMOS active loading. Transistors M5 and M7 provided biasing for the amplifier's second stage. The gain of this amplifier, $A_{dc\text{-}amp}$, neglecting body effect was given by

$$A_{dc\text{-}amp} \approx \left(\frac{g_{mM2}}{2} \cdot Ro_{M2} \left\| \frac{1}{g_{mM4}} \right. \right) \left(g_{mM6} \cdot Ro_{M6} \| Ro_{M8} \right) \approx 16.7 \frac{V}{V}, \quad (3\text{-}20)$$

where g_{mM2}, g_{mM4} and g_{mM6} were the tranconductances of M2, M4 and M6, respectively; and Ro_{M2}, Ro_{M6} and Ro_{M8} were the output impedances of M2, M6 and M8, respectively.

This amplifiers output served as the input to the internal node of the shaping amplifier discussed earlier. The hold capacitor at the amplifier output realized a dominant, low-frequency pole to cause the loop to be much slower than the shaped signal forward path through the ZCC. A high output impedance was achieved with a very low

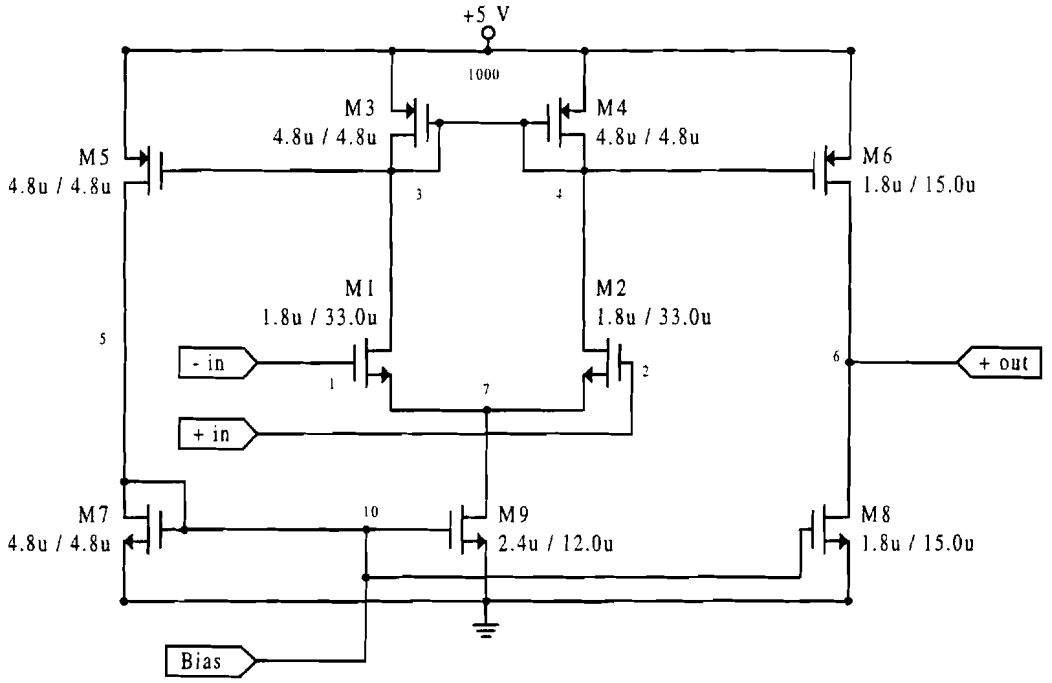


Figure 3-31. Circuit diagram of the ZCC dc feedback amplifier.

bias current and appropriate transistor sizing in the amplifier. The output from the single-ended output amplifier in the ZCC provided the input to the positive input of the dc feedback amplifier. An external voltage reference was connected to the non-inverting input.

Time walk adjustment in the ZCC walk was achieved using the external voltage input to the feedback amplifier and utilizing the mechanism of negative feedback. Figure 3-32 is provided to assist in the explanation of the dc feedback mechanism employed in the ZCC. Inversion through the dc feedback loop was realized from the internal node supplied by the shaping amplifier (node 12 in Figure 3-27) to the shaping amplifier positive output (node 11 in Figure 3-27). All other paths through the dc feedback loop gave non-inverting gain resulting in one inversion around the loop. The second stage in the dc amp possessed PMOS and NMOS transistors sized in such a way to pull the output node toward ground. To produce a dc level at the dc amp output, some differential voltage was required at the inputs. This required output dc level of the dc amp was given by the expression

$$V_{dc\text{-}out} = \left(Vdiff_{in} + V_{os}\right)\left(A_{dc\text{-}amp}\right), \qquad (3\text{-}21)$$

where $Vdiff_{in}$ was some differential voltage, V_{os} was the input offset voltages and $A_{dc\text{-}amp}$ was the dc amp gain. Input offset voltages were determined by processing variations but would typically fall in the few tens of millivolts range for the worst case. The remaining input differential voltage required was then determined by the amplifier gain. Negative feedback in this loop caused the two dc amp inputs to track each other with some input differential voltage required to establish the feedback amplifier output dc level, and this

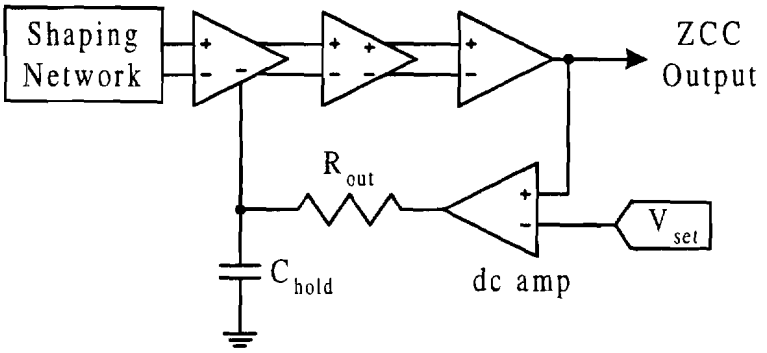


Figure 3-32. Circuit diagram to illustrate the ZCC dc feedback.

feature allowed the time walk adjustment. Due to non-ideal properties in the ZCC, the output signals crossed through zero at various locations. Figure 3-33 shows a simulation plot of ZCC outputs for a 100:1 dynamic range (- 2 V to - 20 mV) of input signal amplitudes. From Figure 3-33 it can be seen that the ZCC possessed some point along the output signal where the various outputs tended to cross closer together. By adjusting the dc amp input V_{set}, this common crossing point could be adjusted toward the trip point of the inverter following the ZCC. Essentially, this adjustment moved the output dc level of the ZCC. Obviously, if the signals were all crossing closer together near the trip point of the inverter, the time walk produced by the CFD was decreased.

Since the PHENIX PbSc CFD required a differential input signal, the dc feedback could not be brought back to the shaping amplifier's inverting input. Although the feedback employed in this CFD does not directly correct for dc offset voltages at the inputs, the external voltage V_{set} allowed for adjustments to compensate for any dc offset effects. Large offset voltages in this application could have arisen due to the large amount of gain required in the ZCC for minimum inputs.

For any negative feedback circuit, the issue of loop stability against oscillation must be investigated. With the dc feedback intact in the simulation file, HSPICE simulation would not converge to an operating point. Stability of the loop against oscillation was then a great concern. The critical corner frequencies were then determined individually for each circuit. Stray capacitances from routing and device capacitance of adjoining stages was included for determination of these characteristics.

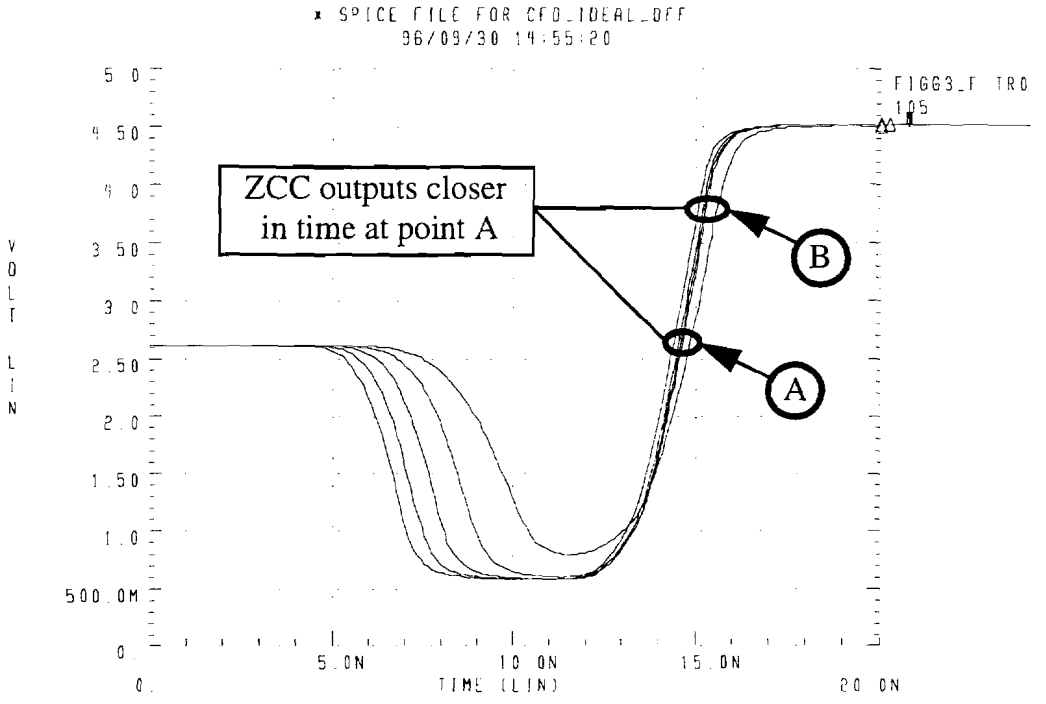


Figure 3-33. HSPICE plot showing ZCC output signal time spread variation along the zero-crossing edge.

Equation 3-22 gives the critical circuit gains and frequency corners encountered in the realization of the dc feedback loop as

$$T \approx -\frac{(-K1)(K2)^5(K3)(K4)}{\left(1+j\frac{f}{f_{p1}}\right)\left(1+j\frac{f}{f_{p2}}\right)^5\left(1+j\frac{f}{f_{p3}}\right)\left(1+j\frac{f}{f_{p4}}\right)},$$

$$T \approx \frac{(-1.25)(2.4)^5(23)(16.7)}{\left(1+j\frac{f}{110\ \text{MHz}}\right)\left(1+j\frac{f}{110\ \text{MHz}}\right)^5\left(1+j\frac{f}{60\ \text{MHz}}\right)\left(1+j\frac{f}{180\ \text{Hz}}\right)}, \quad (3\text{-}22)$$

where K1 and f_{p1} were the shaping amplifier's gain from the internal node to the output and amplifier bandwidth, respectively; K2 and f_{p2} were the gain and bandwidth for the differential amplifiers, respectively; K3 and f_{p3} were the differential to single-ended amplifier gain and bandwidth, respectively; and K4 and f_{p4} were the dc amp gain and bandwidth, respectively. Evaluation of this loop transfer function revealed a phase margin and gain margin of approximately 62° and 12 dB, respectively.

The last aspect of this dc feedback loop on the timing performance involved the signals on the input of the dc amp. The ZCC output swung over a large dynamic range and this caused the output of the dc amp to swing around the output dc voltage. Through the addition of the hold capacitor shown in Figure 3-32 at the dc amp output, a lowpass filter was realized in the signal path between the dc amp output and the shaping amplifier internal node. Large input signals from the ZCC output caused some shift in the feedback amplifier output dc level. The amount of dc error voltage at the internal node of the shaping amplifier was calculated using the relationship [16]

$$Vdc_{error} = W \cdot R \cdot A \approx (20\ ns)(1\ kHz)(50\ mV) \approx 1\ \mu V, \qquad (3\text{-}23)$$

where W was the equivalent pulse width, R was the effective rate (or frequency) and A was the effective output pulse amplitude of the dc amp. An effective rate came from the physics expectation that a significant event would occur at about a 1 kHz rate for a 9 MHz beam-crossing rate. The equivalent pulse width and amplitude were somewhat more difficult to characterize since the ZCC output went below and above the dc baseline voltage. An effective pulse width and amplitude were estimated from simulation data. The error voltage introduced by this dc level shift influenced time walk performance.

3.7.4 Arming Discriminator Design

The arming discriminator shown in the CFD block diagram of Figure 3-24 was composed of 4 differential input and output amplifiers, a differential input to single-ended output amplifier that provided threshold adjustment and a feedback amplifier for dc feedback. Figure 3-34 shows the topology for the first differential amplifier in the arming circuit. Since the arming circuit required a differential input signal from the passive integrator just as the ZCC, the first arming circuit amplifier possessed an internal connection point for dc feedback. A + 4 Vdc baseline level was also seen by the first arming amplifier from the passive integrator. An NMOS differential pair formed by M1 and M2 possessed an NMOS current source M5 which was biased with the same gate voltage as the differential pair current sources in the ZCC differential amplifiers. Diode connected PMOS transistors M3 and M4 provided active loading in the differential pair. The gate of M8 was connected to a + 1 Vdc reference, and dc feedback was brought back

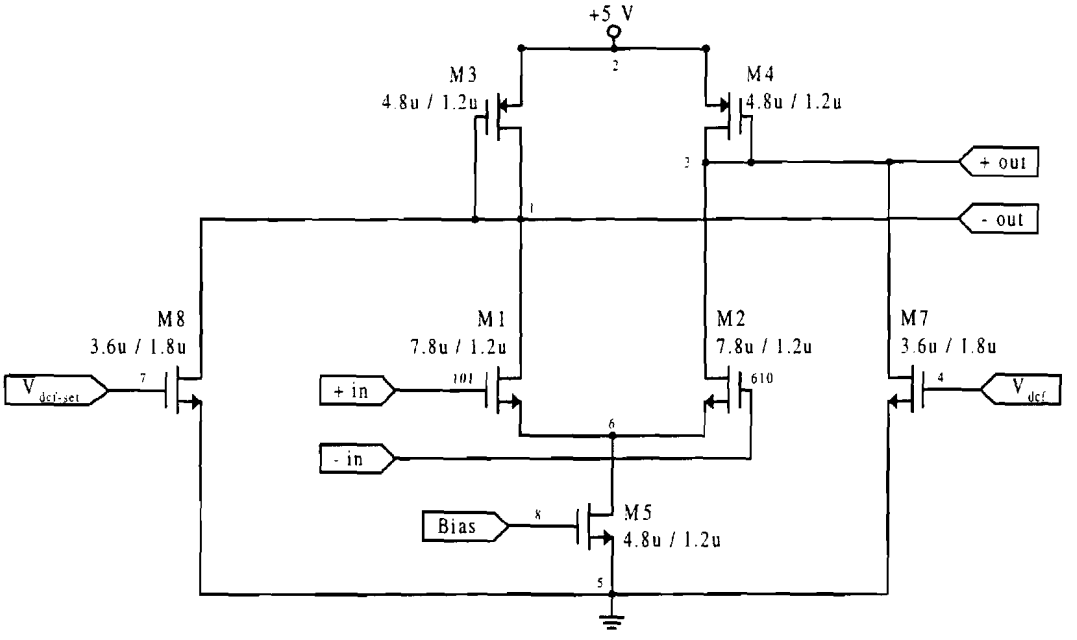


Figure 3-34. Diagram of the first amplifier in the arming channel of the CFD.

to the gate of M7 from the feedback amplifier. Bias currents for M7 and M8 flowed through M3 and M4, respectively. The + 4 Vdc input baseline level limited the sizing of M3 and M4 to maintain small-signal linearity, and area restrictions limited the sizing of M7 and M8.

If the devices were considered identical and body effect neglected, the differential gain, $A_{arming\text{-}dcf}$, for the first arming amplifier was approximately twice the single-ended gain given by

$$A_{arming\text{-}dcf} \approx 2\left(\frac{g_{mM1}}{2}\cdot Ro_{M2}\|Ro_{M7}\left\|\frac{1}{g_{mM4}}\right.\right), \tag{3-24}$$

where g_{mM1} and g_{mM4} were the transconductances of M1 and M4, respectively; and R_{oM2} and R_{oM7} were the output impedances looking into the drains of M2 and M7, respectively. The impedance, $1/g_{mM4}$, seen looking into the diode connected transistor M4 was much lower than the impedance looking into the drains of M2 and M7, and Equation 3-24 was further approximated as

$$A_{arming\text{-}dcf} \approx \left(\frac{g_{mM1}}{g_{mM4}}\right). \tag{3-25}$$

PMOS active loads were chosen over NMOS active loads to give a higher gain for the same size devices. This characteristic was derived from the relationship of the device transconductance dependence on mobility. The transconductance for NMOS and PMOS devices (assuming low channel length modulation) was related to the drain current by [27]

$$g_m \approx \sqrt{2\, I_d \mu C_{ox} \frac{W}{L}}, \tag{3-26}$$

where I_d was the drain current; μ was the electron or hole mobilities for NMOS or PMOS devices, respectively; C_{ox} was the gate-oxide capacitance; W was effective channel width; and L was effective channel length. Substituting Equation 3-26 into Equation 3-25 and simplifying gave a gain expression

$$A_{arming\text{-}dcf} \approx \left(\frac{\sqrt{(I_{dM1})(\mu_{M1})\left(\frac{W_{M1}}{L_{M1}}\right)}}{\sqrt{(I_{dM4})(\mu_{M4})\left(\frac{W_{M4}}{L_{M4}}\right)}} \right). \qquad (3\text{-}27)$$

The IC process used in this work possessed an electron mobility μ_{M1} that was about 2.3 times higher than the hole mobility μ_{M4}. Drain currents in M1 and M2 were less than M3 and M4 by the amount steered into M7 and M8, and this factor was included in the gain expression. The final differential gain expression for this amplifier was approximated as

$$A_{arming\text{-}dcf} \approx \sqrt{\frac{(I_{d1})(2.3)\left(\frac{W_{M1}}{L_{M1}}\right)}{(I_{d4})\left(\frac{W_{M4}}{L_{M4}}\right)}} \approx \sqrt{\frac{(14\mu A)(2.3)\left(\frac{7.8}{1.2}\right)}{(15\mu A)\left(\frac{4.8}{1.2}\right)}} \approx 1.8\,\frac{V}{V}. \qquad (3\text{-}28)$$

If NMOS active loads had been used, the gain would have been lowered by the $\sqrt{2.3}$ factor in Equation 3-28. Using NMOS loads to complement the NMOS input devices could have provided some advantages to lowering gain variations due to process mismatching typically seen across different ICs. A dominant pole at the drain of M4 determined the - 3 dB bandwidth to be

$$f_{-3\,dB} \approx \frac{0.159}{\left(\frac{1}{g_{mM4}}\right)(C_{eq})} \approx 100\,MHz, \qquad (3\text{-}29)$$

where C_{eq} was the equivalent capacitance at node 3 determined by devices M2 and M4; stray capacitances from routing; and the capacitance introduced by the input devices of the next amplifier. The amplifier chosen for the following three cascaded differential amplifiers and shown in Figure 3-35 utilized the same topology as the first arming amplifier with the exception of the two extra transistors for dc feedback. Gain and bandwidth calculations for these amplifiers were similar to Equation 3-24 and Equation 3-29 if the extra terms introduced by the feedback devices were removed. Each of these amplifiers possessed a differential gain of ~ 2.26 V/V, but the amplifier bandwidths varied with load capacitance. The second and third amplifiers possessed bandwidths of ~ 95 MHz, while the fourth amplifier possessed a lower bandwidth of ~ 35 MHz due to the extra capacitance introduced by the large input devices of the dc feedback amplifier and the threshold circuit amplifier.

The threshold circuit amplifier topology is shown in Figure 3-36. PMOS transistor input devices M5 and M6 were active loaded with M3 diode connected and mirrored by M4. The additional transistor M2 provided the means to establish a threshold adjustment for the circuit. Normal bias conditions for this circuit called for some standing current to flow into transistor M2. The bias currents in M5 and M6 were determined by the dc voltage level of the amplifier outputs preceding the threshold amplifier (assumed to be equal for discussion here), and these currents biased M3, M4 and M5. The dc bias currents labeled in Figure 3-36 were constrained by Kirchoff's current laws as

$$I_5 = I_2 + I_3, \tag{3-30}$$

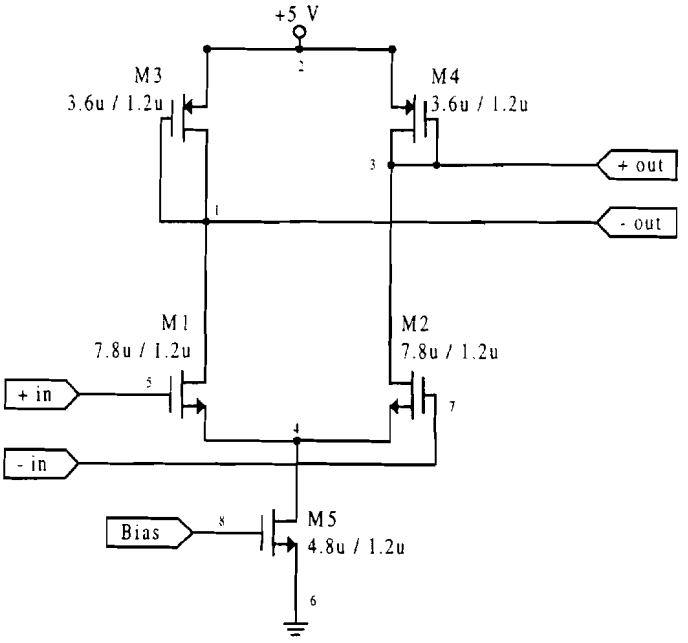


Figure 3-35. Diagram of the cascaded differential input and output amplifiers preceding the threshold circuit.

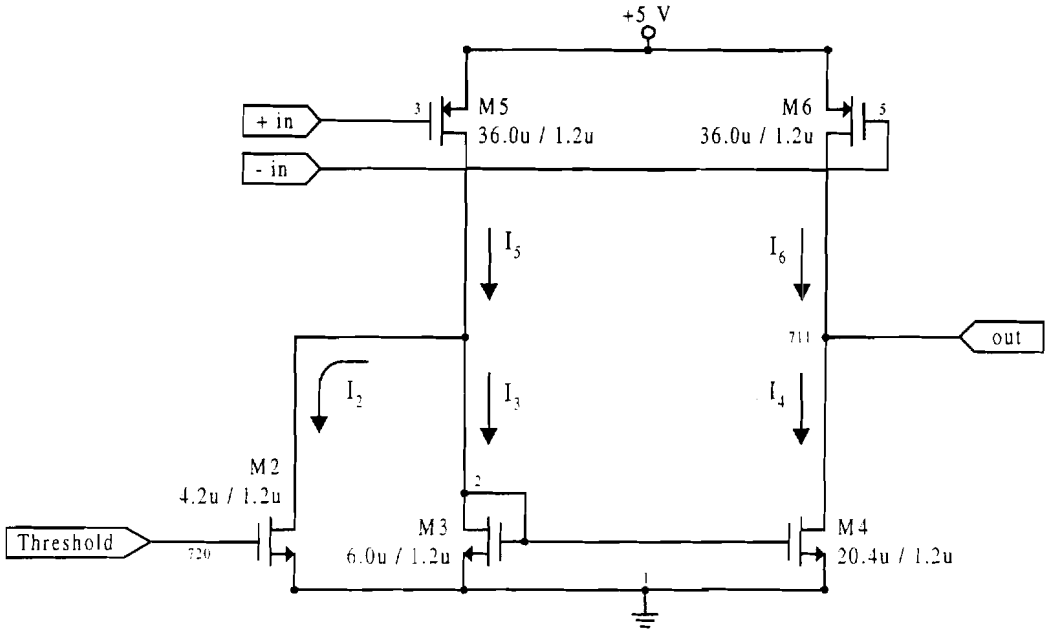


Figure 3-36. Diagram of the arming discriminator threshold circuit amplifier performing differential input to single-ended output conversion.

and

$$I_6 = I_4. \tag{3-31}$$

With the gate-to-source voltage of M3 equal to M4 ($V_{gs3} = V_{gs4}$) in the current mirror and assuming operation of M3 and M4 in the current saturation region, the drain currents I_3 and I_4 would have been related to the channel width and length ratios as

$$I_4 = I_3 \left(\frac{\left[\frac{W_{M4}}{L_{M4}} \right]}{\left[\frac{W_{M3}}{L_{M3}} \right]} \right) \approx I_3[3.4], \tag{3-32}$$

where the subscripts denote the respective transistor as labeled in Figure 3-36. Figure 3-37 illustrates the characteristic curves for M3 and M4 based on $V_{gs3} = V_{gs4}$. Under normal bias conditions, substituting I_3 into Equation 3-32 to calculate the current I_4 gave a larger current than M6 could supply. Since M4 had to operate along the $V_{gs4} = V_{gs3}$ characteristic curve indicated in Figure 3-37 and I_4 had to equal I_6, the operating point for M4 fell into the ohmic region as indicated in Figure 3-37. If the gate voltage (threshold adjustment) of M2 was lowered, more current was steered into M3, and M4 was driven deeper into the ohmic region. On the other hand, a higher gate voltage on M2 decreased I_3 and brought the drain-to-source voltage of M4 closer toward the current saturation region. The function of changing the gate-to-source voltage on M4 through the threshold adjustment effectively changed the gain in this amplifier by changing the impedance looking into the drain of M4. Thus, a lower threshold voltage setting required a higher differential input signal to the threshold circuit to drive the output high. Since the amplifier was designed to have its output pulled down toward the negative supply with no

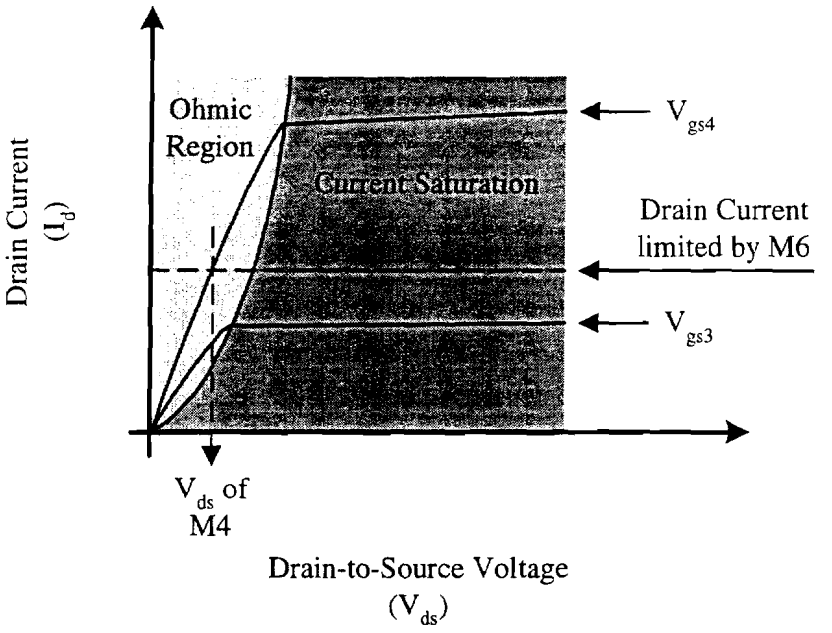


Figure 3-37. Illustration of the effect of current limiting in the threshold circuit by M6 operating M4 in the ohmic region.

input signal applied, a logic low level was supplied to the D flip-flop. Based on the polarity of the arming discriminator connections indicated in Figure 3-24, a negative going signal from the PMT produced the logic high signal at the threshold circuit output to arm the D-input of the flip-flop.

3.7.5 Arming Discriminator dc Feedback Circuit

The arming discriminator possessed a dc feedback loop to correct for dc offsets. An amplifier topology shown in Figure 3-38 was implemented to realize the feedback mechanism, and a hold capacitor was placed at the feedback amplifier output to create the low frequency dominant pole. The amplifier topology was a differential input to single-ended output amplifier, and the circuit was operated at low bias currents to provide a high output impedance at the dominant node. High output impedance and a lower hold capacitor were always desired in the implementation of the dc feedback loops to avoid large areas required for capacitors. The capacitor realized for this amplifier was a MOS capacitor formed by shorting the drain and source contacts. The drain-source contact forming one terminal of the capacitor was grounded, and the gate contact forming the other capacitor terminal was connected to the amplifier output. Gain and bandwidth for the feedback amplifier were calculated to be approximately 35.7 V/V and 1.9 kHz, respectively. One inversion through the loop to achieve negative feedback was realized in the first arming amplifier from the gate to the drain of M7. Stability against oscillation for the arming discriminator feedback loop was analyzed using the loop equation

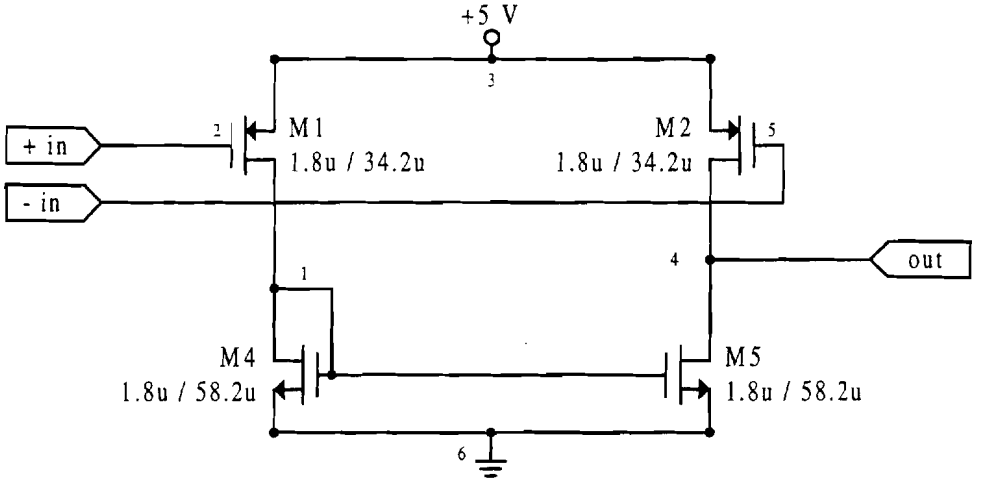


Figure 3-38. Circuit diagram of the arming discriminator dc feedback amplifier.

$$T \approx \frac{(-K1)(K2)^2(K3)(K4)}{\left(1+j\frac{f}{f_{p1}}\right)\left(1+j\frac{f}{f_{p2}}\right)^2\left(1+j\frac{f}{f_{p3}}\right)\left(1+j\frac{f}{f_{p4}}\right)}, \tag{3-33}$$

$$T \approx \frac{(-0.21)(2.26)^2(2.26)(35.7)}{\left(1+j\frac{f}{110\ \text{MHz}}\right)\left(1+j\frac{f}{95\ \text{MHz}}\right)^2\left(1+j\frac{f}{35\ \text{MHz}}\right)\left(1+j\frac{f}{1.9\ \text{kHz}}\right)},$$

where K1 and f_{p1} were the first arming amplifier's gain from the internal node to the output and amplifier bandwidth; K2 and f_{p2} were the gain and bandwidth for the next two differential amplifiers; K3 and f_{p3} were the gain and bandwidth of the last differential amplifier; and K4 and f_{p4} were the dc feedback amplifier gain and bandwidth. An analysis of the loop equation gave a phase and gain margin of approximately 90° and 48 dB, respectively.

3.7.6 CFD Digital Output Circuits

The circuitry providing a logic output pulse for the CFD was realized with custom and standard-cell blocks. A custom inverter followed the ZCC single-ended output amplifier to provide a negative-edged timing signal. The inverter was designed to trip at an input voltage of about + 3.0 V. This prevented the ZCC amplifier dc output level (nominally + 2.6 Vdc) to operate very near the trip point (typically set to + 2.5 V in standard-cell blocks). The D flip-flop was a standard-cell block with a D-input, negative-edge clock, active low reset and a Q-output. A second standard-cell inverter converted the positive-going edge from the flip-flop Q-output to a negative-going pulse for the one-shot. The one-shot implemented in this CFD was an ORNL custom design with output

pulse width adjustment. An initial negative-going edge fired the one-shot, but if the input remained low, the one-shot would retrigger. To prevent retriggerring, two cascaded standard-cell inverters followed the one-shot. The first inverter supplied the appropriate logic low level to the D flip-flop reset when the one-shot fired. The final inverter provided a positive output pulse for the CFD and was designed to drive a larger capacitive load.

Chapter 4

Experimental Results

4.1 Introduction

Each shaping method presented in this thesis was implemented in a fully monolithic CMOS CFD using the Orbit Semiconductor 1.2-μ n-well process. Each IC contained one channel for each shaping method investigated. A set of twelve ICs were fabricated, and a subset of ten ICs from this group were considered suitable for testing purposes. A 4-layer printed circuit board (PCB) was fabricated for testing purposes. Several types of data were taken for each CFD channel including amplitude-dependent time walk, common-mode input effects on time walk, timing jitter, die area required by each shaping method channel and power dissipation per channel. The various aspects of the CFD channel characterizations are discussed below.

4.2 Test Board Construction and Functionality

The test structure implemented in this work was a 4-layer PCB. The top layer contained all fast signal traces for the CFD inputs and outputs fabricated as 25 mil wide lines over a solid ground plane (the second layer). The third and fourth layers contained separate analog and digital power supply lines, various bias lines and the + 4 Vdc reference voltage. Each bias line was bypassed with capacitors placed as close to the chip

pins as possible. On-chip bypassing was also included on each power and bias line. To produce the common-mode signals similar to the passive integrator, a fast current pulse would have been necessary. Since this type of input signal was unavailable during testing, the CFD circuits were tested as shown in Figure 4-1. A negative-going input voltage signal, possessing an approximate 5 ns risetime and 15 ns falltime, was produced with a model 9210 LeCroy pulse generator. A model 839 KAY attenuator provided the input amplitude variation necessary to determine time walk performance. Output from the KAY attenuator was ac coupled into each channel, and the coaxial cable (with 50 Ω characteristic impedance) was terminated through a 50 Ω resistor to the + 4 Vdc reference (ac ground). The + 4 Vdc reference voltage was applied to the other input of each channel corresponding to the energy input from the passive integrator. This configuration presented a + 4 Vdc level to both inputs of the CFD as the voltage was picked-off differentially across the 50 Ω resistor as illustrated in Figure 4-1(b).

Figure 4-2 shows the circuits used to generate the CFD circuit bias voltages. The diode connected transistors shown in Figure 4-2 were fabricated on-chip and in only one channel per IC. All remaining channels on the same IC were biased with these voltages. Since these bias lines were connected only to transistor gate terminals, voltage loss due to current flow was not a problem. All remaining voltages were developed external to the chip using potentiometer settings shown in Figure 4-2. Table 4-1 gives a list of bias voltages recorded for the ten ICs tested. Time walk adjustment and threshold settings are given in the next section. The range shown below the average values represented the worst case deviation in either direction away from the mean. The deviation for the one-

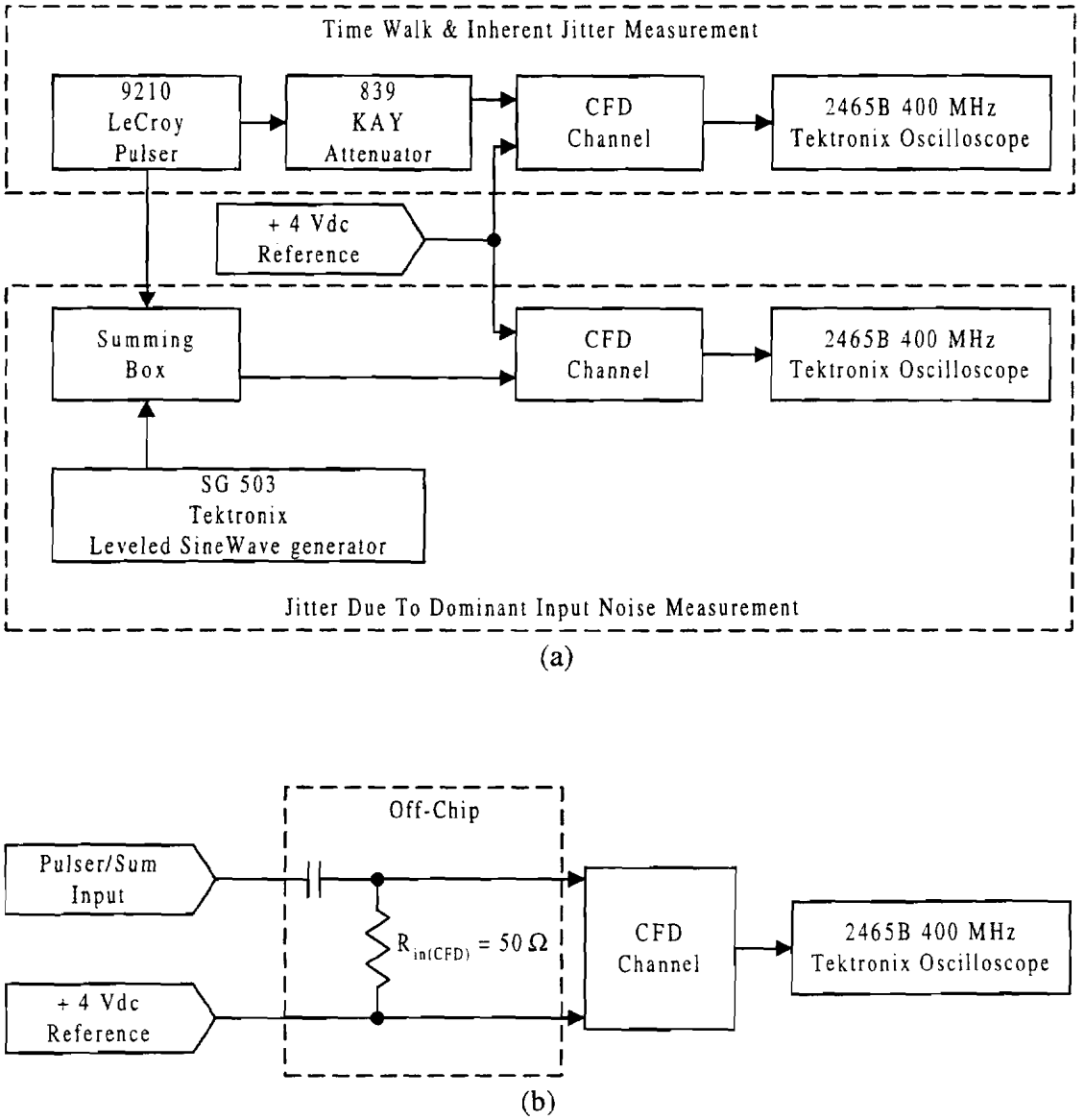


Figure 4-1. Illustration of IC testing configuration. (a) Illustration of the process used to test time walk and inherent noise induced timing jitter. (b) Illustration of the input circuit for each CFD channel showing the + 4 Vdc reference.

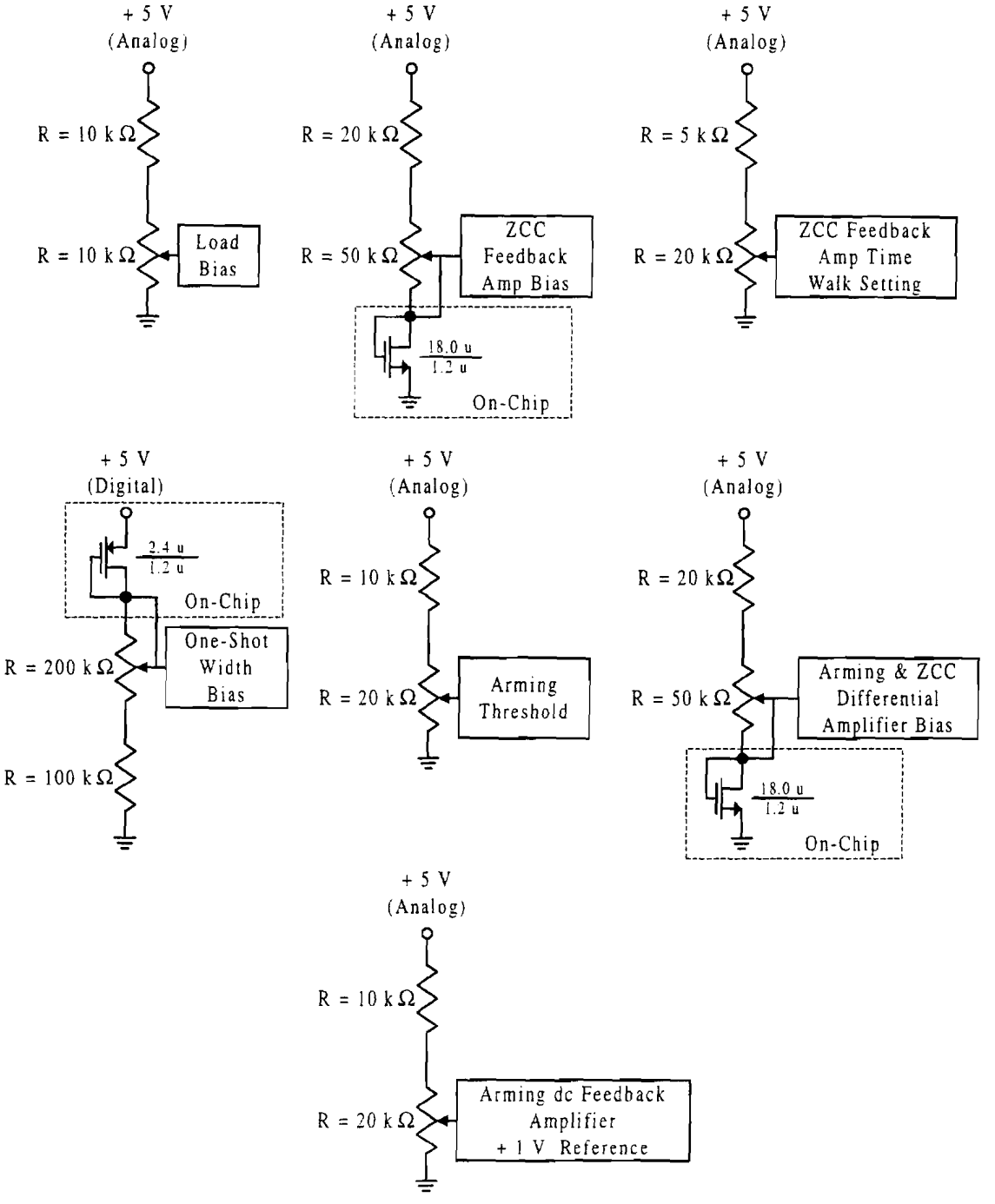


Figure 4-2. Illustration of the test board configurations used to generate the various CFD bias voltages.

Table 4-1. Table of bias voltages for each IC tested.

Chip #	ZCC Load Bias (Volts)	ZCC Feedback Amp Bias (Volts)	One-Shot Width Bias (Volts)	ZCC & Arming Amplifier Bias (Volts)	Arming Feedback Reference (Volts)
1	0.50	1.20	3.26	1.20	1.00
2	0.50	1.22	3.20	1.24	1.00
4	0.50	1.23	3.22	1.24	1.00
5	0.50	1.23	3.22	1.24	1.00
6	0.50	1.25	3.19	1.27	1.00
8	0.50	1.23	3.16	1.24	1.00
9	0.50	1.22	3.22	1.23	1.00
10	0.50	1.24	3.26	1.25	1.00
11	0.50	1.19	3.26	1.21	1.00
12	0.50	1.22	3.23	1.24	1.00
Average	0.50	1.22	3.22	1.24	1.00
Range	± 0.00	± 0.03	± 0.06	± 0.04	± 0.00

shot bias voltage was higher than the other bias voltage deviations for bias voltages generated through diode connected transistors. Figure 4-2 showed that the diode connected transistor used for the one-shot bias voltage possessed a smaller gate area than the diode connected transistors used to generate bias voltages elsewhere. This smaller area has been shown to translate into higher mismatching across die.

4.3 Time Walk Performance

The time walk measurements were measured as described in **Section 3.6** (page 62) for a 100:1 input amplitude dynamic range (- 2 V_{peak} to - 20 mV_{peak}). The time walk adjustment and threshold setting for each channel were adjusted to give the optimum time walk performance. For minimum input signals, the threshold was set to have the CFD output firing at a rate of approximately fifty percent. Time walk curves shown for each shaping method were plotted around a mean of zero and along the x-axis in 5 dB steps.

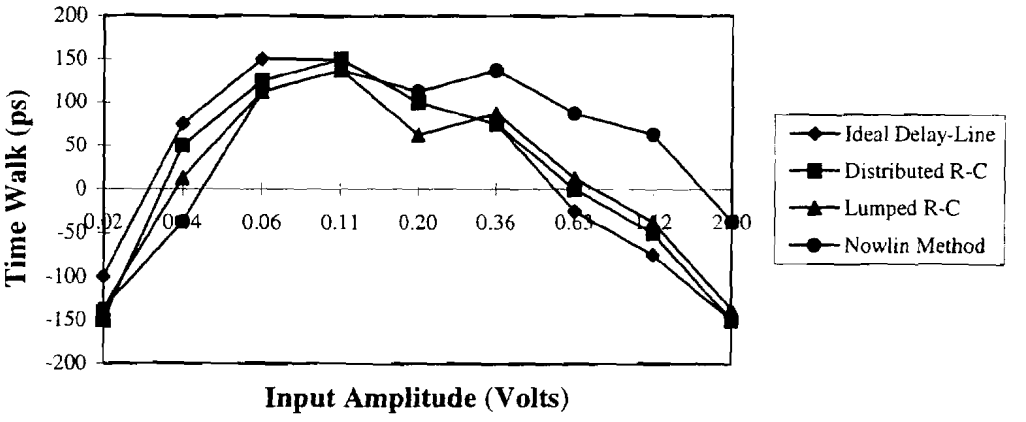
Table 4-2 shows the time walk for each channel tested while Table 4-3 shows the time walk adjustment and threshold settings. Figure 4-3 shows the best case, typical case and worst case time walk curves for each shaping method over the 100:1 dynamic range. For the best case, lumped-element R-C shaping and Nowlin method shaping possessed time walk of ± 135 ps while distributed R-C delay-line shaping and ideal delay-line shaping possessed time walk of ± 150 ps. Typical time walk was measured to be ± 150 ps for the lumped-element R-C shaping and Nowlin method shaping; ± 175 ps for the distributed R-C delay-line; and ± 185 ps for the ideal delay-line. To have some indication

Table 4-2. Table of time walk measurements for each IC tested.

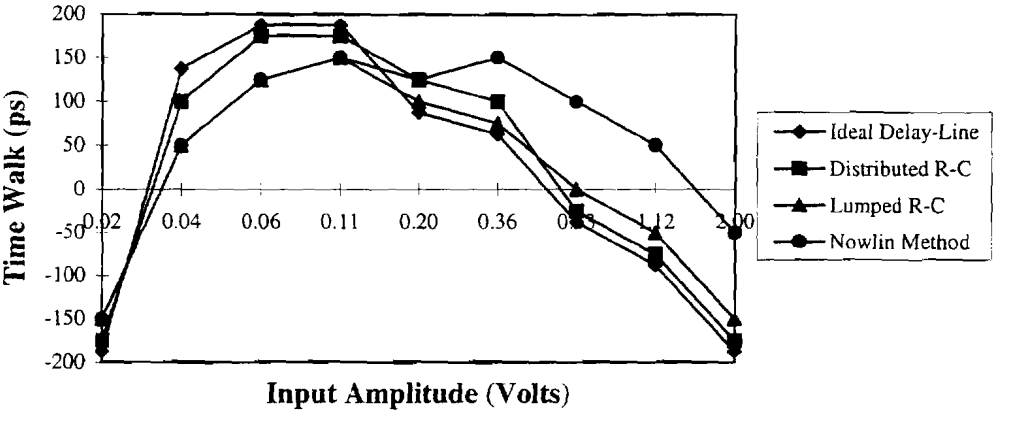
	Time Walk (± ps)			
Chip #	Ideal Delay-Line	Distributed R-C Delay-Line	Lumped-Element R-C	Nowlin Method
1	185	150	160	150
2	300	185	135	135
4	175	175	135	NA
5	225	175	150	350
6	150	175	150	150
8	175	150	160	160
9	210	175	135	175
10	225	200	160	135
11	185	150	150	150
12	160	175	175	185

Table 4-3. Table of time walk adjustment and threshold settings for each IC tested. Vset is the time walk adjustment setting and Thresh is the arming threshold.

	Time Walk and Threshold Settings (Volts)							
	Ideal Delay-Line		Distributed R-C Delay-Line		Lumped-Element R-C		Nowlin Method	
Chip #	Vset	Thresh	Vset	Thresh	Vset	Thresh	Vset	Thresh
1	3.93	1.61	3.79	1.59	3.35	1.52	2.54	1.51
2	4.02	1.47	4.02	1.43	3.67	1.48	3.49	1.48
4	4.01	1.58	3.91	1.55	3.58	1.55	NA	NA
5	4.01	1.57	3.91	1.55	3.61	1.59	3.55	1.63
6	3.54	1.60	3.59	1.61	3.25	1.61	2.89	1.46
8	3.60	1.62	3.43	1.58	3.26	1.64	2.83	1.62
9	4.01	1.44	3.99	1.44	3.69	1.48	3.43	1.49
10	4.01	1.56	3.95	1.55	3.57	1.63	3.47	1.62
11	4.00	1.50	3.80	1.50	3.68	1.56	3.55	1.56
12	3.81	1.65	3.60	1.72	3.48	1.68	3.38	1.74



(a)



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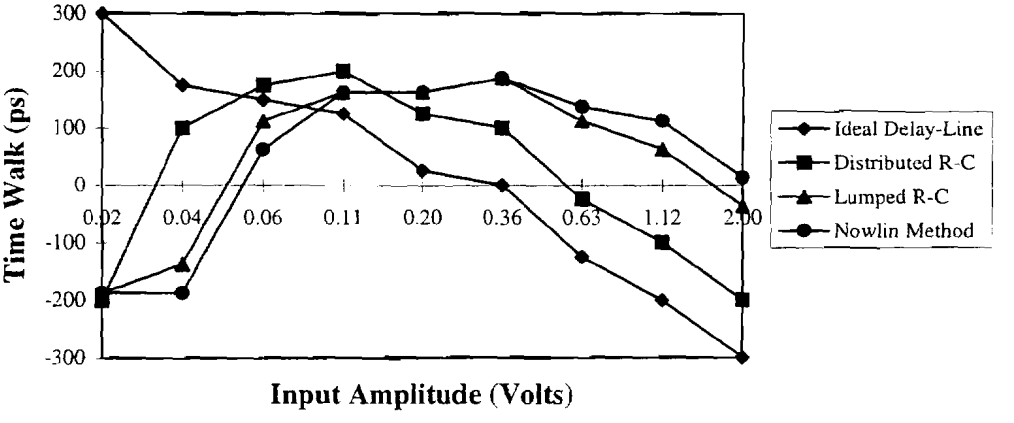


(c)

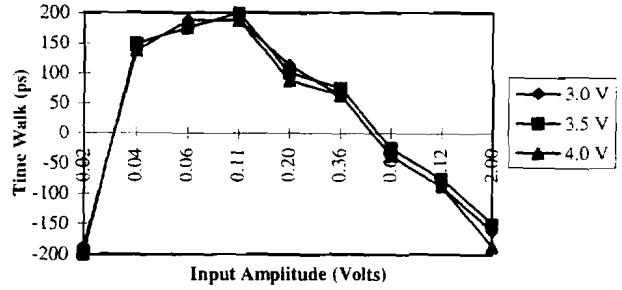
Figure 4-3. Time walk curves for the four shaping methods investigated. (a) Best case time walk. (b) Typical time walk. (c) Worst case time walk.

of time walk performance for common-mode inputs, time walk curves for a typical channel from each shaping method were generated for various input dc levels. Figure 4-4 shows the typical time walk variations with input dc levels for each shaping method. Overall, the time walk for any method appeared to vary by only 50 ps for dc input levels between + 3 Vdc and + 4 Vdc.

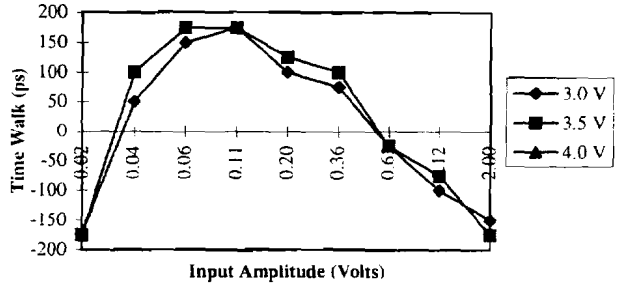
4.4 Timing Jitter Performance

4.4.1 Introduction

Timing jitter performance was evaluated for each shaping method in two categories: timing jitter due to inherent circuit noise (with variation from input test pulse equipment) and timing jitter due specifically to an input noise source. The timing jitter in this work was measured by setting the intensity of the analog oscilloscope to a maximum and determining the peak-to-peak timing jitter exhibited by the output waveform. If the timing jitter was assumed to follow a gaussian distribution, the timing jitter observed on the oscilloscope has been said to give a statistical representation of approximately six sigma (3 standard deviations on either side of the mean) or over ninety-nine percent of all the possible events. Applying this assertion, the peak-to-peak timing jitter data observed in the measurement was divided by six to obtain an approximate value of the rms timing jitter. All the timing jitter data presented in this work was then based on rms values.



(a)



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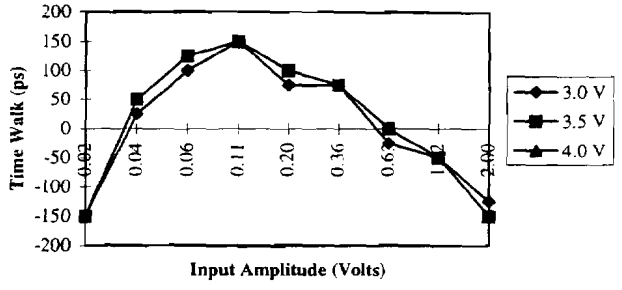

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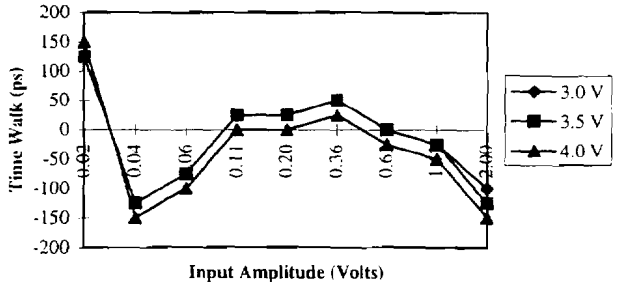


(d)

Figure 4-4. Plots of time walk for various input dc levels. (a) Ideal delay-line. (b) Distributed R-C delay-line. (c) Lumped-Element R-C. (d) Nowlin method.

4.4.2 Circuit Noise Induced Timing Jitter

The timing jitter due to CFD circuit noise (including test input variation) was evaluated during the time walk measurements. This type of timing jitter was measured for each shaping method as the input amplitude was varied over a 100:1 dynamic range. As the input amplitude was decreased, the slope through the zero-crossing decreased and the timing jitter increased. The worst case timing jitter was then determined at the minimum input signal (- 20 mV), and this value was used as the rms timing jitter specification. Table 4-4 shows the rms timing jitter for each shaping method across ten ICs. Figure 4-5 also shows the rms timing jitter for a typical channel of each shaping method as a function of input signal amplitude. The ideal delay-line and distributed R-C delay-line exhibited the lowest rms timing jitter of ± 65 ps. The lumped-element R-C shaping was slightly higher at ± 85 ps rms while the Nowlin shaping method possessed the highest rms timing jitter at ± 100 ps. These values followed the trends seen in the simulation analysis presented earlier for these shaping methods. This result indicates that the jitter due to variances in the generator used to pulse the CFD circuits may have dominated the jitter due to inherent circuit noise.

4.4.3 Input Noise Induced Timing Jitter

During the shaping network analysis, the rms timing jitter was analyzed for an input white noise source of ~ 400 nV/$\sqrt{\text{Hz}}$. Since the bandwidths of the ZCC amplifiers implemented in this work were in the high megahertz range, testing the timing jitter due to input white noise would have required an input noise source to possess a flat spectrum

Table 4-4. Table of rms timing jitter for - 20 mV peak inputs.

	rms Timing Jitter (ps)			
Chip #	Ideal Delay-Line	Distributed R-C Delay-Line	Lumped-Element R-C	Nowlin Method
1	65	85	90	85
2	100	85	85	90
4	75	85	90	NA
5	60	65	90	65
6	75	65	90	100
8	85	85	130	100
9	65	65	90	90
10	65	85	110	115
11	65	85	90	100
12	85	90	90	100

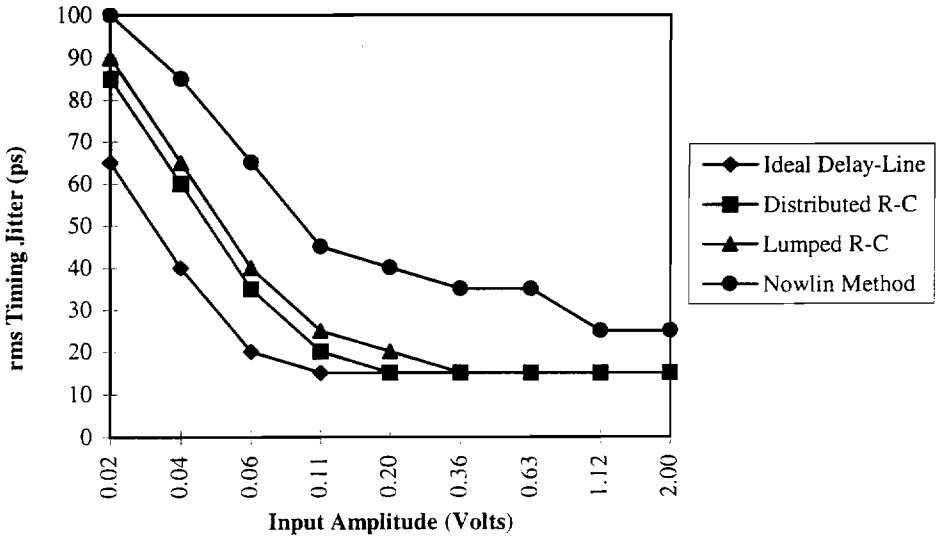


Figure 4-5. Plot of rms timing jitter with input amplitude for a typical channel from each shaping method.

well into the hundreds of megahertz range. This type of noise source was not available, and a different approach was taken to classify each shaping method's rms timing jitter due to a wideband input white noise source.

For a given input signal amplitude, consider the timing jitter to be given by

$$\sigma_t^2 = \int_0^\infty S_v \, |J(f)|^2 \, df \,, \tag{4-1}$$

where σ_t^2 is the square of the rms timing jitter in $(\text{seconds})^2$, S_v is the input noise power spectral density in $(\text{Volts})^2/\text{Hz}$ and $|J(f)|^2$ was the square of the magnitude of the transfer function relating input noise to output timing jitter with frequency in $(\text{second})^2/(\text{Volt})^2$. In the simulation analysis, $\sqrt{S_v}$ was the ~ 400 $\text{nV}/\sqrt{\text{Hz}}$ input white noise spectral density, and the input signal was a - 20 mV pseudo-gaussian input approximating the PMT output response. The purpose of this experiment was to use that same value of input white noise spectral density and input amplitude to compare measured results with simulation data. To accomplish this task, the transfer function J(f) was determined for each shaping method.

The relationship between timing jitter and input noise was determined through the application of linear systems analysis and the use of the triangle rule [21]. Consider a network with the frequency dependent transfer function H(f) representing any of the shaping methods investigated in this work. The output response to an input signal then is

$$V_{\text{network-out(p-p)}}(f) = \left[V_{\text{in(p-p)}}(f)\right] \left[H(f)\right], \tag{4-2}$$

where $V_{network\text{-}out(p\text{-}p)}(f)$ is the peak-to-peak output voltage as a function of frequency and $V_{in(p\text{-}p)}(f)$ is the peak-to-peak input voltage as a function of frequency. A single frequency sine wave introduced into the discriminator coincidentally with a test input pulse produces a deterministic timing jitter given by

$$J_{det(p-p)}(f) = \frac{V_{network\text{-}out(p\text{-}p)}(f)}{K}, \tag{4-3}$$

where $J_{det(p\text{-}p)}(f)$ is the peak-to-peak timing jitter at the network output as a function of input sine wave frequency and K is the pulse signal slope at the network output. The pulse slope at the network output is constant as long as the input pulse amplitude and shape are constant. Rearranging Equation 4-3 and substituting into Equation 4-2 gives

$$J_{det(p\text{-}p)}(f) = \frac{\left[V_{in(p\text{-}p)}(f)\right]\left[H(f)\right]}{K}, \tag{4-4}$$

or

$$\frac{J_{det(p\text{-}p)}(f)}{V_{in(p\text{-}p)}(f)} = \frac{[H(f)]}{K}. \tag{4-5}$$

Equation 4-5 makes the assumption that the timing jitter is due solely to the input sine wave source. Unfortunately, the measured data for each shaping method also possessed the timing jitter due to the inherent circuit noise of the CFD. To compare experimental data with simulation data, the amount of timing jitter due to inherent circuit noise was removed. The approach used to remove this timing jitter component is discussed below in reference to an input square wave and then extended to an input sine wave.

Consider an ideal square wave pulse possessing zero risetime. If this square wave is introduced into the discriminator in coincidence with the input test pulse, a noiseless discriminator would produce an output with pulses at two distinct locations in time. These two edges correspond to the test input pulse producing a zero-crossing that occurs during the high or low level of the square wave. Figure 4-6(a) illustrates the output response of the noiseless discriminator exhibiting some peak-to-peak timing jitter referred to as $J_{SQR_WAVE(p\text{-}p)}$. If the inherent discriminator noise is then added into the system, the discriminator output will produce two distinct pulses again, but each pulse will contain some peak-to-peak jitter $J_{INH(p\text{-}p)}$ centered around each distinct pulse as illustrated in Figure 4-6(b). Each jitter region around a distinct pulse (as observable on an oscilloscope) generated by the inherent circuit noise will mainly extend 3σ around each side of the pulse as illustrated in Figure 4-6(b). If the total peak-to-peak jitter $J_{TOTAL(p\text{-}p)}$ in Figure 4-6(c) is measured as labeled, the relationship between the total peak-to-peak timing jitter and its components at a given input square wave frequency can be given by

$$J_{TOTAL(p\text{-}p)}(f) = \tfrac{1}{2} J_{INH(p-p)} + J_{SQR_WAVE(p\text{-}p)}(f) + \tfrac{1}{2} J_{INH(p-p)}, \qquad (4\text{-}6)$$

where $\frac{1}{2} J_{INH(p-p)}$ represents the 3σ distribution of the inherent circuit noise induced timing jitter on either side of the two distinct pulses and is not dependent on the square wave input frequency. The two $\frac{1}{2} J_{INH(p-p)}$ terms in Equation 4-6 add to give the total peak-to-peak timing jitter due to inherent circuit noise. According to Equation 4-6 and this analysis, the timing jitter due to the square wave input can be calculated as

$$J_{SQR_WAVE(p\text{-}p)}(f) = J_{TOTAL(p\text{-}p)}(f) - J_{INH(p-p)}. \qquad (4\text{-}7)$$

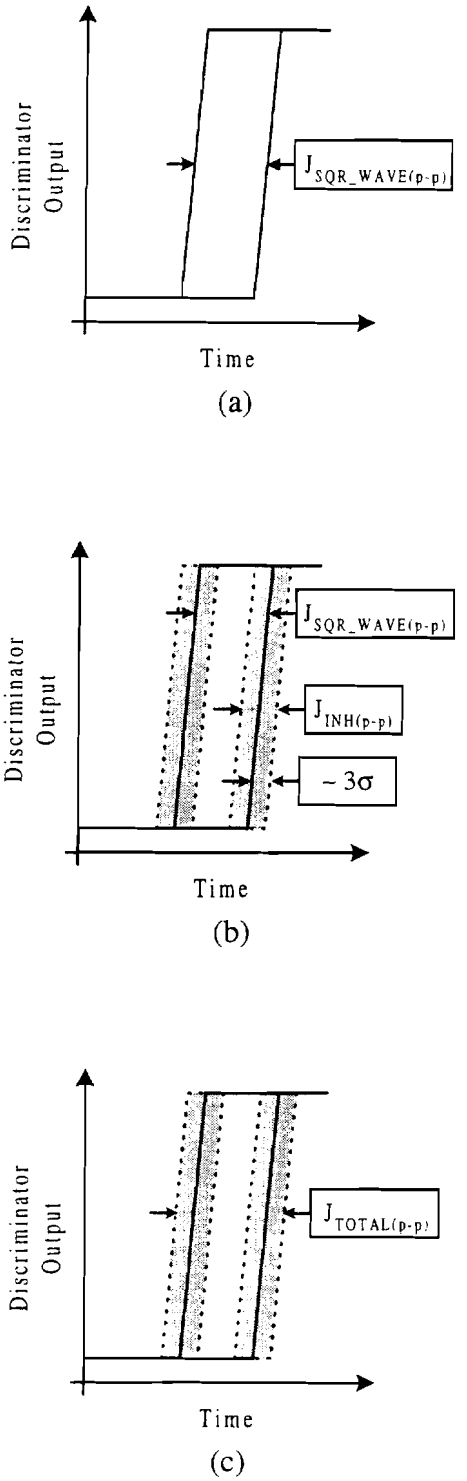


Figure 4-6. Illustration of measured peak-to-peak timing jitter analysis. (a) Timing jitter due to an input square wave with no discriminator noise. (b) Timing jitter due to an input square wave and discriminator circuit noise. (c) Total measured timing jitter.

For the test data measured for this work, the input square wave was replaced by an input sine wave. If the square wave input is replaced with a sine wave input, this analysis will still apply. The difference in the output response due to an equal amplitude sine wave input as opposed to a square wave input is the area between the two pulses. For an input sine wave, the two distinct edges are transformed into a continuous area between two less pronounced pulses which correspond to the peaks of the input sine wave. The distance in time between the edges for the two type inputs will be equal for equal amplitude inputs. Thus, for a sine wave input signal in coincidence with the test pulse, the timing jitter due only to the sine wave input $J_{SINE_WAVE(p\text{-}p)}(f)$ with frequency can be determined by

$$J_{SINE_WAVE(p\text{-}p)}(f) = J_{TOTAL(p\text{-}p)}(f) - J_{INH(p-p)}. \tag{4-8}$$

Both terms in the right side of Equation 4-8 could be determined experimentally and the sine wave induced timing jitter calculated. Through the application of Equation 4-8 to the test data, the timing jitter $J_{SINE_WAVE(p\text{-}p)}(f)$ became the deterministic timing jitter $J_{det(p\text{-}p)}$ defined in Equation 4-5. If the notation in Equation 4-8 is used to rewrite Equation 4-5, Equation 4-9 represents the transfer function needed to perform the integral in Equation 4-1 as

$$J(f) = \frac{J_{SINE_WAVE(p\text{-}p)}(f)}{V_{in(p\text{-}p)}(f)} = \frac{[H(f)]}{K}. \tag{4-9}$$

Finally, substituting Equation 4-9 into Equation 4-1 gives the timing jitter integral to be defined as

$$\sigma_t^2 = \int_0^\infty S_v \left| \frac{J_{SINE_WAVE(p\text{-}p)}(f)}{V_{in(p-p)}(f)} \right|^2 df. \tag{4-10}$$

The final timing jitter σ_t in rms units for a given S_v was found by taking the square root of the integral in Equation 4-8.

The transfer function J(f) was generated by summing an input leveled sinusoidal signal (constant amplitude with frequency) with the input pulse from the LeCroy pulse generator as illustrated in Figure 4-1. For the summation box shown earlier in Figure 4-1 and detailed in Figure 4-7, the looking-in impedance from any port was 50 Ω assuming the devices connected to the other two inputs were back-terminated with 50 Ω. The minimum input signal corresponding to the - 20 mV signal used in simulations was summed with an input sinusoidal level sufficient to dominate the observed timing jitter. With this input realization, the peak-to-peak timing jitter for a typical channel of each shaping method was measured. The peak-to-peak jitter due to inherent CFD circuit noise was measured with the input sine wave amplitude equal to zero.

Figure 4-8 shows the transfer functions for each shaping method generated through the process just described. The y-axis represents measured data after inherent noise induced jitter was removed. The ideal delay-line, the distributed R-C delay-line and the lumped-element R-C shaping networks exhibited lower timing jitter for low frequencies and peaking in the transfer function at higher frequencies. These three transfer functions also possessed some roll-off at lower frequencies. Nowlin shaping exhibited much higher jitter at lower frequencies and roll-off at higher frequencies with no apparent peaking. Total jitter for each shaping method was approximated using Equation 4-8 by performing numerical integration of the transfer functions shown in Figure 4-8 up to 265 MHz. Figure 4-9 shows the four transfer functions on the same plot

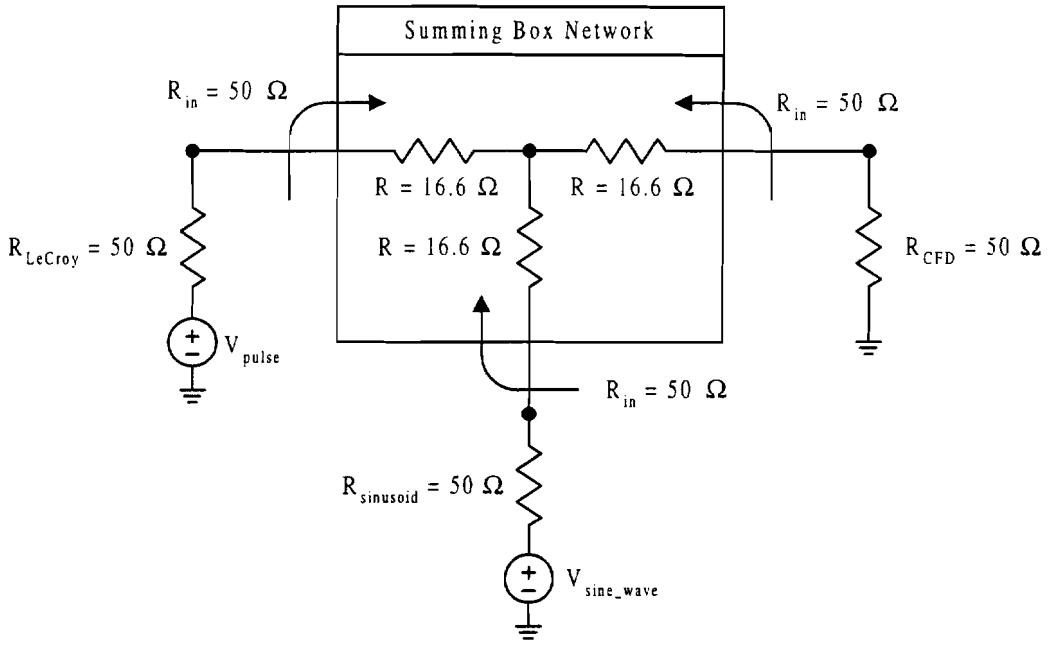
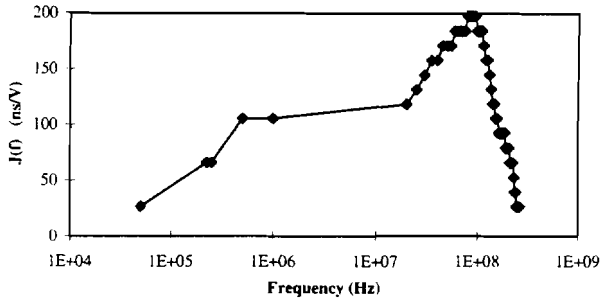
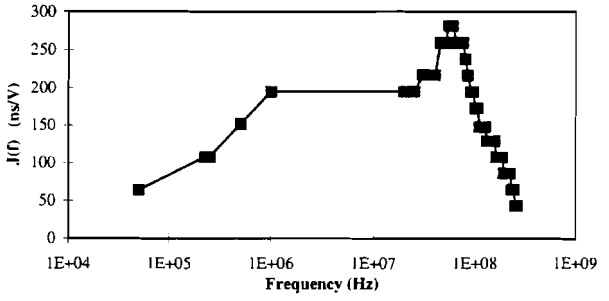


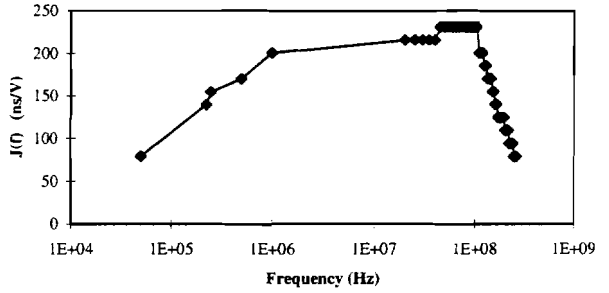
Figure 4-7. Illustration of the summing network used to combine the input pulse with a sine wave.



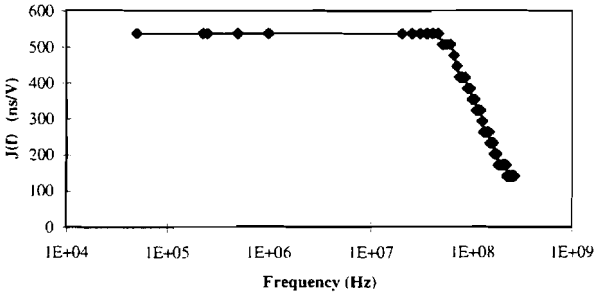
(a)



(b)



(c)



(d)

Figure 4-8. Plot of the input sine wave induced timing jitter transfer function generated for each shaping method. (a) Ideal delay-line. (b) Distributed R-C delay-line (c) Lumped-Element R-C. (d) Nowlin method.

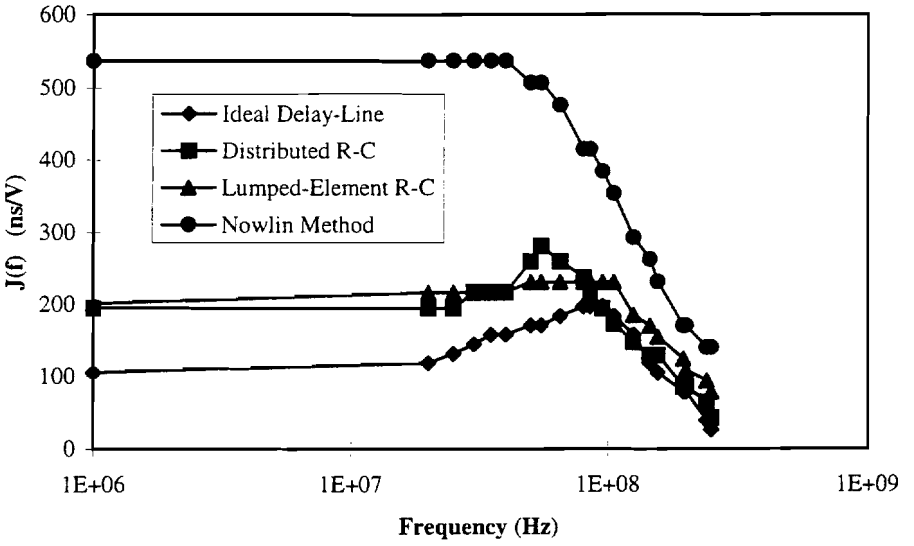


Figure 4-9. Plot of the input sine wave induced timing jitter transfer function showing relative values.

to convey relative values. Table 4-5 compares the rms timing jitter results obtained through simulation and experimental data with $\sqrt{S_n}$ = ~ 400 nV/$\sqrt{Hz}$.

HSPICE simulations during the early stages of this work were based on HSPICE predictions for the bandwidth of each amplifier in the ZCC. The simulated data predicted very little peaking in the frequency response for any of the methods investigated. Nowlin method shaping was expected to possess a higher jitter at lower frequencies as seen in the measured data. If the bandwidths of the amplifiers in the ZCC were higher than that predicted by HSPICE simulations, the peaking seen in the measured data would be expected for the ideal delay-line, distributed R-C delay-line and the lumped-element R-C shaping. Simulations also predicted that a higher bandwidth would decrease the timing jitter in each shaping method investigated. Although the distributed R-C delay-line and the lumped-element R-C shaping methods possessed zero-crossing times slightly different than the ideal delay-line and the Nowlin method shaping, the shaping method experimental timing jitter data followed the general trends predicted by simulation data.

4.5 Die Area and Power Consumption

The necessary die area required to realized each shaping method has been compared in Table 4-6. The ideal delay-line area required only the fraction circuit to be realized on-chip and this area was included to indicate relative size. The distributed R-C delay-line and the lumped-element R-C shaping networks utilized this same fraction circuit as the ideal delay-line. Nowlin shaping required the least die area including fraction circuit and interconnect. Table 4-7 gives the die area required for the full CFD

Table 4-5. Table comparing simulation predictions to measured results for timing jitter due to an input noise source.

Shaping Method	rms Timing Jitter for ~ 400 nV/√Hz		Percent Diff. (%)
	HSPICE (ns)	Measured (ns)	
Ideal Delay-Line	1.05	0.85	- 19.0
Distributed R-C Delay-Line	1.26	1.07	- 15.1
Lumped-Element R-C	1.31	1.15	- 12.2
Nowlin Method	2.27	2.26	- 1.0

Table 4-6. Comparison of die area required to realize each shaping method.
Note: The ideal delay-line possessed external delay and represents only the fraction circuit area.

Shaping Method	Die Dimensions (μm)	Total Die Area $(\mu m)^2$
Distributed R-C Delay-Line	172 x 70	12040
Lumped-Element R-C	160 x 65	10400
Nowlin Method	179 x 53	9487
Ideal Delay-Line	67 x 65	4355

Table 4-7. Comparison of the full CFD implementation for each shaping method.

Shaping Method	Die Dimensions (μm)	Total Die Area $(\mu m)^2$
Distributed R-C Delay-Line	195 x 842	164190
Lumped-Element R-C	195 x 836	163020
Nowlin Method	195 x 817	159315
Ideal Delay-Line	195 x 836	163020

implementations for the four shaping methods investigated. Table 4-8 lists the power drawn from the single + 5 Vdc supply. Seven channels of CFD discriminators were fabricated on each IC, and four were characterized for this work. The other channels implemented on this IC were included for other purposes. Average power dissipation per channel $P_{channel}$ was calculated as

$$P_{channel} = \frac{(I_{total})(5\ V)}{7\ Channels}, \qquad (4\text{-}11)$$

where I_{total} was the total IC current consumed from the + 5 Vdc supply. The IC referenced as Chip #4 possessed a dead Nowlin shaping channel as indicated in the earlier tables of measured data, and the current for this IC was very high compared to the other test ICs. This high value of current was contributed to some defect in the Nowlin shaping channel.

Table 4-8. Table of power dissipation per channel for ten ICs.

Chip #	Total Chip Current (mA)	Power / Channel (mW / Channel)
1	17.09	12.2
2	17.62	12.6
4	32.43	23.2
5	18.40	13.1
6	17.15	12.3
8	16.37	11.7
9	17.39	12.4
10	18.61	13.3
11	17.48	12.5
12	17.21	12.3

Chapter 5

Conclusions and Discussion of Future Work

The suitability of several integratable shaping techniques for the PHENIX Lead-Scintillator Calorimeter CFD has been investigated in this work. Time walk and timing jitter were considered as implemented with a CMOS CFD. Several design enhancements were made to an existing ORNL designed CMOS CFD for integration into the PHENIX Lead-Scintillator Calorimeter readout electronics. Single-ended input was converted to differential input, and the input for dc feedback in the arming circuit was moved to an internal node. This CFD was also altered to operate at a + 4 Vdc level instead of the original + 2.5 Vdc. The logical AND gate coincidence gating architecture was replaced with D flip-flop type coincidence gating to prevent the possibility of leading-edge walk. Each integratable shaping method implementation employed in this work required a relatively small die area and consumed no power from the dc supply. As implemented with the revised CMOS CFD, each shaping method provided subnanosecond time walk and timing jitter for a 100:1 input amplitude dynamic range. These circuits were fabricated in a standard CMOS IC process available through Orbit Semiconductor.

Various shaping methods were presented as possible implementations. The C-R differentiator and Binkley shaping method techniques did not meet the requirements for the PHENIX PbSc CFD. The distributed R-C delay-line and lumped-element R-C

shaping methods were compared based on the amount of signal amplitude and leading-edge slope degradation in the delayed signal. The modeling of the distributed R-C delay-line using the HSPICE Umodel utility with geometrical input parameters was discussed. The HSPICE Umodel utility was found to be sufficient in the analysis of transient response data, but ac analysis showed some discrepancy from an explicit model. The resistance of the delay-line was also modeled as noiseless by the HSPICE Umodel utility during ac analysis. For this work, an explicit 20-lump approximation was used during HSPICE analysis. The Nowlin method was chosen as a candidate CFD shaping method as well, and the design equations presented by Nowlin were used as an approximation for the CFD implemented.

Twelve ICs were fabricated containing one CFD channel for each shaping method investigated, and ten of the twelve ICs were functional. Time walk for each channel was evaluated over the 100:1 dynamic range of input amplitude. Timing jitter was evaluated for each shaping method for inherent circuit noise induced timing jitter and input noise induced timing jitter. Timing jitter evaluated due to input noise was found to follow the same trends as predicted by simulation. The distributed R-C delay-line was deemed the shaping method of choice for integration into the PHENIX Lead-Scintillator readout electronics. Although the Nowlin shaping method possessed the lowest time walk, this method exhibited the highest rms timing jitter due to either the inherent circuit noise or to an input white noise source. Based on these characteristics, the Nowlin method was not chosen as the shaping method of choice. Distributed R-C delay-line shaping method possessed slightly higher time walk than the lumped-element R-C shaping. However, the

distributed R-C delay-line exhibited lower rms timing jitter due to either a white noise input or inherent circuit noise. Overall, the distributed R-C delay-line may provide slightly higher resolution timing data to be used in the separation of photons and charged particles.

Several suggestions are appropriate for considerations of future work. The time walk and timing jitter performance were approximated with oscilloscope readings as rms values. With a TAC and multichannel analyzer, the data distribution could be determined and the related data presented in terms of the given distribution. Since the electronics for the PHENIX Lead-Scintillator Calorimeter at RHIC will be air cooled and the temperature range of operation could be over a moderate range, the temperature effects on timing performance should be investigated. To further characterize the CFD, power supply rejection ratio may also be a concern. The time walk and rms timing jitter data for this work was collected with an input dc level that was constant with input amplitude. Since the passive integrator will present a varying dc level shift to the CFD inputs with varying PMT output amplitude, a fast current pulser and passive integrator circuit should be used to test the CFD for any adverse effects not presently expected.

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Vita

Gentry Jackson was born in Union City, Tennessee on August 18, 1971. He attended Obion County Central High School located in Troy, Tennessee where he graduated as Salutatorian in May, 1989. During the Fall of 1989, he entered the pre-engineering program at The University of Tennessee, Martin. Upon completion of this program, he transferred to The University of Tennessee, Knoxville in August, 1992. He received his Bachelor of Science in Electrical and Computer Engineering from UT-Knoxville in May, 1994 graduating Summa Cum Laude. During his undergraduate study, Gentry was involved with several organizations and honor societies including the IEEE, Tau Beta Pi, Eta Kappa Nu and Phi Kappa Phi.

Gentry entered directly into the Master of Science program at The University of Tennessee, Knoxville in August, 1994. He was awarded a position as a graduate teaching assistant in the Electrical Engineering Department's J. Frank Pierce Electronics Laboratory. After one year, he accepted a new position as a graduate research assistant in UTK's Mixed Signal-VLSI Joint-Program with the Oak Ridge National Laboratory. His assignment was in the Monolithic Systems Development Group of the Instrumentation and Controls Division performing analog circuit design. During his work at ORNL, Gentry has authored his first technical publication and is currently listed as the co-author of five other technical publications.