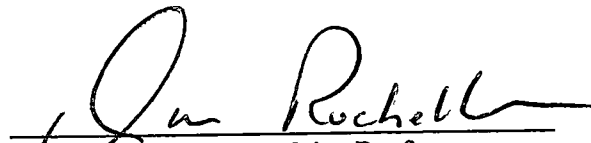
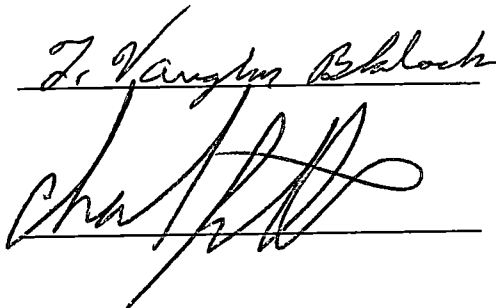


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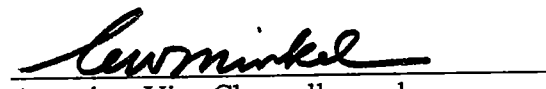
I am submitting herewith a thesis written by Jeffrey Lynn Falin entitled "A CMOS Wideband Amplifier for use in a Microcantilever Sensing Device." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.


James M. Rochelle, Major Professor

We have read this thesis
and recommend its acceptance.


Dr. Vargha Bhattacharya

Accepted for the Council:


Associate Vice Chancellor and
Dean of the Graduate School

**A CMOS Wideband Amplifier for use in a Microcantilever
Sensing Device**

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Jeffrey L. Falin
May 2000

ACKNOWLEDGEMENTS

I would like to acknowledge the following individuals for their roles in helping me to complete this phase of my education. First and foremost, I would like to thank Bruce Warmack who was the Principle Investigator on the research project that funded this work. In addition, I would like to thank T.V Blalock for his role in getting me accepted to the University of Tennessee and his encouragement and support while I completed my second undergraduate degree in Electrical Engineering. I would like to thank Mike Simpson and the UT Joint Program committee for accepting me into the joint program. For Charles "Chuck" Britton and James Rochelle, I give my undying gratitude for enduring me as their graduate student during these past 18 months. I would also like to express my gratitude to all of the researchers and support staff of ORNL's Instrumentation and Controls Division's Monolithic Sensors group, especially Bill Bryan, Nance Ericson, Gayle Jones, Bruce Warmack, and Alan Wintenberg, for their help, guidance and support. All of these individuals have taught me not only about how to be a better engineer but also about how to be a better person and for that I am eternally grateful. I only hope that I have given them something of equal or greater value.

There are other individuals who also deserve thanks. To John Barton, words cannot express the gratitude that I have for all he has done for me. To all of my fellow classmates, especially Chris Arnott, who struggled along with me through this difficult but rewarding graduate program, I am most appreciative for their support and friendship.

Lastly I would like to thank my parents, Robert and Janet Falin, and the remainder of my family. Although not supportive of my career change at first, they were, as always, there when I needed them the most over these past three and one-half years of schooling.

This research was funded in part by a research grant from the Explosives Study Group, Bureau of Alcohol, Tobacco and Firearms, U.S. Treasury Department, Washington, DC. The Principle Investigator for the research was Bruce Warmack. The majority of the work was performed at the Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corp. for the United States Department of Energy under Contract No. DE-AC05-96OR22464.

ABSTRACT

Four different designs for a wideband, open-loop amplifier for potential use in a microcantilever sensor platform were designed, fabricated and evaluated in two different processes, the AMI 0.8 μm and AMI 1.2 μm 5 V CMOS processes. Bench performance testing of the amplifiers was performed and compared to simulation results. The measured amplifiers' gains ranged from approximately 5 to 11 V/V and the bandwidths ranged from approximately 75 MHz to 195 MHz. Power consumption was below 15 mW for all designs. Differences between experimental and simulated results were investigated and the best performing amplifier design was recommended. In conjunction with designing the amplifiers, a review of the two different fabrication processes was performed, primarily through DC characterization of test transistors and comparison with HSpice simulation results

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Chapter 1

The Electronic Nose

1.1 What are MEMS?

Microelectromechanical systems, or MEMS, are not only of interest to researchers in science and engineering but are fast becoming of commercial interest. It has been known since the late 1960's that silicon and other semiconductors could be used for the production of miniature transducers. In fact, pressure sensors and accelerometers have been made from MEMS for many years. More recently, government researchers have developed more complex structures ranging from simple cantilevers and hinges to gear-driven transmissions. Continuing improvements in integrated circuit processing technology, including lithography and bulk etching techniques, have made "micromachining" of these structures possible. In addition, technology improvements allow for ever-decreasing sizes of these structures. Smaller structures not only reduce the volume, weight, and therefore cost of the MEMS devices, but may also lead to improved performance and reliability. For example, it has been theoretically and experimentally proven that the measurement sensitivity of a cantilever is inversely proportional to its thickness [1].

1.2 Cantilever Sensors

Cantilevers perform well as micromechanical sensors. For example, atomic force microscope (AFM) cantilevers have been used to perform different types of physical, chemical, and biological detection. Using cantilevers as sensors requires that the cantilevers be coated with a chemically specific coating. Fig. 1¹ shows a cross section of a coated cantilever. As the species of interest reacts with or is absorbed by the coating, the mass on the cantilever changes. This mass change causes the cantilever's behavior to change, depending on the location of the coating. Fig. 2 illustrates the modes of cantilever operation. If the coating is at the base of the cantilever, the change in mass results in the cantilever bending. When the coating is placed near the end of the cantilever, the cantilever's resonant frequency decreases. A relationship can then be developed between the amount of bending or of the change in resonant frequency and the amount (i.e., concentration) of the species of interest. The typical dimensions of commercially available microcantilevers are 50-200 μm long, 10-40 μm wide and 0.3-3 μm thick, with mass in the range of a few nanograms. The resonant frequency of these cantilevers ranges from a few kHz to a few hundred kHz. Higher modes have been observed in the tens of MHz [1].

AFM microcantilever measurement systems based on resonant frequency changes have been demonstrated in the measurement of temperature, humidity, mercaptans, toluene, mercury vapor, force, pressure, acceleration, flow rate, viscosity

¹ All figures are in Appendix 1

Temperature sensitivities down to 10^{-5} K and mercury vapor and mercaptan ppb or ppt measurements have been obtained [1].

1.3 The Electronic Nose

1.3.1 System Level Design

The proposed electronic nose will be a battery-powered, handheld device that will monitor resonant frequency changes among an array of end-coated microcantilevers in order to measure concentrations of various vapors. Fig. 3 is a block diagram of the proposed electronic nose. The system will consist of an array of end-coated cantilevers each being driven at its base by an oscillator at the undisturbed cantilever's resonant frequency. After an air sample is taken, the cantilever's new resonant frequency, along with higher modes, will be measured, converted to a voltage signal, and amplified as necessary through a series of wideband amplifiers. Then, a bandpass filter will be used to narrow the signal bandwidth to the frequency range of interest. The resonant frequency at the end of the cantilever will be different than the frequency at which the base is being driven if the species of interest was detected. An as yet undesigned frequency detection circuit will then determine if the signal contains the frequencies and higher acoustic modes. A micro-controller will perform a modal analysis and compute the concentration of the gaseous species of interest. The user would then be notified of the presence of the species of interest on the LCD display.

1.3.2 Modal Analysis

In order to achieve the highest level of sensitivity, the micro-controller of the system will perform an analysis of acoustic tones higher than the fundamental mode. The fundamental frequency of a cantilever is

$$f = \frac{1}{2\pi} \sqrt{\frac{k}{m_{eff}}} \quad (1.1)$$

where k is the spring constant and m_{eff} is the effective mass of the cantilever and is typically 10 kHz to 300 kHz depending upon its dimensions. Harmonic overtones are found at non-integer multiples of the fundamental frequency and can be up to several megahertz for a cantilever with a fundamental of under 100 kHz. The sensitivity of vapor concentration measurements can be greatly increased using acoustic overtones in a modal analysis. For the microcantilever, enhancements of as much as two orders of magnitude have been observed [2].

1.3.3 Specifications for a Wideband Amplifier

Sufficient signal amplitude and bandwidth are required for the system to function. In addition, in order to improve sensitivity using modal analysis, higher modes of the signal in the tens of MHz range need to be processed with little harmonic distortion. Since only a system level design for the electronic nose has been finalized, other design constraints have not yet been determined. Therefore, the amplifiers designed in this work were designed to provide overall optimal performance for general applications. Specifically, a gain-bandwidth product of 1 GHz, with DC gain of 10 and 100 MHz bandwidth, was the primary design goal. Only 5-volt CMOS processes were considered because the achievable signal-to-noise ratio is superior to lower voltage processes. The amplifiers were designed to be cascaded so the input common mode voltage must match the output common mode voltage. In order to achieve maximum dynamic range, the

output voltage the amplifier was set at about 2.5 V. Finally, a power dissipation of less than 30 mW was imposed.

1.4 Scope of Thesis

This work presents a preliminary, high-level design for a cantilever based sensor platform, using resonant frequency change of selectively coated cantilever arrays as the detection method. Different designs for the wideband, open-loop amplifier for use in the microcantilever sensor platform were designed, fabricated and evaluated in two different processes, the AMI 0.8 μm and AMI 1.2 μm 5 V CMOS processes. Bench performance testing of the amplifiers was performed and compared to simulation results. Differences between experimental and simulated results were investigated and the best performing amplifier is recommended. In conjunction with designing the amplifiers, a review of the two different fabrication processes is performed, primarily through DC characterization of test transistors and comparison with HSpice simulation results. From this review, one of the two processes is recommended for implementing the entire sensor platform.

Chapter 2 is a discussion of wideband amplifier design. Various design techniques for wideband operation will be presented. The four designs chosen for evaluation, along with hand calculations and simulation results from each process, are then presented. A biasing structure for the amplifier with the potential to improve amplifier operation over process and temperature variation is also presented.

Chapter 3 presents the test chips and the method of testing used in obtaining the measured results. Measured results for the amplifiers and biasing structure are then compared to simulated results. Chapter 3 concludes with possible explanations as to the differences between measured and simulated results.

Chapter 4 is an analysis of the processes in which the amplifier designs were fabricated. Primarily, HSpice model evaluations are performed by comparing measured results of fabricated test transistors with HSpice simulated results.

The thesis is concluded in Chapter 5 with recommendations on which amplifier and process should be used in the sensor platform as well as recommendations for future work.

Chapter 2

Design of a CMOS Wideband Amplifier

2.1 CMOS Amplifier Design

2.1.1 CMOS Modes of Operation

Bipolar transistors have historically been used in high-speed applications because they typically provide a larger transconductance, g_m , and frequency response, f_T , than comparably sized and powered MOSFET transistors. However, with digital design in CMOS processes dominating the design industry, pure bipolar and even BiCMOS processes are becoming less and less accessible and practical for analog circuit design. Therefore, a thorough understanding of CMOS modes of operation and wideband design issues is necessary before designing high-speed amplifiers in CMOS

For the following discussion, the size of the MOSFET is assumed fixed and finite output impedance and body effect are ignored. The CMOS small signal model is shown in Fig. 4. From this model, the frequency response of the transistor can easily be derived and is shown below.

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD} + C_{GB})} \quad (2.1)$$

In order to understand how the transconductance affects the speed of a transistor, a further understanding of MOSFET regions of inversion and modes of operation is required. A MOSFET has three regions of channel inversion with respect to gate-to-source voltage, weak inversion, sometimes called subthreshold, strong inversion, and the transition between weak and strong inversion, referred to as moderate inversion. If the transistor is operating in weak inversion, the gate-to-source voltage is less than the transistor's threshold voltage or $V_{GS} < V_T + n(kT/q)$ where n is approximately 3. Analysis shows that the drain current, I_D , for a transistor operating in the subthreshold region is similar to that of a bipolar transistor and is given by

$$I_D \cong I_{D0} \left(\frac{W}{L} \right) e^{\frac{qV_{GS}}{nkT}} = I_{D0} \left(\frac{W}{L} \right) e^{\frac{V_{GS}}{nV_t}}. \quad (2.2)$$

Simple differentiation of (2.2) gives the transconductance as

$$gm \cong \frac{\partial(I_D)}{\partial(V_{GS})} = I_{D0} \left(\frac{W}{nV_t L} \right) e^{\frac{V_{GS}}{nV_t}} = \frac{I_D}{nV_t}. \quad (2.3)$$

From (2.1), the frequency response for the transistor, f_T , can be rewritten as

$$f_T \cong \frac{I_D}{2\pi(C_{GS} + C_{GD} + C_{GB})nV_t} \quad (2.4)$$

From (2.4), f_T is directly proportional to I_D but is very small at very low values of V_{GS} .

Therefore, subthreshold operation is used mostly for low power, low frequency applications.

For transistors operating in moderate or strong inversion, $V_{GS} > V_T$. Fig. 5 shows normalized I_D vs V_{DS} curves at various gate voltages. In the triode mode of operation,

$V_{DS} < V_{GS} - V_T$ and, as expressed in (2.5), the drain current varies almost linearly with the gate voltage for a given drain to source voltage.

$$I_D = K \frac{W}{L} [V_{GS} - V_T] V_{DS} \quad (2.5)$$

Differentiating (2.5) with respect to V_{GS} gives

$$g_m = K \frac{W}{L} V_{DS} \quad (2.6)$$

Substituting (2.6) for g_m into (2.1) gives

$$f_T = \frac{K \frac{W}{L} V_{DS}}{2\pi(C_{GS} + C_{GD} + C_{GB})}. \quad (2.7)$$

Therefore, for a fixed size transistor with fixed V_{DS} and operating in the triode mode of operation, f_T is constant.

For a transistor to be in strong inversion, $V_{GS} > V_T$ by 150-200 mV. Furthermore, for a transistor to be properly biased in the saturated or active mode, V_{DS} must be greater than $V_{DS-SAT} = V_{GS} - V_T$. In the active mode, the drain current is given by

$$I_D = \frac{K W}{2 L} (V_{GS} - V_T)^2 \quad (2.8)$$

and the transconductance is given by

$$g_m = K \frac{W}{L} (V_{GS} - V_T). \quad (2.9)$$

Substituting (2.9) for g_m into (2.1) gives

$$f_T = \frac{K \frac{W}{L} (V_{GS} - V_T)}{2\pi(C_{GS} + C_{GD} + C_{GB})} = \frac{\sqrt{2K \frac{W}{L} I_D}}{2\pi(C_{GS} + C_{GD} + C_{GB})} \quad (2.10)$$

Eq. (2.10) shows that f_T varies as the square root of the drain current, which means that large currents would further increase the f_T of the transistor. However, the decreasing output resistance, r_o , of short channel length MOS transistors causes a decrease in maximum amplification. Therefore, while biased in the active mode, a compromise between bias point, directly related to transistor speed as shown in (2.10), and gain must be reached [3].

Mobility degradation and velocity saturation impose an upper limit on the amount of current that will effectively increase the speed of the transistor. For large values of V_{GS} , these second order effects result in the current in the MOSFET returning to a linear relationship as illustrated in Fig. 5 and shown below

$$I_D = B_1 (V_{GS} - V_T) \quad (2.11)$$

where B_1 is a scaling constant. Differentiating gives the transconductance as the constant B_1 . The frequency response of the transistor reduces to

$$f_T = \frac{B_1}{2\pi(C_{GS} + C_{GD} + C_{GB})} \quad 2.12$$

which is a constant for a transistor with fixed size and V_{DS}

To summarize, in weak inversion, a fixed size transistor's g_m varies directly with bias current but the currents are so small that the transistor speed suffers. In moderate to strong inversion, only transistors biased in the active region have transconductances that vary as the square root of the drain current. The transconductances of transistors

operating in triode mode or velocity saturation are constant and therefore place lower and upper limits, respectively, on the f_T of the transistor

If the transistor's sizes are not fixed as previously assumed, the transistor's capacitance values in the denominator of (2.1) vary directly with the product of the transistor width and length. In each of the cases previously discussed, the transconductance in the numerator of (2.1) varies as the W/L ratio. Therefore, the transistor width variables in the transconductance and capacitances effectively cancel. However, the transistor length variables from the transconductance and capacitances multiply thereby making f_T vary inversely as the square of the transistor's length. Lastly, the transconductance, and therefore, the f_T , of a transistor biased in the active mode of operation varies directly with the transistor's mobility, μ . Since the mobility of a n-channel transistor is larger than that of a p-channel transistor fabricated in the same process, the n-channel transistor will have a higher transconductance and therefore, f_T , than a p-channel transistor. So using minimum length n-channel devices biased in the active mode of operation is critical for increasing a circuit's frequency response.

2.1.2 High Speed Design Techniques and Structures

High speed circuit design centers around minimizing the resistive-capacitive (RC) load at each node in the circuit, thereby minimizing voltage excursions at each node to cause very small capacitive charging currents. Use of voltage feedback in high speed circuits must be done with great care as feedback circuits inevitably have nodes with large resistors for increasing loop gain and/or large capacitors to provide loop stability, leading to a large RC load at a particular node.

Maximizing gain-bandwidth product can be achieved either by maximizing gain or maximizing bandwidth. Typically, increasing one results in decreasing the other. For example, using large resistors to both provide DC bias in the circuit and to provide large small signal loads provides high gain; however, the large resistor coupled with the capacitance at that node creates a large RC time constant that reduces the bandwidth of the circuit. Another way to provide DC bias and a small signal load is to use a diode-connected MOSFET to form a non-linear resistor, as shown in the simple common-source amplifier in Fig. 6. The small signal equivalent circuit for the common-source amplifier is shown in Fig. 7. Solving for the voltage gain gives

$$g_{m2}v_{d2} + \frac{v_{d2}}{r_{o2}} = -g_{m1}v_{gs1} - \frac{v_{d2}}{r_{o1}}, \quad (2.13)$$

and

$$\frac{v_{d2}}{v_{gs1}} = \frac{v_o}{v_i} = \frac{-g_{m1}}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}}. \quad (2.14)$$

Neglecting channel-length modulation, the gain reduces to

$$\frac{v_o}{v_i} = \frac{-g_{m1}}{g_{m2}} = -\frac{\sqrt{2K_n I_D \frac{W_1}{L_1}}}{\sqrt{2K_p I_D \frac{W_2}{L_2}}} = \frac{\sqrt{u_n \frac{W_1}{L_1}}}{\sqrt{u_p \frac{W_2}{L_2}}}, \quad (2.15)$$

which is simply a ratio of the square root of the device geometries and mobility

Practical device geometries limit the maximum voltage gain for this type of design to about 20. However, since the voltage gain is independent of the dc operating point to first order, the transfer function, as shown in Fig. 8, is highly linear as long as both

devices are in saturation. Also, the maximum dynamic range of the circuit is limited to one threshold voltage below the positive rail. This design is useful for implementing wideband, low-gain amplifiers with high linearity and moderate dynamic range [4].

One way to eliminate the need to charge capacitors at nodes with large RC time constants is to convert from voltage to current and use current amplification as illustrated in the block diagram of Fig. 9. The transconductance stage can be implemented with a simple differential pair. Current amplification can be achieved through the use of current mirrors or with a clever transimpedance design. Note that the first two blocks taken together without feedback form the beginnings of an operational transconductance amplifier. The transimpedance stage can be implemented using a very simple transimpedance amplifier with current feedback. An appropriate output driver is necessary to drive a capacitive load [5].

Other more complex circuit design methods, such as pole-zero cancellation or peaking technique, that increase circuit bandwidth are available. However, these techniques are sensitive to process and temperature variations. In the case of pole-zero cancellation, insufficient cancellation results in long settling times, commonly referred to as the doublet effect [5].

Two final considerations for the design are its linearity and noise. Since the application for this amplifier requires that a wide range of frequencies representing the various modes of the cantilever be passed, high linearity is an important design specification to ensure that harmonic tones due to non-linearity are not interpreted as cantilever modes by the system. A fully differential amplifier would improve linearity by eliminating the even order harmonics. Typically, in fully differential designs, only the

third order harmonics have enough power to be of concern. The fully differential design would also provide an effective method of common mode signal rejection and, if necessary, would provide a way to minimize signal amplitude swing through the conversion of a single-sided signal to a differential signal. Also, assuming each side of the amplifier is physically laid-out beside the other, effects from cross-talk with other devices on the chip and chip voltage gradients would be virtually eliminated.

Noise contribution by any device early in the signal path of a system is of concern because the noise of the device may overwhelm the signal of interest. Since the interface between the cantilever sensor and amplifier has not been specified, there is no input signal level or noise power specification for the amplifier design.

2.2 Two Stage Wideband Amplifier

2.2.1 Circuit Design

The simplest design for a wideband amplifier capable of driving a modest size capacitive load would be an appropriately loaded differential pair followed by a source-follower output driver. Figs. 10 and 11 show two two-stage designs, one with an enhancement-mode load and one with a resistive load. Ignoring body effect, assuming infinite output impedance, and assuming that the source follower output stage has an ideal gain of unity, the gain calculations for each of the amplifiers above are given by (2.15) and (2.16), respectively

$$A_v = \frac{g_{m1}}{g_{m2}} = \sqrt{\frac{u_n \frac{W_1}{L_1}}{u_p \frac{W_2}{L_2}}} \quad (2.15)$$

Table 2.1 - Two-Stage Amplifier Device Sizes and Design Currents

	Device	AMI 0.8um Process		AMI 1.2um Process	
		Size (um)	Designed Bias Current (mA)	Size (um)	Designed Bias Current (mA)
Two Stage	M1	120/1	0.502	480/1.2	0.682
w/ Enhancement	M2	12/1	0.502	36/1.2	0.682
Load	M3	350/1	1.222	600/1.2	1.003
	Mb7	500/5	1.004	840/6	1.363
	Mb8	600/5	1.222	600/6	1.003
Two Stage w/	M1	180/1	0.703	480/1.2	0.730
Resistive Load	M2	350/1	1.230	600/1.2	1.011
	Mb7	700/5	1.406	900/6	1.461
	Mb8	600/5	1.230	600/6	1.011
	Rload	2502 ohm	0.703	2400 ohm	0.730

$$A_V = g_{m1} R_{LOAD} \quad (2.16)$$

Table 2.1 summarizes the device sizes and original design currents. Device sizes and bias currents were chosen to provide maximum gain as predicted by (2.15) and (2.16) while keeping the input transistors close to 200mV into saturation and an output voltage near the common mode input voltage of 1.5 V. Also, the output stage device sizes and currents were chosen to ensure that the output stage would not significantly affect the frequency response of the circuit with a 10 pF load. Therefore, the dominant pole for both amplifiers will be at the drain of the differential pair and is given as

$$f_{DOM} = \frac{1}{2\pi C_{total} R_{eqv}}, \quad (2.17)$$

where R_{eqv} is $1/g_{m2}$ and C_{total} is the sum of C_{GD1} , C_{GS2} and C_{GD3} for the enhancement-mode load device and R_{eqv} is R_{load} and C_{total} is the sum of C_{GD1} , C_{GD2} , and the capacitance

of the resistor for the resistively loaded device. Hand calculations of the gain and bandwidth are presented in Tables 2.2. and 2.3

2.2.2 Simulation Results

Significant design specifications from HSpice simulations using circuit files extracted from MAGIC layouts (see Appendix 2) and BSIM3 models from the AMI 0.8um N88Z and AMI 1.2um N87R MOSIS process runs (see Appendix 3) are summarized and compared to hand approximations in Tables 2.2 and 2.3. An example circuit file for simulating an amplifier's frequency response is included in Appendix 4. For both amplifiers, the amount by which the input transistors were in saturation, $V_{DS-SAT_{in}}$, was important because of the difficulty involved in obtaining the desired gain and output voltage while keeping the input transistors in saturation for modest size input signals. Hand calculations were made using (2.15) through (2.17) and the transistor parameters obtained from the HSpice operating point simulation. Comparing the hand calculated gain values to the simulated gain values, it is apparent that the initial assumptions of no body effect and output stage unity gain were not entirely valid.

Table 2.2 - Two stage amplifier simulation results using the MOSIS AMI 0.8u N87R run parameters and models

	Two Stage Amplifier with Enhancement-Mode Load		Two Stage Amplifier with Resistive Load		Units
	Hand	HSpice	Hand	HSpice	
$V_{OUT\ DC}$	1.5	1.50	1.5	2.1	V
$V_{DS-SAT_{in}}$	N/A	195	N/A	186	mV
DC differential gain	7.7	4.5	14.9	10.6	V/V
f_{3db} for 10 pF load	129	122	87	101	MHz
f_{3db} for 10 pF load	129	180	87	128	MHz
Power dissipation	18.3	18.3	20.4	20.4	mW

Table 2.3 - Two stage amplifier simulation results using the MOSIS AMI 1.2u N88Z run parameters and models

	Two Stage Amplifier with Enhancement-Mode Load		Two Stage Amplifier with Resistive Load		Units
	Hand	HSpice	Hand	HSpice	
$V_{OUT\ DC}$	1.5	1.6	1.5	2.1	V
$V_{DS-SAT\ in}$	N/A	187	N/A	189	mV
DC differential gain	8.82	5.7	15.2	10	V/V
f_{3db} for 10 pF load	116	98	76	80	MHz
f_{3db} for 1 pF load	116	145	76	102	MHz
Power dissipation	17.9	17.9	18.4	18.4	mW

Recomputing the gain values for the AMI 0.8 μm process assuming a source follower gain of 0.85 gives 6.5 V/V for the enhancement mode load amplifier and 12.7 V/V for the resistively loaded amplifier. Recomputing the gain values for the AMI 1.2 μm process assuming a source follower gain of 0.85 gives 7.5 V/V for the enhancement mode load amplifier and 12.9 V/V for the resistively loaded amplifier. The remaining difference between the hand calculated and simulated values is due to the omission of finite output impedance and the body effect for the transistors in the hand calculations. The hand calculated and simulated bandwidths compare favorably. Each of the four amplifiers' frequency responses with a 10 pF load are shown in Figs 12 through 15. The frequency responses are very flat and have a smooth roll-off. Each response roll-off approximates a two-pole roll off due to the second pole at the output of the transistor.

2.3 Four Stage Wideband Amplifiers with Transimpedance Stage

2.3.1 Circuit Design

Practical device geometries make the two-stage amplifier design previously presented difficult to bias. Specifically, in order to keep all of the devices in saturation and to have enough output current to drive a modest size capacitive load, the output voltage is limited to less than the 2.5 V common mode input voltage. Not only can this

limit the dynamic range of the amplifier but it also prevents multiple amplifiers from being cascaded together for more amplification without a level shifter between each block. A slightly more complex design is required to provide an amplifier with a 2.5 V common mode output voltage that can be used as the input common mode voltage. Following the block diagram of Fig 9, two four-stage wideband amplifier designs, each with separate transconductance and transimpedance stages were considered. Figs. 16 and 17 show one side of the fully differential implementation of such a two stage design with a folded cascode stage and a current mirror stage, respectively. The folded cascode design uses the differential pair to perform the voltage to current conversion and the folded cascode stage to convey the current signal into the transimpedance loop for amplification and conversion back to a voltage signal at the output. The current mirror design uses a current mirror to convey the current signal into the transimpedance loop for amplification and conversion back to a voltage signal at the output. The current mirror can also be used for current amplification. In fact, the current mirror amplifier implemented in the AMI 1.2u process uses the current mirror to provide current signal amplification of approximately 1.5 A/A. The transimpedance stages of both amplifiers are essentially identical, with only slightly different resistor sizes for the purpose of providing different bias points and gain values

Fig. 18 illustrates the small signal model for the transimpedance stage. The complex interactions with the other stages of the amplifier are ignored with the input to the loop being represented simply by a current source in parallel with a finite resistance and capacitance. Neglecting body effect and channel length modulation, the dc loop transmission for the transimpedance feedback loop is

$$T_{DC} = \frac{R_1 \parallel (R_f + r_{o_m})}{R_1 \parallel (R_f + r_{o_m}) + \frac{1}{g_{m2}}} \frac{r_{o_m}}{r_{o_m} + R_f} - g_{m1} r_{o1} \cong -g_{m1} r_{o1} \quad (2.20)$$

where r_{o1} is the small signal output resistance of transistor M1 and

$$A_{closed}^{ideal} = \frac{R_f}{R_1} + 1 \quad (2.21)$$

is the ideal current gain of the loop. One of the model's two significant poles for the loop transmission is at the drain of M1 as computed by

$$f_{Loop1} = \frac{1}{2\pi r_{o1} [C_{GD1} + C_{GD2}(1 - A_{VGD2}) + C_{bias}]} \quad (2.22)$$

where the gate to source capacitance of M2 is effectively removed by Miller effect, C_{bias} is the gate to drain capacitance of the bias transistor, and the gain from gate to drain of M1 is given as

$$A_{VGD2} = \frac{-R_{LOAD}}{\frac{1}{g_{m2}} + R_1 \parallel (R_f + r_m)} \quad (2.23)$$

The other pole will be at the gate of M1 and is given as

$$f_{Loop2} = \frac{1}{2\pi [r_m \parallel (R_f + R_1 \parallel \frac{1}{g_{m2}})] (C_m + C_{GS1} + C_{GD1}(1 - A_{VGD1}))} \quad (2.24)$$

where r_m and C_m are the parallel combinations of the output resistances and gate to drain capacitances of the transistors at the input to the loop. Pole f_{Loop1} is most likely the dominant pole due to the large small signal resistance r_{o1} at the drain of M1 and the sum

of the three large capacitances. Therefore, the closed loop bandwidth of the transimpedance loop, and subsequently an additional pole for the entire amplifier, is approximated by

$$f_2 = \frac{T_{DC}}{f_{Loop1}} = \frac{g_{m1}}{2\pi[C_{GD1} + C_{GD2}(1 - A_{VGD2}) + C_{bias}]} \quad (2.25)$$

Resistor R_{LOAD} is a bias resistor that also converts the small signal current back into a voltage. Ignoring body effect, assuming infinite output impedance, and assuming the source follower output stage has an ideal gain of unity, the gain relationship for the folded cascode amplifier is given by (2.26) and for the current mirror amplifier is given by.

$$A_V = g_{m1} \left(\frac{R_f}{R_1} + 1 \right) R_{LOAD}, \quad (2.26)$$

$$A_V = g_{m1} \frac{W_3}{W_2} \left(\frac{R_f}{R_1} + 1 \right) R_{LOAD}. \quad (2.27)$$

Table 2.4 summarizes the device sizes and original design currents. As with the two stage amplifiers, device sizes and bias currents were chosen to provide at least 10 V/V gain as predicted by (2.26) and (2.27) while keeping the input transistors near 200 mV into the saturation region, an output common mode voltage equal to the common mode input voltage, and the transimpedance loop stable. Also, the output stage device sizes and currents were chosen to ensure that the output stage would not significantly affect the frequency response of the circuit with a 10 pF load. The dominant pole will be at the gate of the source follower output transistor, M5 for the folded cascode amplifier

Table 2.4 - Four Stage Amplifier Device Sizes and Design Currents

		AMI 0.8um Process		AMI 1.2um Process	
		Size (um)	Designed Bias Current (mA)	Size (um)	Designed Bias Current (mA)
Four Stage Trans-Impedance Amp With Folded Cascode Stage	M1	60/1	0.305	240/1.2	0.300
	M2	60/2	0.447	30/2.4	0.364
	M3	60/1	0.249	300/1.2	0.261
	M4	120/1	0.646	300/1.2	0.958
	M5	350/1	1.234	600/1.2	1.015
	Mb7	300/5	0.610	360/6	0.600
	Mb8	371/5	0.753	420/6	0.664
	Mb9	125/5	0.249	150/6	0.261
	Mb10	125/5	0.249	150/6	0.261
	Mb11	200/5	0.404	240/6	0.393
	Mb12	600/5	1.234	600/6	1.015
	R_load	1901 ohm	0.646	1506 ohm	0.958
	Rf	1993 ohm	0.044	2001 ohm	0.029
	R1	1001 ohm	0.690	810 ohm	0.929
Four Stage Trans-Impedance Amp With Current Mirror Stage	M1	60/1	0.305	180/1.2	0.250
	M2	30/1	0.305	30/1.2	0.250
	M3	30/1	0.335	45/1.2	0.402
	M4	60/1	0.335	60/1.2	0.402
	M5	60/1	0.249	300/1.2	0.237
	M6	120/1	0.681	300/1.2	0.669
	M7	350/1	1.230	600/1.2	1.021
	Mb7	300/5	0.610	300/6	0.500
	Mb8	150/5	0.303	240/6	0.392
	Mb9	125/5	0.249	150/6	0.237
	Mb10	125/5	0.249	150/6	0.237
	Mb11	600/5	1.230	600/6	1.021
	R_load	1901 ohm	0.681	1506 ohm	0.669
	Rf	1993 ohm	0.032	2001 ohm	0.009
	R1	1001 ohm	0.713	989 ohm	0.677

and M7 for the current mirror amplifier, as approximated by

$$f_{DOM} = \frac{1}{2\pi R_{LOAD} (C_{GDx} + C_{GDy})} \quad (2.28)$$

where x and y are 4 and 5 for the folded cascode design and 6 and 7 for the current mirror design. The gate to source capacitances of transistors M5, for the folded cascode design, and M7, for the current mirror design, will be effectively eliminated by Miller effect.

Both amplifiers will have at least one more important pole from either the transimpedance loop, as approximated in (2.25), the drains of the differential pair or the inputs to the loop at the drain of Mb11. The additional pole(s) lower the -3dB point and cause faster frequency response roll-off and reduced phase margin for both amplifier designs.

2.3.2 Simulation Results

Significant design specifications from HSpice simulations using circuit files extracted from MAGIC layouts (see Appendix 2) and BSIM3 models from the AMI 0.8 μm N88Z and AMI 1.2 μm N87R MOSIS process runs (see Appendix 3) are summarized and compared to hand approximations in Tables 2.5 and 2.6. An example circuit file for simulating an amplifier's frequency response is included in Appendix 4. Hand calculations were made using (2.20) through (2.28) and the transistor parameters obtained from the HSpice operating point simulation. The simulated loop transmission magnitude and phase for both the folded cascode and current mirror amplifiers in both processes are shown in Figs. 19 through 22, respectively. Each amplifier's overall frequency response in both processes is shown in Figs. 23 through 26.

Table 2.5 - Four stage amplifier simulation results using the MOSIS AMI 0.8um N87R run parameters and models

	Transimpedance Amplifier with Folded Cascode		Transimpedance Amplifier with Current Mirror		Units
	Hand	Hspice	Hand	HSpice	
$V_{OUT\ DC}$	2.5	2.6	2.5	2.5	V
$V_{DS-SAT\ in}$	N/A	223	N/A	222	mV
T_{DC}	74	49	74	49.5	V/V
$f_{3dB\ loop}$	8.1	15.4	8.1	8.8	MHz
DC gain	12.7	10.4	12.7	10.4	V/V
$f_{3dB\ amp}$ for 10 pF load	135	115	135	140	MHz
$f_{3dB\ amp}$ for 1 pF load	135	167	135	240	MHz
Power dissipation	30	30	30	29	mW

Table 2.6 - Four stage amplifier simulation results using the MOSIS AMI 1.2um N88Z run parameters and models

	Transimpedance Amplifier with Folded Cascode		Transimpedance Amplifier with Current Mirror		Units
	Hand	HSpice	Hand	HSpice	
$V_{OUT\ DC}$	2.5	2.3	2.5	2.7	V
$V_{DS-SAT\ in}$	N/A	181	N/A	194	mV
T_{DC}	55.5	34.6	55.1	34.5	V/V
$f_{3dB\ loop}$	9.8	11.6	9.7	7.6	MHz
DC gain	11.7	9.8	15.1	10.5	V/V
$f_{3dB\ amp}$ for 10 pF load	146	82	147	106	MHz
$f_{3dB\ amp}$ for 1 pF load	146	100	147	154	MHz
Power dissipation	30	30	27	27	MW

In both processes and for both amplifiers, the loop transmission was simulated by inserting an AC voltage source between the drain of M1 and gate M2 of Fig. 18. Unexpectedly, the loop transmission for both folded cascode amplifiers has significant peaking as seen in Figs. 19 and 21. To confirm the validity of the simulation of loop transmission, a second simulation in which the loop was broken at the same node was performed and resulted the same peaking. The only difference between the transimpedance loops for the folded cascode and current mirror designs is the input load to the transimpedance loop at the drain of Mb11. Further simulation and testing is necessary to understand the cause of the peaking. For all four amplifiers, the simulated

DC loop transmission, T_{DC} , is 50 or less and the simulated phase margin is above 50 degrees.

The hand calculations for T_{DC} and the DC gain of the amplifiers are slightly larger than the simulated values. As with the two stage amplifiers, the difference is due to the omission of finite output impedance of and the body effect on the transistors in the hand calculations and the erroneous assumption that the source follower output stage has unity gain. As a result of the unexplained peaking, the hand calculated and simulated loop bandwidth values for the folded cascode designs do not compare favorably. The hand calculated and simulated loop bandwidth values for the current mirror designs are within a reasonable tolerance. For the AMI 0.8 μm process amplifiers, the hand calculated and simulated amplifier bandwidth values compare favorably. However, the same values for the AMI 1.2 μm process amplifiers are not within a reasonable tolerance and suggest that either the dominant pole is not at the gate of the output source follower as expected or that the models for the process are inaccurate. Modeling is reviewed in Chapter 4.

2.4 Biasing Circuit

2.4.1 Circuit Design

The gain values computed in (2.15), (2.16), (2.26), and (2.27) all depend on the product of the input differential pair transconductance, g_m , and the R_{LOAD} resistor value. Without overall feedback to provide circuit stability against power supply swings and process or temperature variations, the gain values would normally fluctuate dramatically. However, using the bias circuit shown in Fig. 27, the transistor transconductances become inversely proportional to the value of a bias resistor. As documented in Table 2.7, all of the transistors in the bias circuit are the same size except for M2; therefore,

Table 2.7 – Bias circuit transistor sizes and designed currents

Device	AMI 0.8um Process		AMI 1.2um Process	
	Size (um)	Designed Bias Current (mA)	Size (um)	Designed Bias Current (mA)
Mb1	50/5	101	60/6	100
Mb2	200/5	101	240/6	100
Mb3	50/5	101	60/6	100
Mb4	50/5	101	60/6	100
Mb5	50/5	101	60/6	100
Mb6	50/5	101	60/6	100
R_bias	1700 ohm	101	2200 ohm	100
Msu1	2/25	011	2 4/30	003
Msu2	10/2	011	12/2.4	003
Msu3	5/2	462e-12	6/2 4	36e-12

nominally the same current, I_D , set by M2 and R_{BIAS} will run through each side of the circuit. The last three transistors in the table are for a start-up circuit which ensures that the positive feedback loop created by transistors Mb1, Mb2, Mb3 and Mb4 starts up at power on.

Summing voltages around the loop containing R_{BIAS} , M1 and M2 gives

$$V_{GS1} - V_{T1} = V_{GS2} - V_{T2} + I_D R_{BIAS} \quad (2.29)$$

Subtracting V_T from both sides of the equation gives

$$V_{GS1} = V_{GS2} + I_D R_{BIAS} \quad (2.30)$$

Assuming the transistors are in strong inversion and the square law relation holds, (2 30)

can be rewritten as

$$\sqrt{\frac{2I_D}{K \frac{W_1}{L_1}}} = \sqrt{\frac{2I_D}{K \frac{W_2}{L_2}}} + I_D R_{BIAS} \quad (2 31)$$

Recalling that

$$g_m = \sqrt{2K \frac{W}{L} I_D} \quad (2.32)$$

and substituting gives

$$g_{mB1} = \frac{2(1 - \sqrt{\frac{(W/L)_{B1}}{(W/L)_{B2}}})}{R_{BIAS}} \quad (2.33)$$

Therefore, the transconductance of M2 is determined by geometric ratios and the bias resistor only and is independent of bias voltages, process parameters, temperature, etc.

When $(W/L)_{B2} = 4(W/L)_{B1}$, the relationship simplifies to

$$g_{mB1} = \frac{1}{R_{BIAS}}. \quad (2.34)$$

Since the amplifier circuit transistor currents are derived from device geometry ratios of the bias network transistors to the circuit transistors (ignoring second order effects like body effect and finite output impedance), the transconductances are also based on device geometries. Specifically, for the i^{th} n-channel transistor biased from transistor Mb1

$$g_{mi} = \frac{(W/L)_i}{(W/L)_{B1}} \frac{1}{R_{BIAS}}. \quad (2.35)$$

For the p-channel transistors, the equation is the same as that above except for the ratio of the p-channel to n-channel mobilities. Body effect modifies (2.28) and (2.29) slightly but the relationships still depend primarily on device geometries. Finite output impedance causes the relationship to break down, however, by using cascode current mirrors, or

more simply, larger length devices, the detrimental effect due to finite output impedance can be significantly reduced [6].

Using (2.35), the gain relationships for each of the four amplifiers as seen in (2.16), (2.26), and (2.27) can be rewritten as follows

$$A_v = \sqrt{\frac{(W/L)_1(W/L)_{B7}}{2}} \frac{1}{(W/L)_{B1}} \frac{R_{LOAD}}{R_{BIAS}}, \quad (2.36)$$

$$A_v = \sqrt{\frac{(W/L)_1(W/L)_{B7}}{2}} \frac{1}{(W/L)_{B1}} \frac{R_{LOAD}}{R_{BIAS}} \left(\frac{R_f}{R_1} + 1 \right), \quad (2.37)$$

$$A_v = \sqrt{\frac{(W/L)_1(W/L)_{B7}}{2}} \frac{1}{(W/L)_{B1}} \frac{R_{LOAD}}{R_{BIAS}} \frac{W_3}{W_2} \left(\frac{R_f}{R_1} + 1 \right). \quad (2.38)$$

Using the bias circuit of Fig. 27, the gain relations for all four amplifier designs are dependent only on device geometries and resistor ratios to a first order, thereby making the gain independent of power supply swings, process and temperature variations

2.4.2 Simulation Results

Process variations can cause on-chip resistors values to vary $\pm 20\%$. Therefore the absolute resistance values vary greatly between runs. In order to investigate the stability and performance of the amplifiers with the biasing circuit across such process variations, a simulation of the frequency response for the designed resistor value $\pm 20\%$ was performed on each design using the AMI 1.2um N88Z process BSIM3 models. The results of these simulations are summarized in Table 2.8. The simulations confirm that the bias circuit aids in stabilizing the gain against $\pm 20\%$ changes in resistor values. In the

Table 2.8 - Results of frequency response simulation for varying resistor values

Amplifier Design			Resistors as designed	Resistors -20%	Variance from Design	Resistors +20%	Variance from Design
Two Stage Amplifier with Enhancement Mode Load	1	gm of input transistor	-5.2E-03	-6.2E-03	17.97%	-4.4E-03	-16.44%
	2	1/(gm of enhancement mode transistor)	1300	1130	-13.08%	1480	13.85%
	3	Buffer loss	8.4E-01	8.2E-01	-2.02%	8.5E-01	1.19%
		Total gain (1x2x3)	-5.70	-5.77	1.25%	-5.51	-3.32%
Two Stage Amplifier with Resistive Load	1	gm of input transistor	4.9E-03	5.9E-03	19.88%	4.1E-03	-16.39%
	2	Load resistor	2393	1915	-19.97%	2872	20.02%
	3	Buffer loss	8.6E-01	8.5E-01	-1.17%	8.6E-01	0.93%
		Total gain (1x2x3)	-10.00	-9.48	-5.20%	-10.11	1.10%
Trans- impedance Amplifier with Folded Cascode Stage	1	Transconductance from input to output of folded cascode	-2.2E-03	-2.4E-03	6.33%	-1.9E-03	-15.84%
	2	Transimpedance stage current gain	3.37	3.36	-0.30%	3.38	0.30%
	3	Output resistor	1506	1205	-19.99%	1808	20.05%
	4	Buffer loss	8.6E-01	8.6E-01	-0.58%	8.7E-01	0.35%
		Total gain (1x2x3x4)	-9.75	-8.20	-15.90%	-9.88	1.33%
Trans- impedance Amplifier with Current Mirror Stage	1	Transconductance of input transistor	-2.0E-03	-2.4E-03	20.90%	-1.7E-03	-16.92%
	2	Current mirror gain	1.35	1.32	-2.22%	1.37	1.48%
	3	Transimpedance stage current gain	2.96	2.96	0.00%	1.88	-36.49%
	4	Output resistor	1506	1205	-19.99%	1808	20.05%
	5	Buffer loss	8.7E-01	8.7E-01		8.8E-01	
		Total gain(1x2x3x4x5)	-10.54	-9.89	-6.17%	-6.85	-35.01%

case of the -16% gain decrease for the transimpedance amplifier with the folded cascode stage, the current sources feeding the differential pair and the folded cascode stage fell into the triode region and reduced the input transconductance. This problem can easily be remedied by resizing the current source transistors. In the case of the -35% gain decrease for the transimpedance amplifier with the current mirror stage, the transimpedance loop gain falls dramatically from the decrease in bias current due to the increase in the bias resistor. Resizing and adjusting bias currents for the transistors in the loop will be necessary to improve the loop's gain magnitude stability over bias current changes.

Chapter 3

Fabrication and Testing

3.1 Amplifier Circuit Layout and Testing Configuration

Fig. 28 is a screen capture of the MAGIC layout for each of the four amplifier designs and the bias circuit test structure in the AMI 0.8 μm process. The AMI 0.8 μm designs were fabricated from this layout in the N97L run by MOSIS. Each AMI 0.8 μm die was 2.0 mm by 2.1 mm. The AMI 1.2 μm designs were fabricated from an almost identical layout in the N95Y run by MOSIS. Each die was 2.6 mm by 2.5 mm. A 40-pin pad frame was used. To provide space for other devices to be placed on the chip, the amplifiers were laid out around the west, north and half of the east sides of the chip. The amplifiers and test structure share power and ground buses that are tied to external pins. Each amplifier input and output, as well as the test structure's two inputs, four outputs and two bias points are taken to external pins. No test points were taken to external pins for two reasons. First, taking any point in the signal path to an external pin would increase the capacitance at that node and therefore lower the frequency response of the circuit. Second, additional pins were necessary for other devices not related to this project to be placed on the chip.

Figs. 29 through 32 are screen captures of the MAGIC layout for the two stage amplifier with enhancement mode load, the two stage amplifier with resistive load, the transimpedance amplifier with folded cascode stage and the transimpedance amplifier with current mirror stage, respectively. In each layout, the bias circuit is on the far left and the differential pair is approximately in the middle of the layout. The other stages of each amplifier are laid out consecutively from each side of the differential pair, with the source-follower output stage being laid out immediately following the bias circuit on the left and as the last stage on the right. The amplifiers were laid out as independent, separately connected stages in order to reduce the amount of time necessary to lay out a large number of devices with similar components in multiple processes. Using this method for layout caused each amplifier to consume a large amount of space on the chip. However, much of that space was unused and was "plugged" in order to reduce the risk of latch-up from stray currents. If the amplifiers were going to be used in a system, the layout of each amplifier would have to be much tighter. Moreover, each side of the fully differential design would be laid out beside the other in order to reduce the effects of crosstalk with other devices and chip gradients. The AMI 0.8 μm designs were fabricated in the N97L run by MOSIS. The AMI 1.2 μm designs were fabricated in the N95Y run by MOSIS.

As shown in Fig. 33, the initial test board design was simple. The chips were placed on a smaller "daughter" board that was plugged into the main board. Each amplifier input and output was tied directly to a separate LEMO connector and input biasing was to be provided off-board through unterminated 50-ohm lines. Since no differential output sine-wave generator was available, the amplifiers were to be driven

single-ended. In addition, the amplifier outputs were expected to drive the off-board capacitive loads through unterminated 50 ohm lines. Shortly into testing, however, it was discovered that input and output signals above 50 MHz were being distorted when sent through the off-board bias network due to transmission line effects. Also, the single-ended drive resulted in noticeable differences in the gain measurements of each side of each amplifier. Furthermore, the output stages were having difficulty driving the off-board capacitive loads at higher frequencies. Therefore, the test setup was significantly changed. Two different test boards were made through modifications of the original test board. On both boards, the LEMO inputs were terminated in 50-ohms then capacitively coupled to an on-board bias circuit before being connected to each amplifier's inputs. The capacitive coupling resulted in a high-pass filter with a 3dB point slightly below 100 kHz. For DC testing, a DC board was made with the amplifier outputs taken directly to the LEMO outputs as illustrated by the schematic in Fig. 34. For all other tests, an AC board was made with the amplifier outputs taken first to a 300 MHz buffer, Burr-Brown's BUF601, as illustrated by the schematic in Fig. 35. The buffer output was then capacitively coupled (also with a 3 dB point near 100 kHz) to a 50-ohm terminated LEMO output. A picture of the bottom side of the test board after these changes were made is shown in Fig. 36. Two buffers were mounted on a copper strip, functioning as a ground plane, in the "dead bug" upside-down fashion. The strip was attached to the bottom of the main board and the inputs and outputs of the buffers were moved to take measurements of each amplifier. A 400 MHz differential line driver, MAXIM's MAX4447, was also constructed on a separate ground plane using the "dead bug" technique, as shown in Fig. 37, and was used to drive the amplifiers during testing. Fig.

38 shows two of the BUF601 buffers assembled on a ground plane for use in characterization of the buffers frequency response. Both the line driver and buffer outputs were back-terminated into 50 ohms which introduced a loss of approximately 0.5 V/V or 6 dB in power.

3.2 Measurement and Testing of Amplifiers

3.2.1 Measurement of DC bias voltages, currents, and capacitive loading

DC bias voltages and currents were measured using the DC test board illustrated in Fig. 34. A HP 34401A multimeter was used to take voltage and current measurements of each output of each amplifier. Since no test points were available, the current of each output stage of each amplifier was measured by connecting one end of the multimeter ammeter to the output LEMO and the other to the 5 V rail. This configuration turns off the source-follower output transistor and allows the ammeter to measure the current of the output stage current mirror. Tables 3.1 and 3.2 compare measured and designed DC values. For the AMI 0.8 μm amplifiers, the currents are about one-half the original design values and for the AMI 1.2 μm amplifier, the currents are almost one-third the design values. The biasing problems are discussed further in section 3.2.6 and Chapter 4. For the simulated bias currents to match the measured bias currents, the resistors in the simulation files were increased by 40% for the AMI 0.8 μm process and by 60% for the AMI 1.2 μm process. The DC values from the adjusted simulation files match quite well with the measured values.

Capacitive loading of each board's amplifier outputs was tested using a Tektronix active probe and 400 MHz oscilloscope as illustrated by Fig. 39. The amplifier inputs

Table 3.1 - Comparison of measured and simulated DC values for AMI 0.8 um amplifiers

		Simulated as designed	Measured	Simulated at new bias currents	Units
Two stage	Power	18.3	7.7	7.7	mW
Amplifier with	Vdsat_in	0.195	N/A	0.124	V
Enhancement	Vout Side A	1.5	2.2	2.2	V
Mode Load	Vout Side B	1.5	2.1	2.2	V
	Iout Side A	1.222	0.514	0.515	mA
	Iout Side B	1.222	0.515	0.515	mA
Two stage	Power	20.4	8.6	8.6	mW
Amplifier with	Vdsat_in	186	N/A	0.117	V
Resistive Load	Vout Side A	2.1	2.4	2.8	V
	Vout Side B	2.1	2.5	2.8	V
	Iout Side A	1.23	0.537	0.521	mA
	Iout Side B	1.23	0.537	0.521	mA
Transimpedance	Power	29.9	14.5	14.5	mW
Amplifier with	Vdsat_in	0.223	N/A	0.142	V
Folded Cascode	Vout Side A	2.6	2.7	2.6	V
Stage	Vout Side B	2.6	2.6	2.6	V
	Iout Side A	1.066	0.529	0.520	mA
	Iout Side B	1.066	0.529	0.520	mA
Transimpedance	Power	29.1	14.1	14.1	mW
Amplifier with	Vdsat_in	222	N/A	0.141	V
Current Mirror	Vout Side A	2.5	2.6	2.6	V
Stage	Vout Side B	2.5	2.8	2.6	V
	Iout Side A	1.23	0.545	0.519	mA
	Iout Side B	1.23	0.553	0.519	mA

Table 3.2 - Comparison of measured and simulated DC values for AMI 1.2 um amplifiers

		Simulated as designed	Measured	Simulated at new bias currents	Units
Two stage	Power	17.9	6.0	6.0	mW
Amplifier with	V _{dsat_in}	0.187	N/A	0.095	V
Enhancement	V _{out} Side A	1.6	2.5	2.4	V
Mode Load	V _{out} Side B	1.6	2.5	2.4	V
	I _{out} Side A	1.003	0.335	0.342	mA
	I _{out} Side B	1.003	0.336	0.342	mA
Two stage	Power	18.4	6.3	6.3	mW
Amplifier with	V _{dsat_in}	0.189	N/A	0.095	V
Resistive Load	V _{out} Side A	2.1	3.0	2.9	V
	V _{out} Side B	2.1	3.0	2.9	V
	I _{out} Side A	1.011	0.332	0.347	mA
	I _{out} Side B	1.011	0.332	0.347	mA
Transimpedance	Power	29.8	12.1	12.1	mW
Amplifier with	V _{dsat_in}	0.181	N/A	0.095	V
Folded Cascode	V _{out} Side A	2.3	3.0	2.9	V
Stage	V _{out} Side B	2.3	3.0	2.9	V
	I _{out} Side A	1.015	0.400	0.391	mA
	I _{out} Side B	1.015	0.397	0.391	mA
Transimpedance	Power	26.8	10.7	10.7	mW
Amplifier with	V _{dsat_in}	0.194	N/A	0.108	V
Current Mirror	V _{out} Side A	2.7	3.4	3.1	V
Stage	V _{out} Side B	2.7	3.4	3.1	V
	I _{out} Side A	1.021	0.389	0.395	mA
	I _{out} Side B	1.021	0.389	0.395	mA

were driven by an attenuated pulse provided by a HP8013B Pulse Generator. Using the previously measured output current, the measured falling edge slope of the output pulse from the active probe and oscilloscope and the relation

$$I = C * \frac{dV}{dt}, \quad (3.1)$$

where the value of the capacitive load for each board was determined. For the DC board, the capacitive load ranged from approximately 8 pF to 10 pF depending on which amplifier was being measured. Such a wide range of large capacitive loads was due to traces of varying lengths both from the chip to the daughter board headers and from the main-board sockets to the LEMO outputs. For the AC board, the capacitive load varied only between 5 pF and 6 pF. Since the input to the buffers was tied directly to the main board socket, the only variation in trace length was from the chip to the header on the daughter board. Based on the DC and capacitive load testing, all measured values from this point forward are compared to simulated values from simulations adjusted to match the measured current values and with 5 pF loads.

3.2.2 Frequency Response Measurement

Fig. 40 illustrates the test setup for measuring the frequency response of each amplifier. The HP 8753C Network Analyzer and S-parameter test set was used to measure S21 data. The network analyzer was properly calibrated, set to provide a -40 dBm input signal from 300kHz to 500 MHz and set to take 401 points averaged 16 times. S21 magnitude and phase data for the line driver and buffer alone were measured, as shown in Figs. 41 and 42. The phase plots require some clarification. The network analyzer restricts the phase angle measurements between -180 and 180 degrees

Therefore, there are occasional abrupt transitions from -180 to 180 degrees or vice versa. Also, the phase measurement in Fig 42 includes phase distortion from some cables and connectors that interface with the line driver and buffer and for which calibration standards were unavailable. However, since the measured S21 data used in Figs 41 and 42 for the line driver and buffer alone was subtracted from measured S21 data for the line driver, amplifier and buffer, erroneous data caused from the uncalibrated test devices will be removed. Therefore, the S21 gain and phase data for each amplifier, relative to the line driver, buffer and uncalibrated test structures, is shown in Figs. 43 through 66, followed immediately by the HSpice simulation of the gain magnitude and phase. The AMI 0.8 μm amplifiers are shown first followed by the AMI 1.2 μm amplifiers. All of the amplifiers have a flat response. The two-stage amplifiers have approximately a two-pole roll off and the transimpedance amplifiers roll-off faster, indicating more poles. The gain magnitude data is summarized and compared to HSpice simulation results in Tables 3.3 and 3.4 of section 3.2.5

3.2.3 Gain Compression Measurement

Fig. 67 illustrates the test setup for measuring the gain compression point of each amplifier with a 5 pF load at 100 MHz. The HP8656A Signal Generator and RF section was used to provide 100 MHz input signals through the differential line driver at various power levels. The HP89441A Vector Signal Analyzer was used to measure the output spectrum of each amplifier output. The Vector Signal Analyzer was set for a 10kHz resolution bandwidth over a 0-500 MHz display bandwidth and was configured to take 401 points averaged 25 times. After removing the gain contribution of the line driver and buffer, the output power was plotted against the input power for each output of each

amplifier as illustrated in Figs 68 through 83. It was also determined that the line driver and buffer combination does not contribute to the amplifiers' gain compression until the input power is above 10 dBm. Gain compression points at 100 MHz for each output of each amplifier are summarized in Tables 3.3 and 3.4 of section 3.2.5.

3.2.4 Noise Measurement

Fig. 84 illustrates the test setup for measuring the output noise spectrum of each amplifier. The inputs to each amplifier were terminated in 25 ohms and the outputs were connected to the buffer. The amplifier and buffer configuration was then fed to the Rush-Kennedy wideband amplifier. The Rush-Kennedy amplifier has a voltage gain of approximately 60 dB and -3 dB point of approximately 120 MHz. The HP3589A Spectrum/Network Analyzer was used to make the noise measurements. It has a noise floor of about -140 dBm/Hz and was configured to plot the power spectral density using a resolution bandwidth of 9,100 Hz and 50 averages. As illustrated in Fig. 85, the output noise of the Rush-Kennedy amplifier is -112 dBm/Hz at 50 MHz. Dividing by the amplifier gain gives an input referred noise voltage of about 0.8 nV/rt(Hz). This measurement is in reasonable agreement with the 0.5 nV/rt(Hz) noise voltage per the amplifier's datasheet. Fig. 86 shows the output noise of the buffer and the Rush-Kennedy amplifier to be about -104 dBm/Hz at 50 MHz. Comparing Fig 85 to Fig. 86, it is apparent that the slight overshoot in the buffer gain at high frequencies compensates for the roll-off in the Rush-Kennedy amplifier response. Therefore, the shape of the amplifier noise spectrums in Fig 87 through Fig. 94 are close to the actual noise spectrums of the amplifiers, adjusted for the gain of the buffer and Rush-Kennedy amplifier. The input referred noise values of each amplifier, after removing the gain

effects of the buffer and Rush-Kennedy amplifiers, are summarized and compared to HSpice simulation results in Tables 3.3 and 3.4 of section 3.2.5. In the calculation of the input referred noise, the effects of the input 50-ohm terminators, the buffer and Rush-Kennedy amplifier were essentially ignored due to their small noise contribution compared to the noise of the amplifiers.

In many of the noise spectra of Figs. 87 through 94, there is an upturn in the spectrum at lower frequencies beginning at 15 MHz. Further investigation of the HSpice noise simulation results of one of the amplifiers resulted in discovering that the bias circuit was the cause of the upturn. The bias circuit transistors operate at lower currents than the transistors in the signal path; therefore, their transconductances are smaller. Since the noise power varies inversely with transconductance as illustrated by (3.2), the noise contribution by the bias circuit transistors is greater.

$$\overline{e_n^2} = 4kT \frac{2}{3} \frac{1}{g_m} \Delta f_n \quad (3.2)$$

Furthermore, the lower currents of the bias circuit transistors cause the noise bandwidth of those transistors to be lower than the bandwidth of the signal path transistors.

Simulation confirmed that the majority of the bias circuit's noise contribution is through the differential pair current mirror. A plot of the HSpice simulation of the output noise power for the two stage amplifier with enhancement mode load is shown in Fig. 95. The top plot is the output noise over the entire simulated frequency range and the bottom plot is the output noise power over the 10 to 100 MHz range. Two distinct roll-offs are apparent in the bottom plot with the first roll-off being that of the bias circuit and the second being that of the amplifier. Had the measurement and simulation been performed

differentially, the noise contribution of the bias circuit would have been a common mode signal and would have been negligible

3.2.5 Summarization of Test Results

Tables 3.3 and 3.4 summarize the results of the amplifier testing as compared with simulated values. An example circuit file for simulating an amplifier's frequency response is included in Appendix 4 and one for simulating an amplifier's output noise is included in Appendix 5. The frequency response gain magnitude measured and simulated values are within a reasonable tolerance for the AMI 0.8 μm process but are not within a reasonable tolerance for the AMI 1.2 μm process. Slight differences between the measured and simulated -3 dB points can be partially explained by differences in capacitive loads on the amplifier outputs due to varying trace lengths on from the chip to the socket header on the daughter board.

The gain compression points for a 100 MHz input signal and 5 pF load are quite small and therefore limit the effectiveness of all of the designs. Initial frequency response measurements using the DC test board without an output buffer showed that adding a resistive load to the amplifier output, which effectively increases the output stage bias current, reduced the output distortion at higher frequencies. While lowering the frequency response of the amplifier, the resistive load provided an additional path for the output signal to discharge during the low signal swing. Further simulation and analysis would most likely confirm that the majority of the gain compression problem is due to the source-follower output stage's inability to sink current.

Table 3.3 - Comparison of measured and simulated AC values for AMI 0.8 μ m amplifiers

		Measured	Simulated	Units
Two stage	Gain - Side A	2.4	2.8	V/V
Amplifier with	Gain - Side B	2.4	2.8	V/V
Enhancement	-3dB frequency-Side A	142.0	127.0	MHz
Mode Load	-3dB frequency - Side B	137.0	127.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	96.6	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	96.6	N/A	mVpp
	Noise @ 50Mhz	5.6	2.1	nV/rt(Hz)
Two stage	Gain – Side A	6.4	5.8	V/V
Amplifier with	Gain – Side B	6.4	5.8	V/V
Resistive Load	-3dB frequency -Side A	95.0	78.0	MHz
	-3dB frequency - Side B	95.0	78.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	55.0	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	55.0	N/A	mVpp
	Noise @ 50Mhz	3.7	1.2	nV/rt(Hz)
Transimpedance	Gain – Side A	6.3	5.8	V/V
Amplifier with	Gain – Side B	6.3	5.8	V/V
Folded Cascode	-3dB frequency -Side A	144.0	123.0	MHz
Stage	-3dB frequency - Side B	162.0	123.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	33.5	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	35.5	N/A	mVpp
	Noise @ 50Mhz	8.3	4.8	nV/rt(Hz)
Transimpedance	Gain – Side A	6.3	5.8	V/V
Amplifier with	Gain – Side B	6.3	5.8	V/V
Current Mirror	-3dB frequency -Side A	196.0	175.0	MHz
Stage	-3dB frequency - Side B	193.0	175.0	MHz
	Gain Compression Point @ 100 MHz - Side A	37.6	N/A	mVpp
	Gain Compression Point @ 100 MHz- Side B	35.5	N/A	mVpp
	Noise @ 50Mhz	10.1	6.0	nV/rt(Hz)

Table 3.4 - Comparison of non-DC measured and simulated AC values for AMI 1.2 μ m amplifiers

		Measured	Simulated	Units
Two stage	Gain – Side A	2.2	3.3	V/V
Amplifier with	Gain – Side B	2.2	3.3	V/V
Enhancement	-3dB frequency -Side A	106.0	96.0	MHz
Mode Load	-3dB frequency- Side B	101.0	96.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	79.0	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	79.0	N/A	mVpp
	Noise @ 50Mhz	4.6	1.6	nV/rt(Hz)
Two stage	Gain – Side A	4.6	7.0	V/V
Amplifier with	Gain – Side B	4.7	7.0	V/V
Resistive Load	-3dB frequency load -Side A	76.0	63.0	MHz
	-3dB frequency- Side B	76.0	63.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	55.0	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	55.0	N/A	mVpp
	Noise @ 50Mhz	3.6	1.3	nV/rt(Hz)
Transimpedance	Gain – Side A	4.5	6.3	V/V
Amplifier with	Gain – Side B	4.6	6.3	V/V
Folded Cascode	-3dB frequency -Side A	89.0	75.0	MHz
Stage	-3dB frequency - Side B	92.0	75.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	33.0	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	33.0	N/A	mVpp
	Noise @ 50Mhz	8.4	4.2	nV/rt(Hz)
Transimpedance	Gain – Side A	4.6	7.1	V/V
Amplifier with	Gain – Side B	4.9	7.1	V/V
Current Mirror	-3dB frequency -Side A	105.0	121.0	MHz
Stage	-3dB frequency - Side B	108.0	121.0	MHz
	Input Gain Compression Point @ 100 MHz - Side A	33.0	N/A	mVpp
	Input Gain Compression Point @ 100 MHz- Side B	33.0	N/A	mVpp
	Noise @ 50Mhz	8.4	4.2	nV/rt(Hz)

The noise measurements are approximately twice the simulated values for both processes. It is not uncommon for noise measurements to be 120 to 150% larger than simulated values due to poor transistor noise models. Further measurement and simulation would be necessary to determine why there is a larger than expected difference between measured and simulated noise values.

The most likely explanation for the differences between measured and simulated values is poor simulation models. MOSIS DC modeling procedures are evaluated in Chapter 4.

3.3 Testing of Bias Circuit

The purpose of the bias circuit test structure was to provide a means to measure not only the absolute bias current for a given resistor but also to determine whether the transconductance of transistors biased by the bias circuit inversely track the bias resistor as equation 2.34 predicts. The on-chip test structure as shown in Fig. 96 consisted of an n-channel pair and a p-channel pair biased by a current mirror that is mirroring current from the same bias circuit used for the amplifiers. However, the bias circuit test structure has an off-chip bias resistor. Fig. 96 illustrates the test setup for testing the bias circuit using a voltmeter and the HP 4156A Parameter Analyzer. The DC bias current for various resistor values was determined by measuring the voltage across different bias resistors and then dividing by the resistor size. Table 3.5 compares the measured results to simulated values. The measured and simulated values compare favorably. The minor differences do not fully explain why the AMI 0.8 μm currents were one-half designed values and the AMI 1.2 μm were one-third designed values. In order for the HSpice simulated currents to match the measured values, the AMI 0.8 μm resistors were

Table 3.5 - Comparison of measured and simulated bias currents

	Resistor size	Measured Bias Current	Simulated Bias Current
AMI 0.8 μm	1000	2.25E-04	2.25E-04
	1500	1.39E-04	1.17E-04
	2000	8.20E-05	6.00E-05
	2500	5.50E-05	3.80E-05
	3000	4.10E-05	2.75E-05
	3500	3.20E-05	2.26E-05
AMI 1.2 μm	1000	1.50E-04	1.63E-04
	1500	1.39E-04	1.51E-04
	2000	1.17E-04	1.19E-04
	2500	7.80E-05	7.52E-05
	3000	5.60E-05	5.16E-05
	3500	4.25E-05	3.76E-05

increased by 40% while the AMI 1.2 μ m resistors were increased by over 60%.

However, resistor tolerances for on-chip poly-resistors are generally within $\pm 20\%$.

The on-chip resistors used for the amplifiers' bias circuits were laid out using minimum widths. Researchers at ORNL have seen minimum width on-chip resistors result in larger tolerance values, which could explain the reduced bias current values. Such large deviations could also be explained by poor transistor modeling. Transistor modeling for each process is reviewed in Chapter 4.

The HP 4156A Parameter Analyzer was used to take the transconductance measurements. As illustrated in Fig. 96, the inputs to the differential pair were differentially driven from 2.4 to 2.6 V in 1 mV steps and the slope of the differential current in each pair was measured. To reduce the effects of finite output impedance, the n-channel pair drains were tied to 3 V and the p-channel pair drains were tied to 2 V. The

measured transconductance value was then normalized by multiplying by the bias resistor and plotted against bias current. Figs 97 and 98 show the measured and simulated normalized transconductance values plotted against bias current. For lower currents the transconductance is inversely proportional to the bias resistor and the plot of normalized transconductance versus current is flat. At higher currents, the plot is no longer flat because the differential pair current mirror falls into the triode region and the relationship between transistor transconductance and the bias resistor given in equation 2.35 is no longer valid. The AMI 0.8 μm p-channel and both AMI 1.2 μm differential pairs' transconductances are fairly proportional to the resistors as evidenced by the horizontal plotted data. Neither the measured nor the simulated transconductances of the AMI 0.8 μm n-channel differential pair appear to be inversely proportional to the bias resistor. However, the measured amplifier gain values for both the AMI 0.8 μm and AMI 1.2 μm processes support the relationship. Further simulation and testing is needed to determine the reason for this contribution. MOSIS's transistor modeling procedures are reviewed in Chapter 4

Chapter 4

Evaluation of Process Modeling through Transistor Characterization

4.1 Test Transistor Layout and Testing Configuration

Both n-channel and p-channel test transistors and diodes were fabricated in the AMI 0.8 μm N91Y run and the AMI 1.2 μm N95Y run. Two of each type were chosen for analysis. From the AMI 0.8 μm process, the first transistor had a width of 85 μm and a length of 4 μm and the second transistor had a width of 4 μm and a length of 1 μm . From the AMI 1.2 μm process, the first transistor had a width of 102 μm and a length of 4.8 μm and the second transistor had a width of 4.8 μm and a length of 1.2 μm . Fig. 99 shows the equivalent test setup for measuring I_D vs. V_{DS} and I_D vs. V_{GS} curves for both n-channel (configuration A and C) and p-channel (configuration B and C) transistors using the HP 4156A Parameter Analyzer. For each transistor, measured and simulated curves are plotted on the same graph. In addition, linear regression was used to compute and compare the Early voltage from both the measured and simulated I_D vs. V_{DS} curves and the threshold voltage from both the measured and simulated square root of I_D vs. V_{GS} curves.

4.2 AMI 0.8 um Process

The AMI 0.8 um process is a 2-metal, 1-poly with poly-capacitor, n-well 5V process. Per the process summary in Appendix 2, designers using SCMOS rules with a lambda of 0.5 um should manually deduct 0.2 um from transistor lengths extracted from layout. MOSIS replaced the process with the AMI 0.5 um process during the 4th quarter of 1999; however, the AMI 0.8 um process is available through a commercial foundry.

Figs. 100 through 103 are the measured and simulated I_D vs. V_{DS} curves for the AMI 0.8 um test transistors. Table 4.1 compares the Early voltage values that were regressed from the curves.

Table 4.1 - Comparison of measured and simulated Early voltage values for the AMI 0.8 um test transistors

NMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=85um	1	6.82E+01	4.33E+01
L=4um	2	1.11E+02	9.44E+01
	3	1.06E+02	8.76E+01
	4	N/A	5.70E+01
NMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=4um	1	1.06E+01	1.00E+01
L=1um	2	1.78E+01	1.70E+01
	3	2.30E+01	2.27E+01
	4	3.07E+01	2.85E+01
PMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=85um	1	3.46E+01	3.69E+01
L=4um	2	5.50E+01	4.72E+01
	3	4.97E+01	4.75E+01
	4	3.56E+01	3.96E+01
PMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=4um	1	1.11E+00	6.83E-01
L=1um	2	6.19E+00	5.08E+00
	3	6.30E+00	6.38E+00
	4	6.01E+00	6.35E+00

Figs. 104 through 107 are the measured and simulated square root of I_D vs. V_{GS} curves for the AMI 0.8 μm test transistors. Table 4.2 compares the threshold voltage values that were regressed from the curves. With the exception of the first transistor's I_D vs. V_{DS} curve for $V_{GS} = 4$, the measured and simulated curves and regressed values for the Early voltages and threshold voltages are very similar. Therefore, based on the tests performed on these four transistors, MOSIS's DC modeling of transistors in the N91Y run appears to be reliable. The simulations were made ignoring MOSIS's recommendation to deduct 0.2 μm from the extracted gate lengths. The amplifiers under test were fabricated in the N97L run for which no test transistors were available for analysis; however, it is

Table 4.2 - Comparison of measured and simulated threshold voltage for AMI 0.8 μm test transistors

	Measured V_t (V)	Simulated V_t (V)
NMOS, W/L = 85/4	0.640	0.633
NMOS, W/L = 4/1	0.567	0.561
PMOS, W/L = 85/4	0.825	0.810
PMOS, W/L = 4/1	0.755	0.698

reasonable to assume that the N97L transistor models are just as accurate as those for the N91Y run. Under this assumption and based on the bias data from section 3.2.6, it is difficult to explain the reduction in bias current in the bias circuit. Apparently, during fabrication, the resistor sizes were increased from the value that was laid out in and extracted from MAGIC.

4.3 AMI 1.2 μm Process

The AMI 1.2 μm process is a 2-metal, 1-poly with poly-capacitor, n-well 5V process. It was originally a 1.5 μm process in which the gate lengths were shrunk to 1.2 μm . A lateral NPN bipolar transistor is also available. Recent problems with the process

have resulted in MOSIS raising the lambda to 0.8 um, effectively increasing the minimum gate length to 1.6 um. The test transistors analyzed in this section were fabricated using a lambda of 0.6 um or minimum gate length of 1.2 um.

Figs. 108 through 111 are the measured and simulated I_D vs. V_{DS} curves for the AMI 1.2 um test transistors. Table 4.3 compares the Early voltage values that were regressed from the curves.

Figs 112 through 115 are the measured and simulated square root of I_D vs. V_{GS} curves for the AMI 1.2 um test transistors. Table 4.4 compares the threshold voltage values that were regressed from the curves

Table 4.3 - Comparison of measured and simulated Early voltage values for the AMI 1.2 um test transistors

NMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=102um	1	5 45E+01	3 31E+01
L=4.8um	2	5 85E+01	5 61E+01
	3	5 55E+01	5 15E+01
	4	4 14E+01	3 77E+01
NMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=4.8um	1	3 36E+00	6 31E+00
L=1.2um	2	8 22E+00	8 80E+00
	3	1 29E+01	1 15E+01
	4	1 78E+01	1 46E+01
PMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=102um	1	1 94E+01	1 41E+00
L=4.8um	2	2 57E+01	1 48E+01
	3	2 45E+01	2 14E+01
	4	1 87E+01	1 64E+01
PMOS	Vgs	Measured Va (V)	Simulated Va (V)
W=4.8um	1	1 47E-01	1 28E+00
L=1.2um	2	2 58E+00	6 81E+00
	3	3 57E+00	7 96E+00
	4	4 08E+00	7 28E+00

Table 4.4 - Comparison of measured and simulated threshold voltage for AMI 1.2 um test transistors

	Measured Vt (V)	Simulated Vt (V)
NMOS, W/L = 102/4.8	0.563	0.530
NMOS, W/L = 4.8/1.2	0.293	0.266
PMOS, W/L = 102/4.8	0.793	0.720
PMOS, W/L = 4.8/1.2	0.583	0.637

The most significant deviations between measured and simulated results are from the minimum length device. These differences are consistent with the AMI 1.2 um process problems that MOSIS has recently reported. Since the test transistors were fabricated in the same process as the amplifiers, the poor quality simulation models would partially explain the differences between measured and simulated results reported in Tables 3.2 and 3.4. However, the large reduction in the amplifier bias currents and the bias data of section 3.2.6 cannot be so easily explained. As with the AMI 0.8 um process, it appears that during fabrication, the resistor sizes were increased from the value that was laid out in and extracted from MAGIC.

Chapter 5

Conclusion

5.1 Evaluation of Amplifier and Bias Circuit Designs

Selection of one amplifier design for use in the cantilever sensing device is not possible at this time without firmer system design specifications. Each design has positive and negative features. The two stage amplifiers are simple, use less power and less chip space than the four-stage designs. For approximately the same power, both designs provide the same gain-bandwidth product. The amplifier with resistive load provides less noise and higher gains but less bandwidth than the amplifier with enhancement mode load. Both of the four stage amplifiers are easily chainable, as their outputs can easily be made to match their common-mode input voltage, and have higher gains and bandwidths than the two stage designs. The four-stage design with a current mirror has a slight advantage over the folded cascode design in that the current mirror itself can be used to modify the gain without changing the transimpedance loop. The primary limiting feature of all of the designs is the low gain compression point driving 5 pF at 100 MHz, caused primarily by the non-linearity of the source-follower output stage.

Of course, the gain compression point driving on-chip capacitive loads of 1 pF or less would be larger and therefore less of a constraint.

The use of the bias circuit to stabilize transconductances is highly recommended. Even with the DC bias currents being significantly lower than originally designed, the amplifiers in both processes had gains very close to the original design expectations, due almost entirely to the bias circuit. By making the gain relationships of each amplifier design dependent almost exclusively on resistor ratios, the amplifiers were highly independent of process variations, such as varying resistors, and power variations, such as reductions in bias current, as well as temperature and other process variations. However, the noise of the bias circuit is a potential problem that must be addressed if the circuit is used to power non-differential designs

5.2 Selection of a Process

Given the recent problems with the AMI 1.2 μm process, the AMI 0.8 μm process is the preferred process for fabricating the cantilever sensor. Moreover, not only do the AMI 0.8 μm models appear to be more accurate, the AMI 0.8 μm process should be much faster than the AMI 1.2 μm process when comparing equivalently constructed and biased amplifier designs.

5.3 Future Work

Further refinements in the design of each amplifier are expected. Specifically, the two-stage amplifier with enhancement mode load can be optimized to provide higher gain and the two-stage amplifier with resistive load could be optimized to give an output voltage closer to its common-mode input voltage. The transimpedance stage of the four stage amplifiers can be optimized to improve frequency response and give a higher gain

value. Higher gains in the four-stage amplifier with current mirror stage are possible by using the current mirror to provide more gain. Slightly higher bandwidths in the four-stage designs may be possible by optimizing transistor sizes and bias currents. As mentioned previously, further simulation and analysis would most likely confirm that the majority of the gain compression problem is due to the source-follower output stage's inability to sink current. If so, a better CMOS output stage would be instrumental in improving the performance of all of the designs. In relation to process evaluation, further investigation into the cause of the suspected increase in the on-chip resistance values is necessary. One way to determine if the resistors were laid out incorrectly would be to use a microscope to carefully measure the length and width of the fabricated resistors. The reason for the AMI 0.8 μm process bias circuit test results for the n-channel transistors not validating the inverse relationship between the bias resistor and transistor transconductances also needs to be investigated. Furthermore, the AMI 0.5 μm 3-metal, 2-poly, 5 V should be considered in the future as it should allow even smaller devices and therefore provide a platform for an even faster amplifier.

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APPENDICES

APPENDIX 1

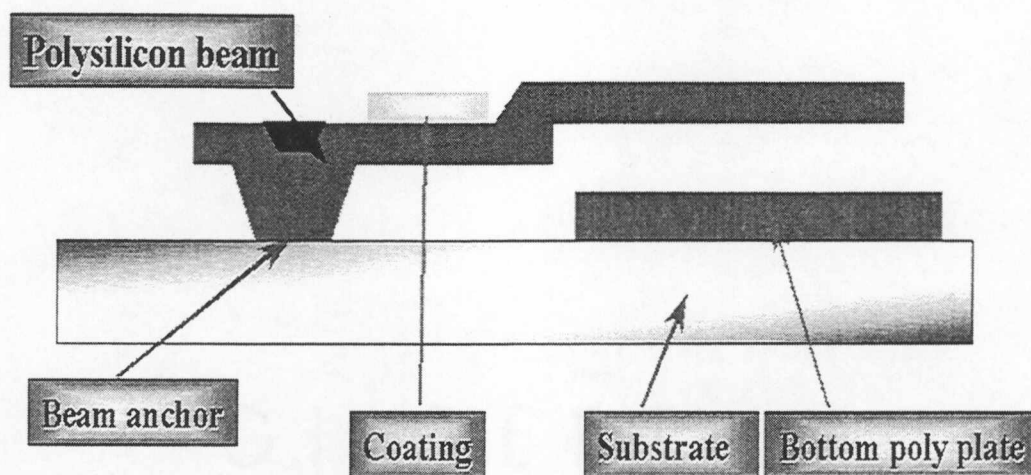


Figure 1 - Cross section of cantilever beam

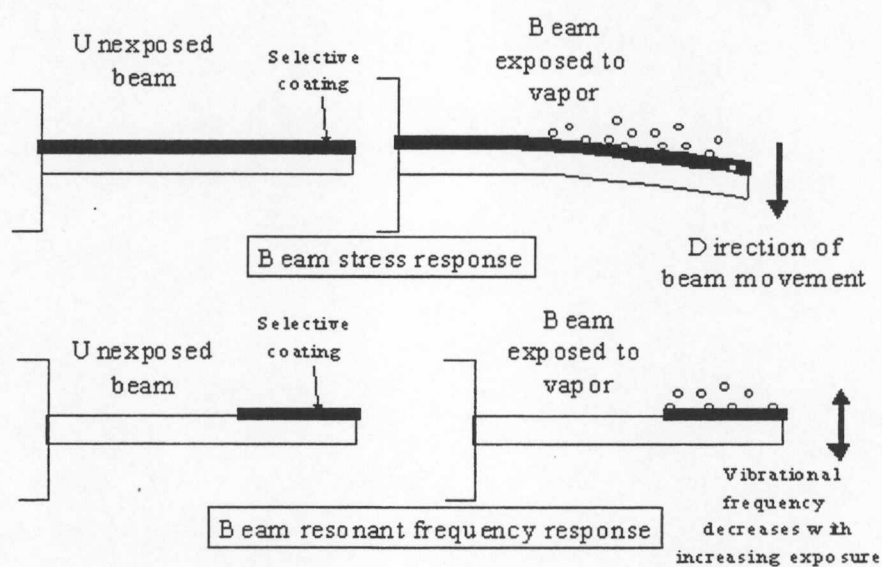


Figure 2 - Modes of cantilever operation

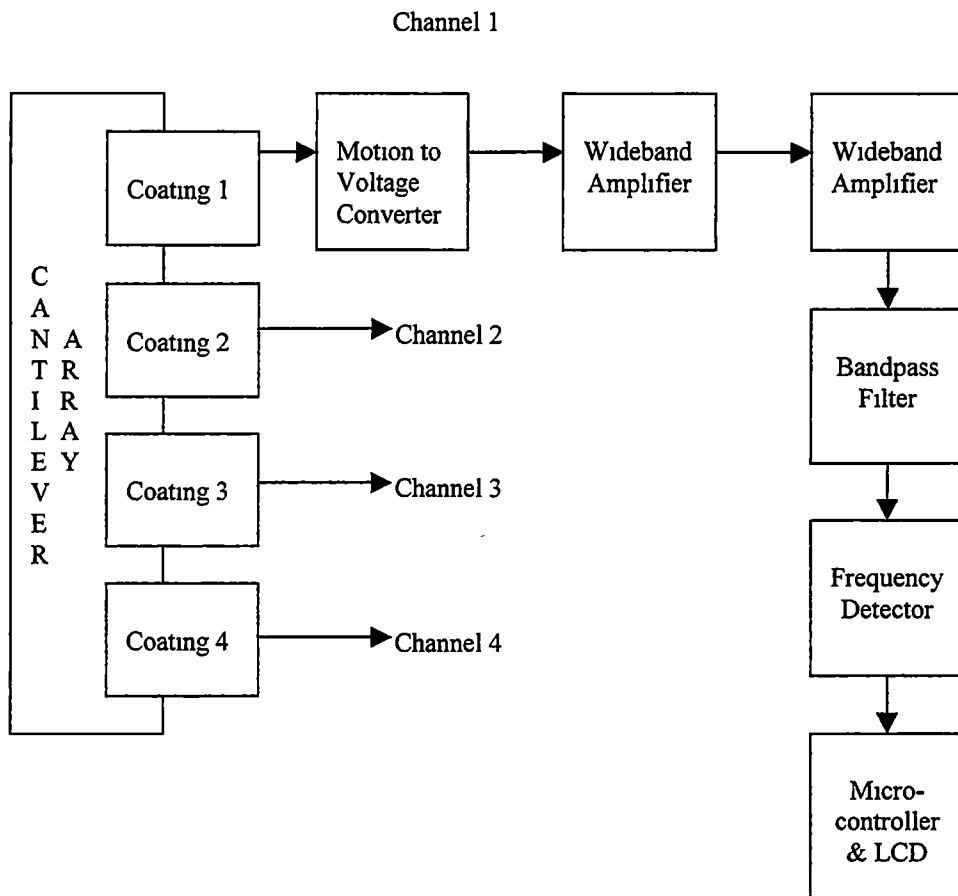


Figure 3 - Block diagram of proposed cantilever sensing system

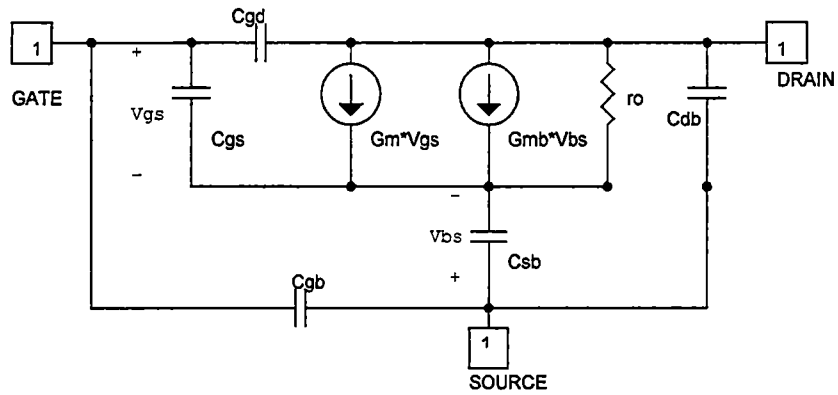


Figure 4 - Small signal equivalent model of an N-MOS transistor

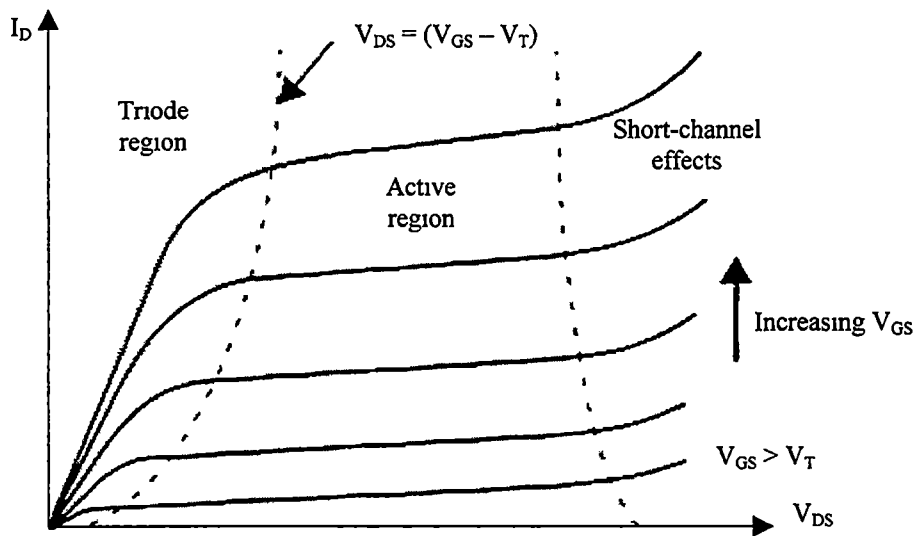


Figure 5 - Normalized I_D vs. V_{DS} curves for an NMOS transistor

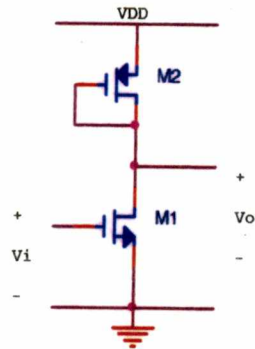


Figure 6 - Common source amplifier with enhancement-mode load

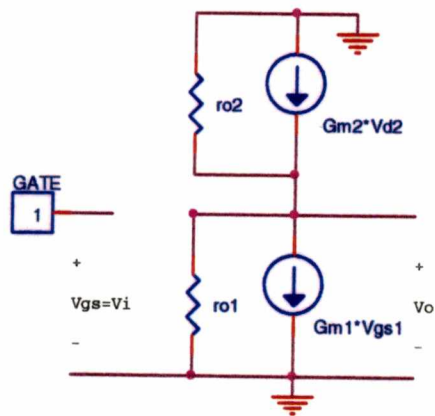


Figure 7 - Small signal equivalent model of a common source amplifier with enhancement-mode load

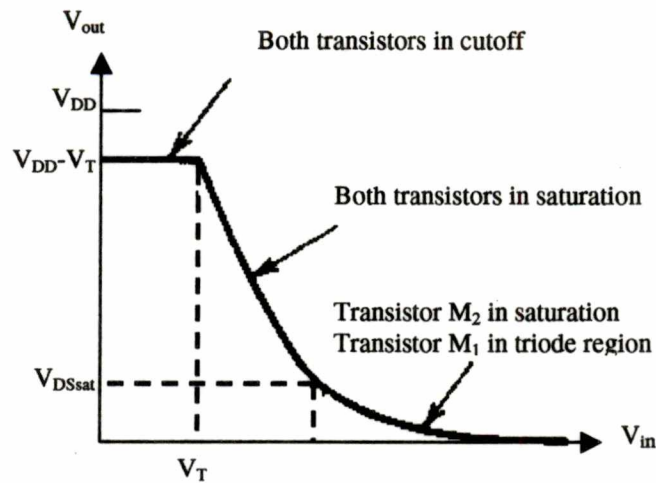


Figure 8 - Transfer characteristic of a common source amplifier with enhancment mode load

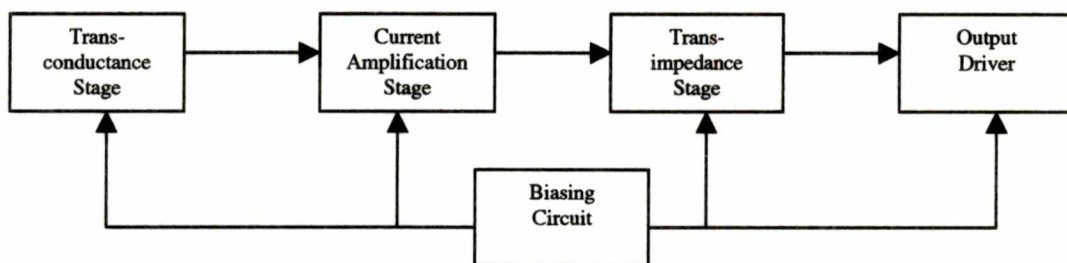


Figure 9 - Block diagram of wideband amplifier design

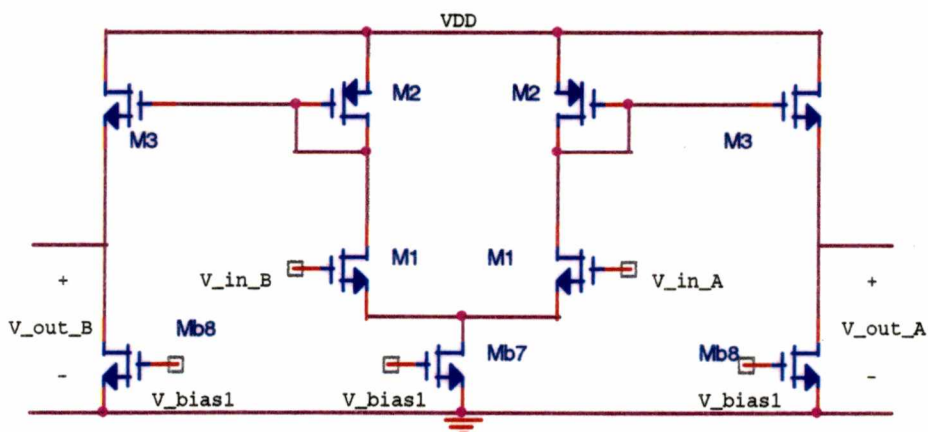


Figure 10 - Two stage amplifier with enhancement mode load

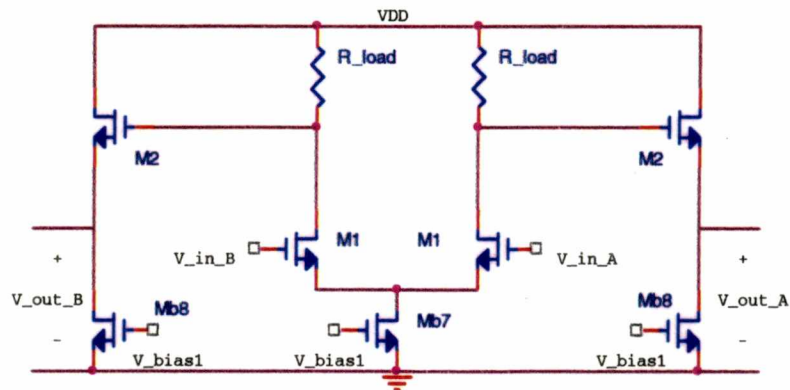


Figure 11 - Two stage amplifier with resistive load

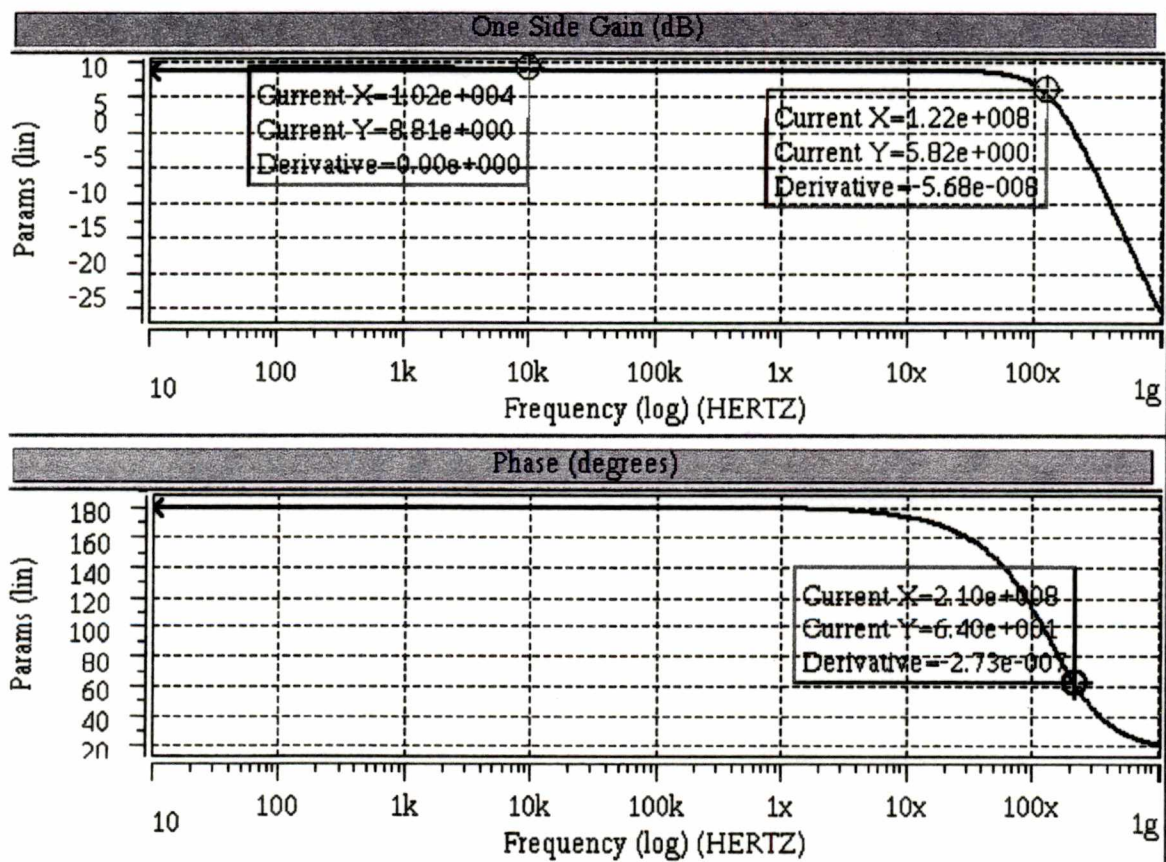


Figure 12 – HSpice simulation of frequency response for two stage amplifier with enhancement mode load and 10 pF output load using AMI 0.8um N87R run BSIM3 models

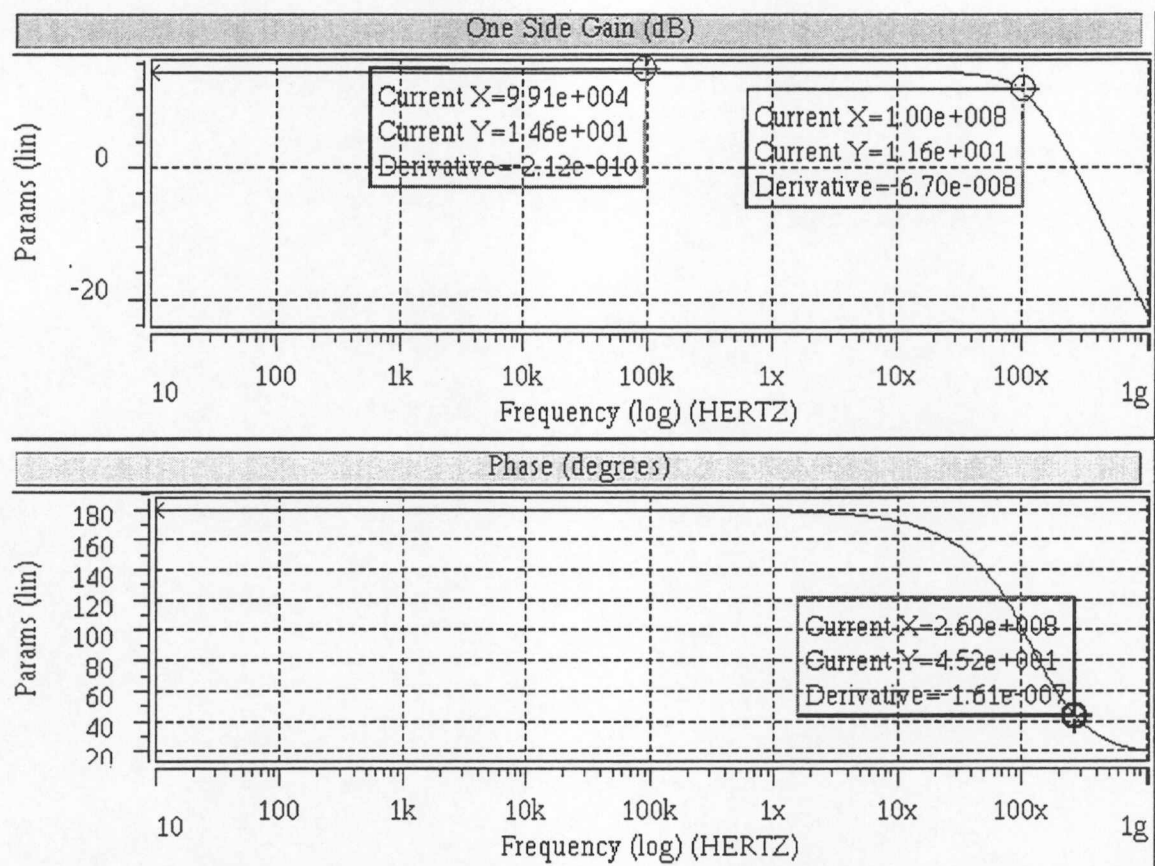


Figure 13 - HSpice simulation of frequency response for two stage amplifier with resistive load and 10 pF output load using AMI 0.8um N87R run BSIM3 models

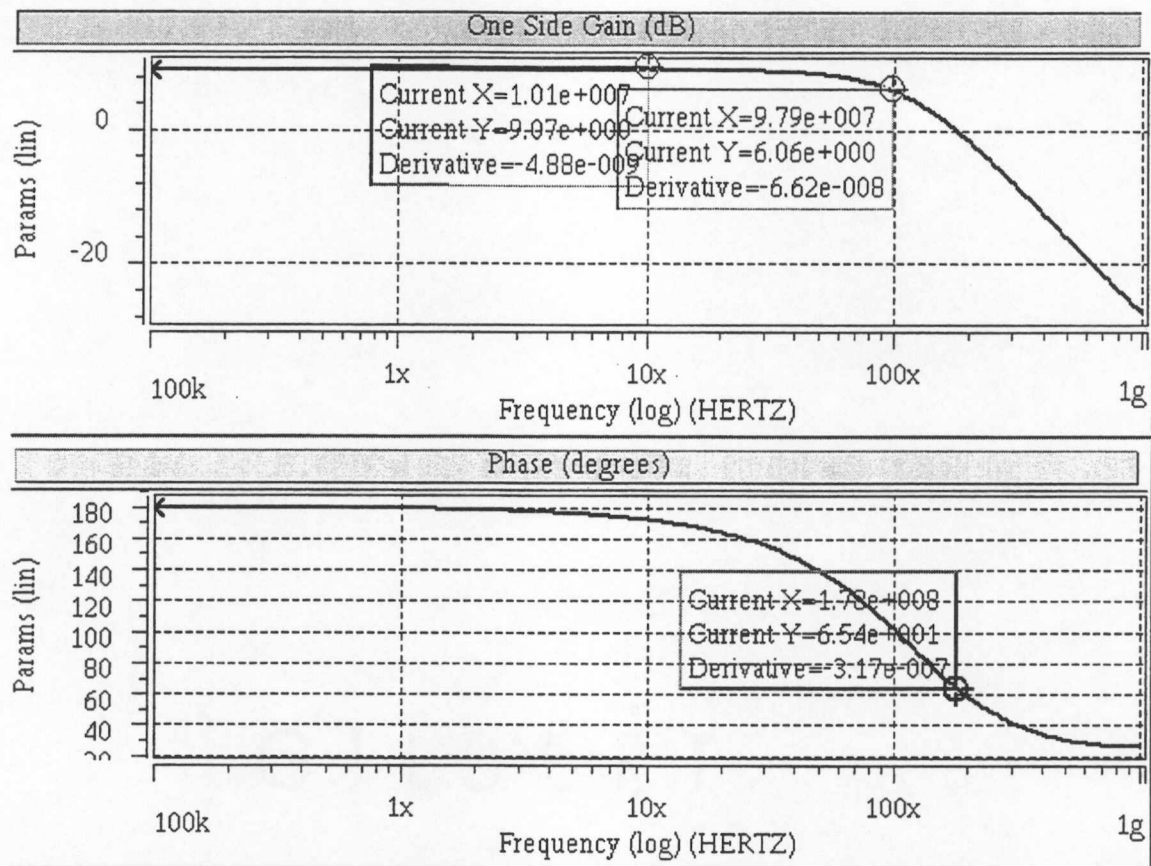


Figure 14 - Hspice simulation of frequency response for two stage amplifier with enhancement mode load and 10 pF output load using AMI 1.2um N88Z run BSIM3 models

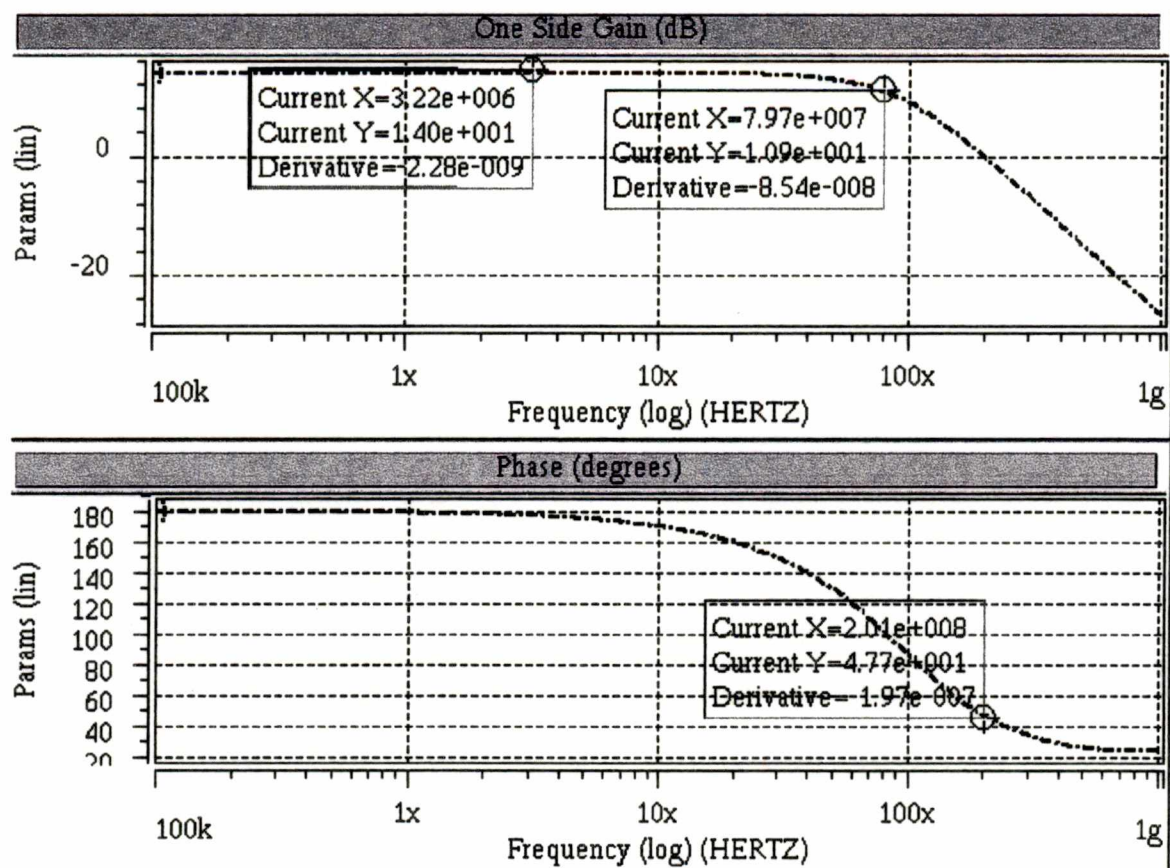


Figure 15 - Hspice simulation of frequency response for two stage amplifier with resistive load and 10 pF output load using AMI 1.2um N88Z run BSIM3 models

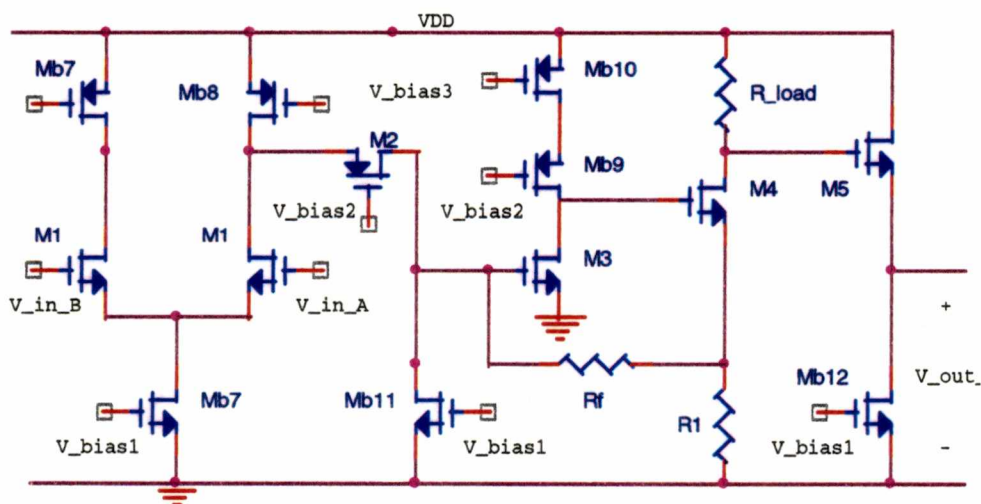
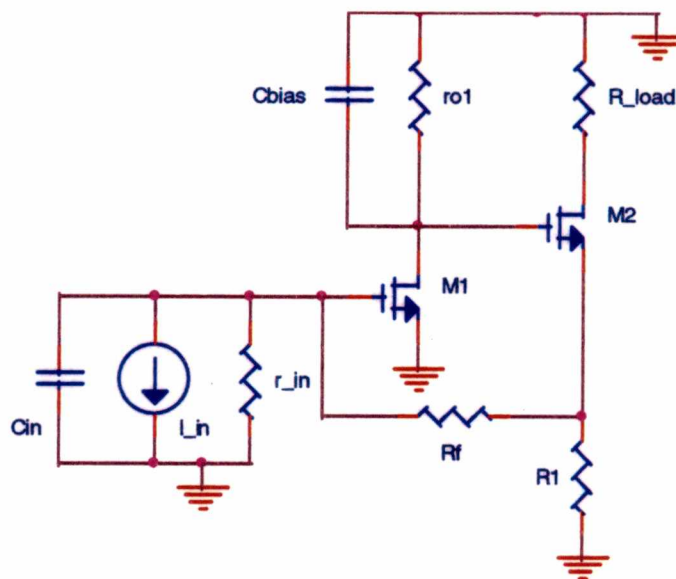
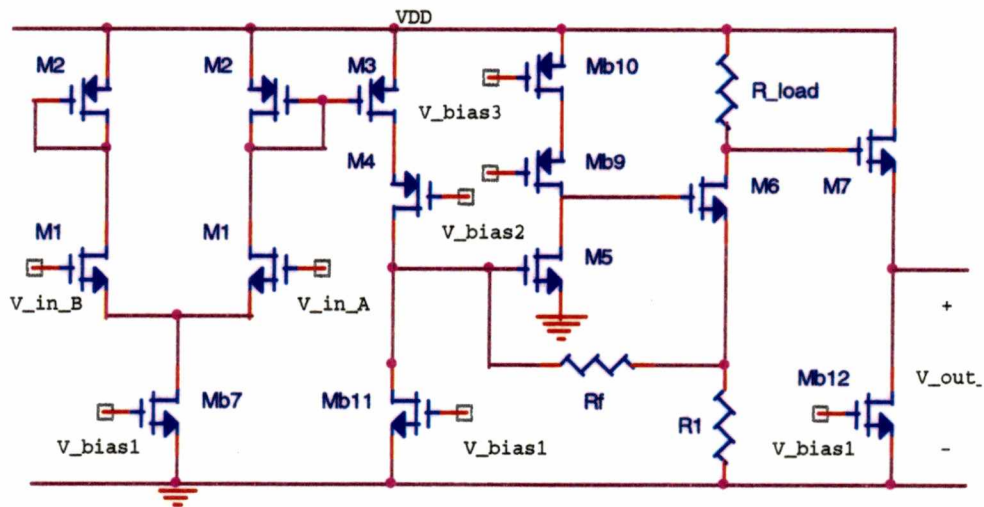


Figure 16 - Four stage transimpedance amplifier design with folded cascode stage



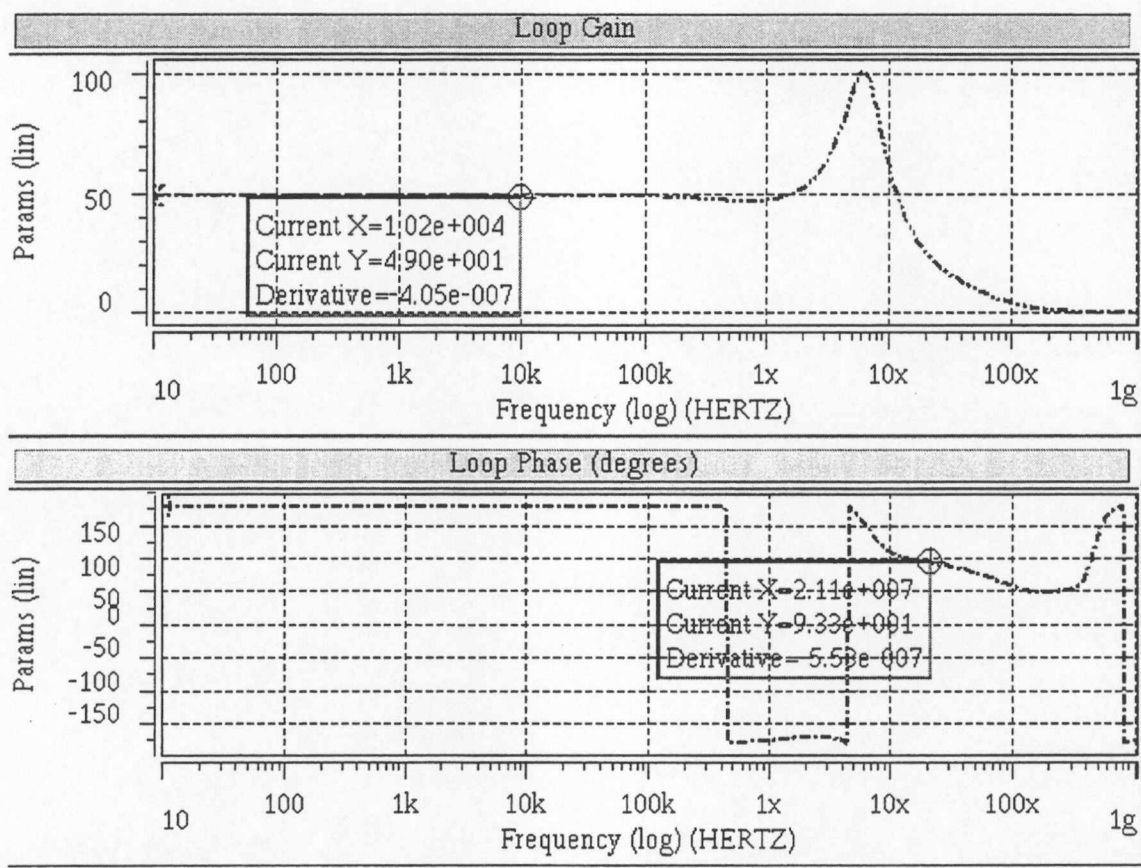


Figure 19 - HSpice simulation of loop transmission magnitude and phase for transimpedance amplifier with folded cascode stage using AMI 0.8um N87R run BSIM3 models

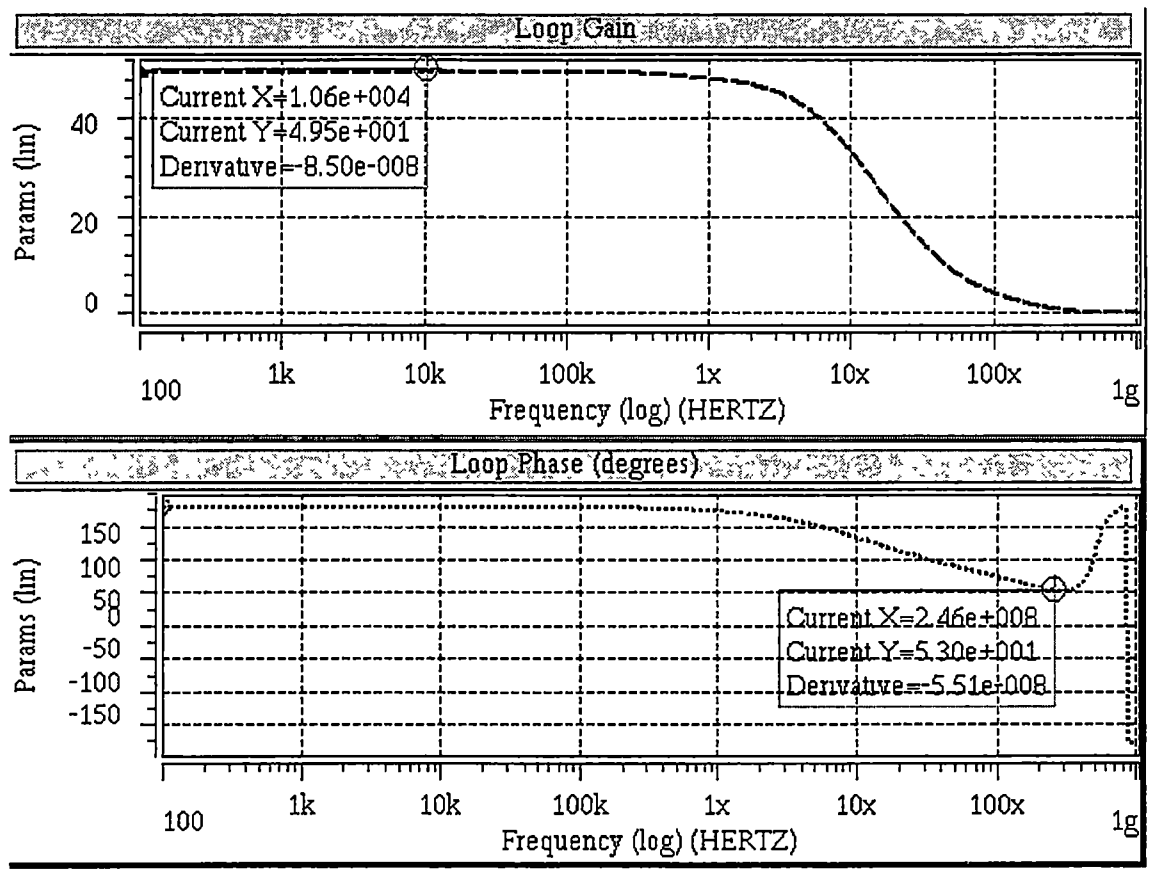


Figure 20 - HSpice simulation of loop transmission magnitude and phase for transimpedance amplifier with current mirror stage using AMI 0.8um N87R run BSIM3 models

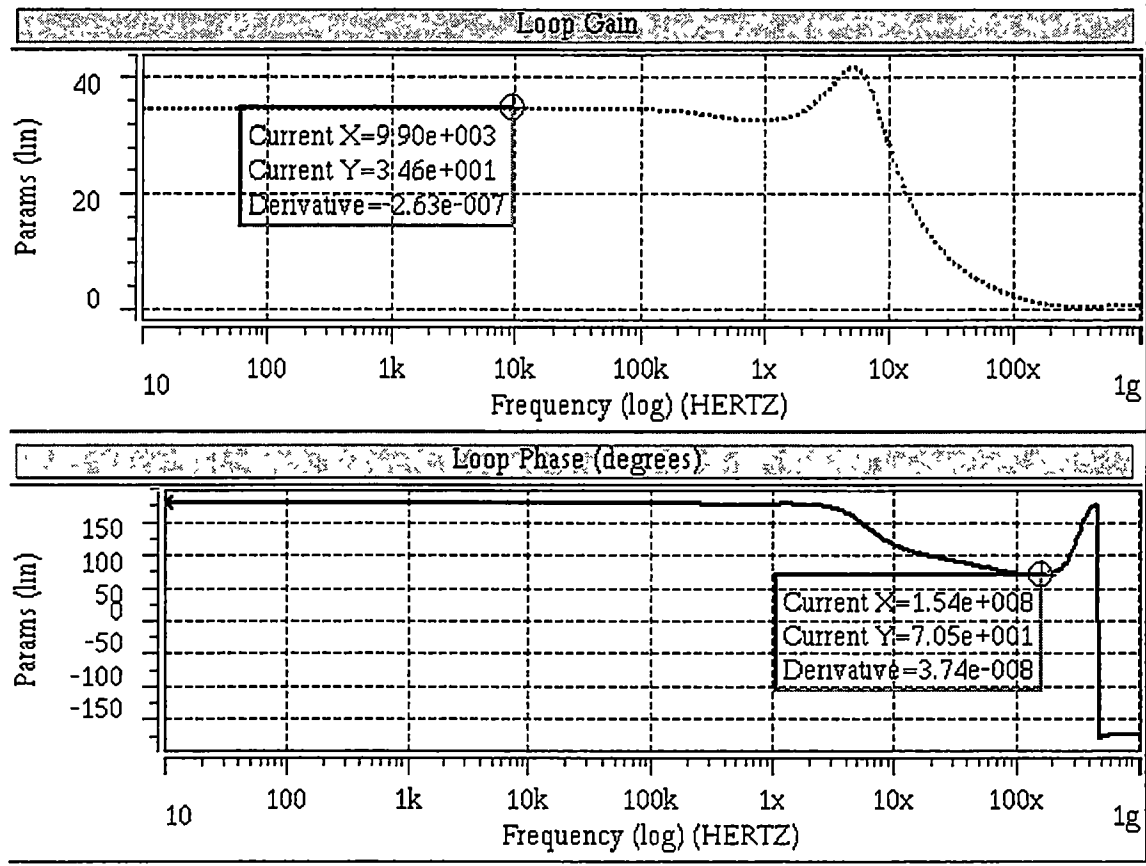


Figure 21 - HSpice simulation of loop transmission magnitude and phase for transimpedance amplifier with folded cascode stage using AMI 1.2um N88Z run BSIM3 models

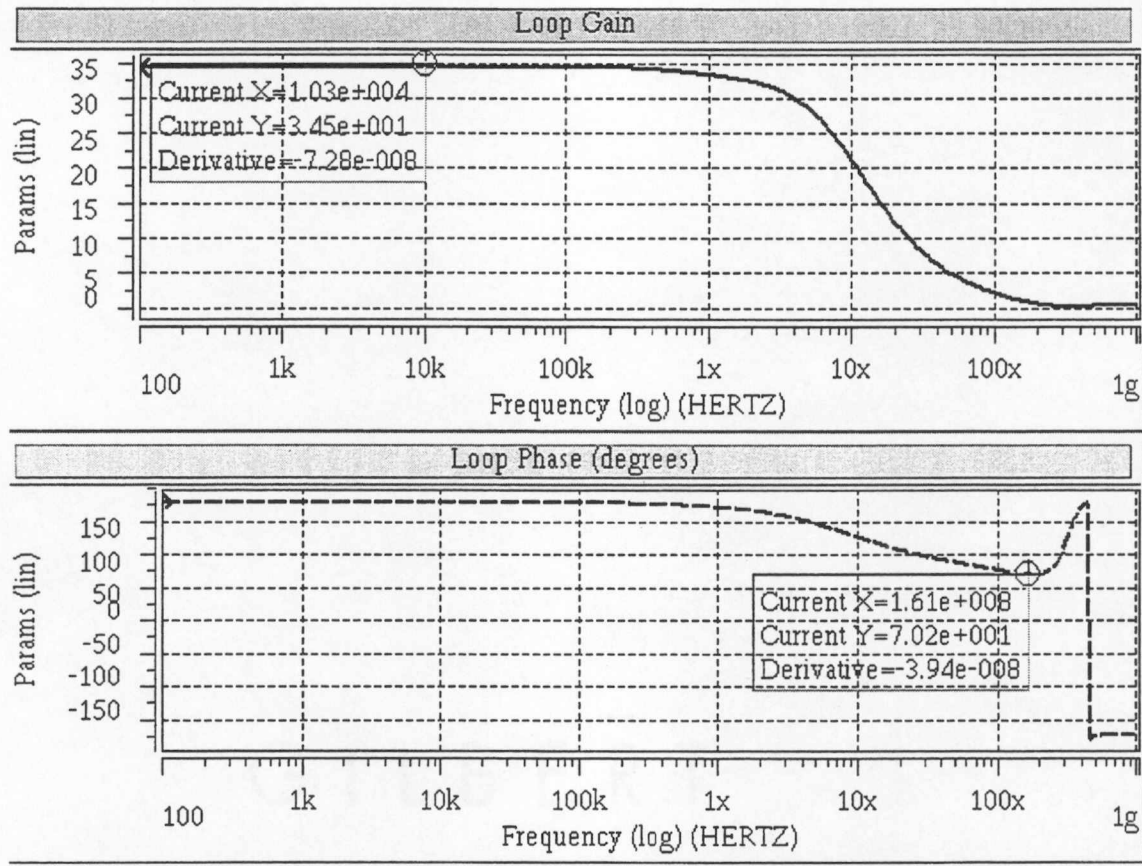


Figure 22 - HSpice simulation of loop transmission magnitude and phase for transimpedance amplifier with current mirror stage using AMI 1.2um N88Z run BSIM3 models

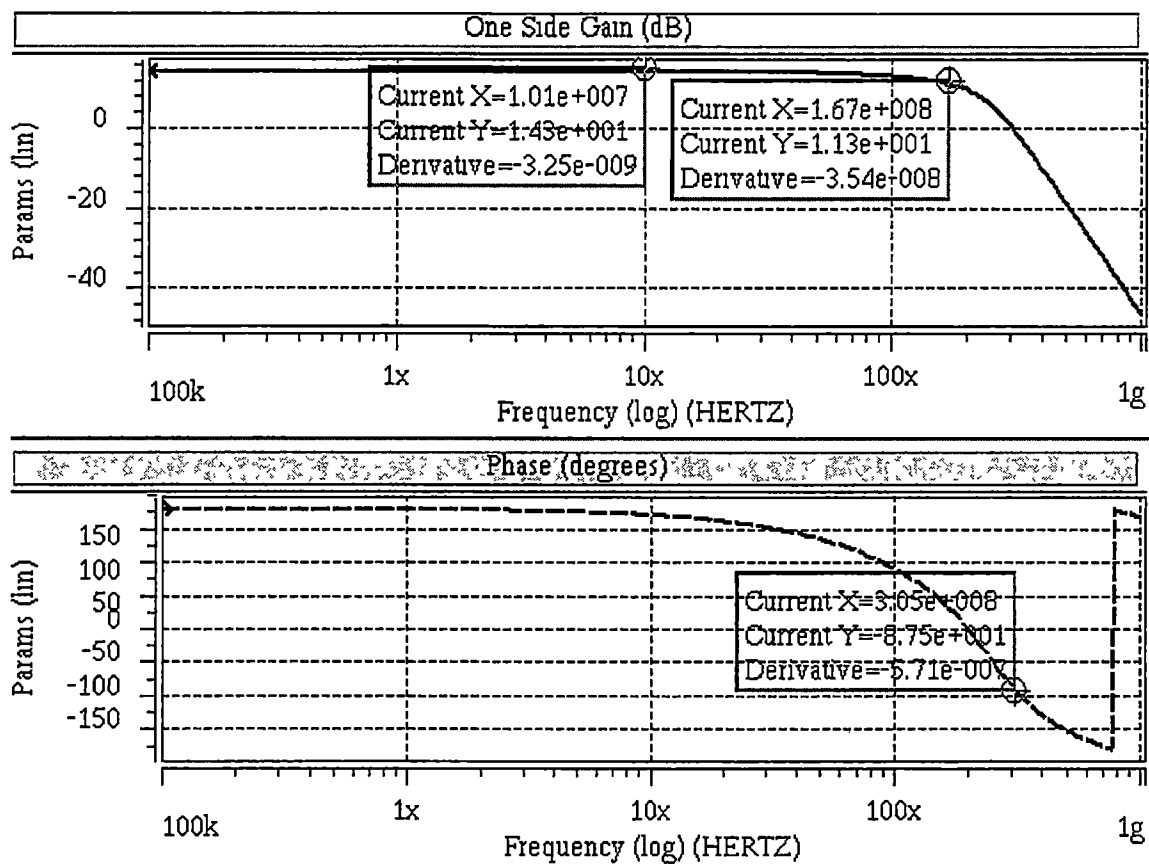


Figure 23 - Hspice simulation of frequency response for transimpedance amplifier with folded cascode stage and 10 pF output load using AMI 0.8um N87R run BSIM3 models

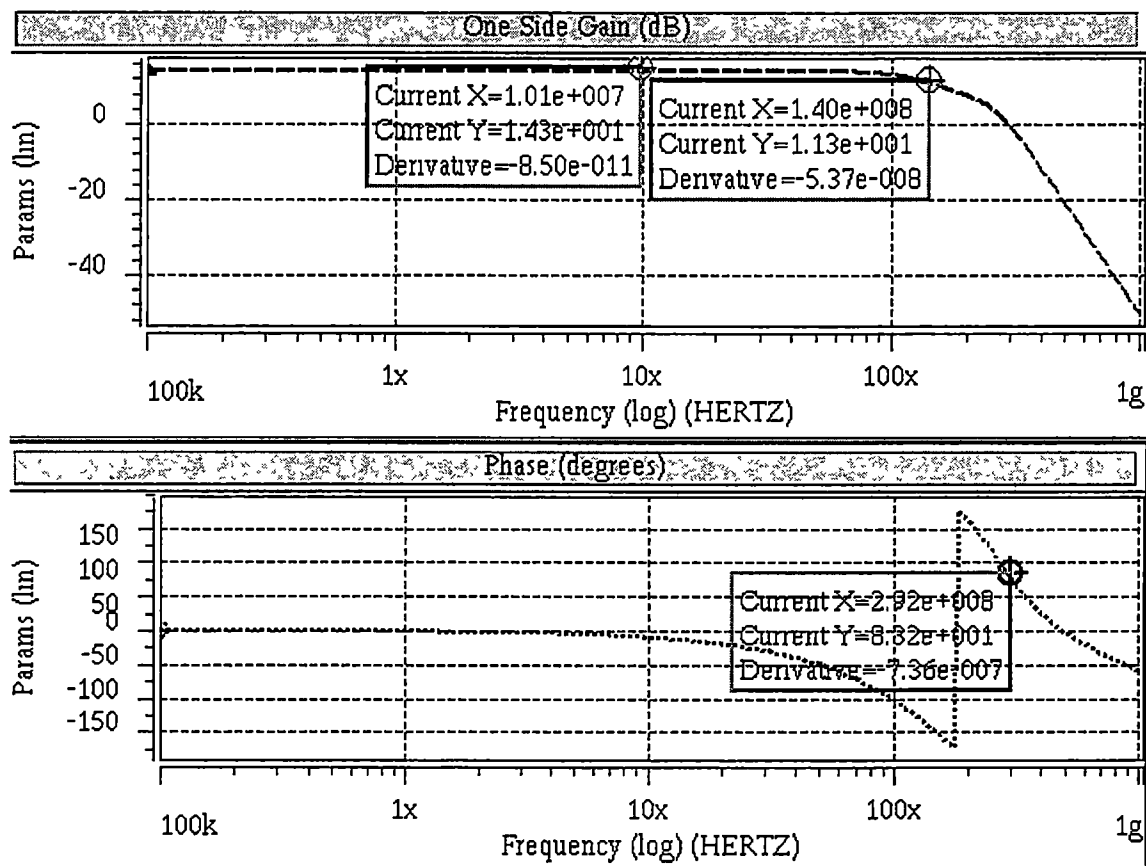


Figure 24 - HSpice simulation of frequency response for transimpedance amplifier with current mirror stage and 10 pF output load using AMI 0.8um N87R run BSIM3 models

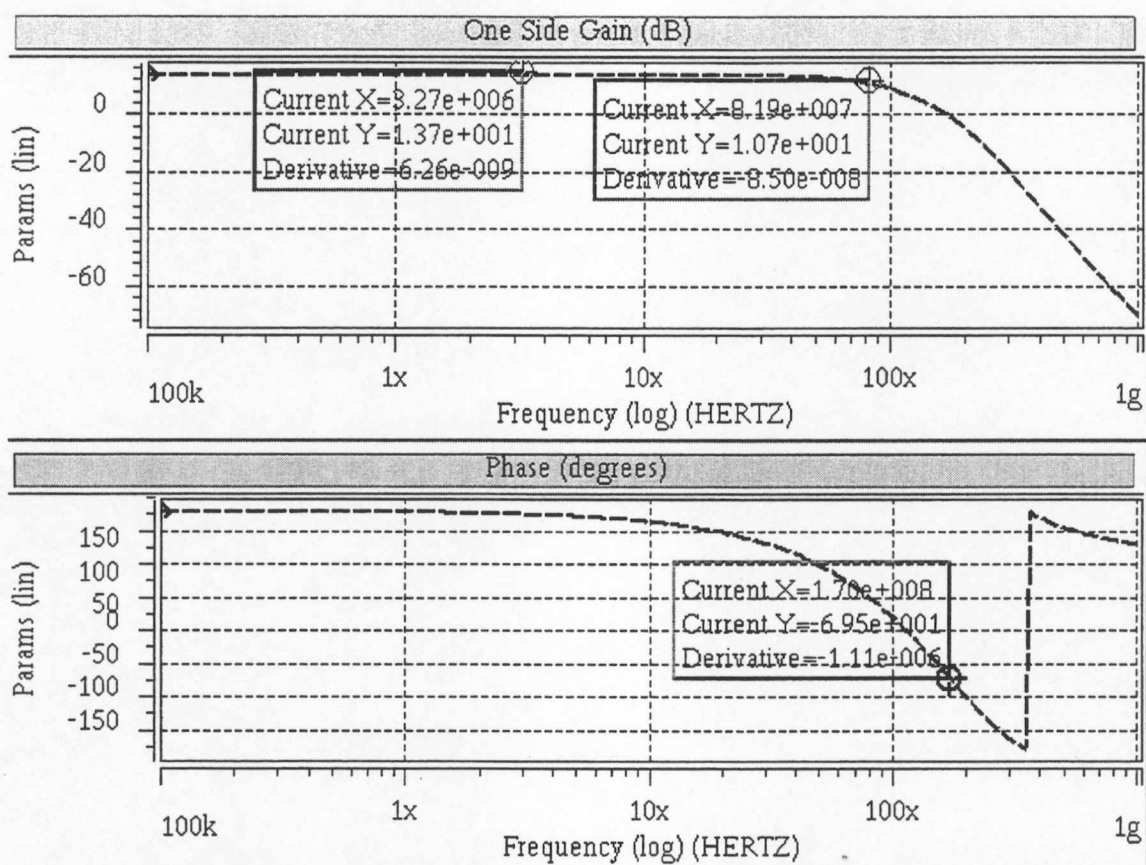


Figure 25 - HSpice simulation of frequency response for transimpedance amplifier with folded cascode stage and 10 pF output load using AMI 1.2um N88Z run BSIM3 models

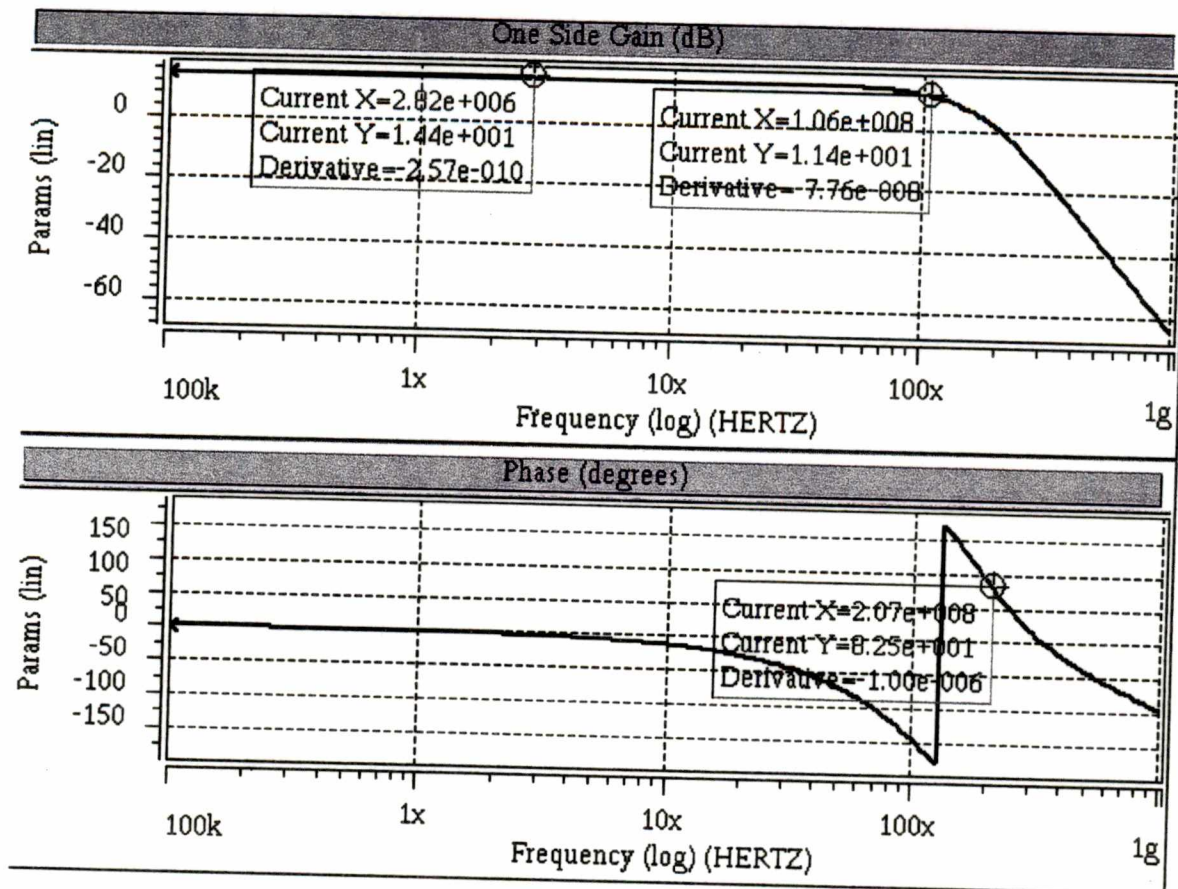


Figure 26 - HSpice simulation of frequency response for transimpedance amplifier with current mirror stage and 10 pF output load using AMI 1.2um N88Z run BSIM3 models

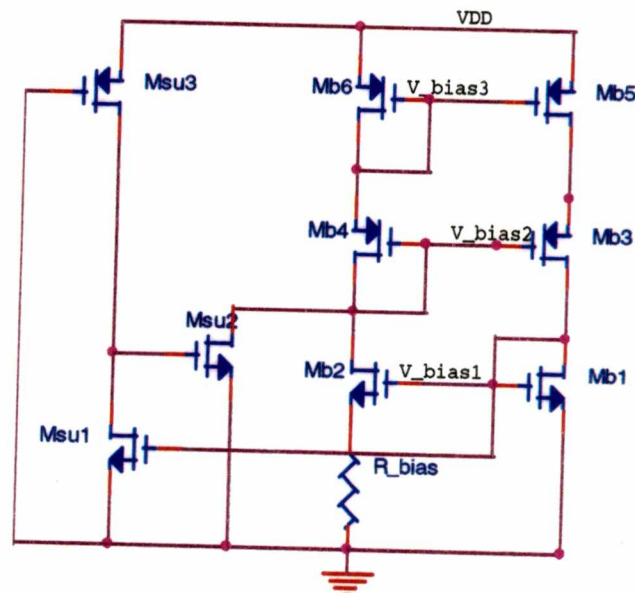


Figure 27 - Schematic of biasing circuit used to stabilize transistor transconductances

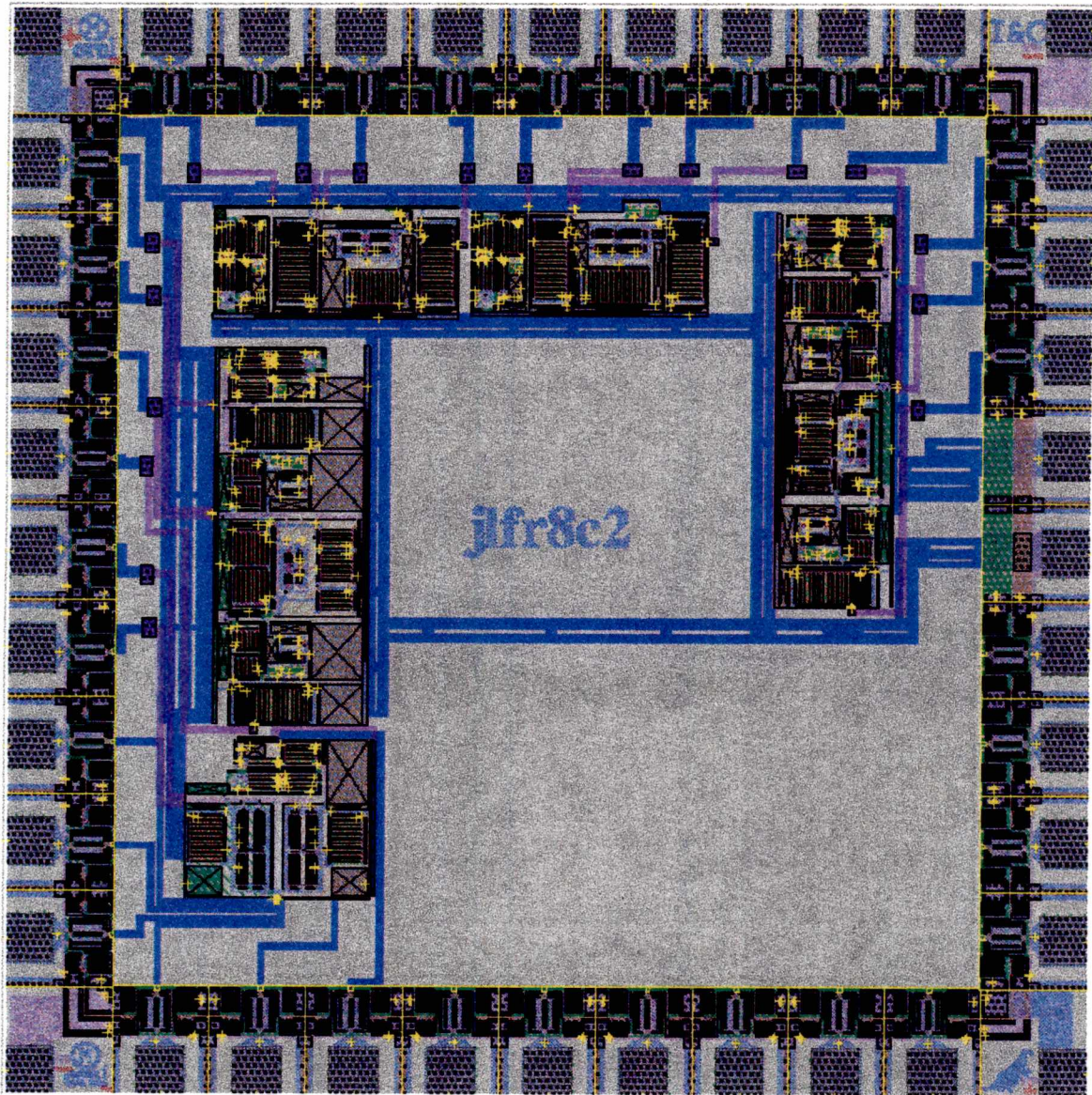


Figure 28 – MAGIC layout of amplifiers and test structure for AMI 0.8um run

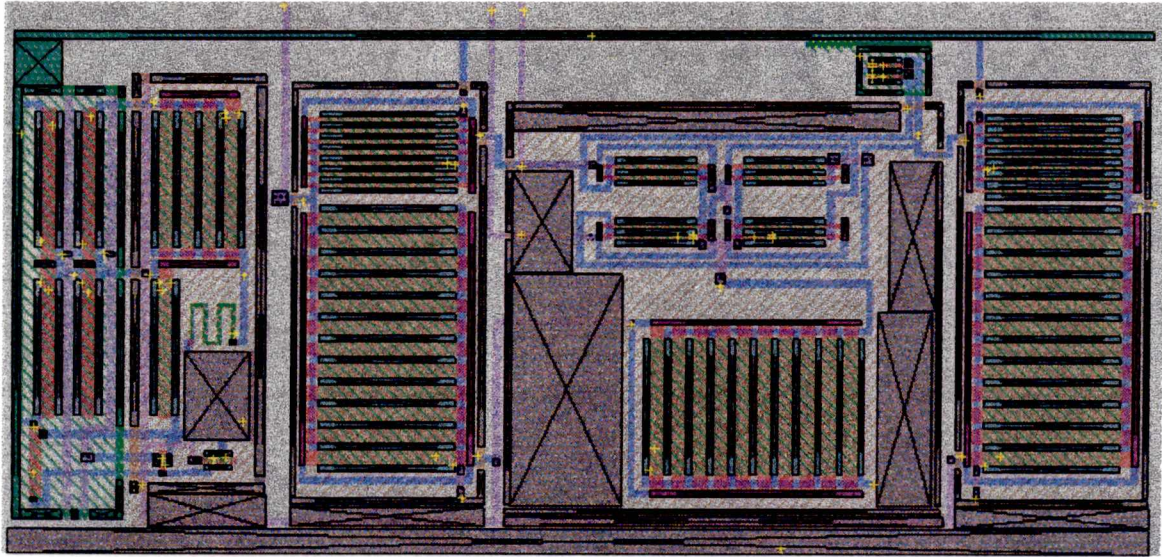


Figure 29 – MAGIC layout of two stage amplifier with enhancement mode load for AMI 0.8 um run

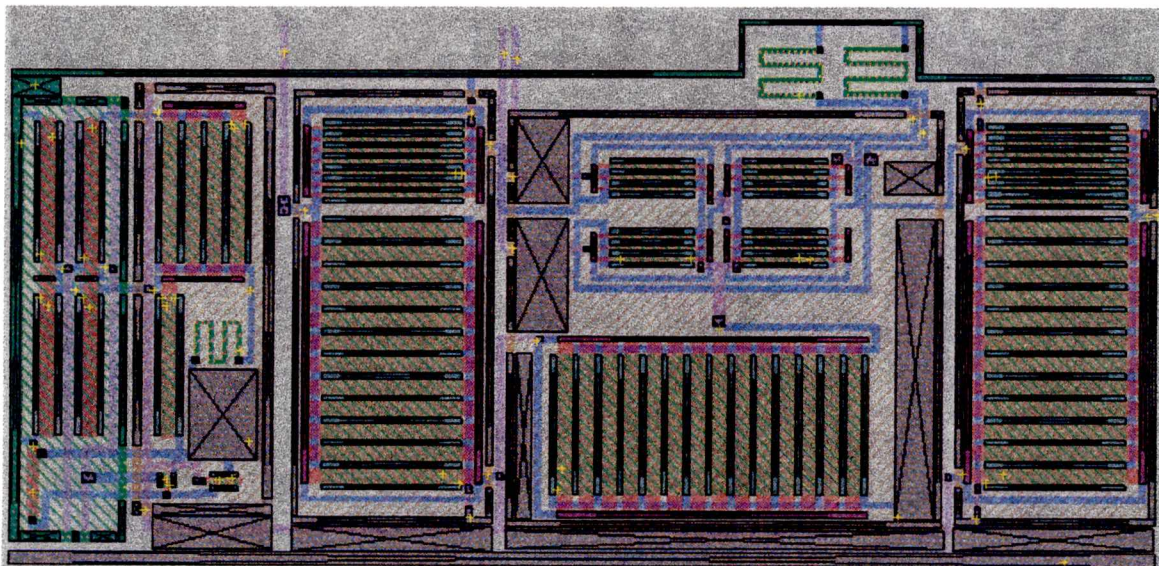


Figure 30 – MAGIC layout of two stage amplifier with resistive load for AMI 0.8 um run

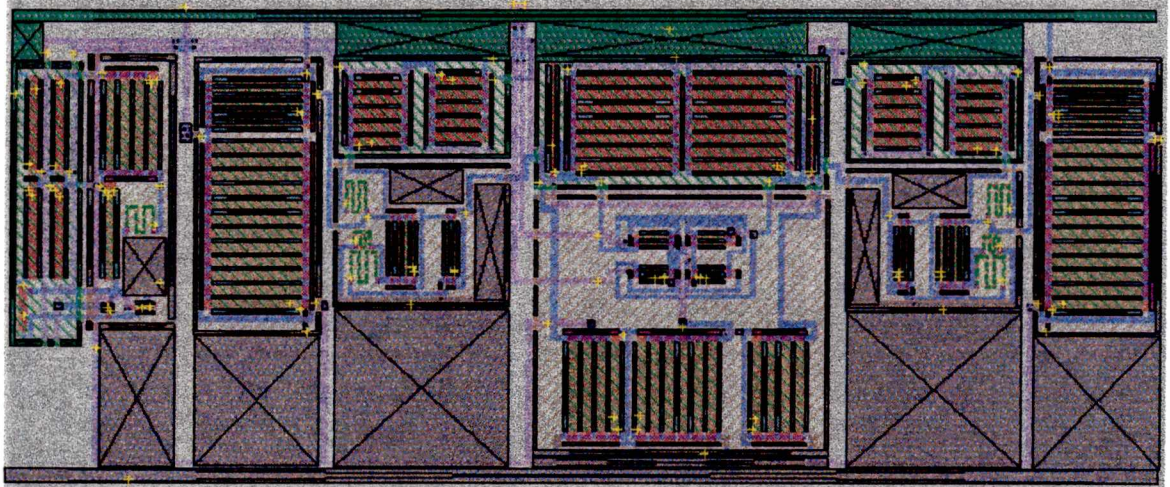


Figure 31 – MAGIC layout of transimpedance amplifier with folded cascode stage for AMI 0.8 um run



Figure 32 - MAGIC layout of transimpedance amplifier with current mirror stage for AMI 0.8 um run

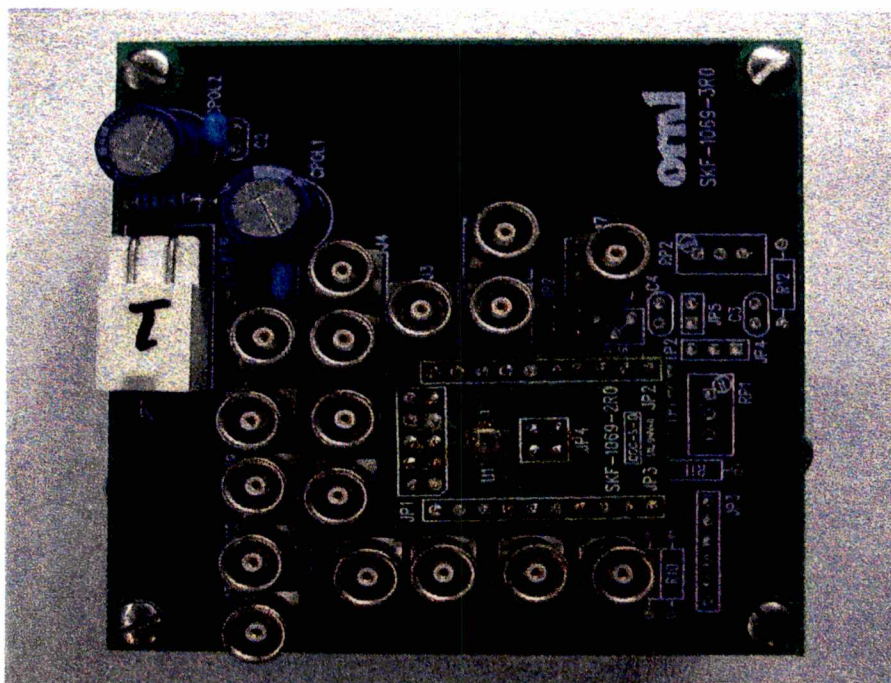


Figure 33 – Amplifier test board top side

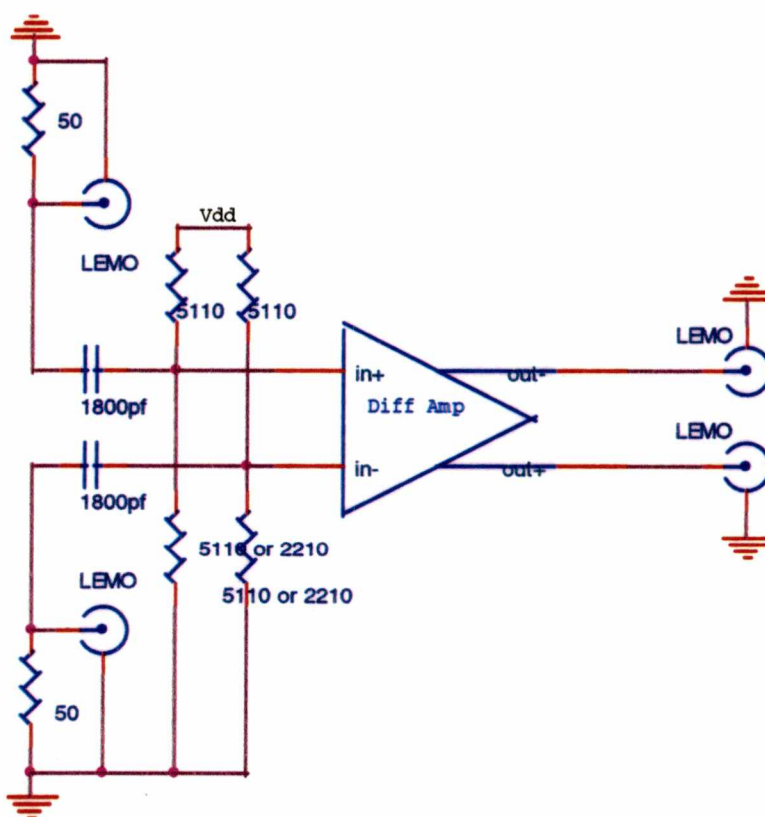


Figure 34 - DC test board schematic

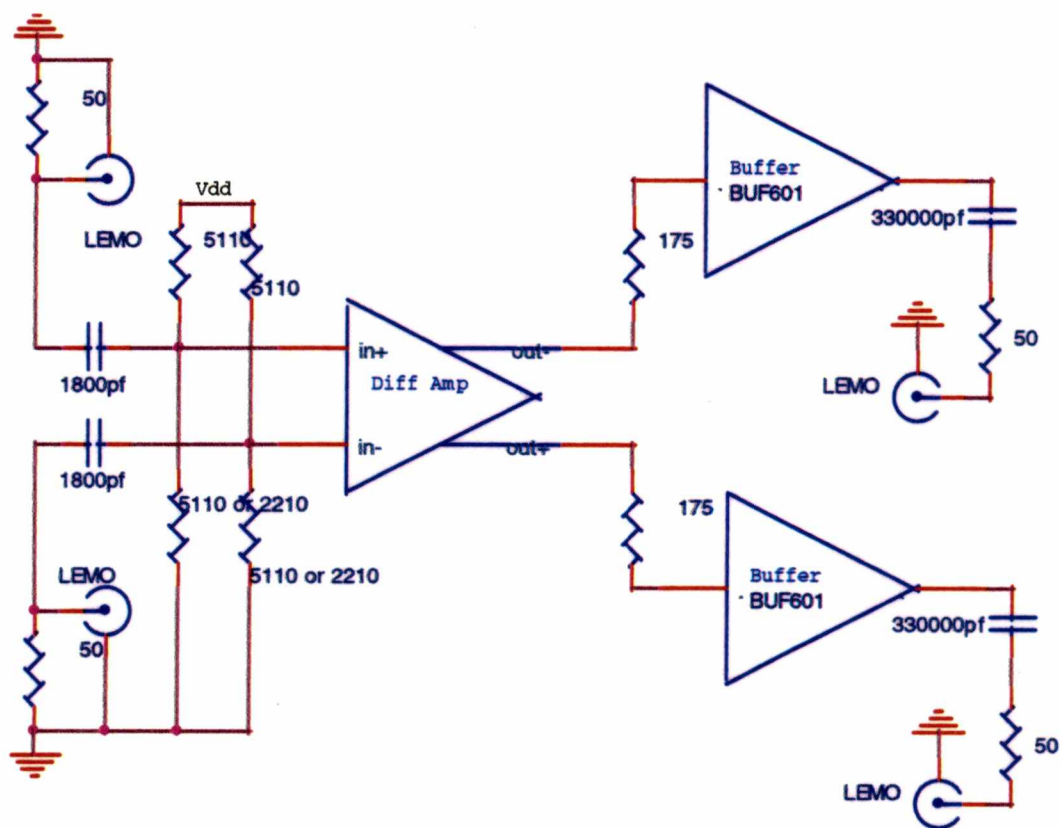


Figure 35 - AC test board schematic

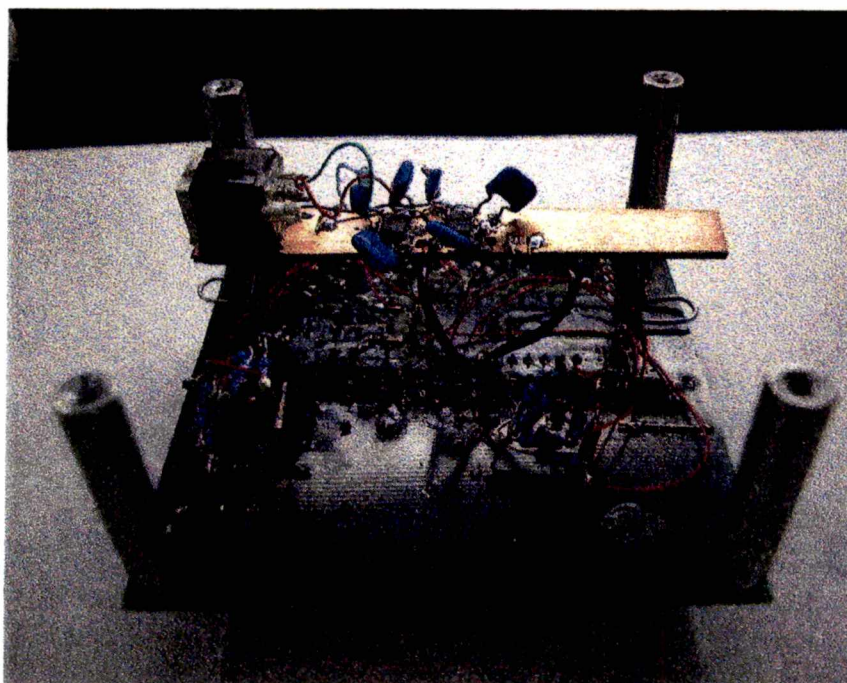


Figure 36 - Amplifier test board bottom side

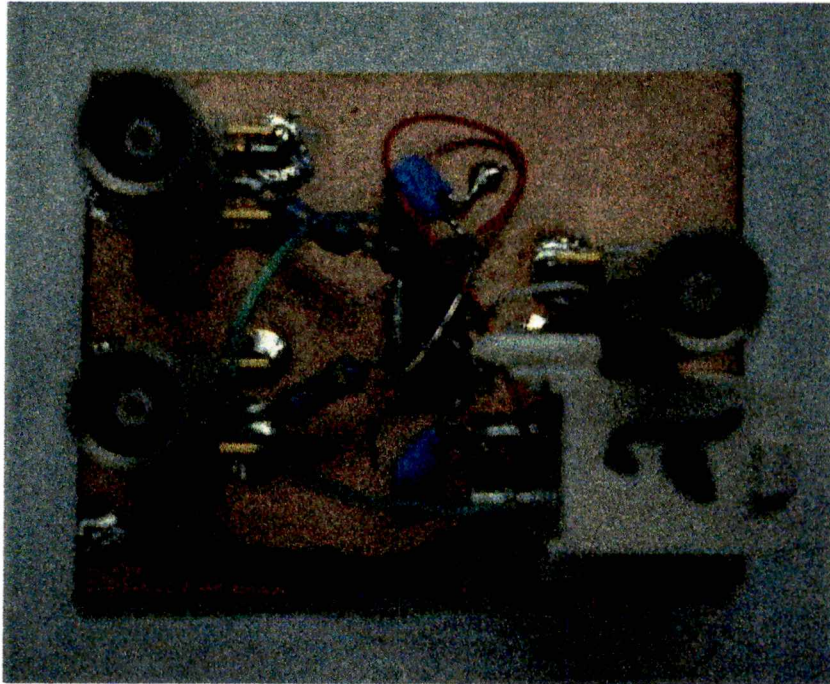


Figure 37 - Differential line driver test board

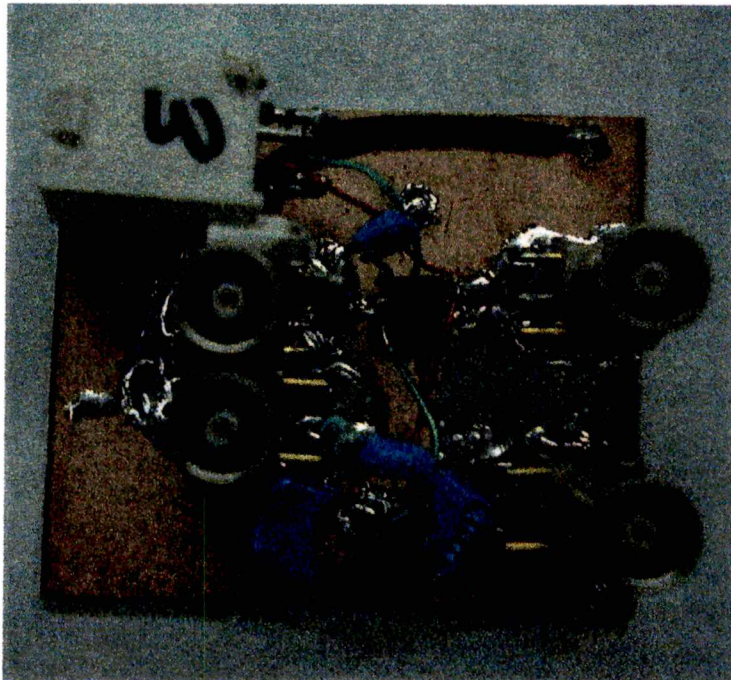


Figure 38 - Output buffer test board

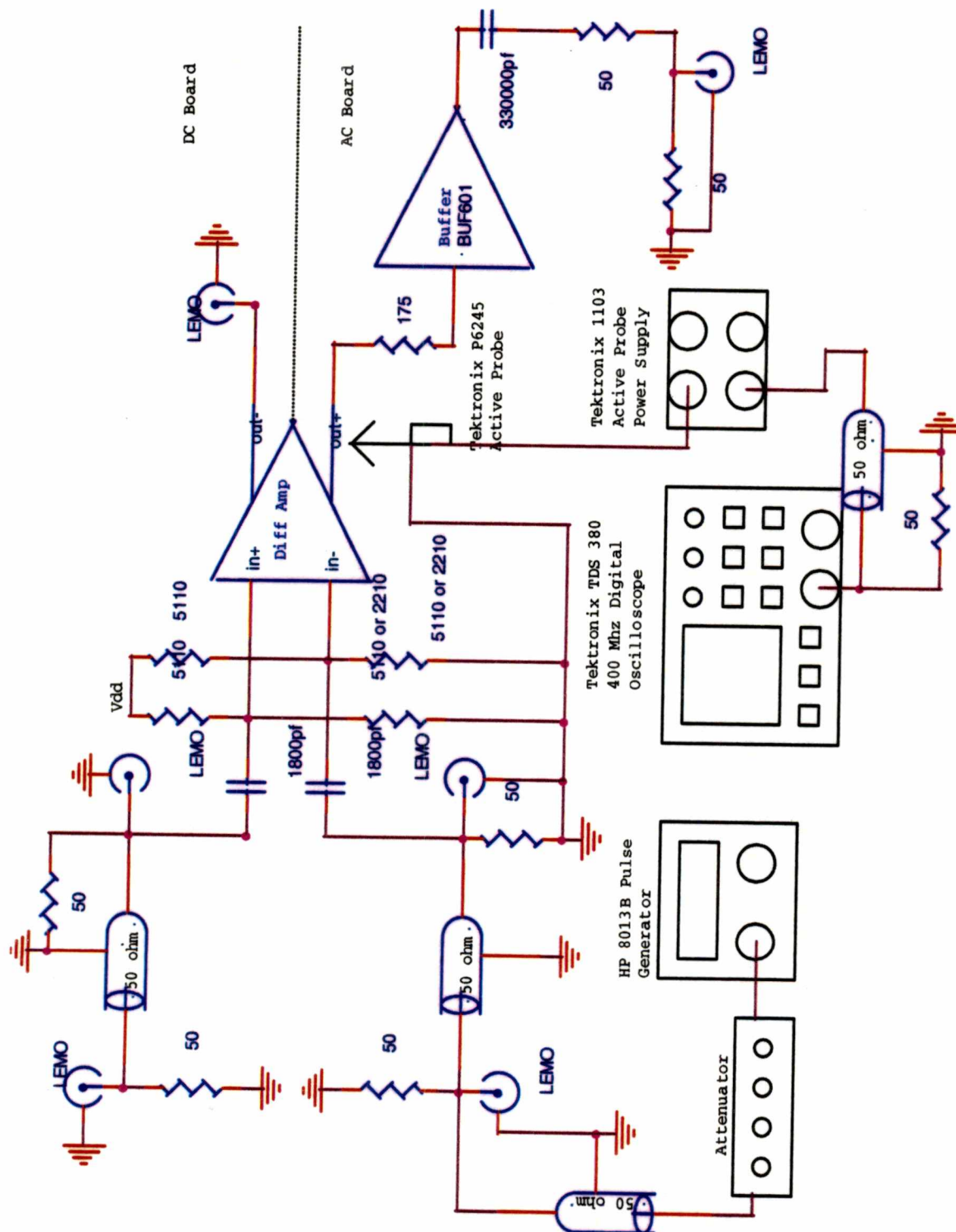


Figure 39 - Test setup for measuring capacitive loading

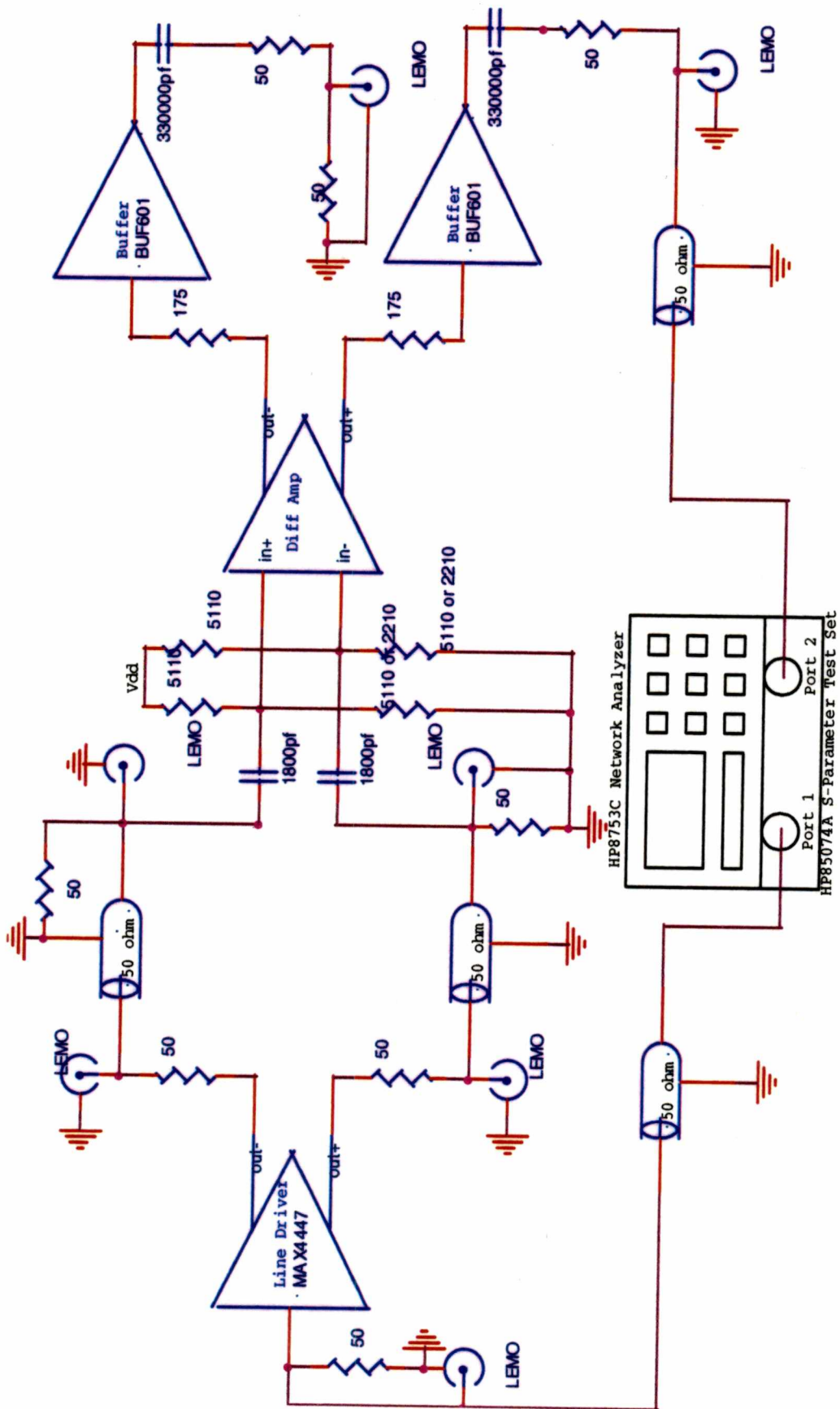


Figure 40 - Test setup for measuring gain magnitude and phase

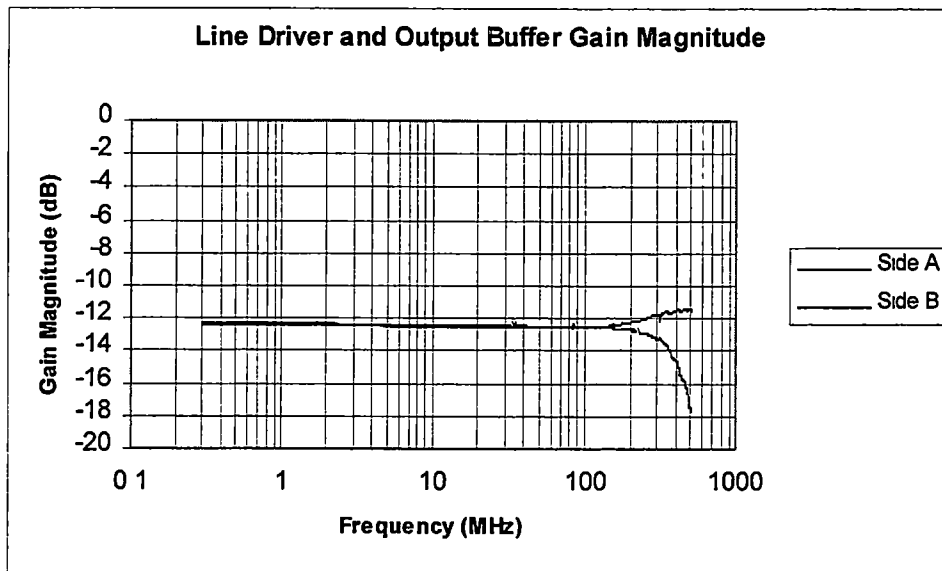


Figure 41 – Line driver and output buffer gain magnitude

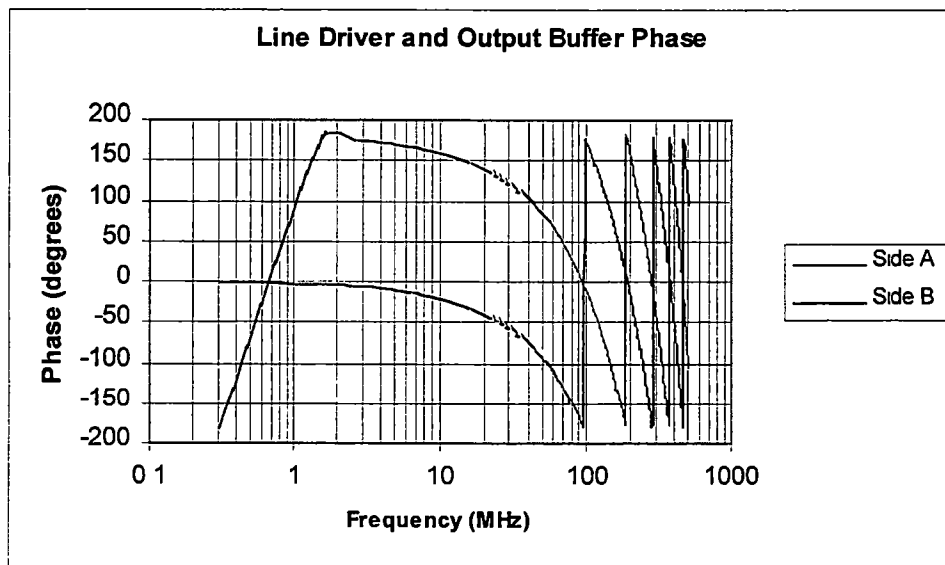


Figure 42 – Line driver and output buffer phase

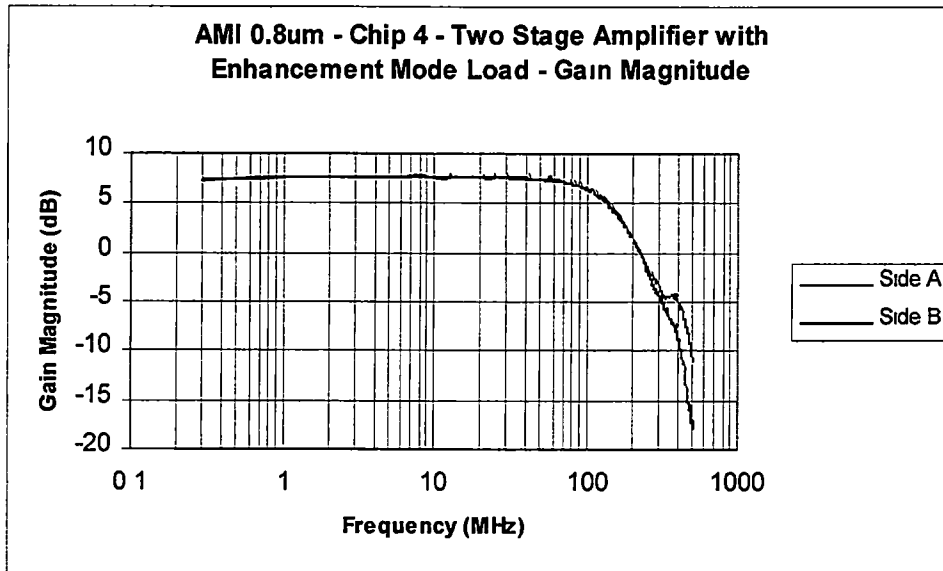


Figure 43 - AMI 0.8 um two-stage amplifier with enhancement mode load - gain magnitude

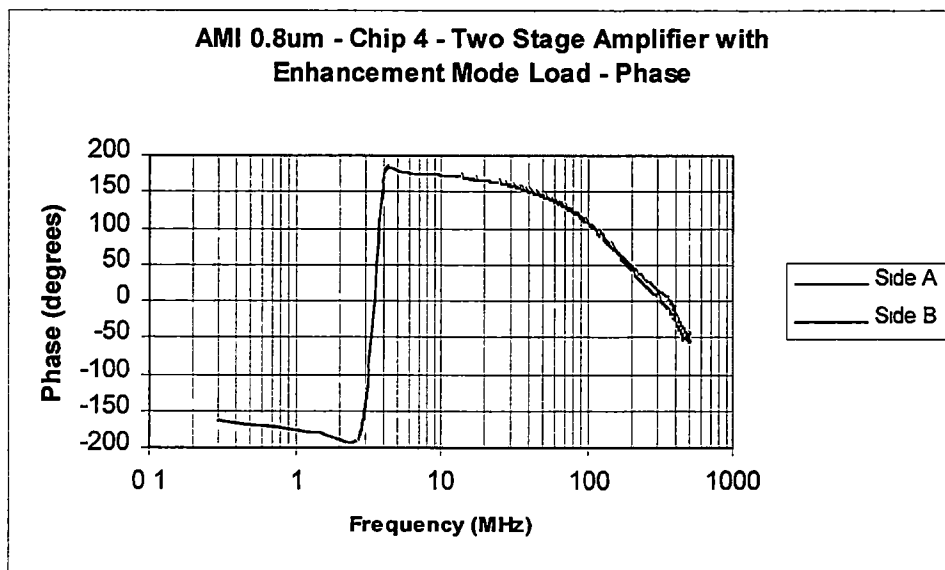


Figure 44 - AMI 0.8 um two-stage amplifier with enhancement mode load - phase

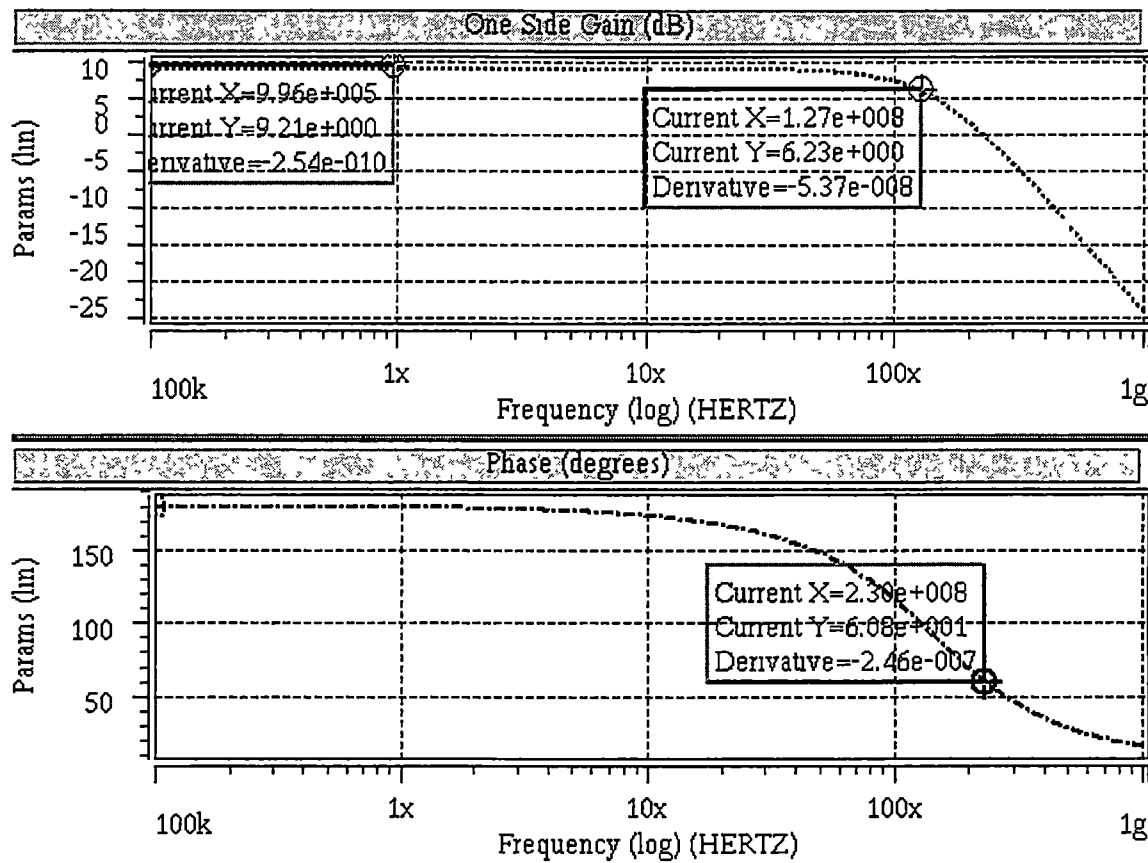


Figure 45 - HSpice simulation of frequency response for two-stage amplifier with enhancement mode load and 5 pF output load using AMI0.8 um N97L run BSIM3 models

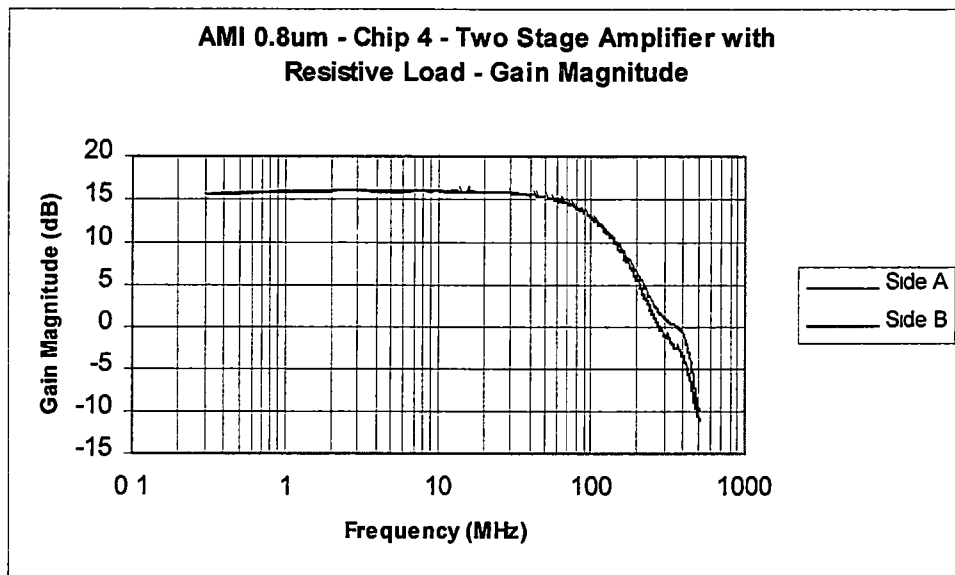


Figure 46 – AMI 0.8 um two-stage amplifier with resistive load - gain magnitude

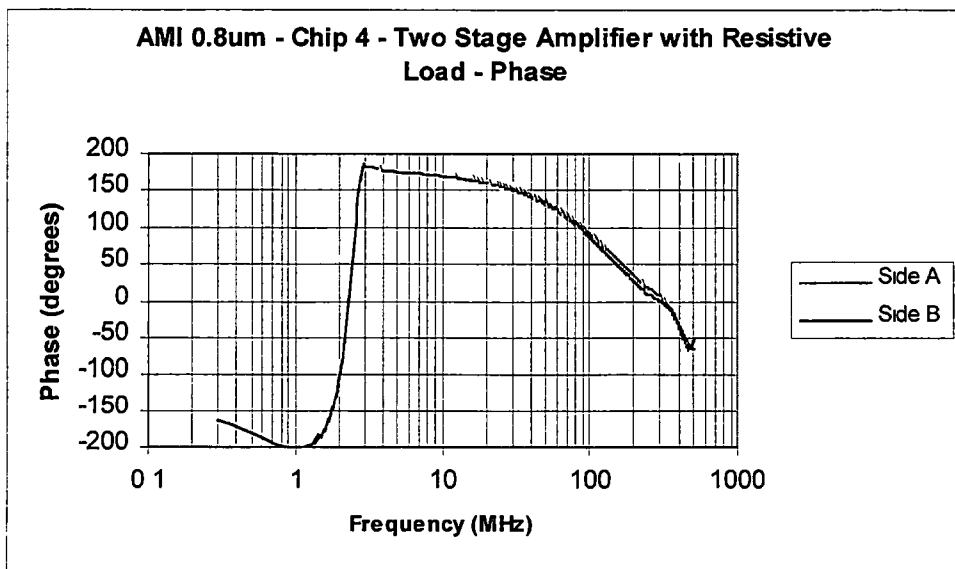


Figure 47 – AMI 0.8 um two-stage amplifier with resistive load - phase

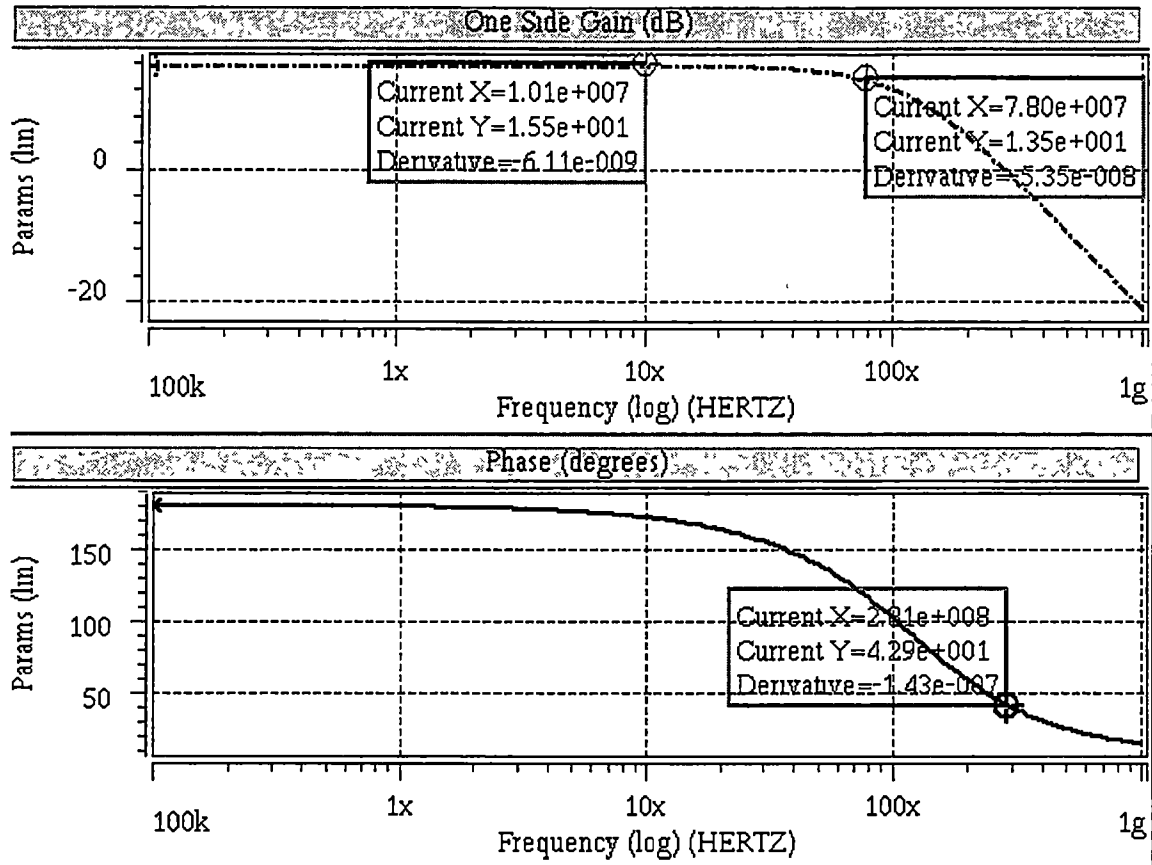


Figure 48 - HSpice simulation of frequency response for two-stage amplifier with resistive load and 5 pF output load using AMI 0.8 um N97L run BSIM3 models

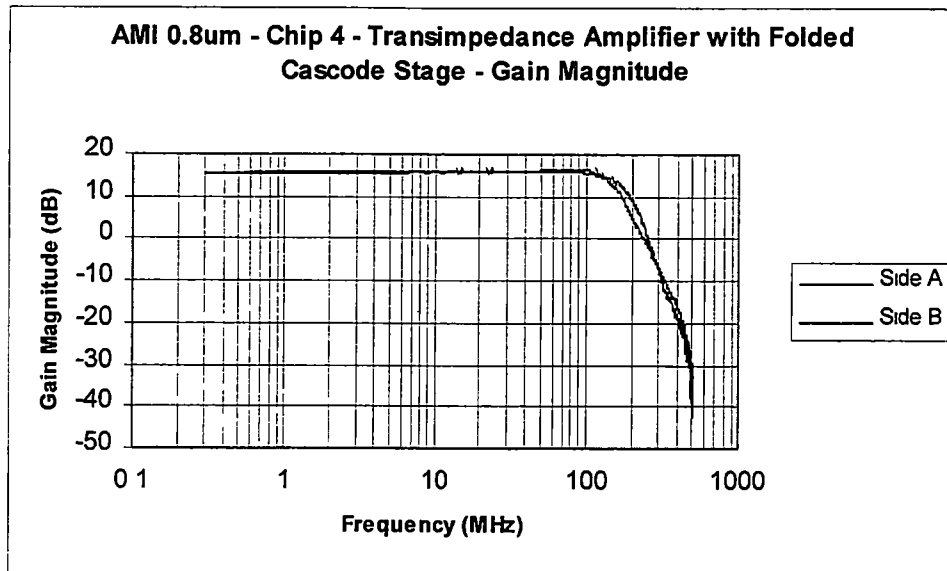


Figure 49 – AMI 0.8 um transimpedance amplifier with folded cascode stage - gain magnitude

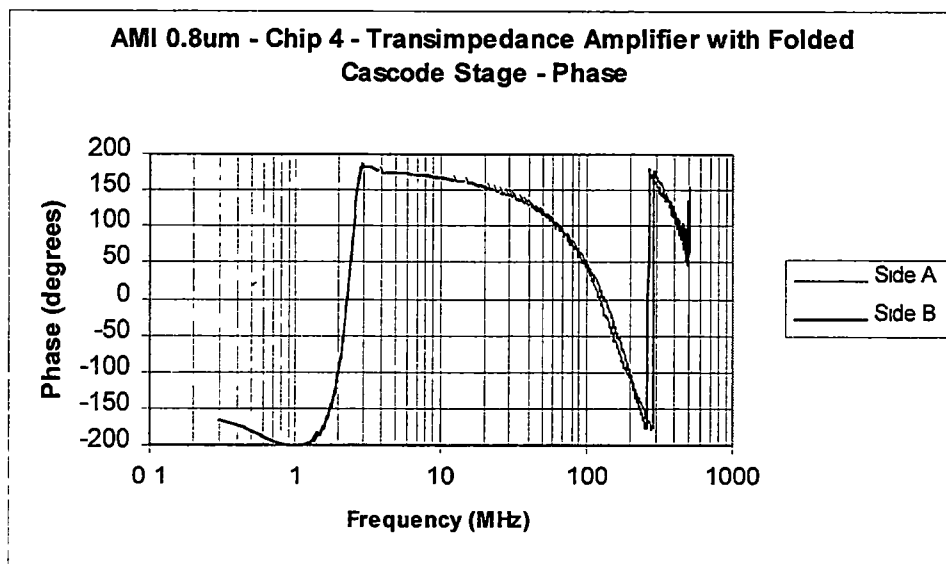


Figure 50 – AMI 0.8 um transimpedance amplifier with folded cascode stage - phase

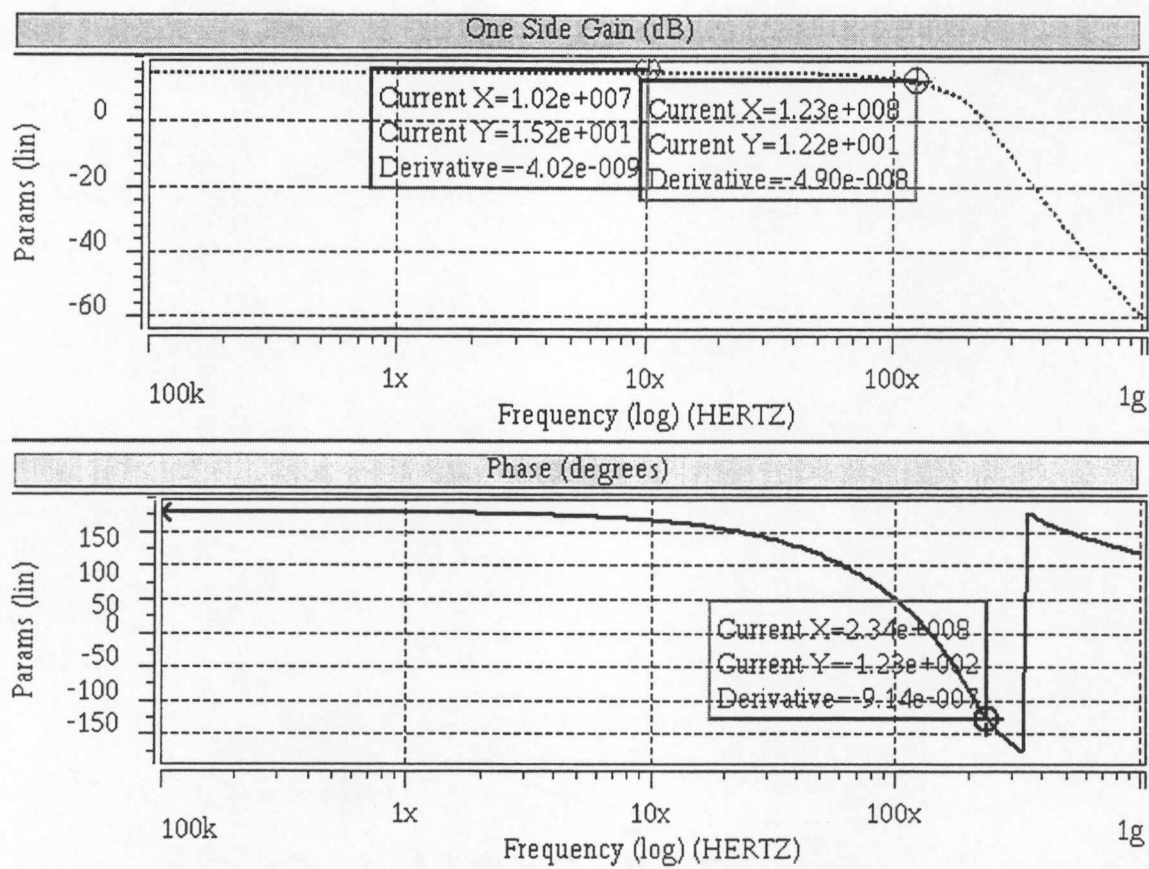


Figure 51 - HSpice simulation of frequency response for transimpedance amplifier with folded cascode stage and 5 pF output load using AMI 0.8 um N97L run BSIM3 models

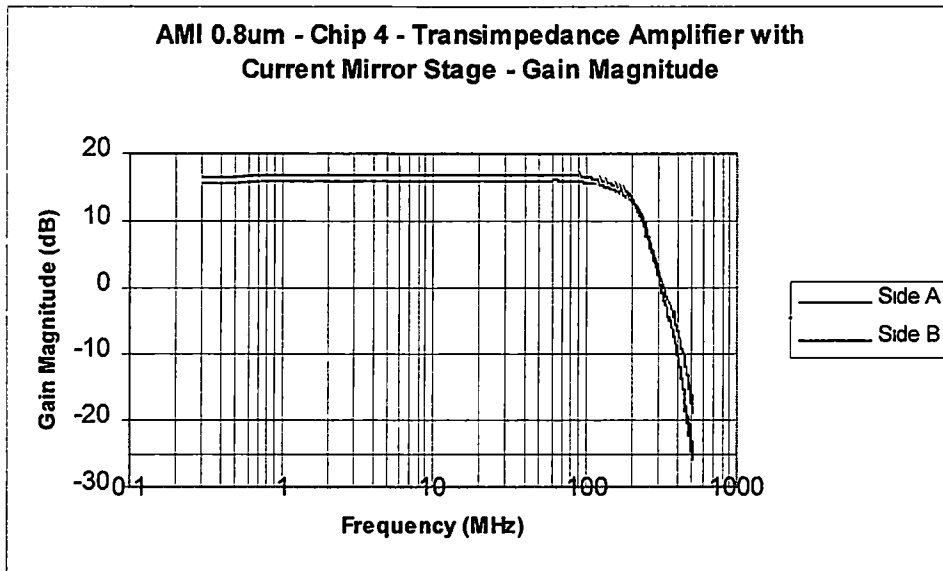


Figure 52 – AMI 0.8 um transimpedance amplifier with current mirror stage - gain magnitude

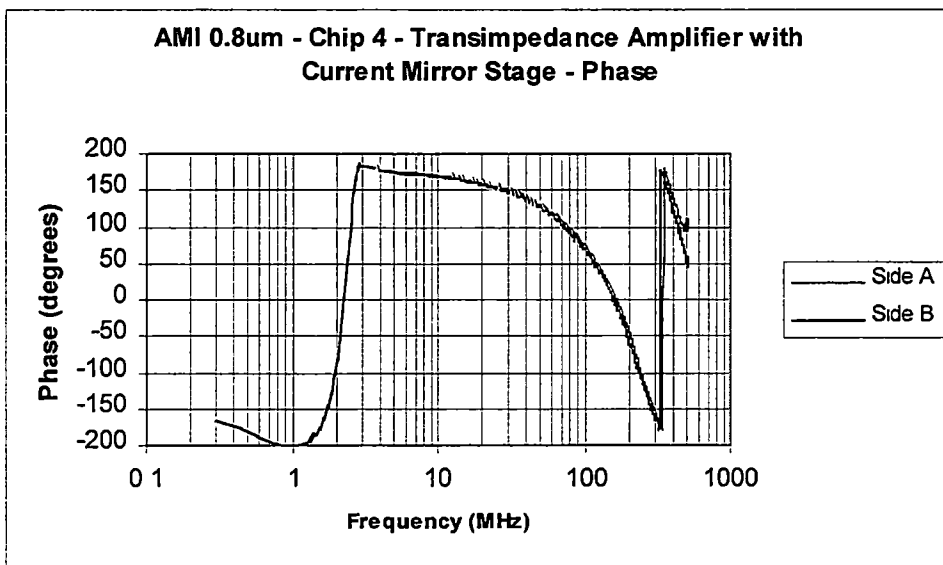


Figure 53 – AMI 0.8 um transimpedance amplifier with current mirror stage - phase

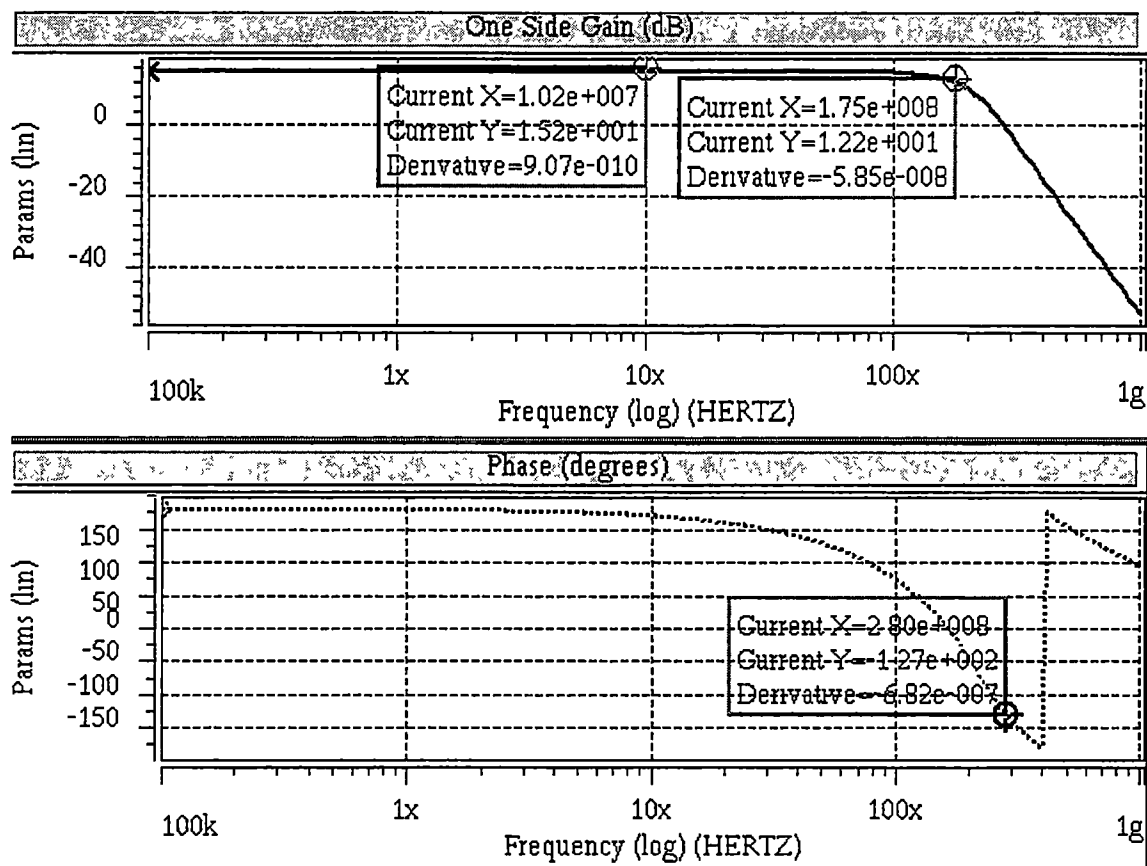


Figure 54 - HSpice simulation of frequency response for transimpedance amplifier with current mirror stage and 5 pF output load using AMI 0.8 um N97L run BSIM3 models

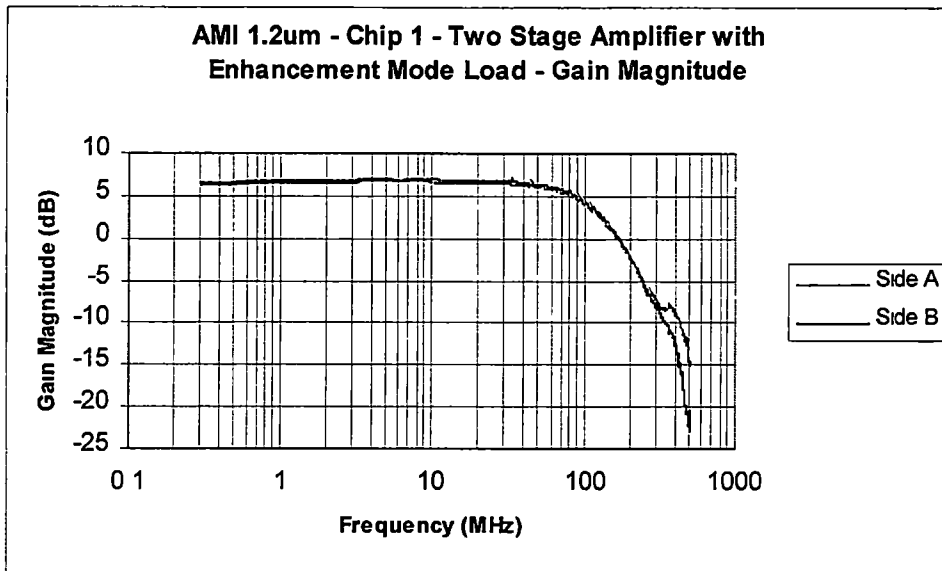


Figure 55 - AMI 1.2 um two-stage amplifier with enhancement mode load - gain magnitude

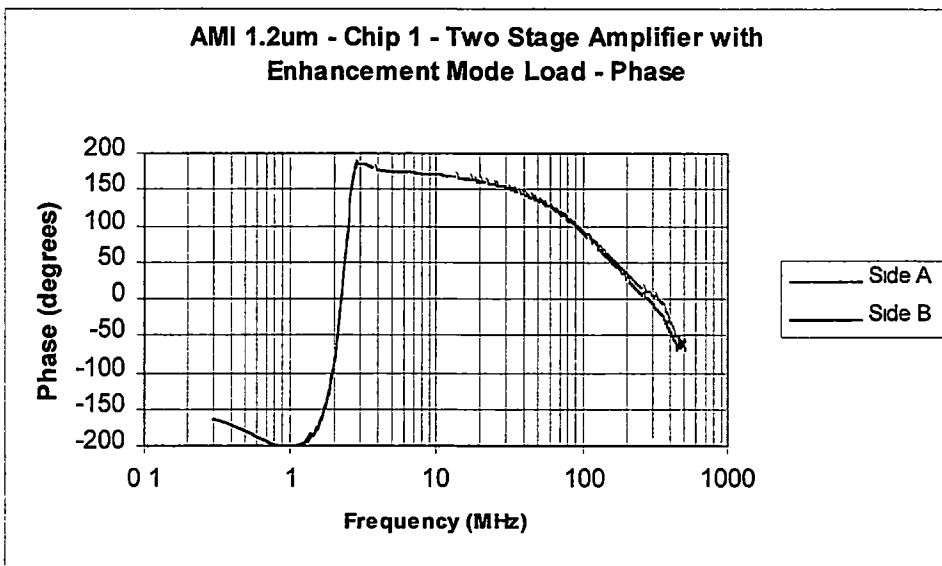


Figure 56 - AMI 1.2 um two-stage amplifier with enhancement mode load - phase

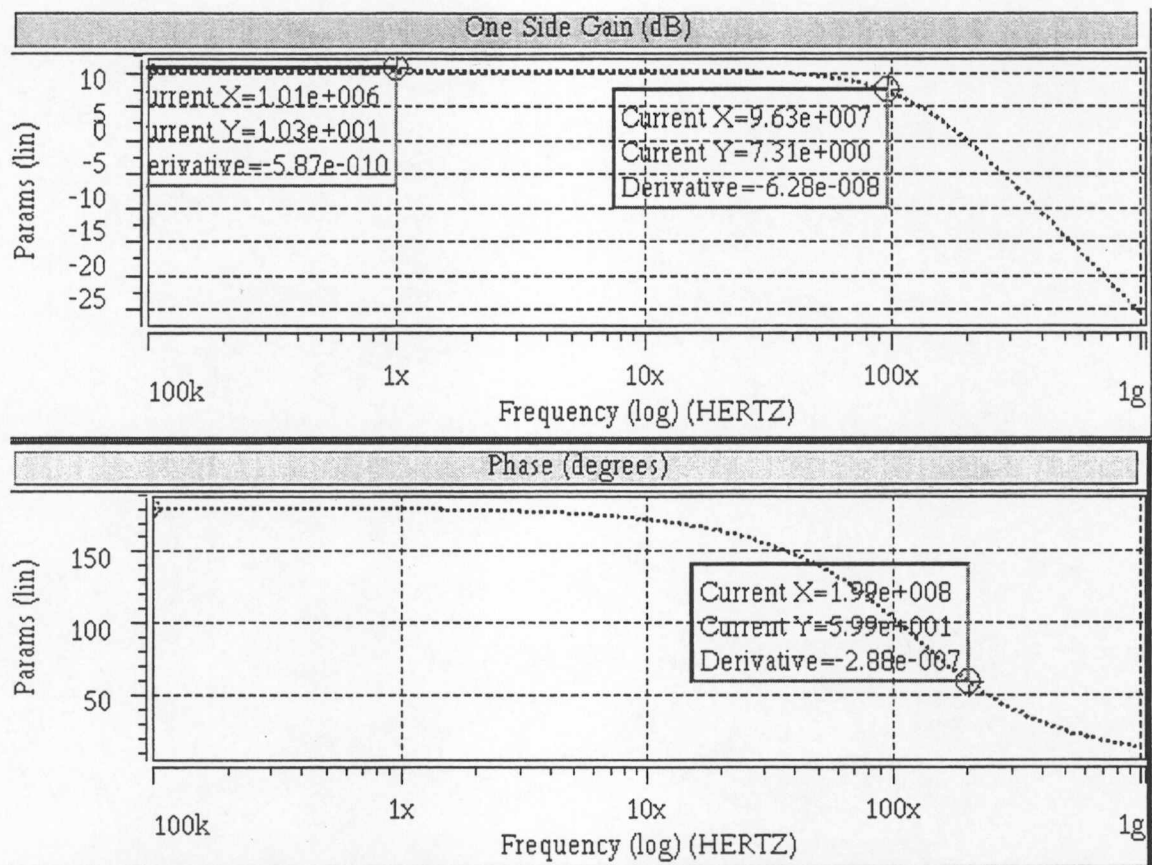


Figure 57 - HSpice simulation of frequency response for two-stage amplifier with enhancement mode load and 5 pF output load using AMI 1.2 um N95Y run BSIM3 models

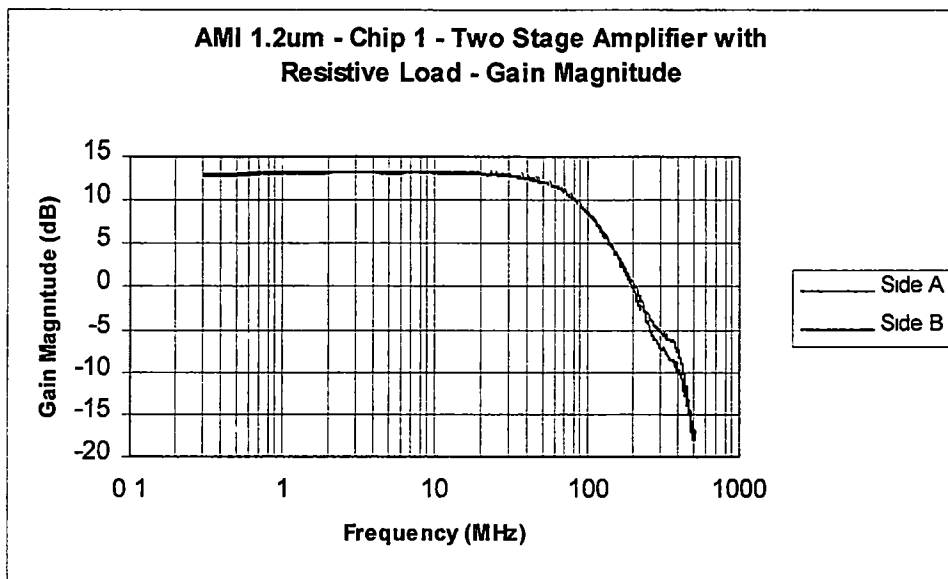


Figure 58 - AMI 1.2 um two-stage amplifier with resistive load - gain magnitude

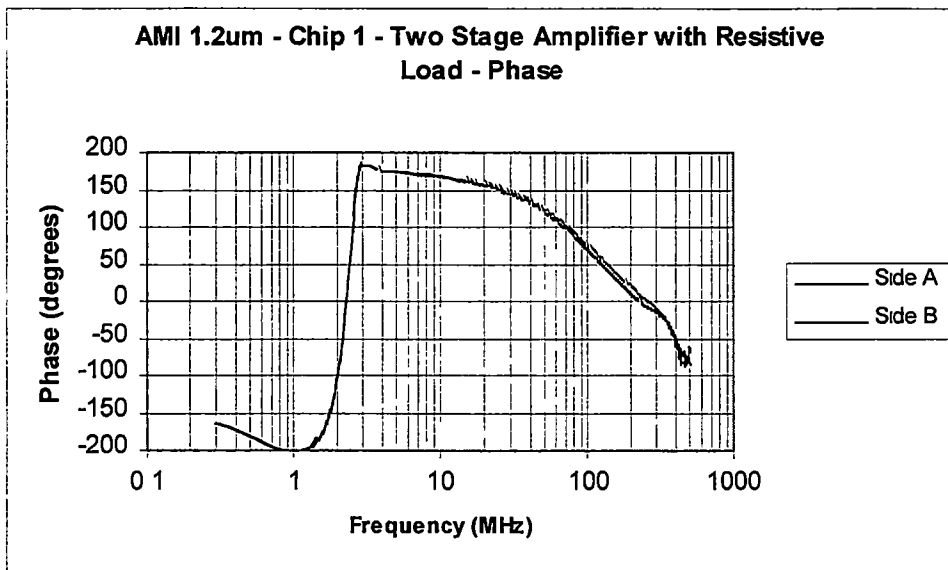


Figure 59 - AMI 1.2 um two-stage amplifier with resistive load - phase

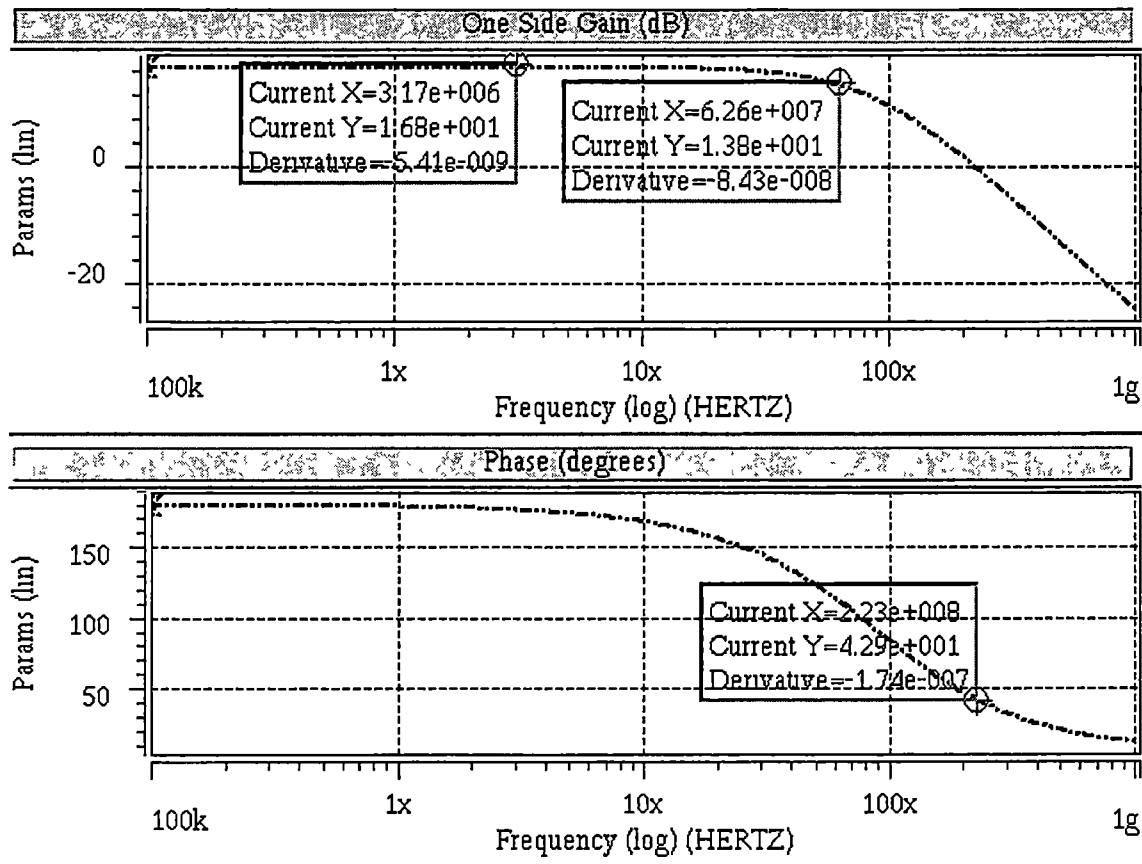


Figure 60 - HSpice simulation of frequency response for two-stage amplifier with resistive load and 5 pF output load using AMI 1.2 um N95Y run BSIM3 models

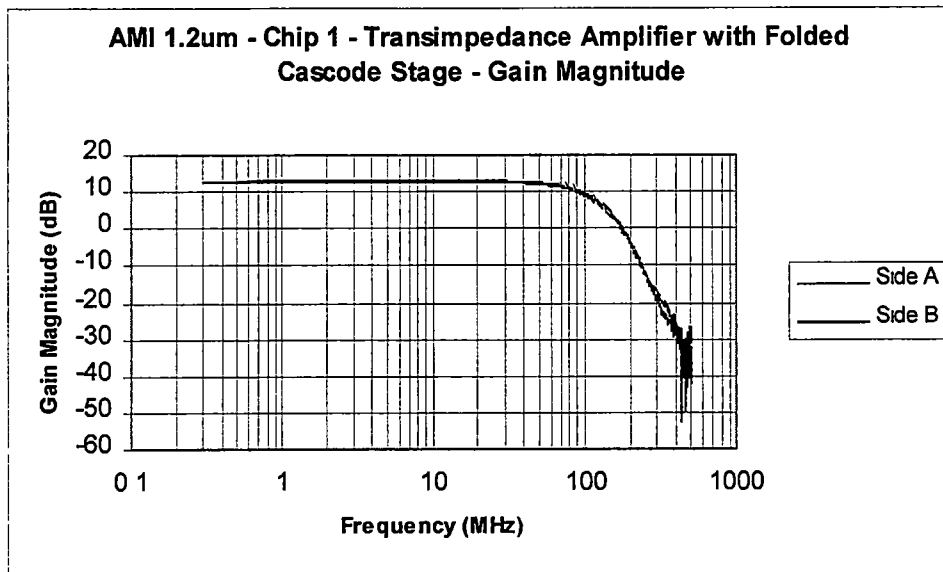


Figure 61 - AMI 1.2 um transimpedance amplifier with folded cascode stage - gain magnitude

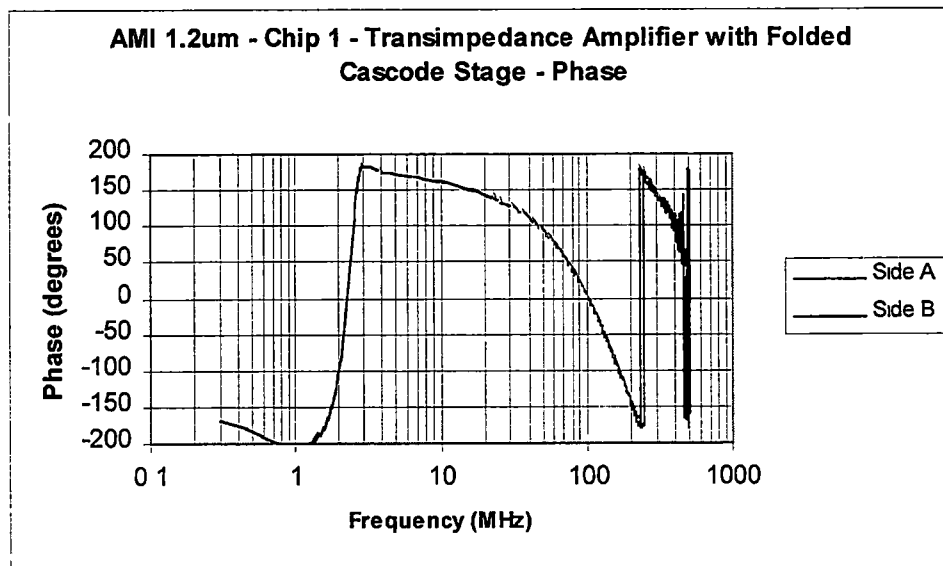


Figure 62 - AMI 1.2 um transimpedance amplifier with folded cascode stage - phase

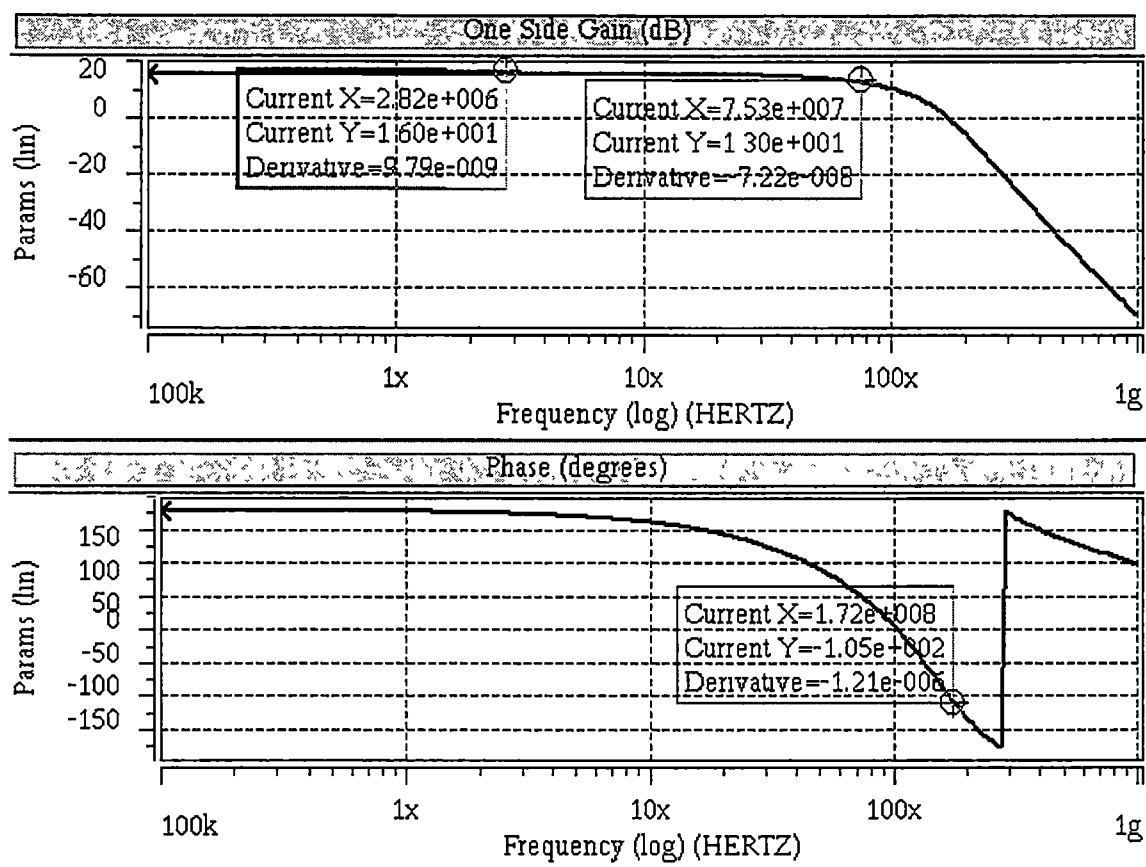


Figure 63 - HSpice simulation of frequency response for transimpedance amplifier with folded cascode stage and 5 pF output load using AMI 1.2 um N95Y run BSIM3 models

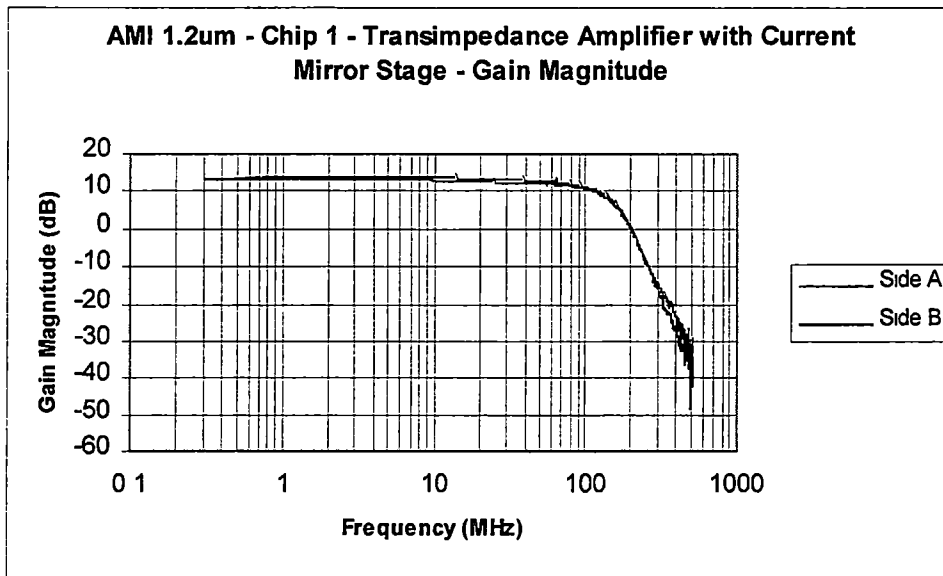


Figure 64 - AMI 1.2 um transimpedance amplifier with current mirror stage - gain magnitude

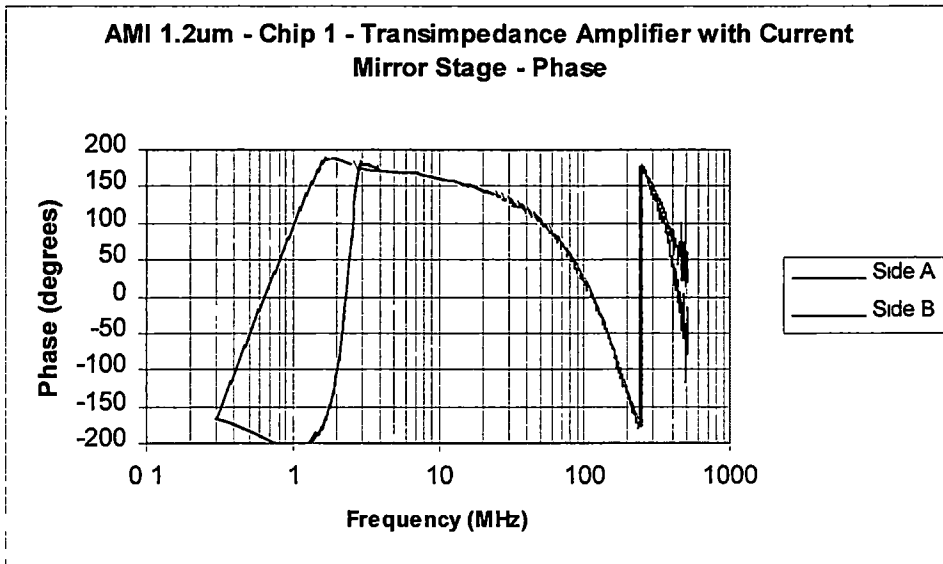


Figure 65 - AMI 1.2 um transimpedance amplifier with current mirror stage - phase

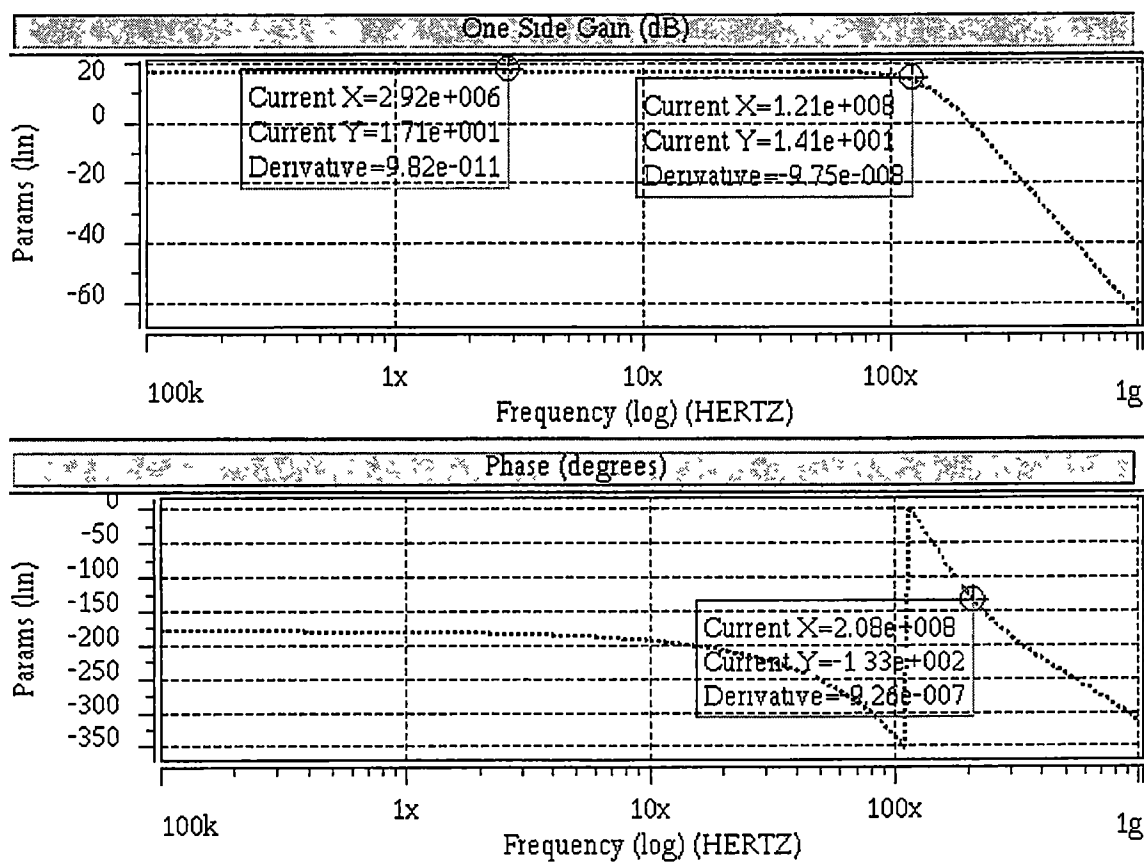


Figure 66 - HSpice simulation of frequency response for transimpedance amplifier with current mirror stage and 5 pF output load using AMI 1.2 um N95Y run BSIM3 models

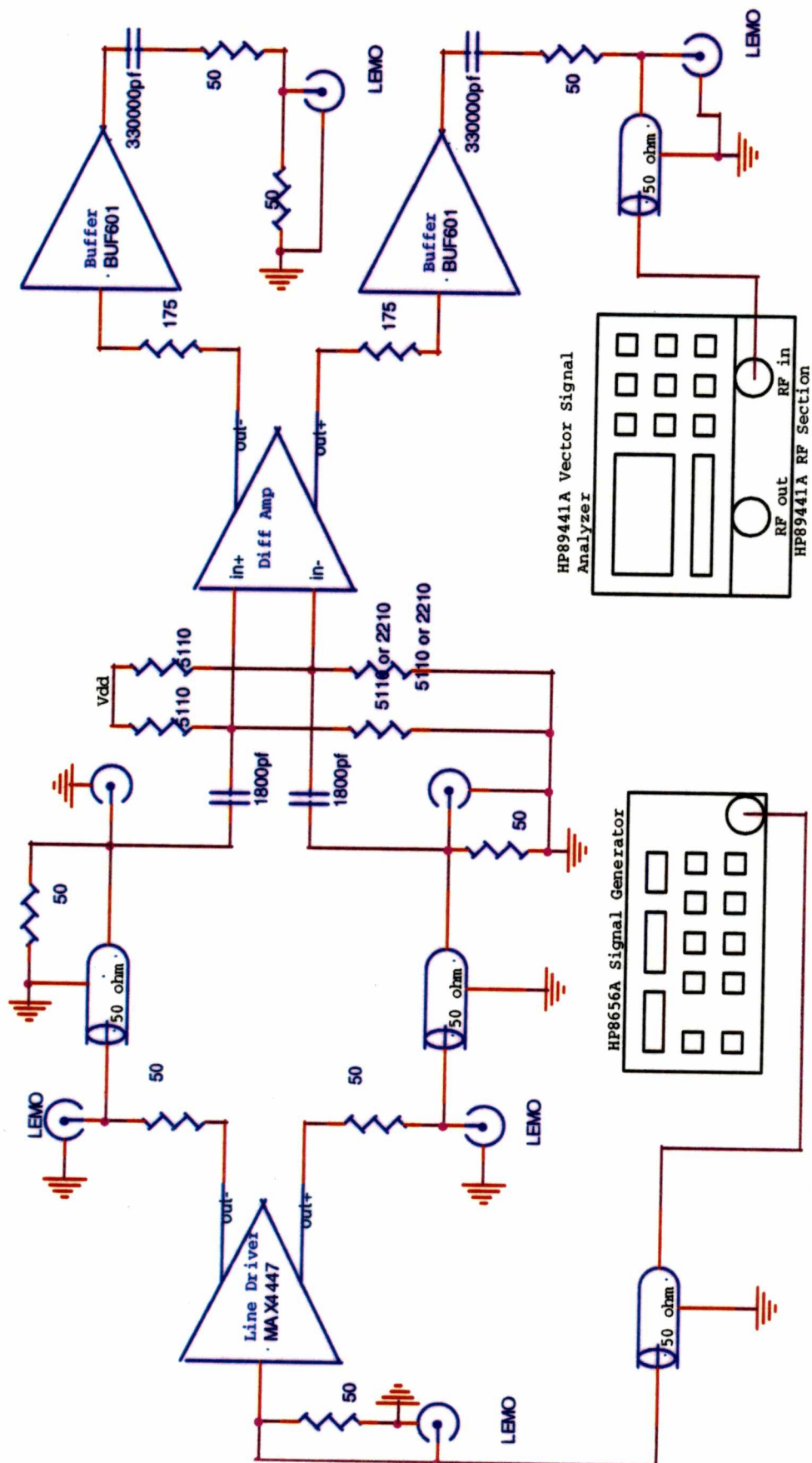


Figure 67 - Test setup for measuring gain compression

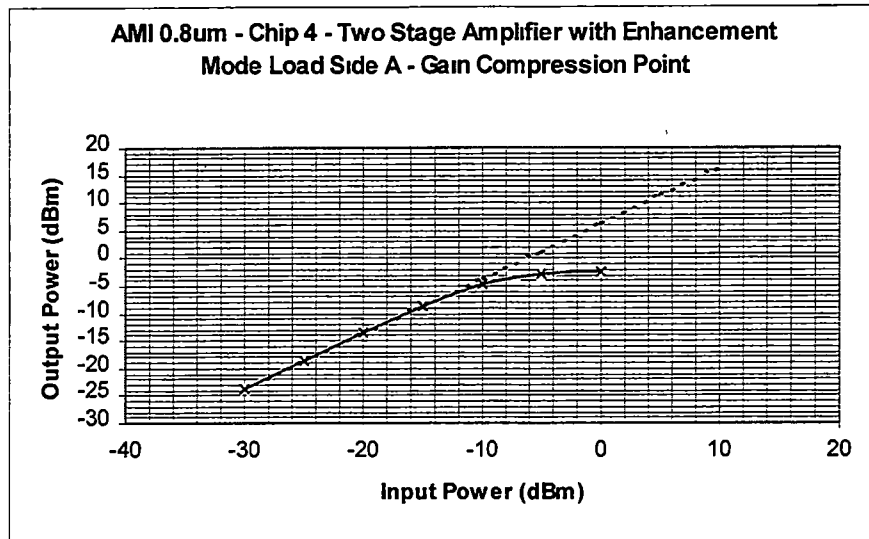


Figure 68 – AMI 0.8 μ m two stage amplifier with enhancement mode load side A – gain compression point data at 100 MHz

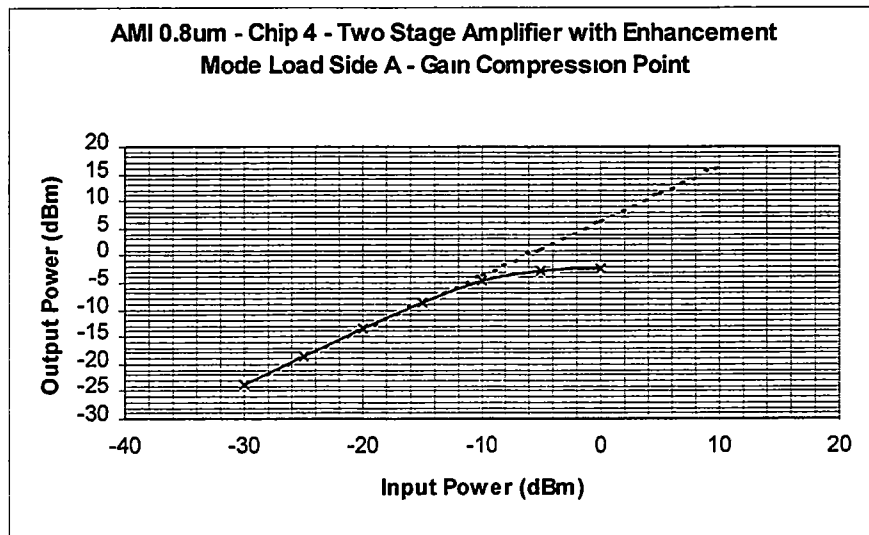


Figure 69 - AMI 0.8 μ m two stage amplifier with enhancement mode load side B – gain compression point data at 100 MHz

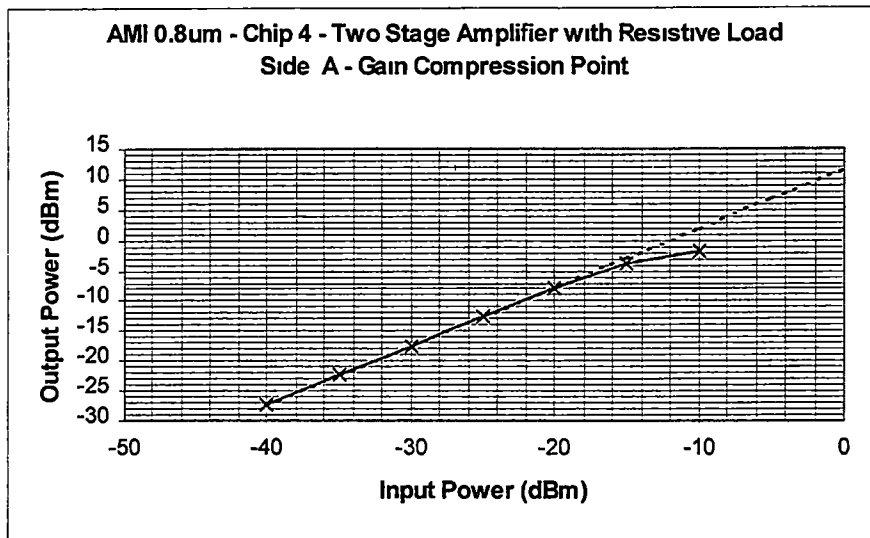


Figure 70 - AMI 0.8 um two stage amplifier with resistive load side A – gain compression point data at 100 MHz

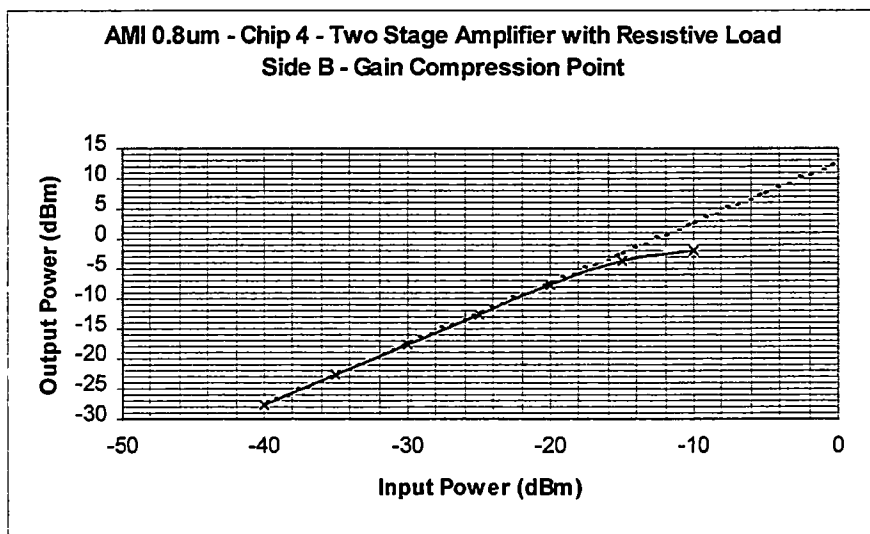


Figure 71 - AMI 0.8 um two stage amplifier with resistive load side B – gain compression point data at 100 MHz

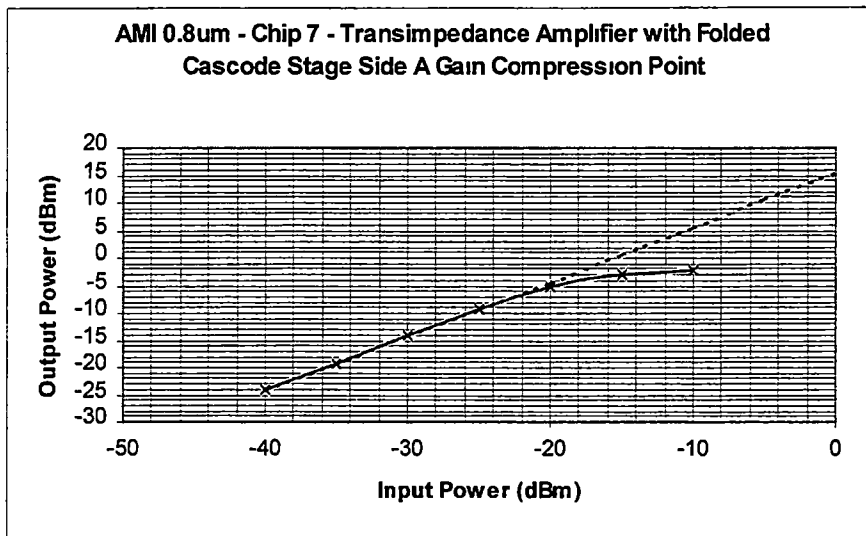


Figure 72 - AMI 0.8 um transimpedance amplifier with folded cascode stage side A – gain compression point data at 100 MHz

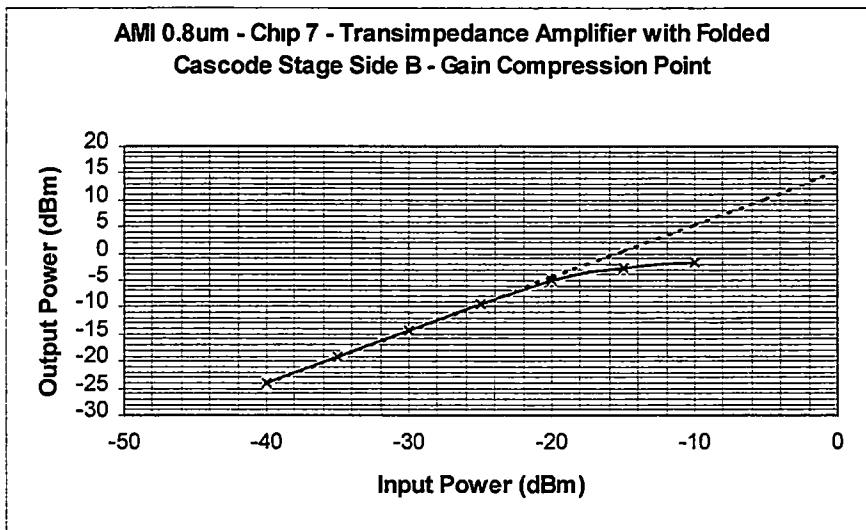


Figure 73 - AMI 0.8 um transimpedance amplifier with folded cascode stage side B – gain compression point data at 100 MHz

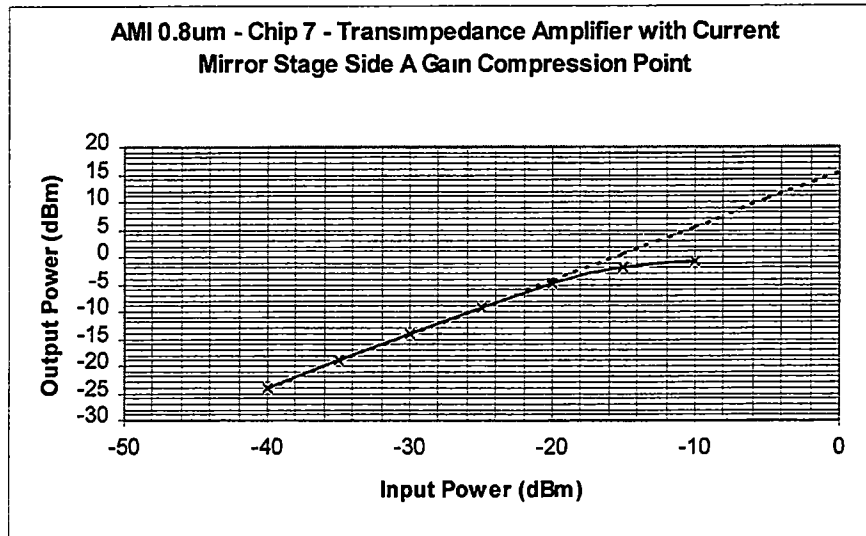


Figure 74 - AMI 0.8 um transimpedance amplifier with current mirror stage side A – gain compression point data at 100 MHz

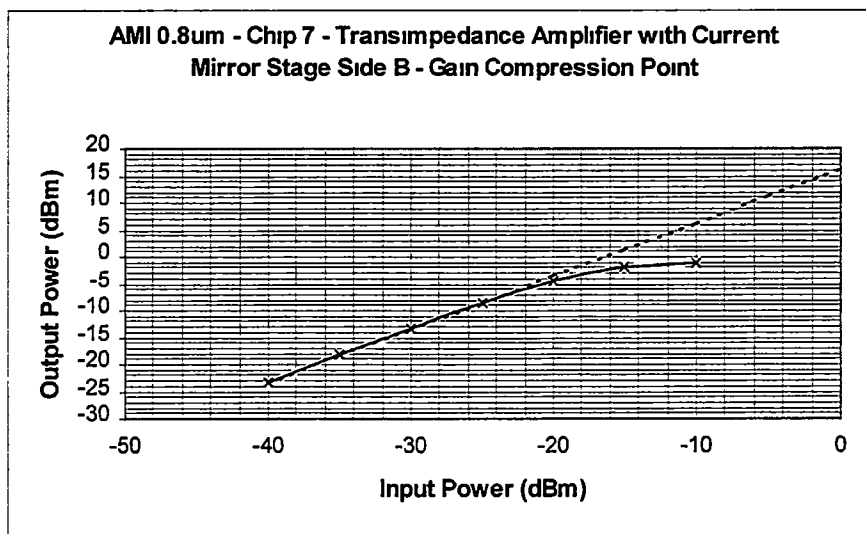


Figure 75 - - AMI 0.8 um transimpedance amplifier with current mirror stage side B – gain compression point data at 100 MHz

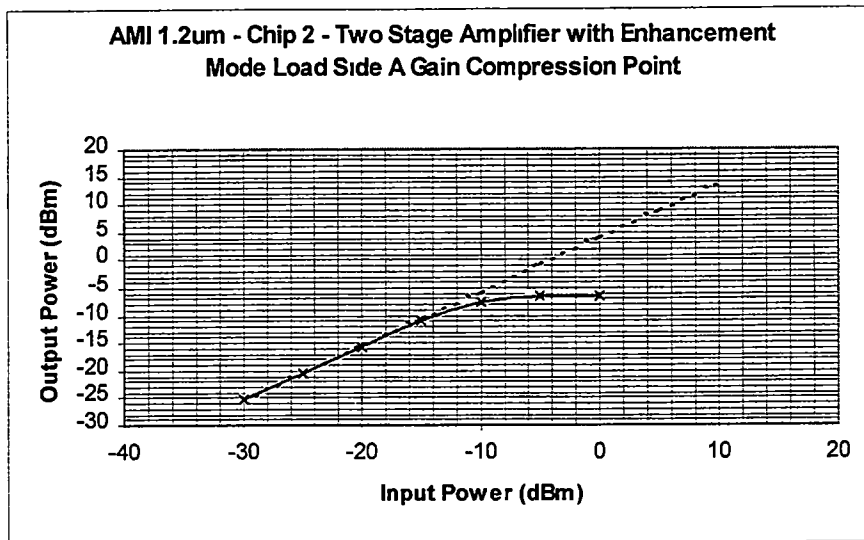


Figure 76 - AMI 1.2 um two stage amplifier with enhancement mode load side A – gain compression point data at 100 MHz

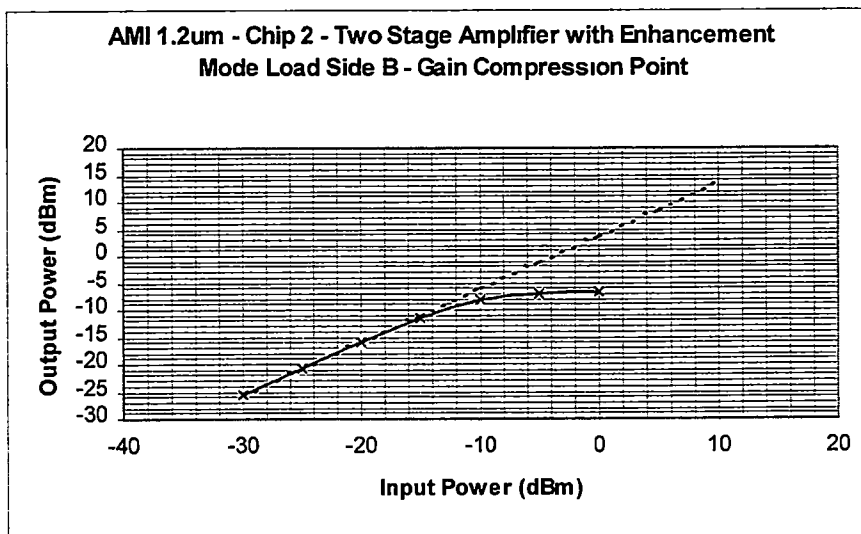


Figure 77 - AMI 1.2 um two stage amplifier with enhancement mode load side B – gain compression point data at 100 MHz

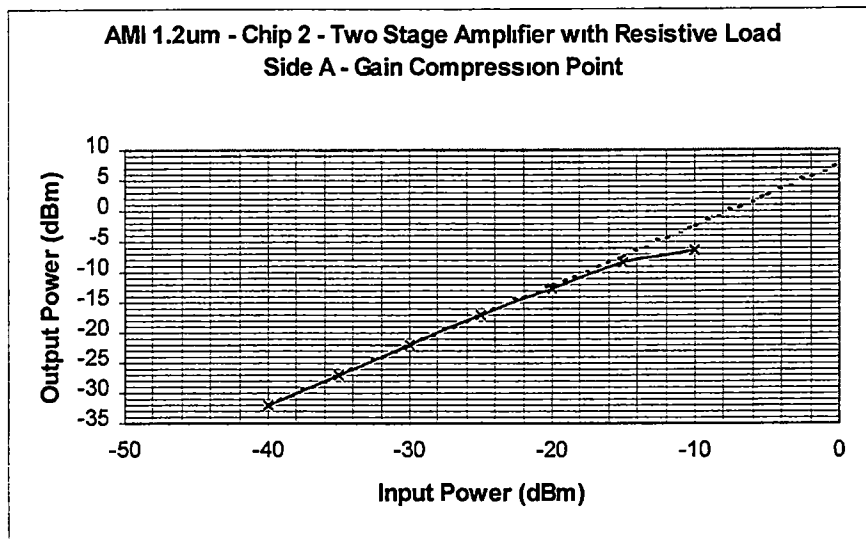


Figure 78 - AMI 1.2 um two stage amplifier with resistive load side A – gain compression point data at 100 MHz

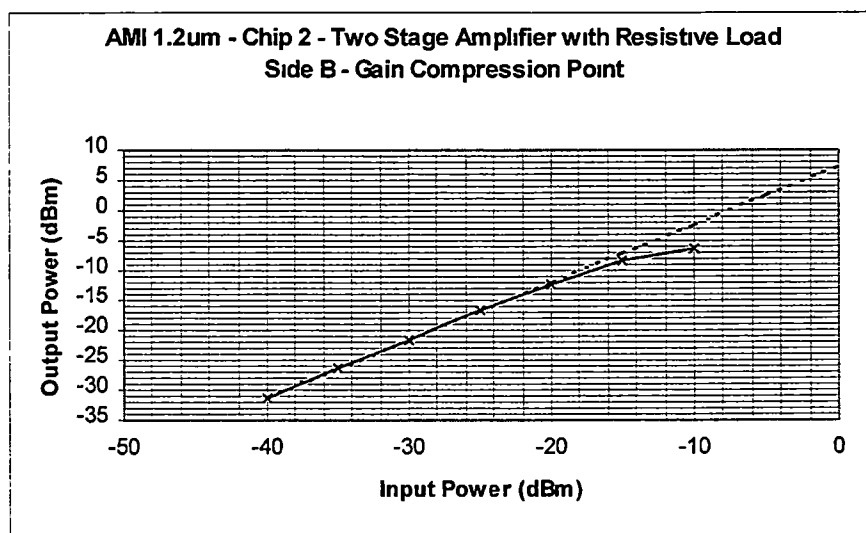


Figure 79 - AMI 1.2 um two stage amplifier with resistive load side B – gain compression point data at 100 MHz

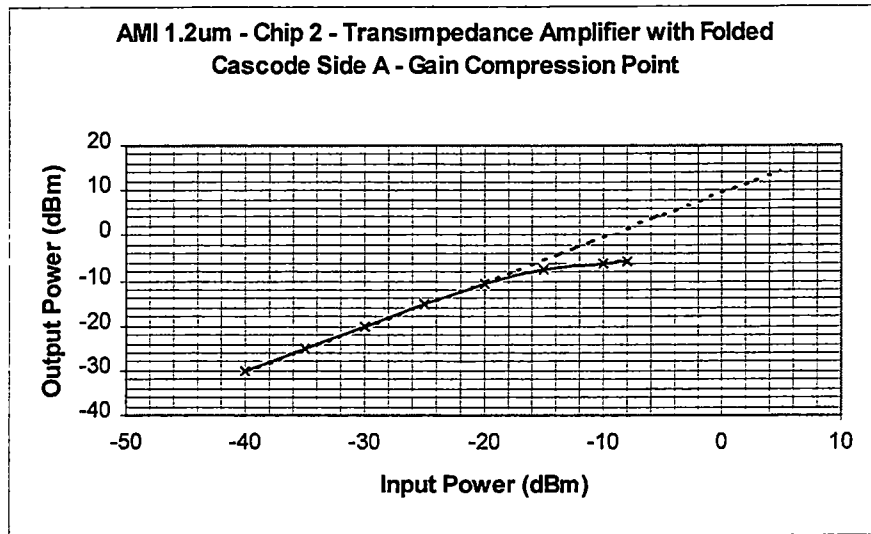


Figure 80 - AMI 1.2 um transimpedance amplifier with folded cascode stage side A – gain compression point data at 100 MHz

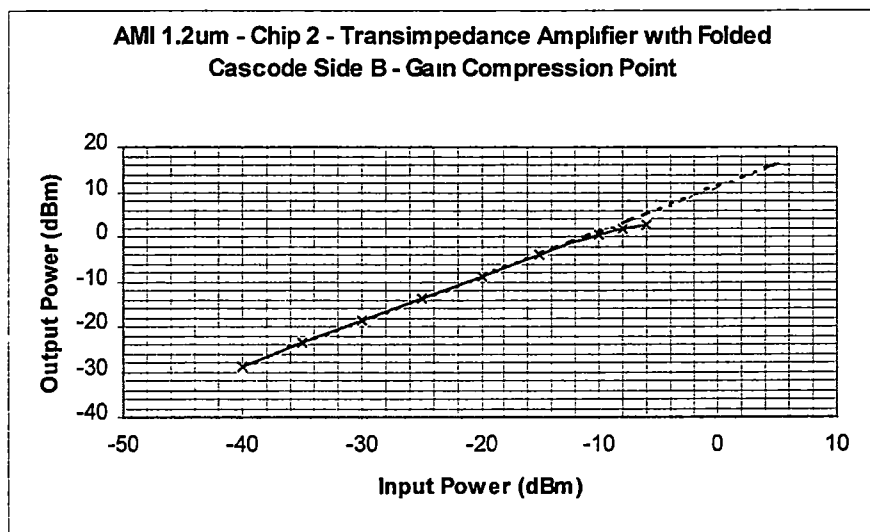


Figure 81 - AMI 1.2 um transimpedance amplifier with folded cascode stage side B – gain compression point data at 100 MHz

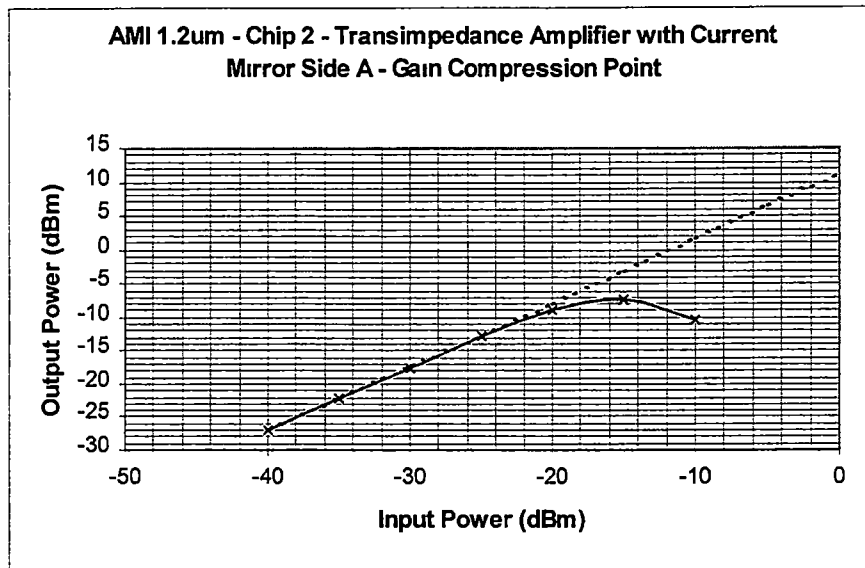


Figure 82 - AMI 0.8 um transimpedance amplifier with current mirror stage side A – gain compression point data at 100 MHz

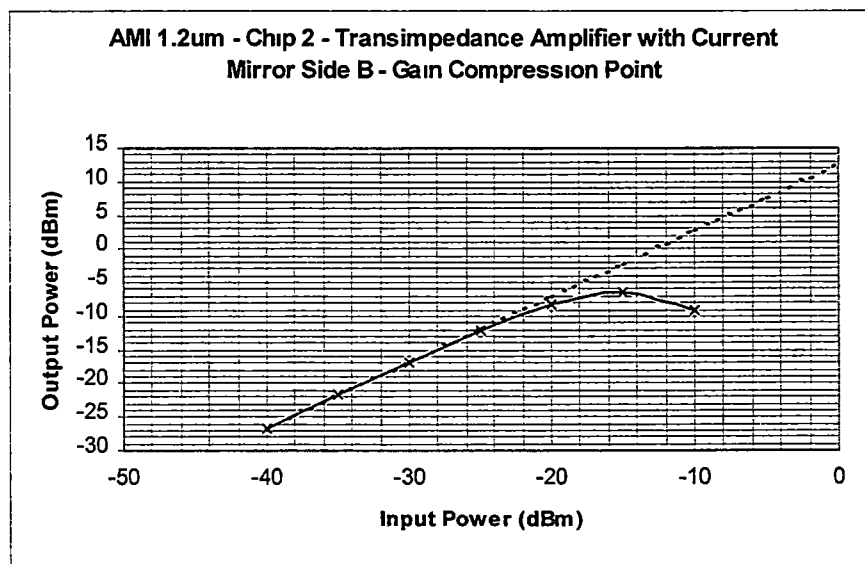


Figure 83 - AMI 0.8 um transimpedance amplifier with current mirror stage side B – gain compression point data at 100 MHz

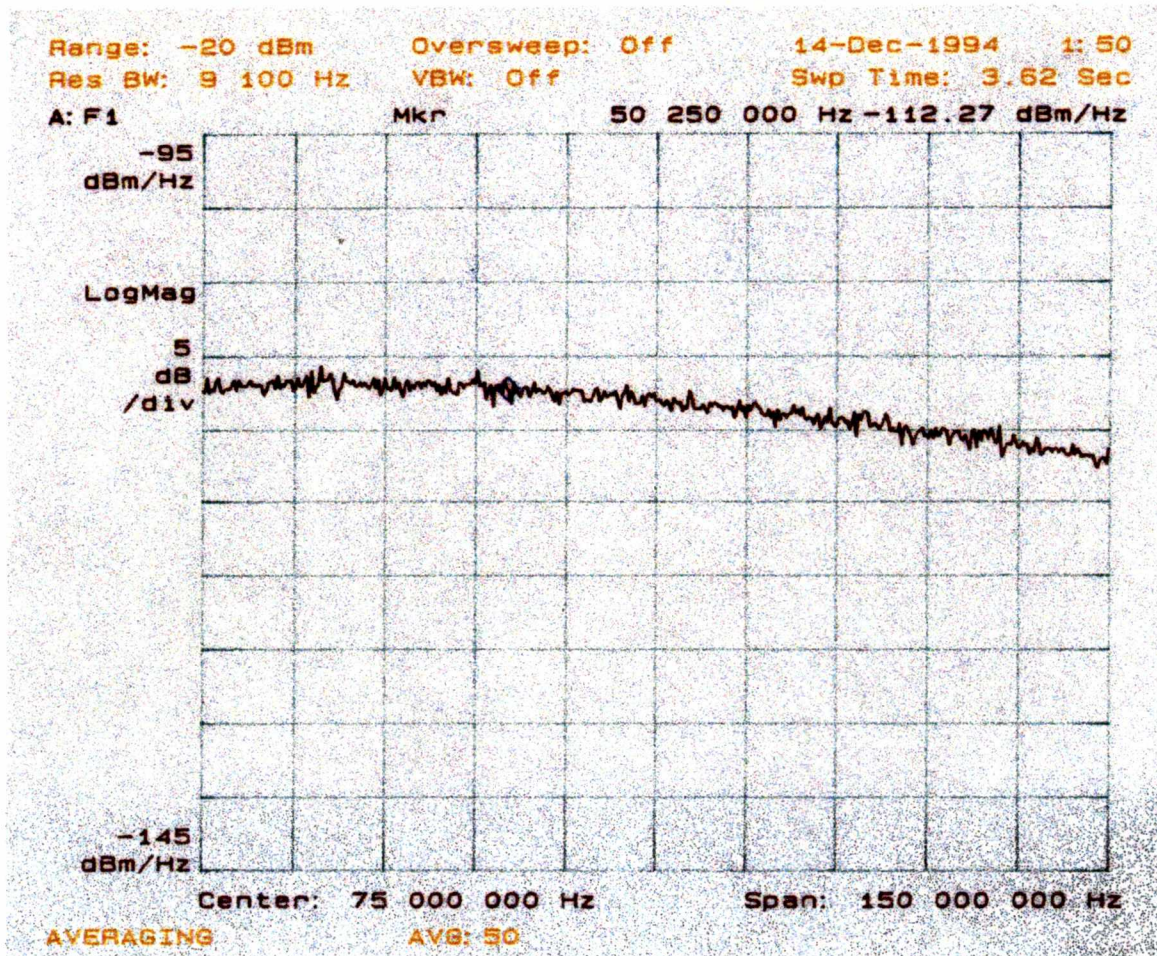


Figure 85 – Rush-Kennedy amplifier noise measurement

Range: -20 dBm Oversweep: On 29-Dec-1994 19:19
Res BW: 17 000 Hz VSW: Off Swp Time: 260.8 mSec

A: D1 Mkr 75 000 000 Hz -104.32 dBm/Hz

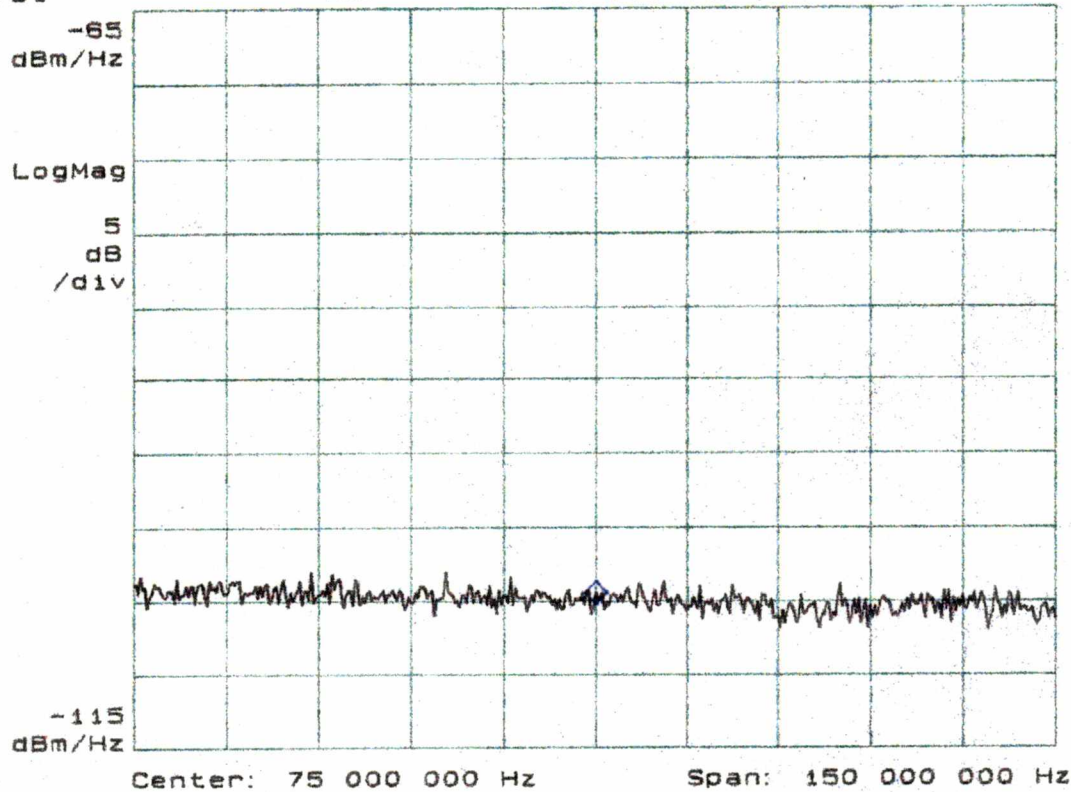


Figure 86 - Noise measurement of buffer

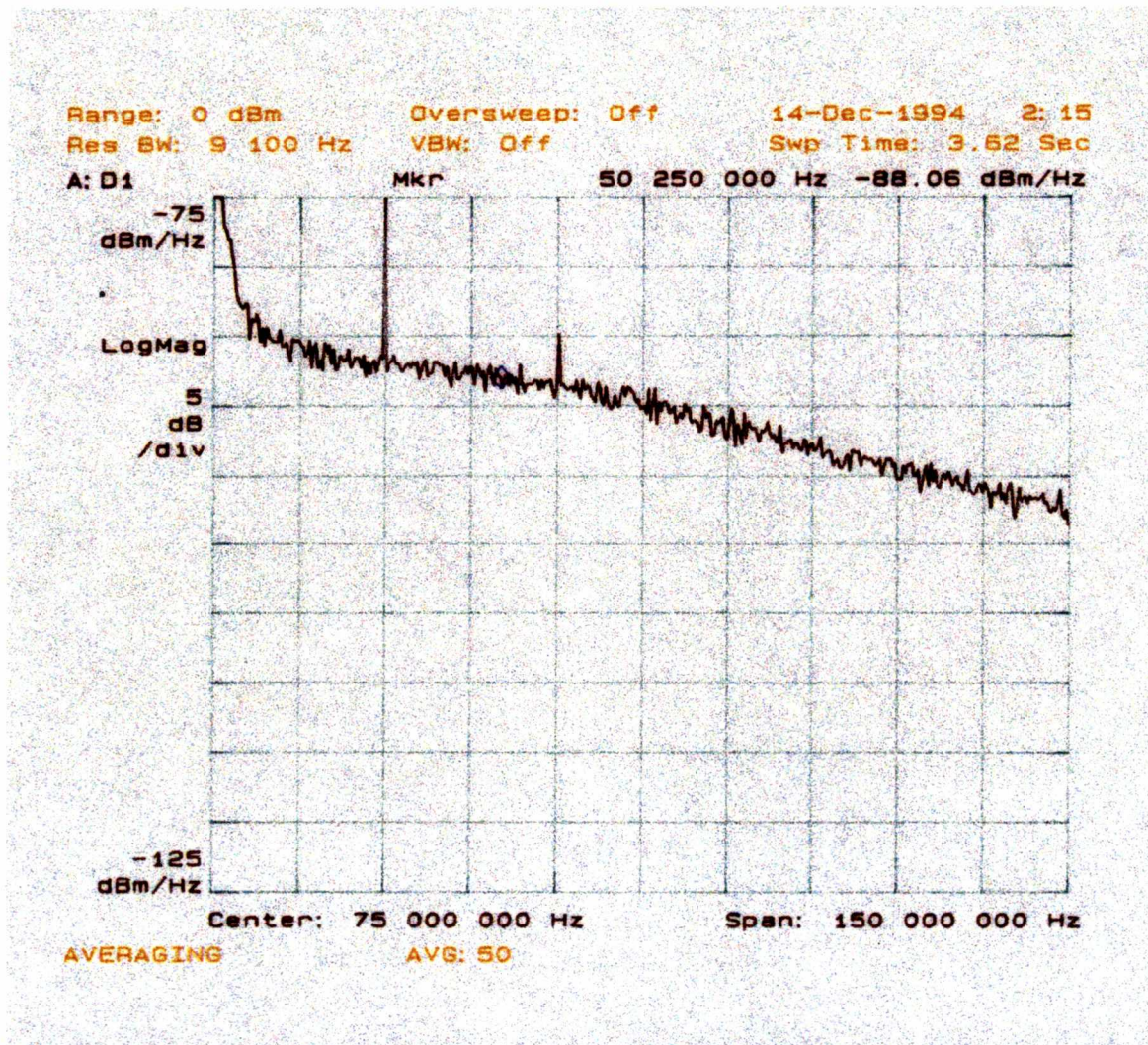


Figure 87 – AMI 0.8 um two stage amplifier with enhancement mode load – noise measurement

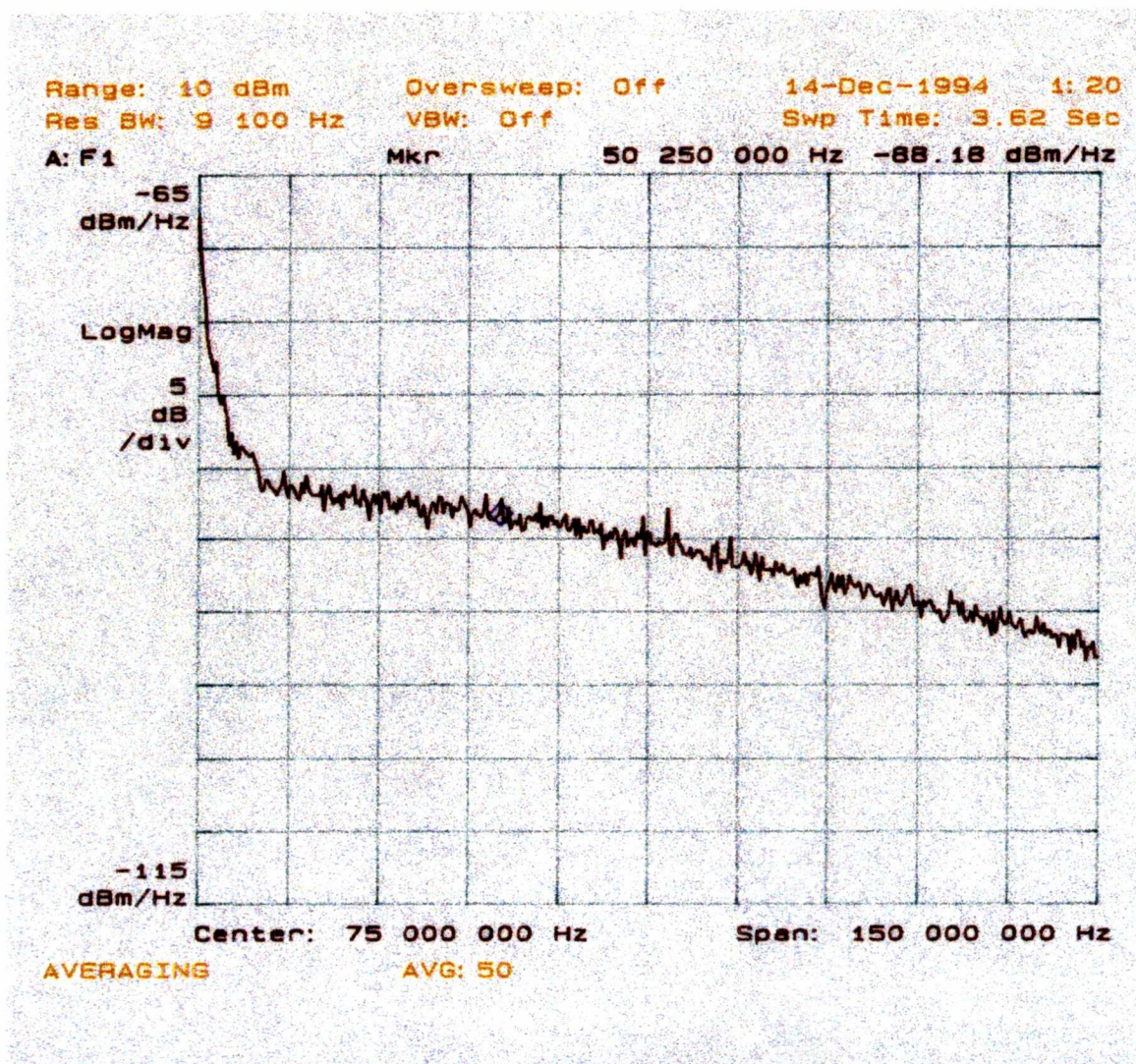


Figure 88 - AMI 0.8 μ m two stage amplifier with resistive load – noise measurement

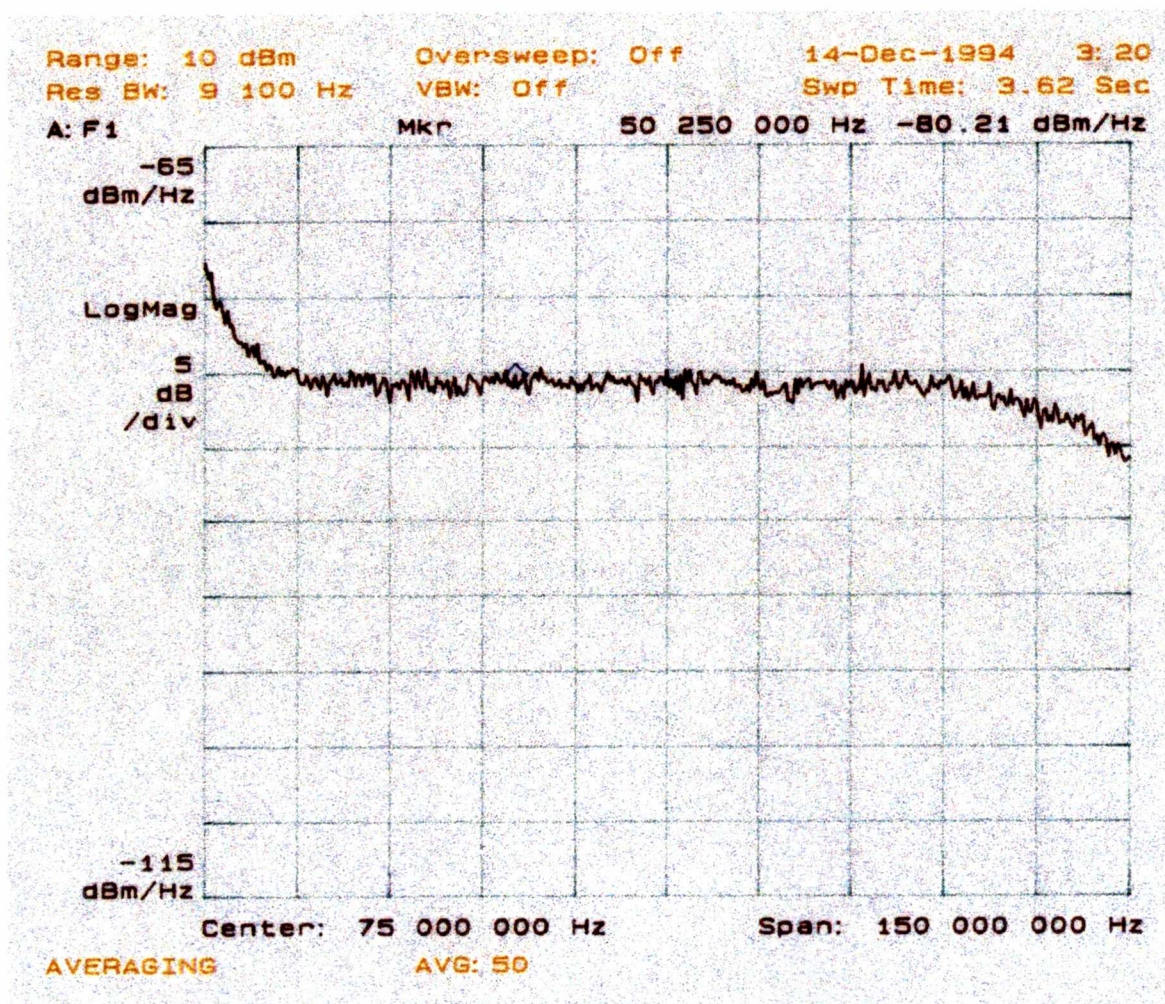


Figure 89 - AMI 0.8 um transimpedance amplifier with folded cascode stage – noise measurement

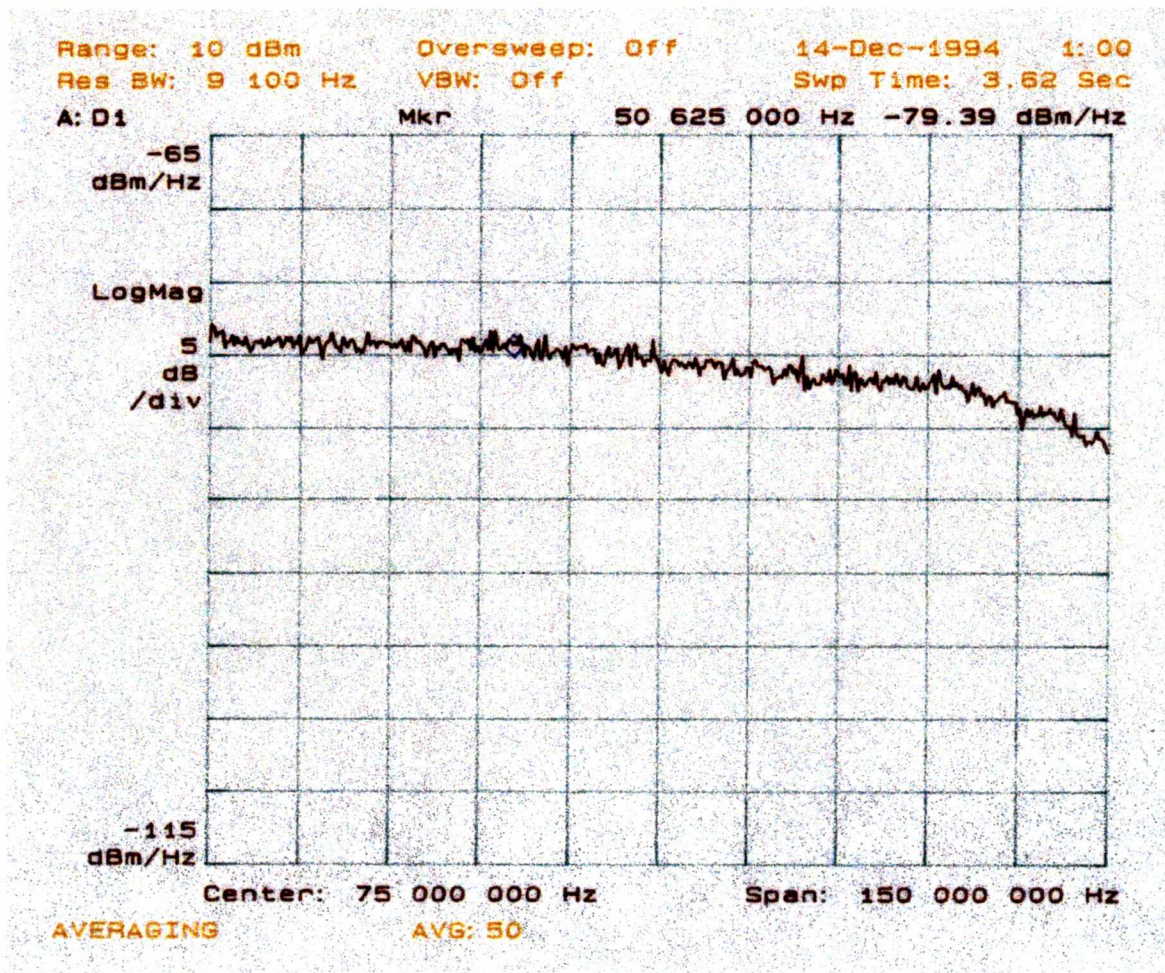


Figure 90 - AMI 0.8 um transimpedance amplifier with current mirror stage – noise measurement

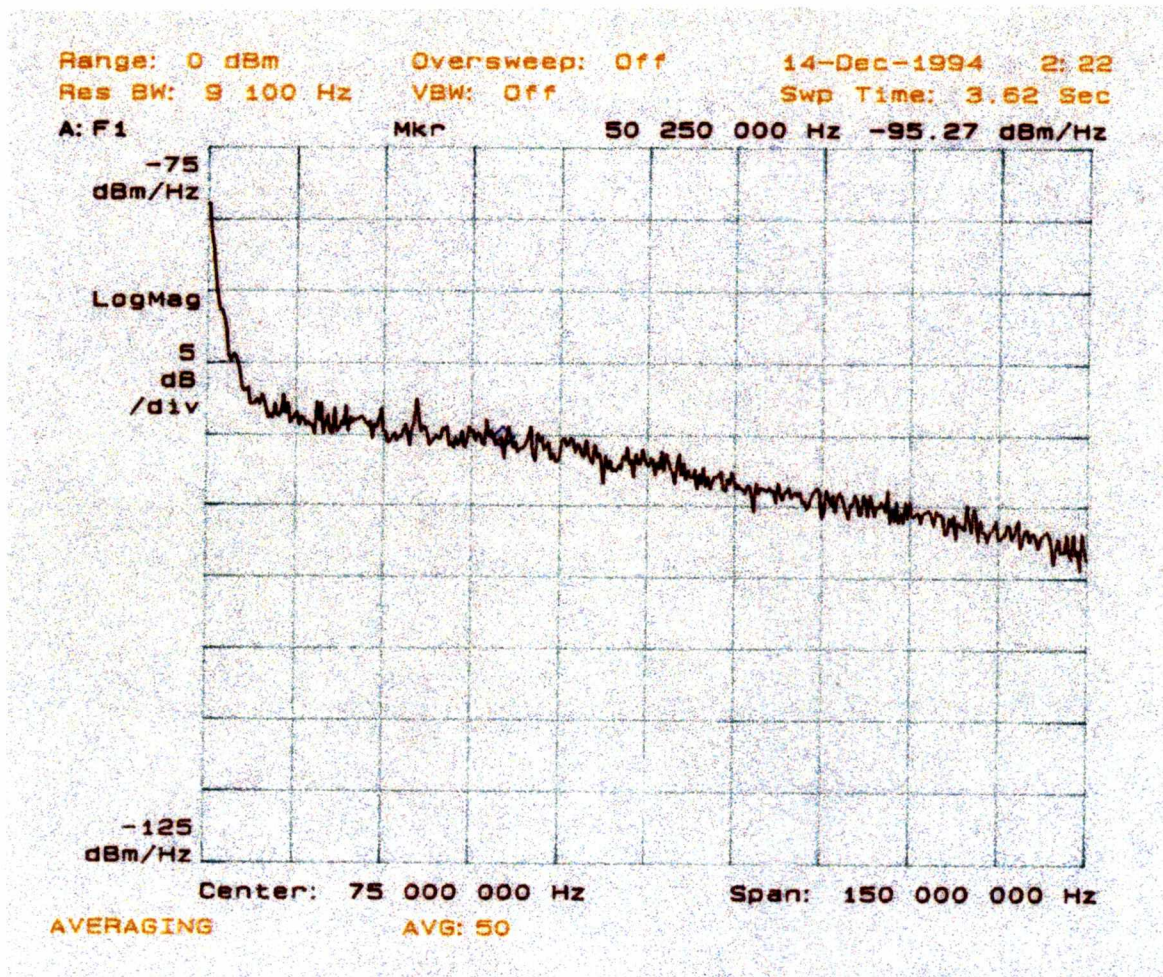


Figure 91 – AMI 1.2um two stage amplifier with enhancement mode load – noise measurement

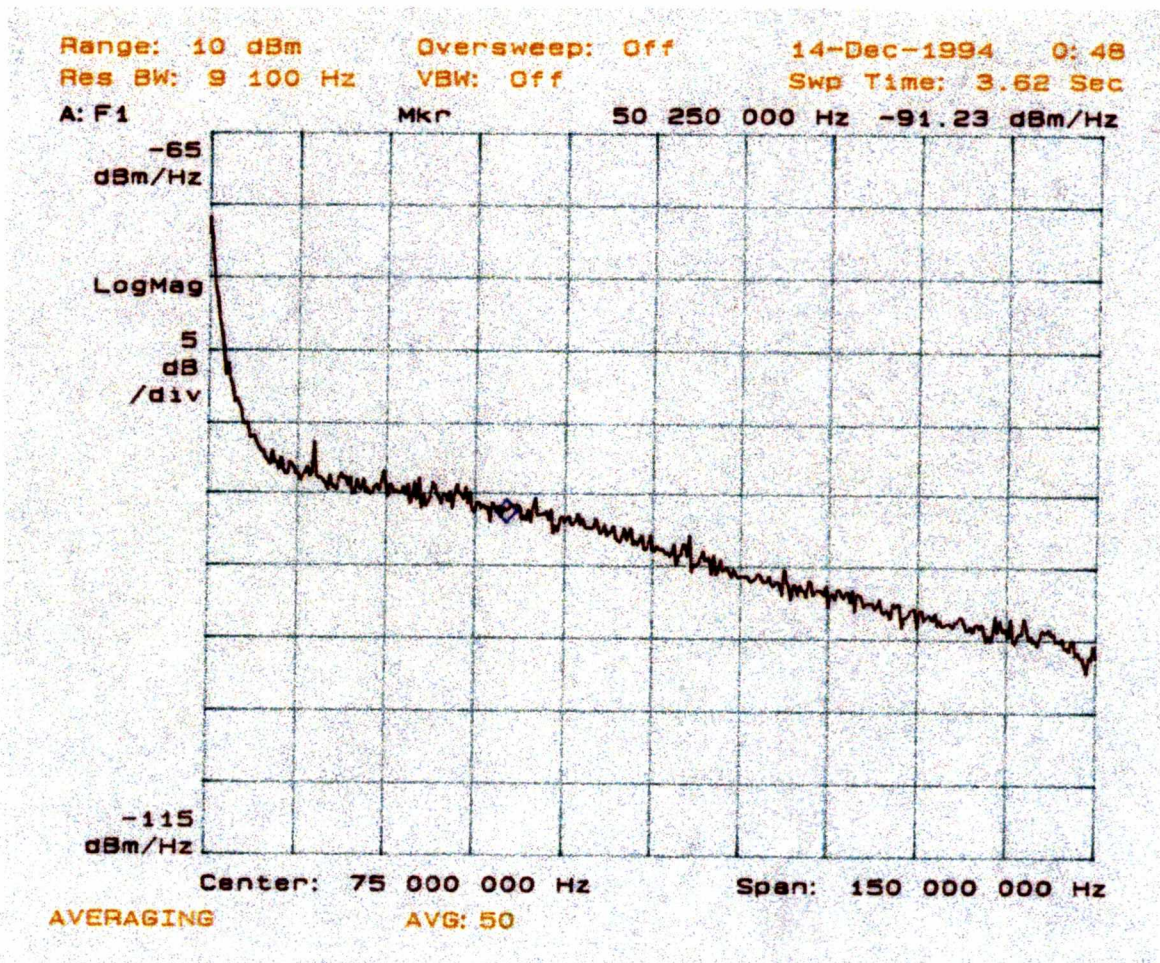


Figure 92 - AMI 1.2 um two stage amplifier with resistive load – noise measurement

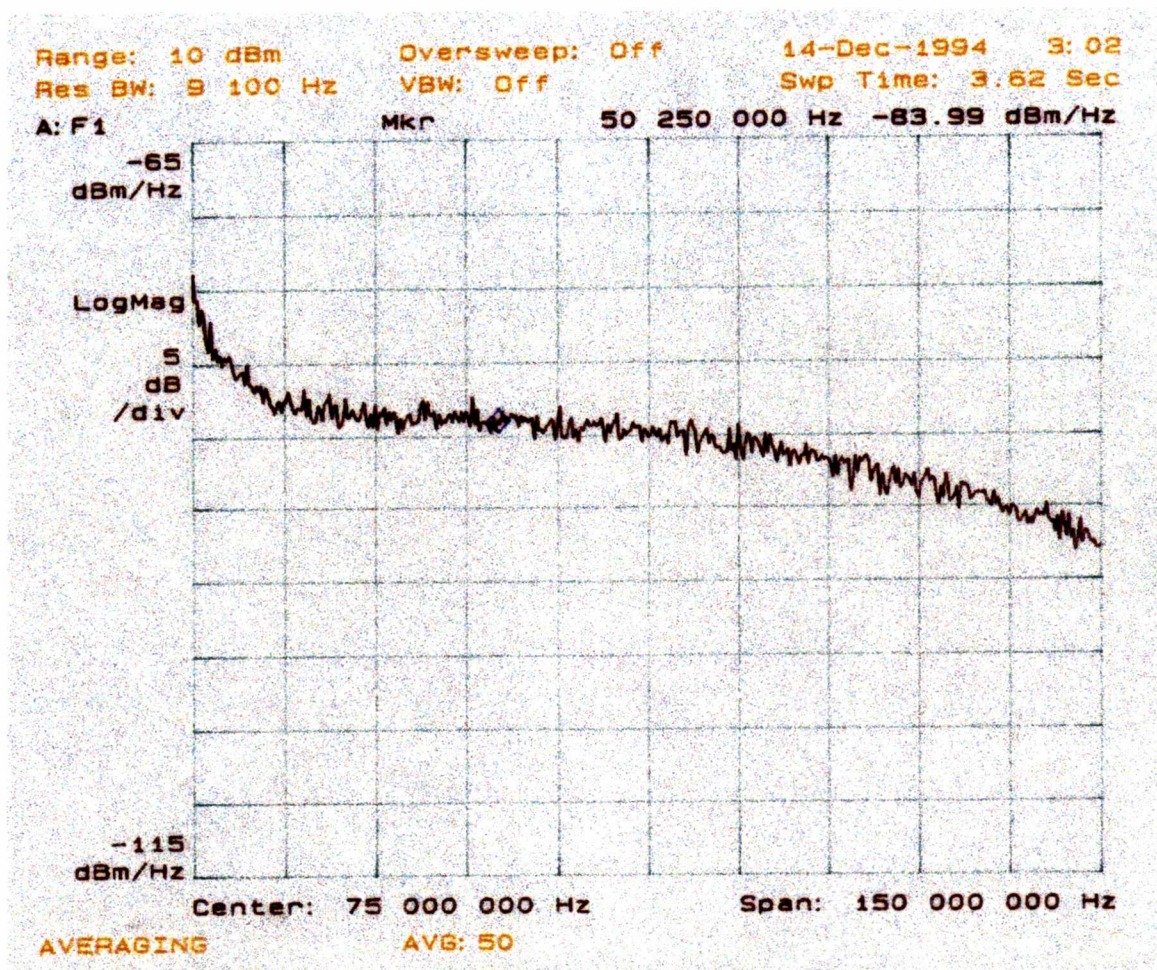


Figure 93 - AMI 1.2 μm - transimpedance amplifier with folded cascode stage noise measurement

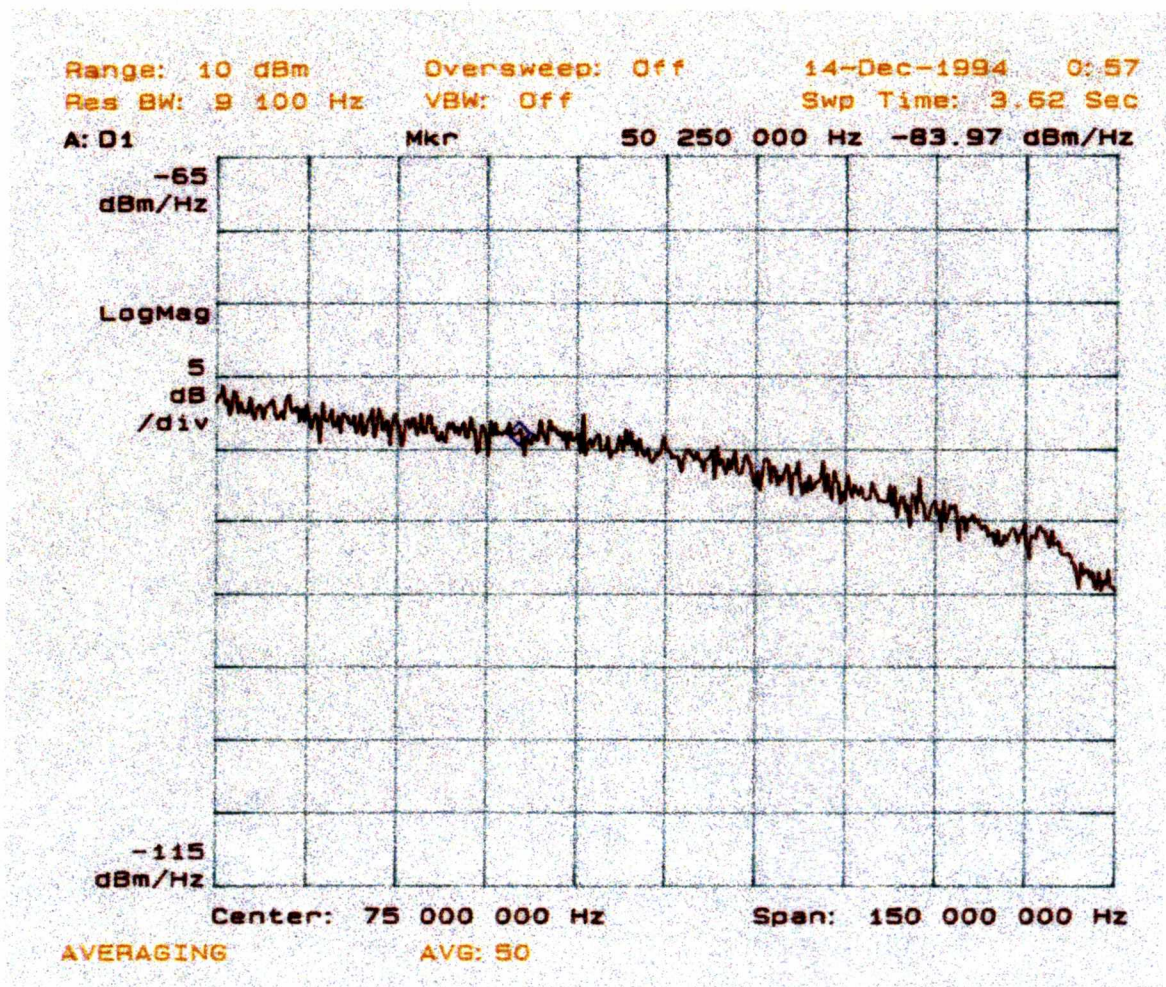


Figure 94 - AMI 1.2 um transimpedance amplifier with current mirror stage – noise measurement

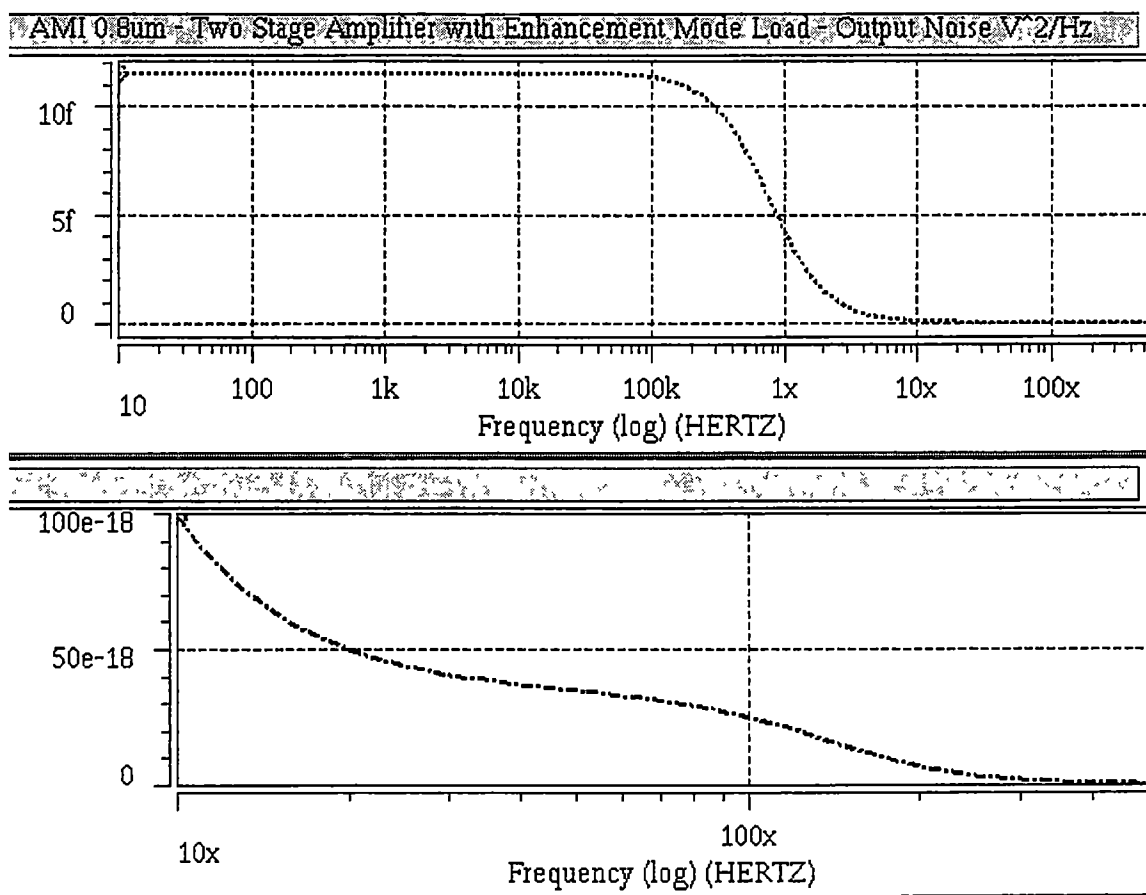


Figure 95 -- HSpice simulation of noise for two stage amplifier using AMI 0.8 um N97L run BSIM3 models

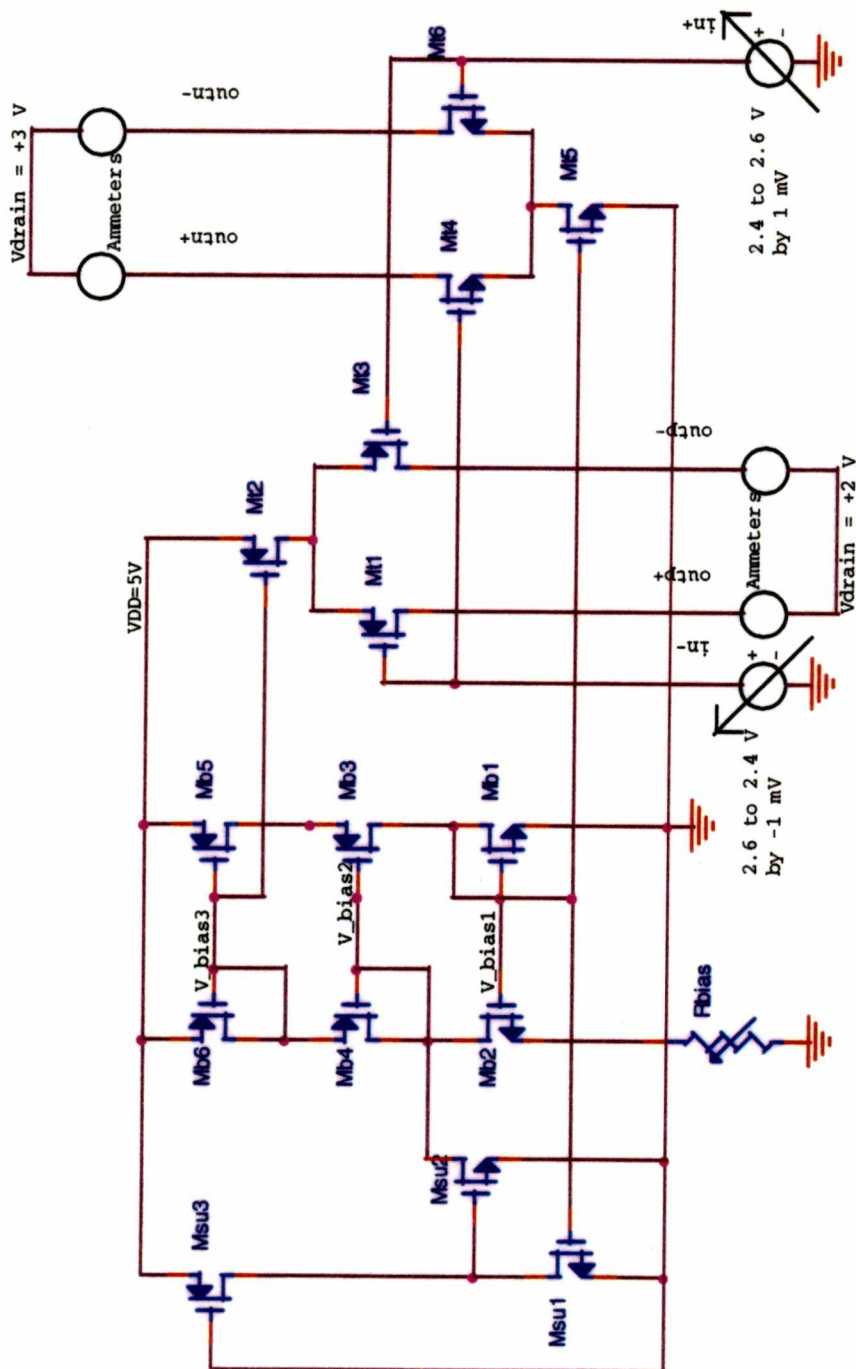


Figure 96 – Equivalent test setup using HP 4156A Parameter Analyzer for testing bias circuit

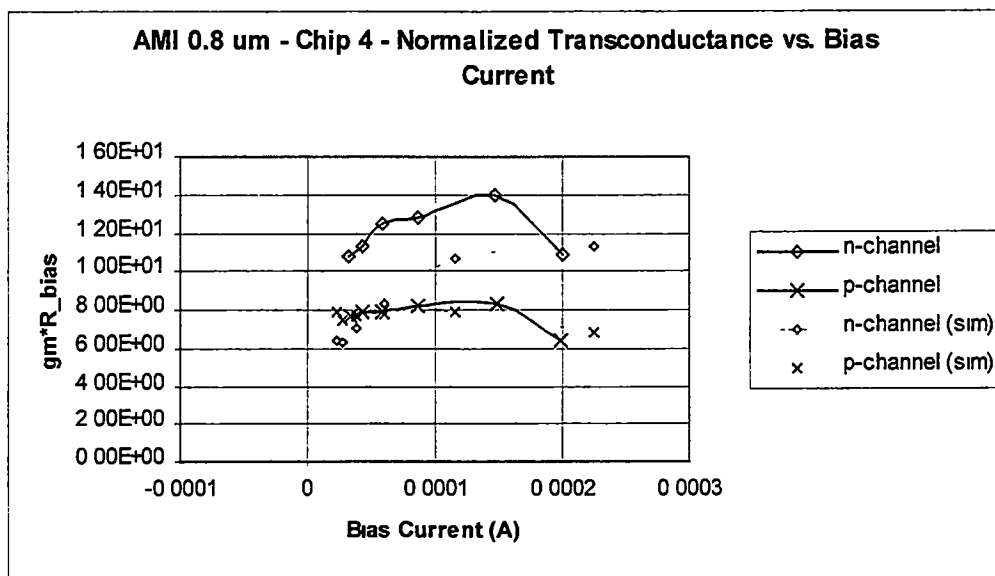


Figure 97 - AMI 0.8 um normalized transconductance vs. bias current – simulated and measured

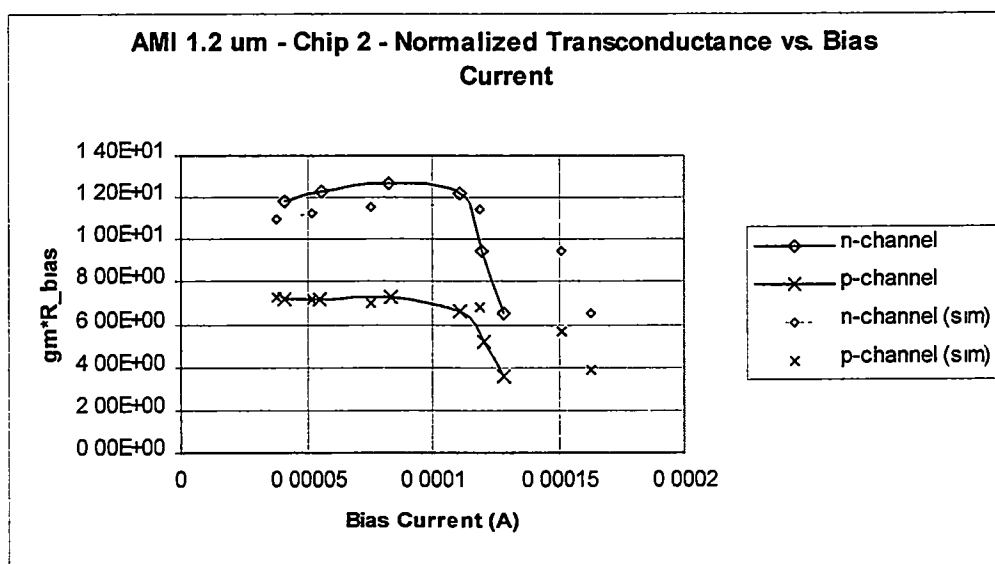


Figure 98 – AMI 1.2 um normalized transconductance vs. bias current – simulated and measured

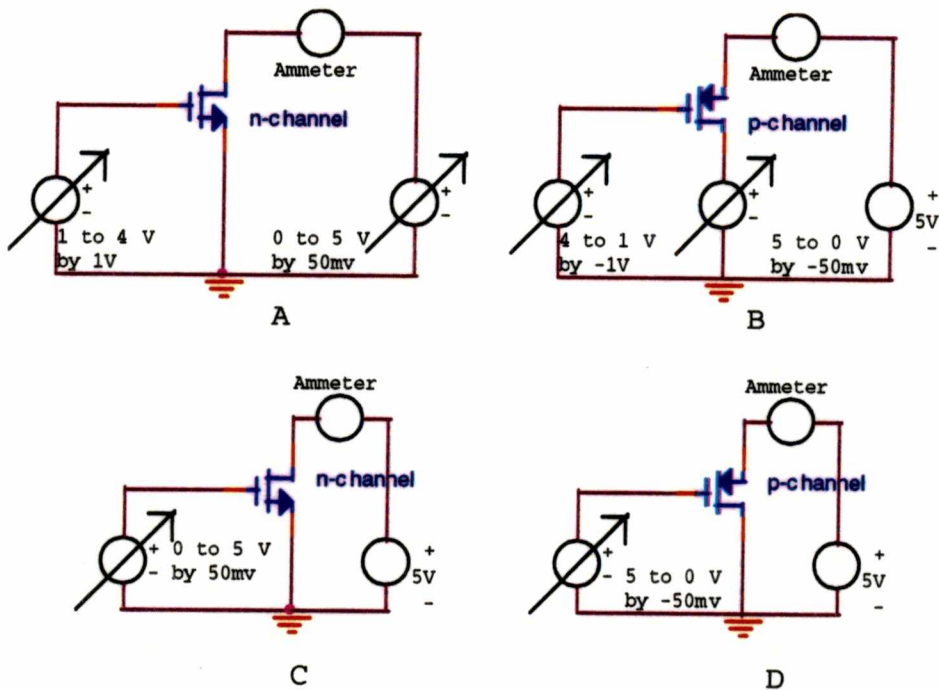


Figure 99 – Equivalent test setup using HP 4156A Parameter Analyzer to characterize an n-channel transistor's I_d vs V_{ds} curve (A) or I_d vs. V_{gs} curve (C) and a p-channel transistor's I_d vs. V_{ds} curve (B) or I_d vs. V_{gs} curve (D)

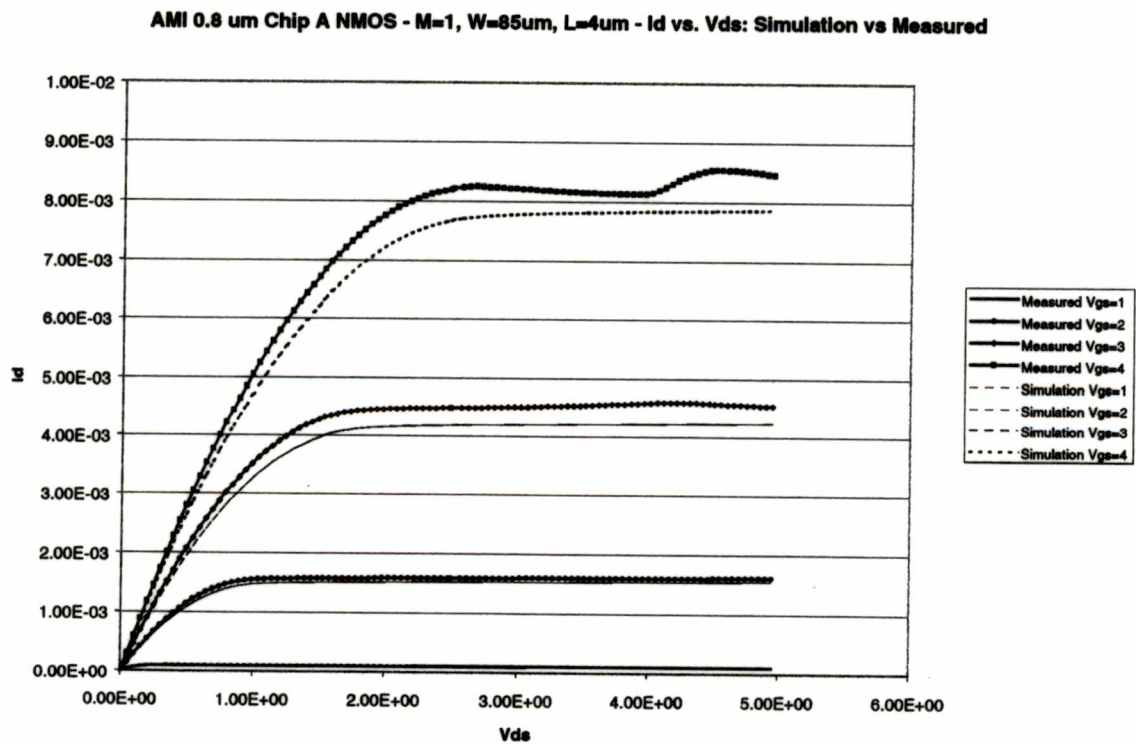


Figure 100 – AMI 0.8 um NMOS M=1, W=85 um, L=4 um I_d vs. V_{ds} plot – measured vs. simulated

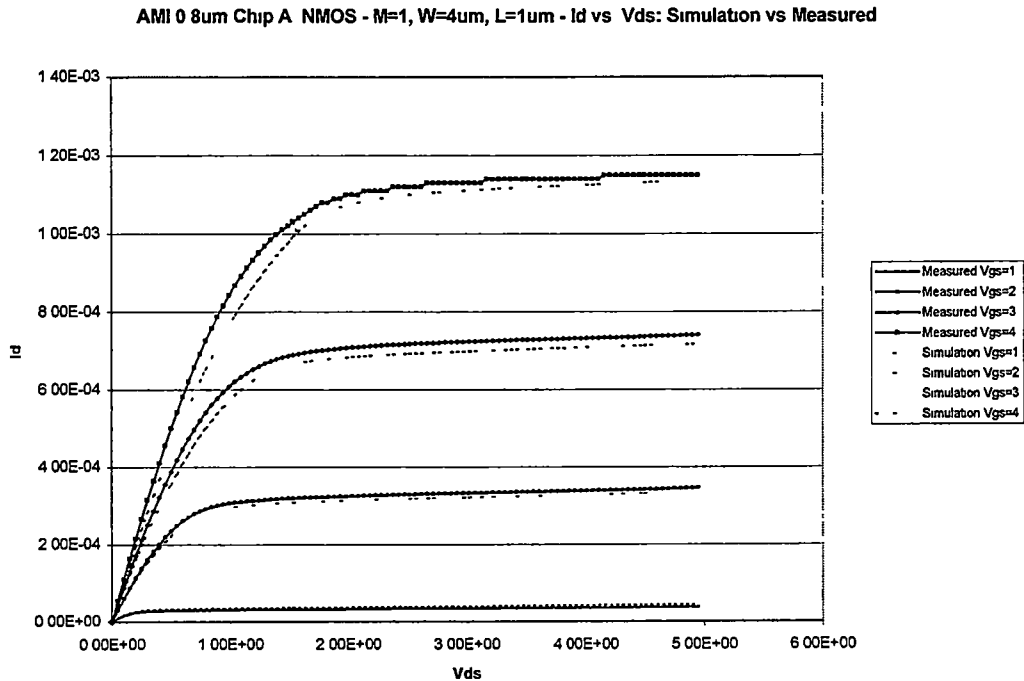


Figure 101 - AMI 0.8 um NMOS M=1, W=4 um, L=1 um Id vs. Vds plot – measured vs. Simulated

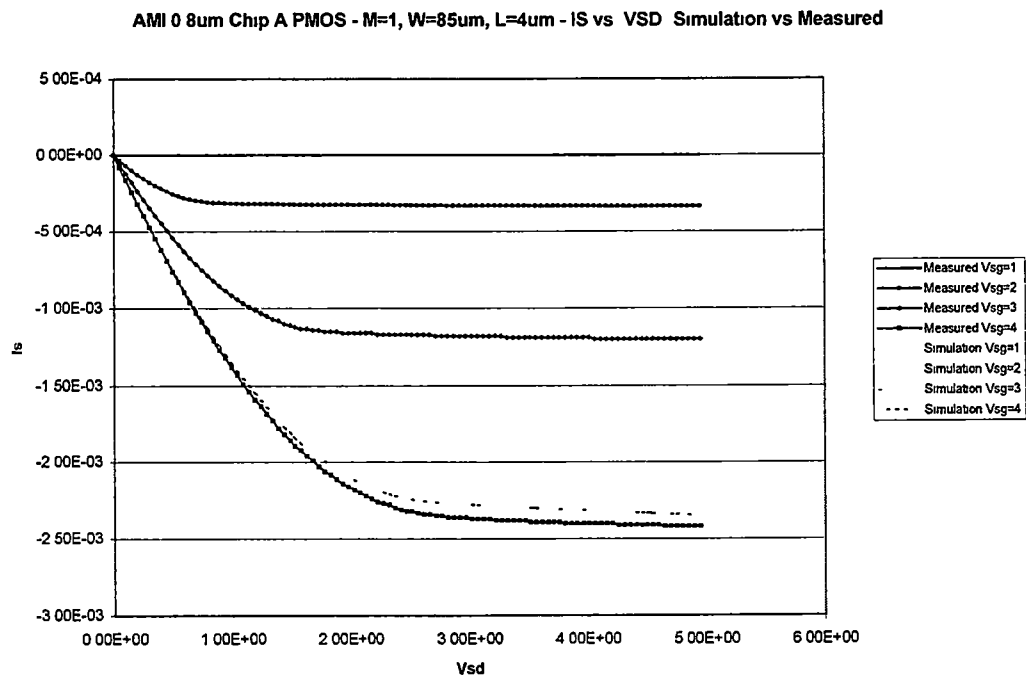


Figure 102 - AMI 0.8 um PMOS M=1, W=85 um, L=4 um Id vs. Vds plot – measured vs. simulated

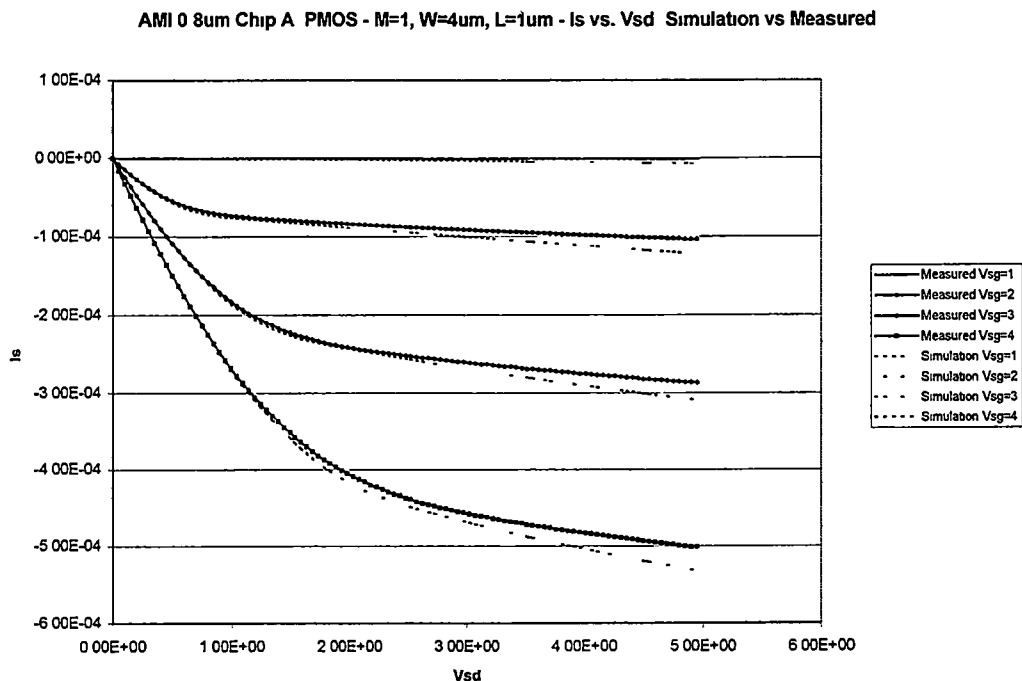


Figure 103 - AMI 0.8 um PMOS M=1, W=4 um, L=1 um I_d vs. V_{ds} plot – measured vs. simulated

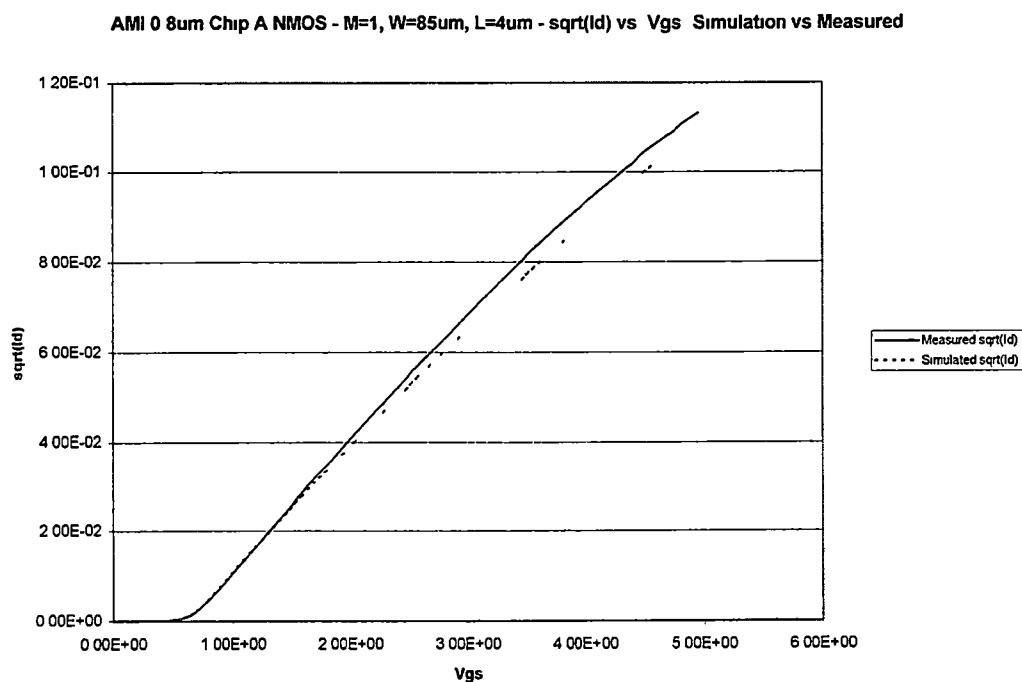


Figure 104 - AMI 0.8 um NMOS M=1, W=85 um, L=4 um $\sqrt{I_d}$ vs. V_{gs} plot – measured vs. simulated

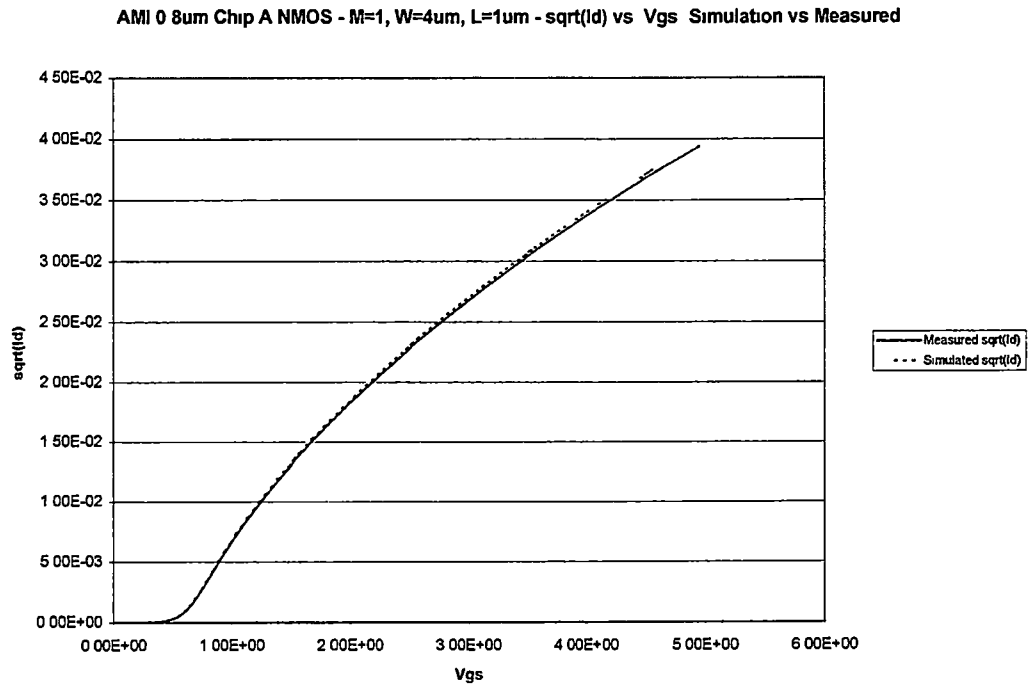


Figure 105 - AMI 0.8 um NMOS M=1, W=4 um, L=1 um measured vs. simulated sqrt(Id) vs. Vgs

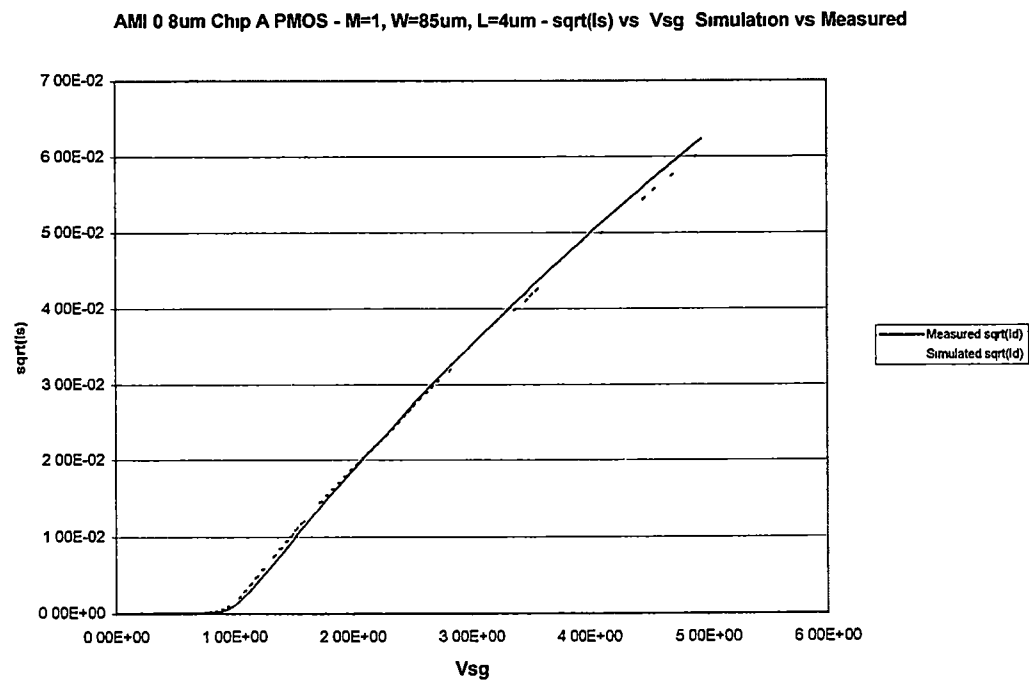


Figure 106 - AMI 0.8 um PMOS M=1, W=85 um, L=4 um measured vs. simulated sqrt(Id) vs. Vgs

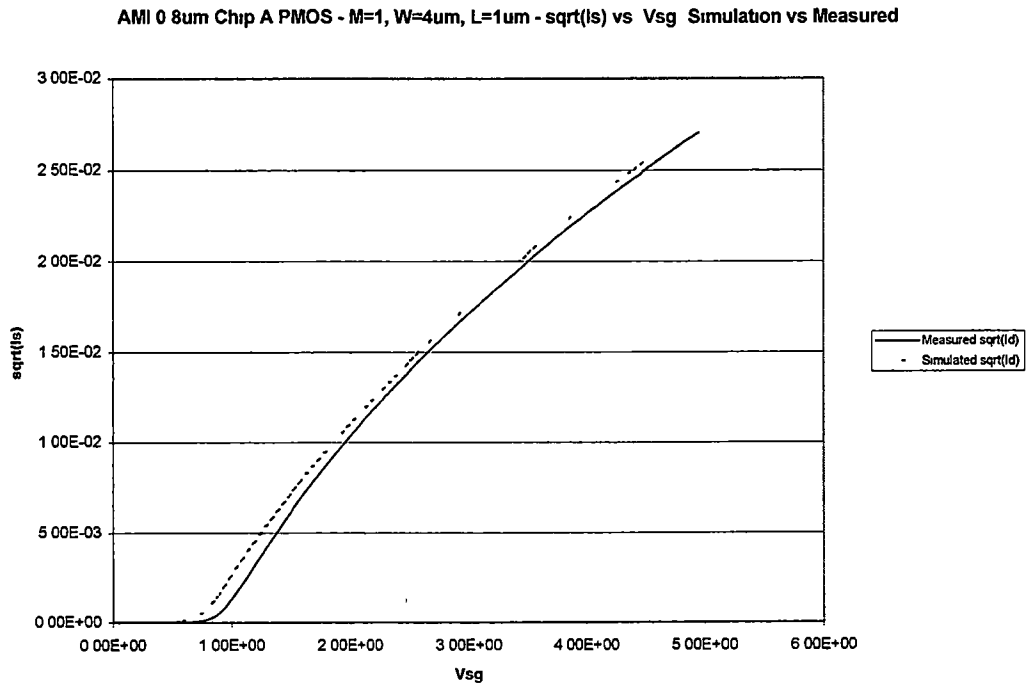


Figure 107 - AMI 0.8 um PMOS M=1, W=4 um, L=1 um measured vs. simulated $\sqrt{I_d}$ vs. V_{gs}

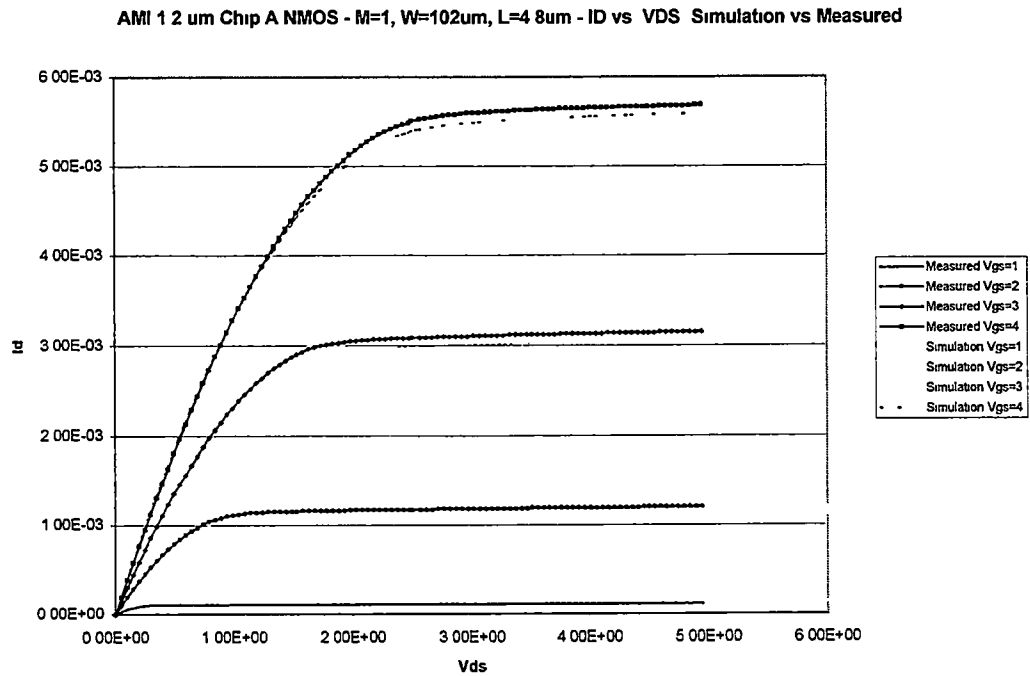


Figure 108 - AMI 1.2 um NMOS M=1, W=102 um, L=4.8 um I_d vs. V_{ds} plot – measured vs. simulated

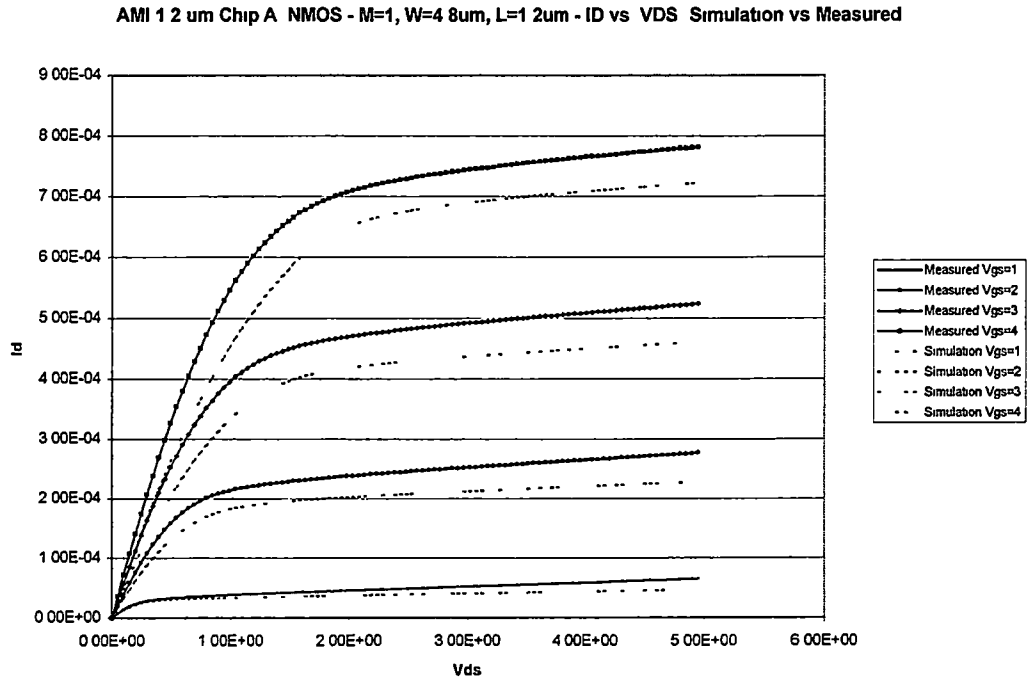


Figure 109 - AMI 1.2 um NMOS M=1, W=4.8 um, L=1.2 um Id vs. Vds plot – measured vs. simulated

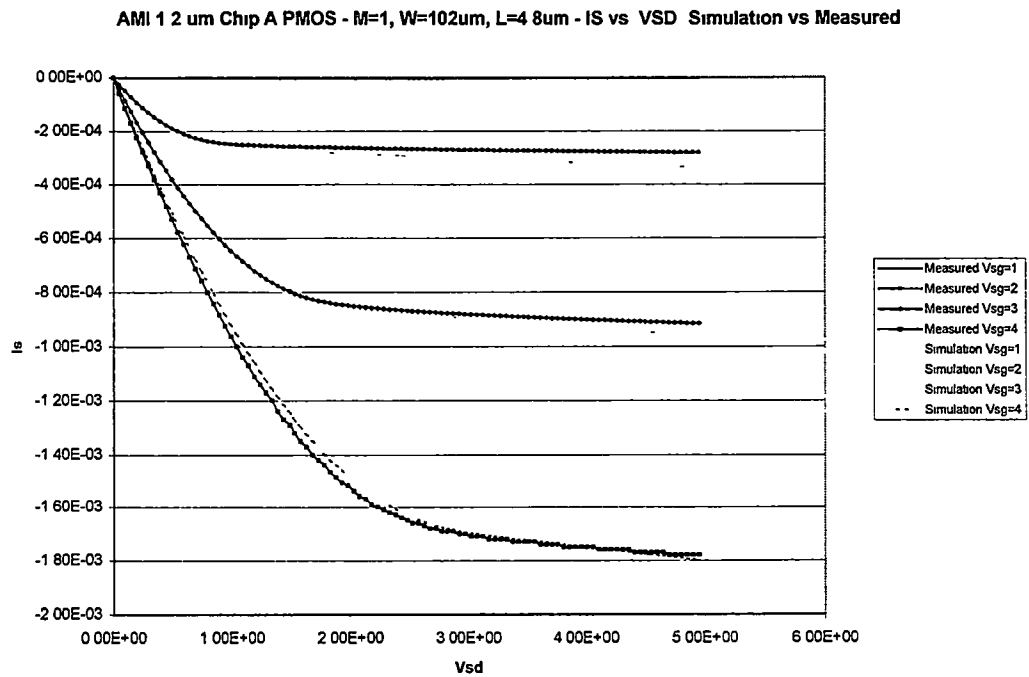


Figure 110 - AMI 1.2 um PMOS M=1, W=102 um, L=4.8 um Id vs. Vds plot – measured vs. simulated

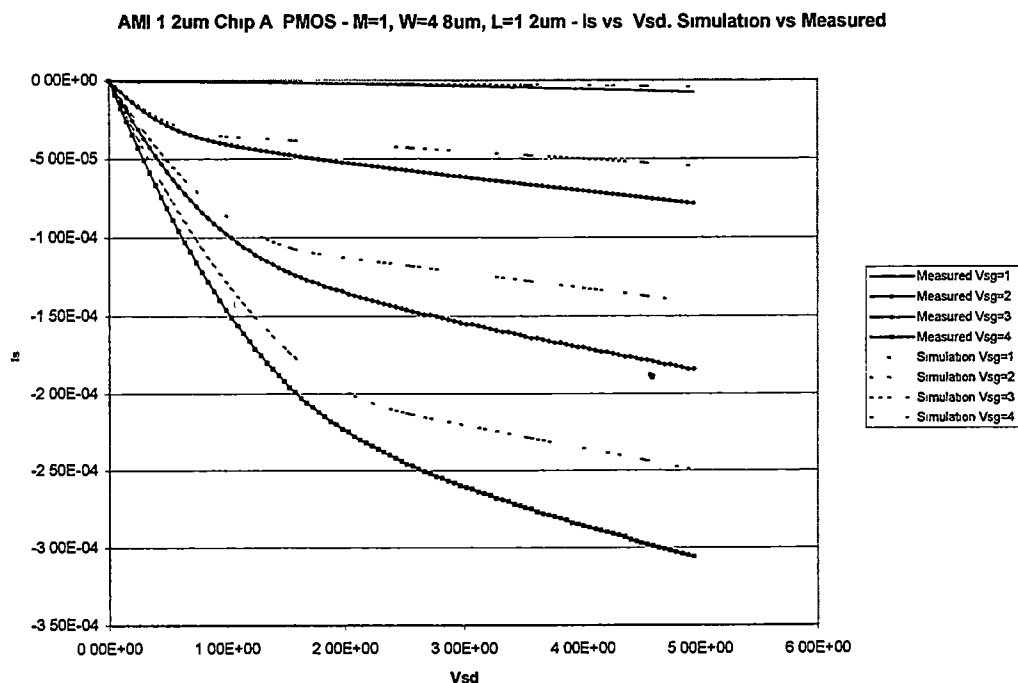


Figure 111 - AMI 1.2 um PMOS M=1, W=4.8 um, L=1.2 um I_d vs. V_{ds} plot – measured vs. simulated

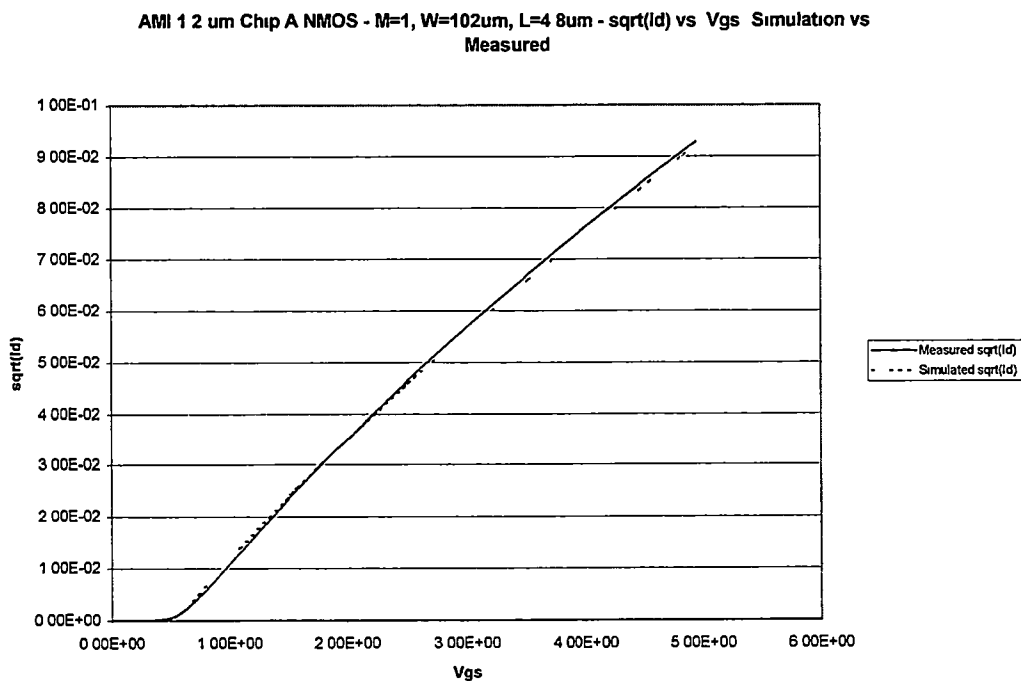


Figure 112 - AMI 1.2 um NMOS M=1, W=102 um, L=4.8 um measured vs. simulated $\sqrt{I_d}$ vs. V_{gs}

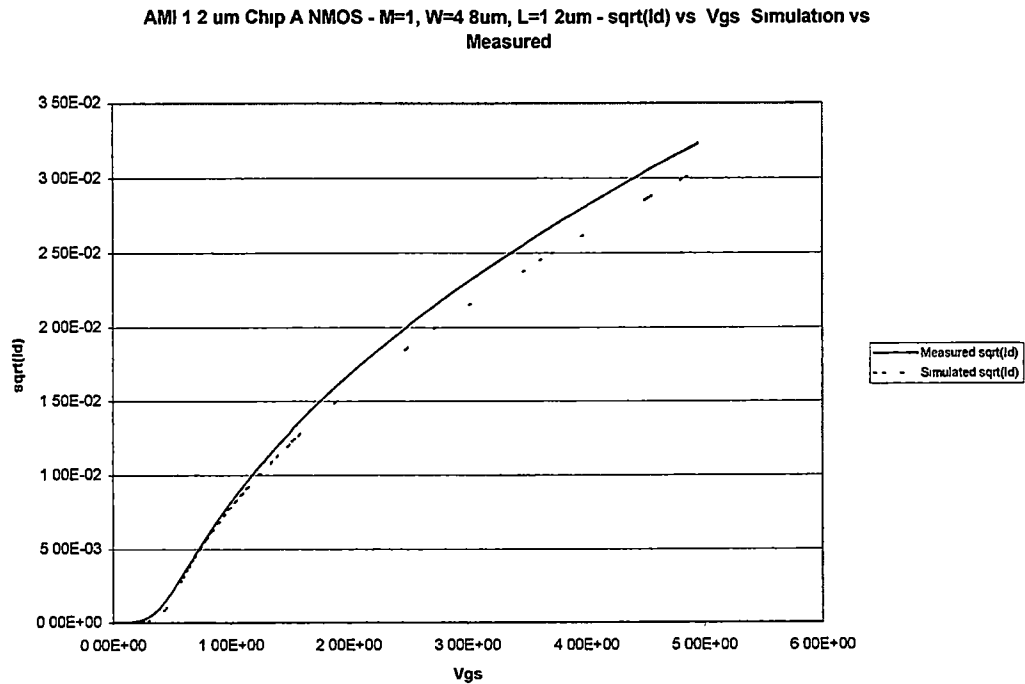


Figure 113 - AMI 1.2 um NMOS M=1, W=4.8 um, L=1.2 um measured vs. simulated sqrt(Id) vs. Vgs

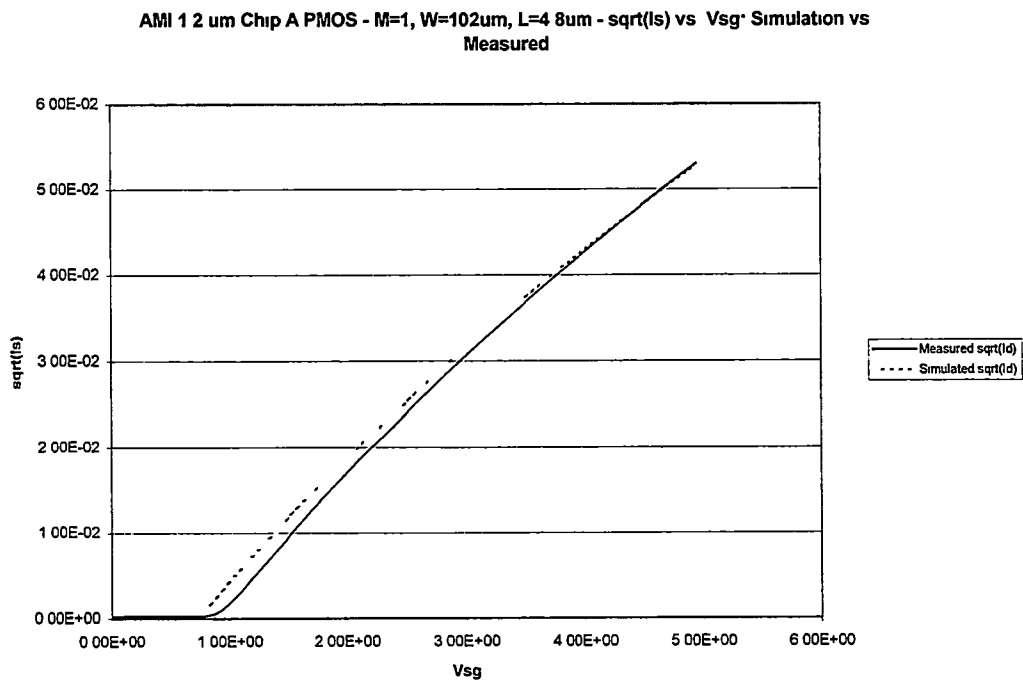


Figure 114 - AMI 1.2 um PMOS M=1, W=102 um, L=4.8 um measured vs. simulated sqrt(Id) vs. Vgs

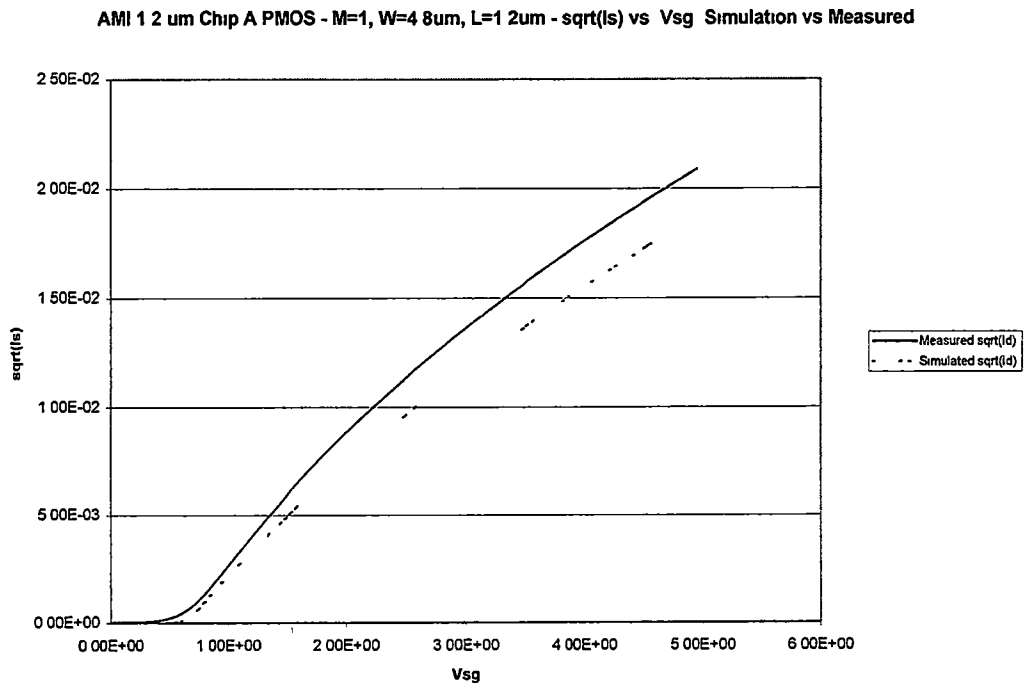


Figure 115 - AMI 1.2 um PMOS M=1, W=4.8 um, L=1.2 um measured vs. simulated sqrt(Id) vs. Vgs

APPENDIX 2

AMI 0.8 um Two Stage Amplifier with Enhancement Mode Load

* simple_res.spice

*

* File Location /msd16/falini/thesis/amir8/iclayout/jlfr8c2

* File Created Sat Sep 25 17:04:49 1999

* Ext2spice Version ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998

* Options -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g

*

** Subcircuit definition for buffern_r

** Extraction file is /msd16/falini/thesis/amir8/iclayout/jlfr8c2/buffern_r.ext

SUBCKT buffern_r vdd in out gnd bias1

M1 vdd in out gnd CMOSN M=7 W=50.00U L=1.00U GEO=0

M2 out bias1 gnd gnd CMOSN M=12 W=50.00U L=5.00U GEO=0

C1 vdd in 1.8F

C2 gnd bias1 12.4F

C3 in out 1.2F

C4 out bias1 10.8F

C5 gnd 0.644F

C6 out 0.486F

C7 vdd 0.204F

C8 bias1 0.977F

C9 in 0.322F

*** Node Listing for subckt buffern_r

** N0 == IdealGND

** bias1 [U=2]

** gnd [U=4]

** in [U=2]

** out [U=3]

** vdd [U=2]

ENDS

** Subcircuit definition for diffpair

** Extraction file is /msd16/falini/thesis/amir8/iclayout/jlfr8c2/diffpair.ext

SUBCKT diffpair d1n vdd d1p damn gnd damp bias1

M1n d1n damp dabias gnd CMOSN M=4 W=30.00U L=1.00U GEO=0

M1p d1p damn dabias gnd CMOSN M=4 W=30.00U L=1.00U GEO=0

M2n d1n d1n vdd vdd CMOSP W=12.00U L=1.00U GEO=0

M2p d1p d1p vdd vdd CMOSP W=12.00U L=1.00U GEO=0

Mdabias dabias bias1 gnd gnd CMOSN M=10 W=50.00U L=5.00U GEO=0

C1 damp dabias 1.5F

C2 damn d1n 1.5F

C3 damp d1n 3.2F

C4 bias1 gnd 9.9F

C5 bias1 dabias 8.8F

C6 d1p d1n 2.1F

C7 damn d1p 4.3F

C8 dabias damn 1.6F

C9 damp d1p 1.7F

C10 gnd 0.3694F

C11 d1n 0.500F

C12 d1p 0.453F

C13 dabias 0.620F

```

C14 vdd 0 6 7F
C15 damn 0 34 4F
C16 damp 0 34 6F
C17 bias1 0 87 4F
*** Node Listing for subckt: diffpair
** N0 == IdealGND
*****
** bias1 [U=2]
** d1n [U=4]
** d1p [U=4]
** dabias [U=3]
** damn [U=2]
** damp [U=2]
** gnd [U=5]
** vdd [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falnl/thesis/amir8/iclayout/jlfr8c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0
M2 out bias1 gnd gnd CMOSN M=12 W=50 00U L=5 00U GEO=0
C1 vdd in 1 8F
C2 gnd bias1 12 4F
C3 in out 1.2F
C4 out bias1 10 8F
C5 gnd 0 66 3F
C6 out 0 48 9F
C7 vdd 0 19 2F
C8 bias1 0 97 8F
C9 in 0 32 4F
*** Node Listing for subckt buffern_1
** N0 == IdealGND
*****
** bias1 [U=2]
** gnd [U=4]
** in [U=2]
** out [U=3]
** vdd [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falnl/thesis/amir8/iclayout/jlfr8c2/npbias ext
SUBCKT npbias vdd gnd bias1
vinbias bias1g bias1 dc 0 ac 0
MB1 bias1 bias1g gnd gnd CMOSN W=50 00U L=5 00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=50 00U L=5 00U GEO=0
Mb3 bias1 bias2 sb3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 00U L=25 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=10 00U L=2 00U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=5.00U L=2 00U GEO=0

```

Rbias rb gnd bias_r

*R_1 7k rb gnd RPOLYAMI0r8 SCALE=64 85

* R_1 7k=1692 6 (width=1 00U)

C1 bias2 bias1 4 0F

C2 bias1 rb 4 0F

C3 gnd bias2 1 1F

C4 rb 0 19 7F

C5 gnd 0 91 4F

C6 sb3 0 8 3F

C7 3 0 13 2F

C8 vdd 0 49 7F

C9 bias1 0 60 0F

C10 bias2 0 47 9F

C11 bias3 0 32 3F

*** Node Listing for subckt npbias

** N0 == IdealGND

** N3 [U=3] == 8 290 332#

** bias1 [U=6]

** bias2 [U=5]

** bias3 [U=4]

** gnd [U=10]

** rb [U=2]

** sb3 [U=2]

** vdd [U=9]

ENDS

***** top level cell is /msd16/falunjl/thesis/amir8/iclayout/jlfr8c2/simple.ext

** Instance-id buffern_r_0

X1 vdd 2 outn gnd bias1 buffern_r

** Instance-id diffpair_0

X2 2 vdd 6 inn gnd inp bias1 diffpair

** Instance-id buffern_l_0

X3 vdd 6 outp gnd bias1 buffern_l

** Instance-id npbias_0

X4 vdd gnd bias1 npbias

C1 gnd 0 271 4F

C2 outp 0 10 4F

C3 inn 0 6 0F

C4 inp 0 9 1F

C5 6 0 2 8F

C6 vdd 0 64 1F

C7 2 0 1 9F

C8 bias1 0 47.2F

*** Node Listing for subckt simple

** N0 == IdealGND

** N2 [U=2] == buffern_r_0/\$in

** N6 [U=2] == buffern_l_0/\$in

** bias1 [U=4]

** gnd [U=4]

** inn [U=1]

** inp [U=1]

```

** outn      [U=1]
** outp      [U=1]
** vdd       [U=4]
*****
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLYAMI0r8 R RES=26 1
MODEL CAPAMI0r8P C CAP=0 064FF
*0 errors and 0 warnings found

```

```

*AMI 0 8 um Two Stage Amplifier with Resistive Load
* simplr_res spice
*
* File Location      /msd16/falinj1/thesis/amir8/iclayout/jlfr8c2
* File Created       Sat Sep 25 17 05 00 1999
* Ext2spice Version  ORNL 2 6 4 <=> Tue Jan 27 17 32:51 EST 1998
* Options -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g

** Subcircuit definition for buffern_r
** Extraction file is /msd16/falinj1/thesis/amir8/iclayout/jlfr8c2/buffern_r ext
SUBCKT buffern_r vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0
M2 out bias1 gnd gnd CMOSN M=12 W=50 00U L=5 00U GEO=0
C1 vdd in 1 8F
C2 gnd bias1 12 4F
C3 in out 1 2F
C4 out bias1 10 8F
C5 gnd 0 64 4F
C6 out 0 48 6F
C7 vdd 0 20 4F
C8 bias1 0 97 7F
C9 in 0 32 2F
*** Node Listing for subckt buffern_r
** N0 == IdealGND
*****
** bias1 [U=2]
** gnd [U=4]
** in [U=2]
** out [U=3]
** vdd [U=2]
ENDS

** Subcircuit definition for diffpair2
** Extraction file is /msd16/falinj1/thesis/amir8/iclayout/jlfr8c2/diffpair2 ext
SUBCKT diffpair2 d1p damn gnd d1n damp bias1
M1n d1n damp dabias gnd CMOSN M=6 W=30 00U L=1 00U GEO=0
M1p d1p damn dabias gnd CMOSN M=6 W=30 00U L=1 00U GEO=0
Mdabias dabias bias1 gnd gnd CMOSN M=14 W=50 00U L=5 00U GEO=0
C1 dabias bias1 12 7F
C2 d1p damp 1 7F
C3 damn d1n 1 5F
C4 d1p d1n 2 0F
C5 damp d1n 3 6F
C6 dabias damn 2.3F
C7 damn d1p 2 9F
C8 dabias damp 2 1F
C9 gnd bias1 13 9F
C10 gnd 0 218 4F
C11 d1n 0 50 8F
C12 d1p 0 45 0F
C13 dabias 0 79 0F
C14 damn 0 41 3F
C15 damp 0 40 6F
C16 bias1 0 118 1F

```

```

*** Node Listing for subckt diffpair2
** N0 == IdealGND
*****
** bias1 [U=2]
** d1n [U=2]
** d1p [U=2]
** dabias [U=3]
** damn [U=2]
** damp [U=2]
** gnd [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falinj/thesis/amir8/iclayout/jlfr8c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0
M2 out bias1 gnd gnd CMOSN M=12 W=50 00U L=5 00U GEO=0
C1 vdd in 1 8F
C2 gnd bias1 12 4F
C3 in out 1 2F
C4 out bias1 10 8F
C5 gnd 0 66 3F
C6 out 0 48 9F
C7 vdd 0 19 2F
C8 bias1 0 97 8F
C9 in 0 32 4F
*** Node Listing for subckt buffern_1
** N0 == IdealGND
*****
** bias1 [U=2]
** gnd [U=4]
** in [U=2]
** out [U=3]
** vdd [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falinj/thesis/amir8/iclayout/jlfr8c2/npbias ext
SUBCKT npbias vdd gnd bias1
MB1 bias1 bias1 gnd gnd CMOSN W=50 00U L=5 00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=50 00U L=5 00U GEO=0
Mb3 bias1 bias2 sb3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 00U L=25 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=10 00U L=2 00U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=5 00U L=2 00U GEO=0

Rbias rb gnd bias_r

*R_1 7k rb gnd RPOLYAMI0r8 SCALE=64 85
*R_1 7k=1692 6 (width=1 00U)
C1 bias2 bias1 4 0F

```

```

C2 bias1 rb 4 0F
C3 gnd bias2 1 1F
C4 rb 0 19 7F
C5 gnd 0 91 4F
C6 sb3 0 8 3F
C7 3 0 13 2F
C8 vdd 0 49 7F
C9 bias1 0 60 0F
C10 bias2 0 47.9F
C11 bias3 0 32 3F
*** Node Listing for subckt npbias
** N0 == IdealGND
** N3 [U=3] == 8_290_332#
*****
** bias1 [U=6]
** bias2 [U=5]
** bias3 [U=4]
** gnd [U=10]
** rb [U=2]
** sb3 [U=2]
** vdd [U=9]
ENDS
***** top level cell is /msd16/falimj/thesis/amir8/iclayout/jlfr8c2/simpler ext
** Instance-id buffern_r_0
X1 vdd 3 outn gnd bias1 buffern_r
** Instance-id diffpair2_0
X2 1 inn gnd 3 mp bias1 diffpair2
** Instance-id buffern_l_0
X3 vdd 1 outp gnd bias1 buffern_l
** Instance-id npbias_0
X4 vdd gnd bias1 npbias

Rn 3 vdd load_r

*R_2 5kn 3 vdd RPOLYAMI0r8 SCALE=95 85
*R_2 5kn=2501 7 (width=1 00U)

Rp 1 vdd load_r

*R_2 5kp 1 vdd RPOLYAMI0r8 SCALE=95 85
*R_2 5kp=2501.7 (width=1 00U)
C1 gnd bias1 13 7F
C2 inp inn 1 2F
C3 1 inp 1 8F
C4 outp 0 9 0F
C5 inn 0 5 3F
C6 mp 0 7 2F
C7 3 0 6 7F
C8 1 0 10 7F
C9 vdd 0 42 7F
C10 gnd 0 242 2F
C11 bias1 0 38 2F
*** Node Listing for subckt simpler
** N0 == IdealGND

```

```

** N1      [U=3]  == buffern_l_0/$in
** N3      [U=3]  == buffern_r_0/$in
*****
** bias1   [U=4]
** gnd     [U=4]
** inn     [U=1]
** inp     [U=1]
** outn    [U=1]
** outp    [U=1]
** vdd     [U=5]
*****
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLYAMI0r8 R RES=26 1
MODEL CAPAMI0r8P C CAP=0 064FF
*0 errors and 0 warnings found

```

```

*AMI 0.8 um Transimpedance Amplifier with Folded Cascode Stage
* fccgti2_res spice
*
* File Location      /msd16/falini/thesis/amir8/iclayout/jlfr8c2
* File Created       Sat Sep 25 17 05 45 1999
* Ext2spice Version  ORNL 2.6.4 <=> Tue Jan 27 17 32 51 EST 1998
* Options    -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g
*
** Subcircuit definition for buffern_r
** Extraction file is /msd16/falini/thesis/amir8/iclayout/jlfr8c2/buffern_r ext
SUBCKT buffern_r vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0
M2 out bias1 gnd gnd CMOSN M=12 W=50 00U L=5 00U GEO=0
C1 vdd in 1 8F
C2 gnd bias1 12 4F
C3 in out 1 2F
C4 out bias1 10 8F
C5 gnd 0 64 4F
C6 out 0 48 6F
C7 vdd 0 20 4F
C8 bias1 0 97 7F
C9 in 0 32 2F
*** Node Listing for subckt: buffern_r
** N0 == IdealGND
*****
** bias1 [U=2]
** gnd [U=4]
** in [U=2]
** out [U=3]
** vdd [U=2]
ENDS

** Subcircuit definition for tiloop2_r
** Extraction file is /msd16/falini/thesis/amir8/iclayout/jlfr8c2/tiloop2_r ext
SUBCKT tiloop2_r bias3 vdd bias2 in gnd out
M3n 4 in gnd gnd CMOSN M=2 W=30 00U L=1 00U GEO=0
M4n out 4 9 gnd CMOSN M=4 W=30 00U L=1 00U GEO=0
Mb8n 1 bias3 vdd vdd CMOSP M=5 W=25 00U L=5 00U GEO=0
Mb9n 4 bias2 1 vdd CMOSP M=5 W=25 00U L=5 00U GEO=0

Rout out vdd out_r
*R_1 9k out vdd RPOLYAMI0r8 SCALE=72 85
* R_1 9k=1901 4 (width=1 00U)

R1 9 gnd bias1_r
*R_1k 9 gnd RPOLYAMI0r8 SCALE=38 35
* R_1k=1000 9 (width=1 00U)

Rf 9 in f_r
*R_2k 9 in RPOLYAMI0r8 SCALE=76 35
* R_2k=1992 7 (width=1 00U)

C1 bias3 vdd 4 0F

```

```

C2 in gnd 2 9F
C3 9 4 1 0F
C4 1 bias3 4 9F
C5 bias2 1 5.4F
C6 4 bias2 4 9F
C7 gnd 0 119 8F
C8 4 0 42 9F
C9 1 0 23 6F
C10 out 0 12 1F
C11 vdd 0 34 3F
C12 9 0 14 4F
C13 bias2 0 42 1F
C14 bias3 0 42 8F
C15 in 0 30 1F
*** Node Listing for subckt: tiloop2_r
** N0          == IdealGND
** N1          [U=2] == 8_160_666#
** N4          [U=3] == 8_220_376#
** N9          [U=3] == 8_300_376#
*****
** bias2       [U=2]
** bias3       [U=2]
** gnd         [U=5]
** in          [U=3]
** out         [U=3]
** vdd         [U=5]
ENDS

** Subcircuit definition for diffpair5
** Extraction file is /msd16/falinjl/thesis/amir8/iclayout/jlfr8c2/diffpair5 ext
SUBCKT diffpair5 1 bias2 vdd bias3 7 damn gnd damp bias1
M1n d1n damp dabias gnd CMOSN M=4 W=15 00U L=1 00U GEO=0
M1p d1p damn dabias gnd CMOSN M=4 W=15 00U L=1 00U GEO=0
M2n 7 bias2 d1n vdd CMOSP W=60 00U L=2 00U GEO=0
M2p 1 bias2 d1p vdd CMOSP W=60 00U L=2 00U GEO=0
Mb7n d1n bias3 vdd vdd CMOSP M=7 W=53 00U L=5 00U GEO=0
Mb7p d1p bias3 vdd vdd CMOSP M=7 W=53 00U L=5 00U GEO=0
Mb11n 7 bias1 gnd gnd CMOSN M=4 W=50 00U L=5 00U GEO=0
Mb11p 1 bias1 gnd gnd CMOSN M=4 W=50 00U L=5 00U GEO=0
Mdabias dabias bias1 gnd gnd CMOSN M=6 W=50 00U L=5 00U GEO=0
C1 d1p damn 2 0F
C2 bias2 1 1 9F
C3 1 bias1 3 7F
C4 d1p damp 1 2F
C5 vdd bias3 14 4F
C6 d1n damp 2 2F
C7 dabias damn 1 9F
C8 dabias damp 1 9F
C9 7 bias1 2 9F
C10 d1p bias3 6 9F
C11 dabias bias1 5 5F
C12 d1n bias3 6 9F
C13 gnd bias1 14 4F
C14 gnd 0 95 1F

```

```

C15 d1n 0 65 8F
C16 d1p 0 61 8F
C17 dabias 0 44 1F
C18 7 0 42 7F
C19 1 0 36 3F
C20 vdd 0 75.5F
C21 damn 0 31 4F
C22 damp 0 31 4F
C23 bias1 0 137 4F
C24 bias2 0 23 1F
C25 bias3 0 109 7F
*** Node Listing for subckt diffpair5
** N0 == IdealGND
** N1 [U=3] == 8_16_646#
** N7 [U=3] == 8_508_64#
*****
** bias1 [U=4]
** bias2 [U=3]
** bias3 [U=3]
** d1n [U=3]
** d1p [U=3]
** dabias [U=3]
** damn [U=2]
** damp [U=2]
** gnd [U=9]
** vdd [U=7]
ENDS

** Subcircuit definition for tloop2_1
** Extraction file is /msd16/falnjl/thesis/amir8/iclayout/jlfr8c2/tloop2_1 ext
SUBCKT tloop2_1 bias2 vdd bias3 out gnd in
M3p 1 in gnd gnd CMOSN M=2 W=30 00U L=1 00U GEO=0
M4p out 1 7 gnd CMOSN M=4 W=30 00U L=1 00U GEO=0
Mb8p 1 bias2 3 vdd CMOSP M=5 W=25 00U L=5 00U GEO=0
Mb9p 3 bias3 vdd vdd CMOSP M=5 W=25 00U L=5 00U GEO=0

Rout out vdd out_r
*R_1 9k out vdd RPOLYAMI0r8 SCALE=72 85
* R_1 9k=1901 4 (width=1 00U)

R1 7 gnd bias1_r
*R_1k 9 gnd RPOLYAMI0r8 SCALE=38 35
* R_1k=1000 9 (width=1 00U)

Rf 7 in f_r
*R_2k 9 in RPOLYAMI0r8 SCALE=76 35
* R_2k=1992 7 (width=1 00U)

C1 7 1 1 0F
C2 3 bias2 5 4F
C3 1 bias2 4 9F
C4 bias3 vdd 4.0F
C5 bias3 3 4 9F

```

```

C6 in gnd 2.9F
C7 gnd 0 119 8F
C8 7 0 14 4F
C9 out 0 12 1F
C10 vdd 0 34 3F
C11 3 0 23 6F
C12 1 0 42 9F
C13 bias2 0 42 1F
C14 bias3 0 42 7F
C15 in 0 30 1F
*** Node Listing for subckt tiloop2_1
** N0          == IdealGND
** N1          [U=3] == 8_144_686#
** N3          [U=2] == 8_144_656#
** N7          [U=3] == 8_178_436#
*****
** bias2       [U=2]
** bias3       [U=2]
** gnd         [U=5]
** in          [U=3]
** out         [U=3]
** vdd         [U=5]
.ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falnlj/thesis/amir8/iclayout/jlfr8c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0
M2 out bias1 gnd gnd CMOSN M=12 W=50 00U L=5 00U GEO=0
C1 vdd in 1 8F
C2 gnd bias1 12 4F
C3 in out 1 2F
C4 out bias1 10.8F
C5 gnd 0 66 3F
C6 out 0 48 9F
C7 vdd 0 19 2F
C8 bias1 0 97 8F
C9 in 0 32 4F
*** Node Listing for subckt buffern_1
** N0          == IdealGND
*****
** bias1       [U=2]
** gnd         [U=4]
** in          [U=2]
** out         [U=3]
** vdd         [U=2]
.ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falnlj/thesis/amir8/iclayout/jlfr8c2/npbias ext
SUBCKT npbias bias3 vdd 3 gnd bias2 bias1
MB1 bias1 bias1 gnd gnd CMOSN W=50 00U L=5 00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=50 00U L=5 00U GEO=0
Mb3 bias1 bias2 sb3 vdd CMOSP W=50 00U L=5 00U GEO=0

```

```

Mb4 bias2 bias2 bias3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 00U L=25 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=10 00U L=2 00U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=5 00U L=2 00U GEO=0

Rbias rb gnd bias_r
*R_1 7k rb gnd RPOLYAMI0r8 SCALE=64 85
*R_1 7k=1692 6 (width=1 00U)
C1 bias2 bias1 4 0F
C2 bias1 rb 4 0F
C3 gnd bias2 1 1F
C4 rb 0 19 7F
C5 gnd 0 91 4F
C6 sb3 0 8 3F
C7 3 0 13 2F
C8 vdd 0 49 7F
C9 bias1 0 60 0F
C10 bias2 0 47 9F
C11 bias3 0 32 3F
*** Node Listing for subckt: npbias
** N0 == IdealGND
** N3 [U=4] == 8_290_332#
*****
** bias1 [U=6]
** bias2 [U=6]
** bias3 [U=5]
** gnd [U=10]
** rb [U=2]
** sb3 [U=2]
** vdd [U=9]
.ENDS
***** top level cell is /msd16/falini/thesis/amir8/iclayout/jlfr8c2/fccgti2 ext
** Instance-id buffern_r_0
X1 vdd 2 outn gnd bias1 buffern_r
** Instance-id tiloop2_r_0
X2 bias3 vdd bias2 8 gnd 2 tiloop2_r
** Instance-id diffpair5_0
X3 9 bias2 vdd bias3 8 inn gnd inp bias1 diffpair5
** Instance-id tiloop2_l_0
X4 bias2 vdd bias3 12 gnd 9 tiloop2_l
** Instance-id buffern_l_0
X5 vdd 12 outp gnd bias1 buffern_l
** Instance-id npbias_0
X6 bias3 vdd 14 gnd bias2 bias1 npbias
C1 inn 9 1 4F
C2 bias2 inn 1 7F
C3 inp inn 3.6F
C4 bias3 bias2 13 4F
C5 gnd bias1 1 4F
C6 gnd 0 1306 2F
C7 outp 0 12 4F
C8 inn 0 15 7F

```

```

C9 imp 0 19 0F
C10 12 0 12 5F
C11 2 0 12.5F
C12 9 0 7.2F
C13 8 0 5 9F
C14 vdd 0 430.9F
C15 bias1 0 93 7F
C16 bias2 0 69 9F
C17 bias3 0 59 2F
*** Node Listing for subckt fccgt12
** N0          == IdealGND
** N2          [U=2] == buffern_r_0/$in
** N8          [U=2] == tiloop2_r_0/$in
** N9          [U=2] == tiloop2_l_0/$in
** N12         [U=2] == buffern_l_0/$in
** N14         [U=1] == npbias_0/8_290_332#
*****
** bias1       [U=4]
** bias2       [U=4]
** bias3       [U=4]
** gnd         [U=6]
** inn         [U=1]
** inp         [U=1]
** outn        [U=1]
** outp        [U=1]
** vdd         [U=6]
*****
*
* Model Definitions for HSPICE
*
*****
.MODEL RPOLYAMI0r8 R RES=26 1
.MODEL CAPAMI0r8P C CAP=0 064FF
*0 errors and 0 warnings found.

```

AMI 0.8 um Transimpedance Amplifier with Current Mirror Stage

* cmcgt1_res spice

*

* File Location /msd16/falinjl/thesis/amir8/iclayout/jlfr8c2

* File Created Sat Sep 25 17 06 01 1999

* Ext2spice Version ORNL 2.6.4 <=> Tue Jan 27 17 32 51 EST 1998

* Options -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g

*

** Subcircuit definition for buffern_r

** Extraction file is /msd16/falinjl/thesis/amir8/iclayout/jlfr8c2/buffern_r ext

.SUBCKT buffern_r vdd in out gnd bias1

M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0

M2 out bias1 gnd gnd CMOSN M=12 W=50 00U L=5 00U GEO=0

C1 vdd in 1 8F

C2 gnd bias1 12 4F

C3 in out 1 2F

C4 out bias1 10.8F

C5 gnd 0 64 4F

C6 out 0 48 6F

C7 vdd 0 20 4F

C8 bias1 0 97 7F

C9 in 0 32 2F

*** Node Listing for subckt buffern_r

** N0 == IdealGND

** bias1 [U=2]

** gnd [U=4]

** in [U=2]

** out [U=3]

** vdd [U=2]

ENDS

** Subcircuit definition for tiloop_r

** Extraction file is /msd16/falinjl/thesis/amir8/iclayout/jlfr8c2/tiloop_r ext

SUBCKT tiloop_r bias3 vdd bias2 in gnd out

M3n 4 in gnd gnd CMOSN M=2 W=30 00U L=1 00U GEO=0

M4n out 4 9 gnd CMOSN M=4 W=30 00U L=1 00U GEO=0

Mb8n 1 bias3 vdd vdd CMOSP M=5 W=25 00U L=5 00U GEO=0

Mb9n 4 bias2 1 vdd CMOSP M=5 W=25 00U L=5 00U GEO=0

Rout out vdd out_r

* R_1 9k out vdd RPOLYAMI0r8 SCALE=72 85

* R_1 9k=1901 4 (width=1 00U)

R1 9 gnd bias1_r

* R_1k 9 gnd RPOLYAMI0r8 SCALE=38 35

* R_1k=1000 9 (width=1 00U)

Rf 9 in f_r

* R_2k 9 in RPOLYAMI0r8 SCALE=76 35

* R_2k=1992 7 (width=1 00U)

C1 vdd bias3 4 0F

C2 bias3 1 4 9F

```

C3 4 9 1 0F
C4 1 bias2 5 4F
C5 gnd in 2 9F
C6 bias2 4 4 9F
C7 gnd 0 119 8F
C8 4 0 42 9F
C9 1 0 23 6F
C10 out 0 12 1F
C11 vdd 0 34 3F
C12 9 0 14 4F
C13 bias2 0 42 1F
C14 bias3 0 42 8F
C15 in 0 30 1F
*** Node Listing for subckt tiloop_r
** N0 == IdealGND
** N1 [U=2] == 8_160_666#
** N4 [U=3] == 8_220_376#
** N9 [U=3] == 8_300_376#
*****
** bias2 [U=2]
** bias3 [U=2]
** gnd [U=5]
** in [U=3]
** out [U=3]
** vdd [U=5]
.ENDS

** Subcircuit definition for diffpair3
** Extraction file is /msd16/falinjl/thesis/amir8/iclayout/jlfr8c2/diffpair3 ext
SUBCKT diffpair3 1 2 vdd damn gnd damp 12 13 bias1
M1n 9 damp dabias gnd CMOSN M=4 W=15 00U L=1.00U GEO=0
M1p 5 damn dabias gnd CMOSN M=4 W=15 00U L=1.00U GEO=0
M2na 9 9 vdd vdd CMOSP W=30 00U L=1 00U GEO=0
M2nb 11 9 vdd vdd CMOSP W=30 00U L=1.00U GEO=0
M2nc 12 13 11 vdd CMOSP W=60 00U L=1 00U GEO=0
M2pa 5 5 vdd vdd CMOSP W=30 00U L=1 00U GEO=0
M2pb 3 5 vdd vdd CMOSP W=30 00U L=1 00U GEO=0
M2pc 1 2 3 vdd CMOSP W=60 00U L=1 00U GEO=0
Mb11n 12 bias1 gnd gnd CMOSN M=3 W=50 00U L=5 00U GEO=0
Mb11p 1 bias1 gnd gnd CMOSN M=3 W=50 00U L=5 00U GEO=0
Mdabias dabias bias1 gnd gnd CMOSN M=6 W=50 00U L=5 00U GEO=0
C1 12 bias1 3 1F
C2 1 bias1 3 1F
C3 damn damp 1 0F
C4 damp 9 2 2F
C5 dabias bias1 6 4F
C6 5 damn 2 1F
C7 gnd bias1 8 8F
C8 dabias damn 1 9F
C9 5 damp 1 2F
C10 dabias damp 1 9F
C11 gnd 0 179 1F
C12 5 0 38 2F
C13 13 0 2 9F

```

```

C14 1 0 22 0F
C15 3 0 10 2F
C16 dabias 0 48 2F
C17 9 0 38 3F
C18 11 0 10 2F
C19 vdd 0 104 0F
C20 12 0 21 0F
C21 2 0 2 8F
C22 damn 0 35 5F
C23 damp 0 34 7F
C24 bias1 0 117 8F
*** Node Listing for subckt diffpair3
** N0 == IdealGND
** N1 [U=3] == 8_197_135#
** N2 [U=2] == 8_189_112#
** N3 [U=2] == 8_183_135#
** N5 [U=4] == 8_157_135#
** N9 [U=4] == 8_50_81#
** N11 [U=2] == 8_440_121#
** N12 [U=3] == 8_320_419#
** N13 [U=2] == 8_466_108#
*****
** bias1 [U=4]
** dabias [U=3]
** damn [U=2]
** damp [U=2]
** gnd [U=9]
** vdd [U=11]
.ENDS

** Subcircuit definition for tiloop_1
** Extraction file is /msd16/faliny/thesis/amir8/iclayout/jlfr8c2/tiloop_1 ext
SUBCKT tiloop_1 bias2 vdd bias3 out gnd in
M3p 1 in gnd gnd CMOSN M=2 W=30 00U L=1 00U GEO=0
M4p out 1 7 gnd CMOSN M=4 W=30 00U L=1 00U GEO=0
Mb8p 1 bias2 3 vdd CMOSP M=5 W=25 00U L=5 00U GEO=0
Mb9p 3 bias3 vdd vdd CMOSP M=5 W=25 00U L=5 00U GEO=0

Rout out vdd out_r
*R_1 9k out vdd RPOLYAMI0r8 SCALE=72 85
*R_1 9k=1901.4 (width=1 00U)

R1 7 gnd bias1_r
*R_1k 9 gnd RPOLYAMI0r8 SCALE=38 35
*R_1k=1000 9 (width=1 00U)

Rf 7 in f_r
*R_2k 9 in RPOLYAMI0r8 SCALE=76 35
*R_2k=1992 7 (width=1 00U)

C1 1 7 1 0F
C2 bias2 1 4 9F
C3 vdd bias3 4 0F
C4 bias2 3 5 4F

```

```

C5 3 bias3 4 9F
C6 gnd in 2 9F
C7 gnd 0 119 8F
C8 7 0 14 4F
C9 out 0 12 1F
C10 vdd 0 34 3F
C11 3 0 23 6F
C12 1 0 42 9F
C13 bias2 0 42 1F
C14 bias3 0 42 7F
C15 in 0 30 1F
*** Node Listing for subckt  tiloop_1
** N0          == IdealGND
** N1          [U=3] == 8_144_686#
** N3          [U=2] == 8_144_656#
** N7          [U=3] == 8_178_436#
*****
** bias2       [U=2]
** bias3       [U=2]
** gnd         [U=5]
** in          [U=3]
** out         [U=3]
** vdd         [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falnj1/thesis/amir8/iclayout/jlfr8c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=7 W=50 00U L=1 00U GEO=0
M2 out bias1 gnd CMOSN M=12 W=50 00U L=5 00U GEO=0
C1 vdd in 1 8F
C2 gnd bias1 12 4F
C3 in out 1 2F
C4 out bias1 10 8F
C5 gnd 0 66 3F
C6 out 0 48 9F
C7 vdd 0 19 2F
C8 bias1 0 97 8F
C9 in 0 32 4F
*** Node Listing for subckt  buffern_1
** N0          == IdealGND
*****
** bias1       [U=2]
** gnd         [U=4]
** in          [U=2]
** out         [U=3]
** vdd         [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falnj1/thesis/amir8/iclayout/jlfr8c2/npbias ext
SUBCKT npbias bias3 vdd 3 gnd bias2 bias1
MB1 bias1 bias1 gnd gnd CMOSN W=50 00U L=5 00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=50 00U L=5 00U GEO=0

```

```

Mb3 bias1 bias2 sb3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=50 00U L=5 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=50 00U L=5 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 00U L=25 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=10 00U L=2 00U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=5 00U L=2 00U GEO=0

Rbias rb gnd bias_r
*R_1 7k rb gnd RPOLYAMI0r8 SCALE=64 85
*R_1 7k=1692 6 (width=1 00U)
C1 bias2 bias1 4 0F
C2 bias1 rb 4 0F
C3 gnd bias2 1 1F
C4 rb 0 19 7F
C5 gnd 0 91 4F
C6 sb3 0 8 3F
C7 3 0 13 2F
C8 vdd 0 49 7F
C9 bias1 0 60 0F
C10 bias2 0 47 9F
C11 bias3 0 32 3F
*** Node Listing for subckt npbias
** N0 == IdealGND
** N3 [U=4] == 8_290_332#
*****
** bias1 [U=6]
** bias2 [U=6]
** bias3 [U=5]
** gnd [U=10]
** rb [U=2]
** sb3 [U=2]
** vdd [U=9]
.ENDS
***** top level cell is /msd16/falini/thesis/amir8/iclayout/jlfr8c2/cmcgti.ext
** Instance-id buffern_r_0
X1 vdd 2 outn gnd bias1 buffern_r
** Instance-id tiloop_r_0
X2 bias3 vdd bias2 8 gnd 2 tiloop_r
** Instance-id diffpair3_0
X3 9 bias2 vdd inn gnd inp 8 bias2 bias1 diffpair3
** Instance-id tiloop_l_0
X4 bias2 vdd bias3 12 gnd 9 tiloop_l
** Instance-id buffern_l_0
X5 vdd 12 outp gnd bias1 buffern_l
** Instance-id npbias_0
X6 bias3 vdd 14 gnd bias2 bias1 npbias
C1 bias3 inn 1 1F
C2 inp inn 2 8F
C3 vdd bias3 25 7F
C4 vdd bias2 25 4F
C5 gnd bias1 1 9F
C6 bias3 bias2 8.0F
C7 gnd 0 675 5F

```

```

C8 outp 0 12 5F
C9 8 0 5 5F
C10 inn 0 12 3F
C11 inp 0 13 3F
C12 2 0 12 5F
C13 9 0 6 8F
C14 12 0 12 5F
C15 vdd 0 414 8F
C16 bias1 0 90 7F
C17 bias2 0 66 2F
C18 bias3 0 57 5F
*** Node Listing for subckt. cmcgti
** N0          == IdealGND
** N2          [U=2] == buffern_r_0/$in
** N8          [U=2] == tiloop_r_0/$in
** N9          [U=2] == tiloop_l_0/$in
** N12         [U=2] == buffern_l_0/$in
** N14         [U=1] == npbias_0/8_290_332#
*****
** bias1       [U=4]
** bias2       [U=5]
** bias3       [U=3]
** gnd         [U=6]
** inn         [U=1]
** inp         [U=1]
** outn        [U=1]
** outp        [U=1]
** vdd         [U=6]
*****
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLYAMI0r8 R RES=26 1
.MODEL CAPAMI0r8P C CAP=0 064FF
*0 errors and 0 warnings found

```

AMI 1.2 um Two Stage Amplifier with Enhancement Mode Load

* simple spice

*

* File Location /msd16/falinj1/thesis/ami1r2/iclayout/j1f1r2c2

* File Created Sat Sep 25 14 13 35 1999

* Ext2spice Version ORNL 2.6.4 <=> Tue Jan 27 17 32 51 EST 1998

* Options -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g

*

** Subcircuit definition for buffern_r

** Extraction file is /msd16/falinj1/thesis/ami1r2/iclayout/j1f1r2c2/buffern_r ext

.SUBCKT buffern_r vdd 2 out gnd bias1

M1 vdd 2 out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0

M2 out bias1 gnd gnd CMOSN M=10 W=60 00U L=6 00U GEO=0

C1 out 2 1 3F

C2 out bias1 5 8F

C3 vdd 2 1 4F

C4 gnd bias1 7.2F

C5 out 0 19 8F

C6 2 0 50 0F

C7 vdd 0 10 4F

C8 bias1 0 100 1F

C9 gnd 0 14 9F

*** Node Listing for subckt: buffern_r

** N0 == IdealGND

** N2 [U=2] == 8_14_326#

** bias1 [U=2]

** gnd [U=4]

** out [U=3]

** vdd [U=2]

ENDS

** Subcircuit definition for diffpair

** Extraction file is /msd16/falinj1/thesis/ami1r2/iclayout/j1f1r2c2/diffpair ext

SUBCKT diffpair d1n vdd d1p damn gnd damp bias1

M1n d1n damp dabias gnd CMOSN M=8 W=60 00U L=1 20U GEO=0

M1p d1p damn dabias gnd CMOSN M=8 W=60 00U L=1 20U GEO=0

M2n d1n d1n vdd vdd CMOSP W=36 00U L=1 20U GEO=0

M2p d1p d1p vdd vdd CMOSP W=36 00U L=1 20U GEO=0

Mdabias dabias bias1 gnd gnd CMOSN M=14 W=60 00U L=6 00U GEO=0

C1 dabias damn 1 3F

C2 bias1 dabias 8 3F

C3 bias1 gnd 9.0F

C4 damp dabias 1 3F

C5 damp d1n 1 3F

C6 d1p damn 1 1F

C7 gnd 0 24 1F

C8 d1n 0 57.3F

C9 d1p 0 48 1F

C10 dabias 0 50.7F

C11 damn 0 61 2F

C12 damp 0 60 1F

C13 bias1 0 141.3F

```

*** Node Listing for subckt diffpair
** N0 == IdealGND
*****
** bias1 [U=2]
** d1n [U=4]
** d1p [U=4]
** dabias [U=3]
** damn [U=2]
** damp [U=2]
** gnd [U=5]
** vdd [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falinjl/thesis/am1r2/iclayout/jlf1r2c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0
M2 out bias1 gnd gnd CMOSN M=10 W=60.00U L=6 00U GEO=0
C1 out in 1 3F
C2 out bias1 5 8F
C3 vdd in 1 4F
C4 gnd bias1 7.2F
C5 gnd 0 14.9F
C6 out 0 19 8F
C7 vdd 0 10 3F
C8 bias1 0 100 1F
C9 in 0 50 0F
*** Node Listing for subckt buffern_1
** N0 == IdealGND
*****
** bias1 [U=2]
** gnd [U=4]
** in [U=2]
** out [U=3]
** vdd [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falinjl/thesis/am1r2/iclayout/jlf1r2c2/npbias ext
.SUBCKT npbias vdd gnd bias1
MB1 bias1 bias1 gnd gnd CMOSN W=60 00U L=6 00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=60 00U L=6 00U GEO=0
Mb3 bias1 bias2 sb3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 40U L=30.00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=12 00U L=2 40U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=6 00U L=2 40U GEO=0

Rbias rb gnd bias_r

*R2_2 2k rb gnd RPOLY SCALE=98 35
*R2_2 2k=2203 0 (width=1 20U)

```

```

C1 rb bias1 2 6F
C2 bias1 bias2 2 7F
C3 gnd bias2 1 7F
C4 rb 0 12 3F
C5 gnd 0 22 5F
C6 sb3 0 2 1F
C7 3 0 14 0F
C8 vdd 0 11 1F
C9 bias1 0 63 0F
C10 bias2 0 43 0F
C11 bias3 0 29 7F
*** Node Listing for subckt npbias
** N0 == IdealGND
** N3 [U=3] == 8_290_332#
*****
** bias1 [U=6]
** bias2 [U=5]
** bias3 [U=4]
** gnd [U=10]
** rb [U=2]
** sb3 [U=2]
** vdd [U=9]
ENDS
***** top level cell is /msd16/faliny/thesis/am1r2/iclayout/jlfr2c2/simple ext
** Instance-id buffern_r_0
X1 vdd 2 outn gnd bias1 buffern_r
** Instance-id diffpair_0
X2 2 vdd 6 inn gnd inp bias1 diffpair
** Instance-id buffern_l_0
X3 vdd 6 outp gnd bias1 buffern_l
** Instance-id npbias_0
X4 vdd gnd bias1 npbias
C1 gnd 0 38 2F
C2 outn 0 1 0F
C3 outp 0 15 6F
C4 6 0 3 8F
C5 inn 0 7 7F
C6 inp 0 11 8F
C7 vdd 0 14 6F
C8 2 0 2 8F
C9 bias1 0 56 9F
*** Node Listing for subckt simple
** N0 == IdealGND
** N2 [U=2] == diffpair_0/$d1n
** N6 [U=2] == buffern_l_0/$in
*****
** bias1 [U=4]
** gnd [U=4]
** inn [U=1]
** inp [U=1]
** outn [U=1]
** outp [U=1]
** vdd [U=4]
*****

```

```
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLY R RES=22 4
*0 errors and 0 warnings found
```

AMI 1.2 um Two Stage Amplifier with Resistive Load

* simpler_res.spice

*

* File Location /msd16/falinj1/thesis/am1r2/iclayout/jlf1r2c2

* File Created Sat Sep 25 13:38 40 1999

* Ext2spice Version ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998

* Options -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g

*

** Subcircuit definition for buffern_r

** Extraction file is /msd16/falinj1/thesis/am1r2/iclayout/jlf1r2c2/buffern_r.ext

SUBCKT buffern_r vdd 2 out gnd bias1

M1 vdd 2 out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0

M2 out bias1 gnd gnd CMOSN M=10 W=60 00U L=6 00U GEO=0

C1 out 2 1 3F

C2 out bias1 5.8F

C3 vdd 2 1 4F

C4 gnd bias1 7.2F

C5 out 0 19 8F

C6 2 0 50 0F

C7 vdd 0 10 4F

C8 bias1 0 100 1F

C9 gnd 0 14.9F

*** Node Listing for subckt buffern_r

** N0 == IdealGND

** N2 [U=2] == 8_14_326#

** bias1 [U=2]

** gnd [U=4]

** out [U=3]

** vdd [U=2]

ENDS

** Subcircuit definition for diffpair2

** Extraction file is /msd16/falinj1/thesis/am1r2/iclayout/jlf1r2c2/diffpair2.ext

SUBCKT diffpair2 d1p damn gnd d1n damp bias1

M1n d1n damp dabias gnd CMOSN M=8 W=60 00U L=1 20U GEO=0

M1p d1p damn dabias gnd CMOSN M=8 W=60 00U L=1 20U GEO=0

Mdabias dabias bias1 gnd gnd CMOSN M=15 W=60 00U L=6 00U GEO=0

C1 bias1 dabias 9 0F

C2 damp dabias 1 3F

C3 bias1 gnd 9 6F

C4 damn d1p 1 1F

C5 d1n damp 1 3F

C6 damn dabias 1 3F

C7 gnd 0 22 9F

C8 d1n 0 52 6F

C9 d1p 0 45 0F

C10 dabias 0 52 3F

C11 damn 0 61 2F

C12 damp 0 60 1F

C13 bias1 0 150 1F

*** Node Listing for subckt diffpair2

** N0 == IdealGND

```

*****
** bias1      [U=2]
** d1n        [U=2]
** d1p        [U=2]
** dabias     [U=3]
** damn       [U=2]
** damp       [U=2]
** gnd        [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falinj/thesis/am1r2/iclayout/jlf1r2c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0
M2 out bias1 gnd CMOSN M=10 W=60 00U L=6 00U GEO=0
C1 out in 1 3F
C2 out bias1 5 8F
C3 vdd in 1 4F
C4 gnd bias1 7 2F
C5 gnd 0 14 9F
C6 out 0 19 8F
C7 vdd 0 10 3F
C8 bias1 0 100.1F
C9 in 0 50 0F
*** Node Listing for subckt buffern_1
** N0          == IdealGND
*****
** bias1      [U=2]
** gnd        [U=4]
** in         [U=2]
** out        [U=3]
** vdd        [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falinj/thesis/am1r2/iclayout/jlf1r2c2/npbias ext
SUBCKT npbias vdd gnd bias1
MB1 bias1 bias1 gnd gnd CMOSN W=60 00U L=6 00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=60 00U L=6 00U GEO=0
Mb3 bias1 bias2 sb3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 40U L=30 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=12 00U L=2 40U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=6 00U L=2 40U GEO=0

Rbias rb gnd bias_r

*R2_2 2k rb gnd RPOLY SCALE=98 35
*R2_2 2k=2203 0 (width=1.20U)
C1 rb bias1 2 6F
C2 bias1 bias2 2 7F
C3 gnd bias2 1 7F

```

```

C4 rb 0 12 3F
C5 gnd 0 22 5F
C6 sb3 0 2 1F
C7 3 0 14 0F
C8 vdd 0 11 1F
C9 bias1 0 63 0F
C10 bias2 0 43 0F
C11 bias3 0 29 7F
*** Node Listing for subckt npbias
** N0 == IdealGND
** N3 [U=3] == 8_290_332#
*****
** bias1 [U=6]
** bias2 [U=5]
** bias3 [U=4]
** gnd [U=10]
** rb [U=2]
** sb3 [U=2]
** vdd [U=9]
ENDS
***** top level cell is /msd16/falunj/thesis/am1r2/iclayout/jlf1r2c2/simpler ext
** Instance-id buffern_r_0
X1 vdd 3 outn gnd bias1 buffern_r
** Instance-id diffpair2_0
X2 2 inn gnd 3 inp bias1 diffpair2
** Instance-id buffern_l_0
X3 vdd 2 outp gnd bias1 buffern_l
** Instance-id npbias_0
X4 vdd gnd bias1 npbias

Rn 3 vdd load_r

*R5n_2 4k vdd 3 RPOLY SCALE=106 85
* R5n_2 4k=2393 4 (width=1 20U)

Rp 2 vdd load_r

*R5p_2 4k vdd 2 RPOLY SCALE=106 85
* R5p_2 4k=2393 4 (width=1 20U)
C1 bias1 gnd 8 2F
C2 gnd 0 48 9F
C3 3 0 6 2F
C4 outp 0 13 6F
C5 inn 0 6 9F
C6 mp 0 10 3F
C7 2 0 10 3F
C8 vdd 0 8 1F
C9 bias1 0 49 1F
*** Node Listing for subckt simpler
** N0 == IdealGND
** N2 [U=3] == buffern_l_0/$in
** N3 [U=3] == diffpair2_0/$din
*****
** bias1 [U=4]

```

```

** gnd      [U=4]
** inn      [U=1]
** inp      [U=1]
** outn     [U=1]
** outp     [U=1]
** vdd      [U=5]
*****
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLY R RES=22 4
*0 errors and 0 warnings found

```

```

AMI 1 2 um Transimpedance Amplifier with Folded Cascode Stage
* fccgti2_res spice
*
* File Location      /msd16/falini/thesis/ami1r2/iclayout/jlf1r2c2
* File Created       Sat Sep 25 13 39 46 1999
* Ext2spice Version  ORNL 2 6 4 <=> Tue Jan 27 17 32.51 EST 1998
* Options            -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g
*
** Subcircuit definition for buffern_r
** Extraction file is /msd16/falini/thesis/ami1r2/iclayout/jlf1r2c2/buffern_r ext
SUBCKT buffern_r vdd 2 out gnd bias1
M1 vdd 2 out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0
M2 out bias1 gnd gnd CMOSN M=10 W=60 00U L=6 00U GEO=0
C1 out 2 1 3F
C2 out bias1 5 8F
C3 vdd 2 1 4F
C4 gnd bias1 7 2F
C5 out 0 19.8F
C6 2 0 50.0F
C7 vdd 0 10 4F
C8 bias1 0 100 1F
C9 gnd 0 14 9F
*** Node Listing for subckt buffern_r
** N0                == IdealGND
** N2                [U=2] == 8_14_326#
*****
** bias1             [U=2]
** gnd               [U=4]
** out               [U=3]
** vdd               [U=2]
ENDS

** Subcircuit definition for tiloop2_r
** Extraction file is /msd16/falini/thesis/ami1r2/iclayout/jlf1r2c2/tiloop2_r ext
SUBCKT tiloop2_r bias3 vdd bias2 in gnd out
**loop test
M3n 1 in gnd gnd CMOSN M=5 W=60 00U L=1 20U GEO=0
M4n out 1 9 gnd CMOSN M=5 W=60 00U L=1 20U GEO=0
Mb8n 1 bias3 vdd vdd CMOSP M=5 W=30 00U L=6 00U GEO=0
Mmb9n 4 bias2 1 vdd CMOSP M=5 W=30 00U L=6 00U GEO=0

Rf 9 in f_r

*R3_2k 9 in RPOLY SCALE=89.35
* R3_2k=2001 4 (width=1 20U)

Rout out vdd out_r

*R4_1 5k out vdd RPOLY SCALE=67 25
* R4_1 5k=1506 4 (width=1 20U)

R1 9 gnd bias1_r

```

```

*R6_800 9 gnd RPOLY SCALE=36 15
* R6_800=809 8 (width=1 20U)
C1 4 bias2 3 2F
C2 vdd bias3 2 8F
C3 1 bias3 3 2F
C4 in gnd 1 1F
C5 1 bias2 3 4F
C6 gnd 0 30 9F
C7 9 0 12 3F
C8 1 0 16 8F
C9 out 0 13 7F
C10 vdd 0 20 2F
C11 4 0 50 4F
C12 bias2 0 52 8F
C13 bias3 0 50 9F
C14 in 0 46 2F
*** Node Listing for subckt tiloop2_r
** N0 == IdealGND
** N1 [U=2] == 8_142_666#
** N4 [U=3] == 8_156_376#
** N9 [U=3] == 8_304_376#
*****
** bias2 [U=2]
** bias3 [U=2]
** gnd [U=5]
** in [U=3]
** out [U=3]
** vdd [U=5]
ENDS

** Subcircuit definition for diffpair5
** Extraction file is /msd16/falnlj/thesis/am11r2/iclayout/j1f1r2c2/diffpair5 ext
SUBCKT diffpair5 1 bias2 vdd bias3 7 damn gnd damp bias1
M1n d1n damp dabias gnd CMOSN M=8 W=30 00U L=1 20U GEO=0
M1p d1p damn dabias gnd CMOSN M=8 W=30 00U L=1 20U GEO=0
M2n 7 bias2 d1n vdd CMOSP W=30 00U L=2 40U GEO=0
M2p 1 bias2 d1p vdd CMOSP W=30 00U L=2 40U GEO=0
Mb7n d1n bias3 vdd vdd CMOSP M=7 W=60 00U L=6 00U GEO=0
Mb7p d1p bias3 vdd vdd CMOSP M=7 W=60 00U L=6 00U GEO=0
Mb11n 7 bias1 gnd gnd CMOSN M=4 W=60 00U L=6 00U GEO=0
Mb11p 1 bias1 gnd gnd CMOSN M=4 W=60 00U L=6 00U GEO=0
Mdabias dabias bias1 gnd gnd CMOSN M=6 W=60 00U L=6 00U GEO=0
C1 1 bias2 1 1F
C2 damp dabias 1 3F
C3 d1p bias2 2 7F
C4 bias3 vdd 9 4F
C5 bias1 1 4 6F
C6 d1p damn 1 1F
C7 bias3 d1n 4 5F
C8 damp d1n 1 3F
C9 bias1 gnd 9 0F
C10 dabias damn 1 3F
C11 bias1 dabias 3 5F
C12 bias3 d1p 4 5F

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```

C13 bias1 7 1 9F
C14 1 0 37.3F
C15 gnd 0 25 2F
C16 d1n 0 64 9F
C17 d1p 0 57.6F
C18 dabias 0 34 8F
C19 7 0 37 4F
C20 vdd 0 19 0F
C21 damn 0 56 3F
C22 damp 0 55 2F
C23 bias1 0 162 8F
C24 bias2 0 29 6F
C25 bias3 0 121 1F
*** Node Listing for subckt diffpair5
** N0 == IdealGND
** N1 [U=3] == 8_18_716#
** N7 [U=3] == 8_508_64#
*****
** bias1 [U=4]
** bias2 [U=3]
** bias3 [U=3]
** d1n [U=3]
** d1p [U=3]
** dabias [U=3]
** damn [U=2]
** damp [U=2]
** gnd [U=9]
** vdd [U=7]
ENDS

** Subcircuit definition for tiloop2_1
** Extraction file is /msd16/falunjl/thesis/am1r2/iclayout/jlfr2c2/tiloop2_1 ext
SUBCKT tiloop2_1 bias2 vdd bias3 out gnd in
M3p 1 in gnd gnd CMOSN M=5 W=60 00U L=1 20U GEO=0
M4p out 1 7 gnd CMOSN M=5 W=60 00U L=1 20U GEO=0
Mb8n 3 bias3 vdd vdd CMOSP M=5 W=30 00U L=6 00U GEO=0
Mb8p 1 bias2 3 vdd CMOSP M=5 W=30 00U L=6 00U GEO=0

Rf 7 in f_r

*R3_2k in 7 RPOLY SCALE=89 35
* R3_2k=2001 4 (width=1 20U)

Rout out vdd out_r

*R4_1 5k vdd out RPOLY SCALE=67 25
* R4_1 5k=1506 4 (width=1 20U)

R1 7 gnd bias1_r

*R6_800 gnd 7 RPOLY SCALE=36 15
* R6_800=809 8 (width=1 20U)
C1 bias3 3 3 2F
C2 bias2 3 3 4F

```

```

C3 vdd bias3 2 8F
C4 1 bias2 3 2F
C5 in gnd 1 2F
C6 gnd 0 30 8F
C7 3 0 16 8F
C8 out 0 13 5F
C9 1 0 50 4F
C10 vdd 0 20 1F
C11 7 0 12 3F
C12 bias2 0 52 6F
C13 bias3 0 51 0F
C14 in 0 46 2F
*** Node Listing for subckt  tiloop2_1
** N0                == IdealGND
** N1                [U=3] == 8_162_686#
** N3                [U=2] == 8_162_656#
** N7                [U=3] == 8_162_358#
*****
** bias2            [U=2]
** bias3            [U=2]
** gnd              [U=5]
** in               [U=3]
** out              [U=3]
** vdd              [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falinj/thesis/am1r2/iclayout/jlflr2c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0
M2 out bias1 gnd gnd CMOSN M=10 W=60 00U L=6 00U GEO=0
C1 out in 1 3F
C2 out bias1 5 8F
C3 vdd in 1 4F
C4 gnd bias1 7 2F
C5 gnd 0 14 9F
C6 out 0 19 8F
C7 vdd 0 10 3F
C8 bias1 0 100 1F
C9 in 0 50 0F
*** Node Listing for subckt  buffern_1
** N0                == IdealGND
*****
** bias1            [U=2]
** gnd              [U=4]
** in               [U=2]
** out              [U=3]
** vdd              [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falinj/thesis/am1r2/iclayout/jlflr2c2/npbias ext
SUBCKT npbias bias3 vdd 3 gnd bias2 bias1
MB1 bias1 bias1 gnd gnd CMOSN W=60 00U L=6 00U GEO=0

```

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MB2 bias2 bias1 rb gnd CMOSN M=4 W=60 00U L=6 00U GEO=0
Mb3 bias1 bias2 sb3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 40U L=30 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=12 00U L=2 40U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=6 00U L=2 40U GEO=0

Rbias rb gnd bias_r

*R2_2 2k rb gnd RPOLY SCALE=98 35
* R2_2 2k=2203 0 (width=1 20U)
C1 rb bias1 2 6F
C2 bias1 bias2 2 7F
C3 gnd bias2 1 7F
C4 rb 0 12 3F
C5 gnd 0 22 5F
C6 sb3 0 2 1F
C7 3 0 14 0F
C8 vdd 0 11 1F
C9 bias1 0 63 0F
C10 bias2 0 43 0F
C11 bias3 0 29 7F
*** Node Listing for subckt npbias
** N0 == IdealGND
** N3 [U=4] == 8_290_332#
*****
** bias1 [U=6]
** bias2 [U=6]
** bias3 [U=5]
** gnd [U=10]
** rb [U=2]
** sb3 [U=2]
** vdd [U=9]
.ENDS
***** top level cell is /msd16/falmlj/thesis/am1r2/iclayout/jlf1r2c2/fccgti2 ext
** Instance-id buffern_r_0
X1 vdd 2 outn gnd bias1 buffern_r
** Instance-id tiloop2_r_0
X2 bias3 vdd bias2 8 gnd 2 tiloop2_r
** Instance-id diffpair5_0
X3 9 bias2 vdd bias3 8 inn gnd inp bias1 diffpair5
** Instance-id tiloop2_l_0
X4 bias2 vdd bias3 12 gnd 9 tiloop2_l
** Instance-id buffern_l_0
X5 vdd 12 outp gnd bias1 buffern_l
** Instance-id npbias_0
X6 bias3 vdd 14 gnd bias2 bias1 npbias
C1 9 inn 1 0F
C2 bias2 bias3 2 2F
C3 gnd 0 78 4F
C4 outp 0 17 5F
C5 inn 0 20 1F

```

```

C6 inp 0 24 3F
C7 2 0 11 1F
C8 9 0 7 7F
C9 8 0 6 9F
C10 vdd 0 55 9F
C11 12 0 11 1F
C12 bias1 0 120 5F
C13 bias2 0 98 0F
C14 bias3 0 75 4F
*** Node Listing for subckt fccgt12
** N0          == IdealGND
** N2          [U=2] == t1loop2_r_0/$out
** N8          [U=2] == t1loop2_r_0/$in
** N9          [U=2] == t1loop2_l_0/$in
** N12         [U=2] == buffer1_l_0/$in
** N14         [U=1] == npbias_0/8_290_332#
*****
** bias1       [U=4]
** bias2       [U=4]
** bias3       [U=4]
** gnd         [U=6]
** inn         [U=1]
** inp         [U=1]
** outn        [U=1]
** outp        [U=1]
** vdd         [U=6]
*****
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLY R RES=22 4
*0 errors and 0 warnings found

```

AMI 1.2 um Transimpedance Amplifier with Current Mirror Stage

* cmcgti spice

*

* File Location /msd16/falinj1/thesis/ami1r2/iclayout/jlf1r2c2

* File Created Sat Sep 25 13.39.21 1999

* Ext2spice Version ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998

* Options -m -n -M -N -m -n -mg -M -N -h -n -mm -V -g

*

** Subcircuit definition for buffern_r

** Extraction file is /msd16/falinj1/thesis/ami1r2/iclayout/jlf1r2c2/buffern_r.ext

SUBCKT buffern_r vdd 2 out gnd bias1

M1 vdd 2 out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0

M2 out bias1 gnd gnd CMOSN M=10 W=60 00U L=6 00U GEO=0

C1 out 2 1 3F

C2 out bias1 5 8F

C3 vdd 2 1 4F

C4 gnd bias1 7 2F

C5 out 0 19 8F

C6 2 0 50 0F

C7 vdd 0 10 4F

C8 bias1 0 100 1F

C9 gnd 0 14 9F

*** Node Listing for subckt buffern_r

** N0 == IdealGND

** N2 [U=2] == 8_14_326#

** bias1 [U=2]

** gnd [U=4]

** out [U=3]

** vdd [U=2]

ENDS

** Subcircuit definition for tiloop_r

** Extraction file is /msd16/falinj1/thesis/ami1r2/iclayout/jlf1r2c2/tiloop_r.ext

SUBCKT tiloop_r bias3 vdd bias2 in gnd out

M3n 4 in gnd gnd CMOSN M=5 W=60 00U L=1 20U GEO=0

M4n out 4 9 gnd CMOSN M=5 W=60 00U L=1 20U GEO=0

Mb8n 1 bias3 vdd vdd CMOSP M=5 W=30 00U L=6 00U GEO=0

Mmb9n 4 bias2 1 vdd CMOSP M=5 W=30 00U L=6 00U GEO=0

R1 9 gnd bias1_r

*R1_1k 9 gnd RPOLY SCALE=44.15

* R1_1k=989 0 (width=1 20U)

Rf 9 in f_r

*R3_2k 9 in RPOLY SCALE=89.35

* R3_2k=2001.4 (width=1 20U)

Rout out vdd out_r

*R4_1.5k out vdd RPOLY SCALE=67.25

```

* R4_1 5k=1506.4 (width=1 20U)
C1 4 bias2 3 2F
C2 vdd bias3 2 8F
C3 1 bias3 3 2F
C4 in gnd 1 1F
C5 1 bias2 3 4F
C6 gnd 0 30 9F
C7 9 0 12 3F
C8 1 0 16 8F
C9 out 0 13 7F
C10 vdd 0 20 2F
C11 4 0 50 4F
C12 bias2 0 52.8F
C13 bias3 0 50 9F
C14 in 0 46 2F
*** Node Listing for subckt tiloop_r
** N0 == IdealGND
** N1 [U=2] == 8_142_666#
** N4 [U=3] == 8_156_376#
** N9 [U=3] == 8_304_376#
*****
** bias2 [U=2]
** bias3 [U=2]
** gnd [U=5]
** in [U=3]
** out [U=3]
** vdd [U=5]
.ENDS

** Subcircuit definition for diffpair3
** Extraction file is /msd16/falinjl/thesis/am1r2/iclayout/jlflr2c2/diffpair3 ext
.SUBCKT diffpair3 1 2 vdd damn gnd damp 12 13 bias1
M1n 9 damp dabias gnd CMOSN M=6 W=30 00U L=1 20U GEO=0
M1p 5 damn dabias gnd CMOSN M=6 W=30 00U L=1 20U GEO=0
M2na 9 9 vdd vdd CMOSP W=30 00U L=1 20U GEO=0
M2nb 11 9 vdd vdd CMOSP W=45 00U L=1 20U GEO=0
M2nc 12 13 11 vdd CMOSP W=60 00U L=1 20U GEO=0
M2pa 5 5 vdd vdd CMOSP W=30 00U L=1 20U GEO=0
M2pb 3 5 vdd vdd CMOSP W=45 00U L=1 20U GEO=0
M2pc 1 2 3 vdd CMOSP W=60 00U L=1 20U GEO=0
Mb1ln 12 bias1 gnd gnd CMOSN M=4 W=60.00U L=6 00U GEO=0
Mb1lp 1 bias1 gnd gnd CMOSN M=4 W=60 00U L=6 00U GEO=0
Mdabias dabias bias1 gnd gnd CMOSN M=5 W=60 00U L=6 00U GEO=0
C1 bias1 gnd 8 3F
C2 damn 5 1 1F
C3 bias1 12 1 9F
C4 bias1 dabias 2 8F
C5 damp dabias 1 0F
C6 bias1 1 1 9F
C7 damn dabias 1 0F
C8 gnd 0 32 5F
C9 12 0 11 8F
C10 5 0 44 6F
C11 9 0 44 9F

```

```

C12 1 0 13 1F
C13 3 0 2 6F
C14 13 0 3 8F
C15 dabias 0 29 9F
C16 11 0 2 6F
C17 2 0 3 4F
C18 vdd 0 40 3F
C19 damn 0 50 5F
C20 damp 0 49 9F
C21 bias1 0 147 7F
*** Node Listing for subckt diffpair3
** N0          == IdealGND
** N1          [U=3] == 8_197_125#
** N2          [U=2] == 8_189_86#
** N3          [U=2] == 8_183_125#
** N5          [U=4] == 8_157_135#
** N9          [U=4] == 8_10_81#
** N11         [U=2] == 8_440_121#
** N12         [U=3] == 8_318_419#
** N13         [U=2] == 8_466_76#
*****
** bias1       [U=4]
** dabias      [U=3]
** damn        [U=2]
** damp        [U=2]
** gnd         [U=9]
** vdd         [U=11]
ENDS

** Subcircuit definition for tiloop_1
** Extraction file is /msd16/falini/thesis/am1r2/iclayout/jlflr2c2/tiloop_1.ext
SUBCKT tiloop_1 bias2 vdd bias3 out gnd in
M3p 1 in gnd gnd CMOSN M=5 W=60 00U L=1 20U GEO=0
M4p out 1 7 gnd CMOSN M=5 W=60 00U L=1 20U GEO=0
Mb8n 3 bias3 vdd vdd CMOSP M=5 W=30 00U L=6 00U GEO=0
Mb8p 1 bias2 3 vdd CMOSP M=5 W=30 00U L=6 00U GEO=0

R1 7 gnd bias1_r

*R1_1k gnd 7 RPOLY SCALE=44 15
* R1_1k=989 0 (width=1 20U)

Rf 7 in f_r

*R3_2k in 7 RPOLY SCALE=89 35
* R3_2k=2001 4 (width=1 20U)

Rout out vdd out_r

*R4_1.5k vdd out RPOLY SCALE=67 25
* R4_1 5k=1506 4 (width=1 20U)
C1 bias3 3 3 2F
C2 bias2 3 3 4F
C3 vdd bias3 2 8F

```

```

C4 1 bias2 3 2F
C5 in gnd 1 2F
C6 gnd 0 30 8F
C7 3 0 16 8F
C8 out 0 13 5F
C9 1 0 50 4F
C10 vdd 0 20 1F
C11 7 0 12 3F
C12 bias2 0 52 6F
C13 bias3 0 51 0F
C14 in 0 46 2F
*** Node Listing for subckt  tiloop_1
** N0                == IdealGND
** N1                [U=3] == 8_162_686#
** N3                [U=2] == 8_162_656#
** N7                [U=3] == 8_162_358#
*****
** bias2            [U=2]
** bias3            [U=2]
** gnd              [U=5]
** in               [U=3]
** out              [U=3]
** vdd              [U=5]
ENDS

** Subcircuit definition for buffern_1
** Extraction file is /msd16/falinj1/thesis/am11r2/iclayout/jlf1r2c2/buffern_1 ext
SUBCKT buffern_1 vdd in out gnd bias1
M1 vdd in out gnd CMOSN M=10 W=60 00U L=1 20U GEO=0
M2 out bias1 gnd gnd CMOSN M=10 W=60 00U L=6 00U GEO=0
C1 out in 1 3F
C2 out bias1 5 8F
C3 vdd in 1 4F
C4 gnd bias1 7 2F
C5 gnd 0 14 9F
C6 out 0 19 8F
C7 vdd 0 10 3F
C8 bias1 0 100 1F
C9 in 0 50 0F
*** Node Listing for subckt  buffern_1
** N0                == IdealGND
*****
** bias1            [U=2]
** gnd              [U=4]
** in               [U=2]
** out              [U=3]
** vdd              [U=2]
ENDS

** Subcircuit definition for npbias
** Extraction file is /msd16/falinj1/thesis/am11r2/iclayout/jlf1r2c2/npbias ext
SUBCKT npbias bias3 vdd 3 gnd bias2 bias1
MB1 bias1 bias1 gnd gnd CMOSN W=60 00U L=6.00U GEO=0
MB2 bias2 bias1 rb gnd CMOSN M=4 W=60 00U L=6 00U GEO=0

```

```

Mb3 bias1 bias2 sb3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb4 bias2 bias2 bias3 vdd CMOSP W=60 00U L=6 00U GEO=0
Mb5 sb3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
Mb6 bias3 bias3 vdd vdd CMOSP W=60 00U L=6 00U GEO=0
MSU1 3 gnd vdd vdd CMOSP W=2 40U L=30 00U GEO=0
MSU2 3 bias1 gnd gnd CMOSN W=12 00U L=2 40U GEO=0
MSU3 bias2 3 gnd gnd CMOSN W=6 00U L=2 40U GEO=0

Rbias rb gnd bias_r

*R2_2 2k rb gnd RPOLY SCALE=98 35
* R2_2 2k=2203 0 (width=1 20U)
C1 rb bias1 2 6F
C2 bias1 bias2 2 7F
C3 gnd bias2 1 7F
C4 rb 0 12 3F
C5 gnd 0 22.5F
C6 sb3 0 2 1F
C7 3 0 14 0F
C8 vdd 0 11 1F
C9 bias1 0 63 0F
C10 bias2 0 43 0F
C11 bias3 0 29 7F
*** Node Listing for subckt npbias
** N0      ✓      = IdealGND
** N3      [U=4]  = 8_290_332#
*****
** bias1    [U=6]
** bias2    [U=6]
** bias3    [U=5]
** gnd      [U=10]
** rb       [U=2]
** sb3      [U=2]
** vdd      [U=9]
ENDS
***** top level cell is /msd16/falinj1/thesis/am1r2/iclayout/jlf1r2c2/cmcgti ext
** Instance-id buffern_r_0
X1 vdd 2 outn gnd bias1 buffern_r
** Instance-id tiloop_r_0
X2 bias3 vdd bias2 8 gnd 2 tiloop_r
** Instance-id diffpair3_0
X3 9 bias2 vdd inn gnd inp 8 bias2 bias1 diffpair3
** Instance-id tiloop_l_0
X4 bias2 vdd bias3 12 gnd 9 tiloop_l
** Instance-id buffern_l_0
X5 vdd 12 outp gnd bias1 buffern_l
** Instance-id npbias_0
X6 bias3 vdd 14 gnd bias2 bias1 npbias
C1 bias2 bias3 1 9F
C2 gnd 0 97 5F
C3 outp 0 17 5F
C4 8 0 6 5F
C5 inn 0 15.5F
C6 inp 0 16 9F

```

```

C7 12 0 11 1F
C8 2 0 11 1F
C9 9 0 7 8F
C10 vdd 0 66 5F
C11 bias1 0 116 7F
C12 bias2 0 99.5F
C13 bias3 0 80 1F
*** Node Listing for subckt cmcgti
** N0          == IdealGND
** N2          [U=2] == tiloop_r_0/$out
** N8          [U=2] == tiloop_r_0/$in
** N9          [U=2] == tiloop_l_0/$in
** N12         [U=2] == buffern_l_0/$in
** N14         [U=1] == npbias_0/8_290_332#
*****
** bias1       [U=4]
** bias2       [U=5]
** bias3       [U=3]
** gnd         [U=6]
** inn         [U=1]
** mp          [U=1]
** outn        [U=1]
** outp        [U=1]
** vdd         [U=6]
*****
*
* Model Definitions for HSPICE
*
*****
MODEL RPOLY R RES=22 4
*0 errors and 0 warnings found

```

APPENDIX 3

* AMI 0.8 um N87R SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

*Used for initial designs

* DATE 98 Sep 14

* LOT. n87r WAF 106

```
MODEL CMOSN NMOS ( ACM=3 HDIF=1.0u LEVEL =49
+VERSION=3.1 TNOM =27 TOX =1.65E-8
+XJ =1.5E-7 NCH =1.7E17 VTH0 =0.6475503
+K1 =0.8734941 K2 =-0.045857 K3 =17.9015005
+K3B =-1.8111522 W0 =1E-6 NLX =1.105246E-9
+DVT0W =0 DVT1W =5.3E6 DVT2W =-0.032
+DVT0 =2.8726722 DVT1 =0.4252235 DVT2 =-0.1128732
+U0 =568.5118192 UA =1.357156E-9 UB =2.975976E-19
+UC =3.854652E-11 VSAT =1.05052E5 A0 =0.7236503
+AGS =0.1204483 B0 =2.260419E-7 B1 =6.503398E-7
+KETA =-0.0100045 A1 =0 A2 =1
+RDSW =1.782947E3 PRWG =-9.689924E-4 PRWB =-6.924912E-7
+WR =1 WINT =1.542158E-7 LINT =2.137216E-7
+DWG =-1.384742E-8 DWB =3.140163E-8 VOFF =-0.0807621
+NFACTOR=1.2659085 CIT =0 CDSC =1.506004E-4
+CDSCD =0 CDSCB =0 ETA0 =2.313075E-3
+ETAB =-9.030716E-4 DSUB =0.0428175 PCLM =0.8408931
+PDIBLC1=0.0623678 PDIBLC2=1.507727E-3 PDIBLCB=-1E-3
+DROUT =0.4497387 PSCBE1 =4.664096E9 PSCBE2 =2.985985E-8
+PVAG =0.0163863 DELTA =0.01 MOBMOD =1
+PRT =-104.8 UTE =-1.5 KT1 =-0.3059
+KTIL =1.094E-9 KT2 =-0.02846 UA1 =2.151E-9
+UB1 =-3.961E-18 UC1 =-7.346E-11 AT =3.3E4
+WL =0 WLN =1 WW =0
+WWN =1 WWL =0 LL =0
+LLN =1 LW =0 LWN =1
+LWL =0 CAPMOD =2 CGDO =3.5E-10
+CGSO =3.5E-10 CGBO =0 CJ =4.342775E-4
+PB =0.9592711 MJ =0.4534652 CJSW =3.256445E-10
+PBSW =0.2561474 MJSW =0.158096 PVTH0 =-5.837896E-5
+PRDSW =-474.7501239 PK2 =0.0122217 WKETA =4.600566E-3
+LKETA =1.41793E-3 )
```

*

```
MODEL CMOSP PMOS (ACM=3 HDIF=1.0u LEVEL =49
+VERSION=3.1 TNOM =27 TOX =1.65E-8
+XJ =1.5E-7 NCH =1.7E17 VTH0 =-1.0082743
+K1 =0.4081232 K2 =0.0297155 K3 =12.6429294
+K3B =-1.3119983 W0 =1.068181E-6 NLX =5.461663E-8
+DVT0W =0 DVT1W =5.3E6 DVT2W =-0.032
+DVT0 =3.7963632 DVT1 =0.5066295 DVT2 =-0.0825464
+U0 =224.8724776 UA =2.665604E-9 UB =1.163208E-18
+UC =-4.32667E-11 VSAT =1.806072E5 A0 =1.0129268
+AGS =0.1352013 B0 =1.237387E-6 B1 =2E-6
+KETA =-2.376454E-3 A1 =0 A2 =1
+RDSW =2.353688E3 PRWG =-6.109639E-5 PRWB =-1E-3
+WR =1 WINT =2.19873E-7 LINT =1.731755E-7
+DWG =-2.936332E-8 DWB =2.385534E-8 VOFF =-0.0787892
+NFACTOR=1.0882083 CIT =0 CDSC =4.363744E-4
+CDSCD =0 CDSCB =0 ETA0 =0.0895166
```

```

+ETAB =-0 0102423  DSUB =0 3402012  PCLM =7 1674779
+PDIBLC1=9 999667E-4  PDIBLC2=0 01  PDIBLCB=-1E-3
+DROUT =0 5924894  PSCBE1 =3 519381E9  PSCBE2 =5 004941E-9
+PVAG =14 6719474  DELTA =0 01  MOBMOD =1
+PRT =-450 8  UTE =-1 5  KT1 =-0 4576
+KT1L =2 98E-9  KT2 =-0 02865  UA1 =-4 244E-10
+UB1 =-1.619E-18  UC1 =-1 138E-12  AT =3 3E4
+WL =0  WLN =1  WW =0
+WWN =1  WWL =0  LL =0
+LLN =1  LW =0  LWN =1
+LWL =0  CAPMOD =2  CGDO =3 5E-10
+CGSO =3.5E-10  CGBO =0  CJ =6 197711E-4
+PB =0 9224372  MJ =0 4882693  CJSW =4 753739E-10
+PBSW =0 99  MJSW =0 445593  PVTH0 =0 0407148
+PRDSW =-680 3241219  PK2 =4 241444E-3  WKETA =7 531357E-3
+LKETA =-1 310892E-3 )
*
* AMI 0 8 um N91Y SPICE BSIM3 VERSION 3 1 (HSPICE Level 49) PARAMETERS
*Use for test transistor simulations
* DATE Mar 3/99
* LOT n91y WAF 03
* Temperature_parameters=Default
.MODEL CMOSN NMOS ( LEVEL =49
+VERSION=3.1  TNOM =27  TOX =1 64E-8
+XJ =2 5E-7  NCH =8E16  VTH0 =0 6812727
+K1 =0.884817  K2 =-0 0436447  K3 =13 4787949
+K3B =-2 3815393  W0 =6 12328E-7  NLX =1 20287E-9
+DVT0W =0  DVT1W =5 3E6  DVT2W =-0 032
+DVT0 =2 1839642  DVT1 =0 5679128  DVT2 =-0 15
+U0 =557 4473897  UA =1 034171E-9  UB =8 414321E-19
+UC =4 336661E-11  VSAT =1 052228E5  A0 =0 7878654
+AGS =0 148654  B0 =9 326963E-7  B1 =4 880547E-6
+KETA =-9 388917E-3  A1 =0  A2 =1
+RDSW =1 872799E3  PRWG =9 46047E-4  PRWB =-5 027015E-8
+WR =1  WINT =1.756516E-7  LINT =1 191556E-7
+XL =-2E-7  XW =0  DWG =-1 85177E-8
+DWB =2 209169E-8  VOFF =-0.127116  NFACTOR=0 6149106
+CIT =0  CDSC =1 506004E-4  CDSCD =0
+CDSCB =0  ETA0 =4 632235E-4  ETAB =-1 662268E-3
+DSUB =0 2190063  PCLM =0 6861394  PDIBLC1=0 0335521
+PDIBLC2=5 116937E-3  PDIBLCB=0  DROUT =0 3858137
+PSCBE1 =6 150319E9  PSCBE2 =3 885201E-8  PVAG =8 173574E-3
+DELTA =0 01  MOBMOD =1  PRT =0
+UTE =-1.5  KT1 =-0 11  KT1L =0
+KT2 =0 022  UA1 =4 31E-9  UB1 =-7 61E-18
+UC1 =-5.6E-11  AT =3 3E4  WL =0
+WLN =1  WW =0  WWN =1
+WWL =0  LL =0  LLN =1
+LW =0  LWN =1  LWL =0
+CAPMOD =2  XPART =0 4  CGDO =3 50E-10
+CGSO =3 50E-10  CGBO =0  CJ =4 342201E-4
+PB =0 99  MJ =0 4609667  CJSW =3 334674E-10
+PBSW =0 1237512  MJSW =0 1236883  PVTH0 =-0 0224301
+PRDSW =-533 5283178  PK2 =7.749552E-4  WKETA =6 071497E-4

```

```

+LKETA =-5 617395E-3 )
*
MODEL CMOS PMOS (          LEVEL = 49
+VERSION=3 1      TNOM =27      TOX =1.64E-8
+XJ  =2 5E-7      NCH  =5E16      VTH0 =-0 9462535
+K1   =0 4190301   K2   =0 0239883   K3   =17 3448063
+K3B  =-2 8701495   W0   =1 699874E-6   NLX  =2 357712E-10
+DVT0W =0          DVT1W =5 3E6      DVT2W =-0 032
+DVT0  =4 5327967   DVT1  =0 7694776   DVT2  =-0 0793944
+U0   =213 1081162   UA   =2 44944E-9   UB   =9 341763E-19
+UC   =-4 61844E-11  VSAT =1 316508E5   A0   =1 0047963
+AGS  =0 1711866    B0   =1 994481E-6   B1   =5E-6
+KETA  =-4 005141E-3  A1   =0          A2   =1
+RDSW  =2 036346E3   PRWG  =-1 168572E-4  PRWB  =-1E-3
+WR   =1            WINT  =2 383435E-7   LINT  =4 876362E-8
+XL   =-2E-7        XW   =0          DWG   =-2 485686E-8
+DWB  =1 659405E-8   VOFF  =-0 1009826   NFACTOR=2
+CIT  =0            CDSC  =4 363744E-4   CDSCD  =0
+CDSCB =0           ETA0  =0.0978267   ETAB  =0
+DSUB  =0 3387922    PCLM  =9 9914184   PDIBLC1=2 485702E-5
+PDIBLC2=0 01        PDIBLCB=0          DROUT  =0 999105
+PSCBE1 =3 49925E9   PSCBE2 =4 976312E-9   PVAG  =10 9858631
+DELTA =0 01         MOBMOD =1          PRT   =0
+UTE   =-1 5        KT1   =-0 11        KTIL  =0
+KT2   =0 022        UA1   =4 31E-9       UB1   =-7 61E-18
+UC1   =-5 6E-11     AT    =3 3E4        WL    =0
+WLN   =1           WW    =0           WWN    =1
+WWL   =0           LL    =0           LLN    =1
+LW    =0           LWN   =1           LWL    =0
+CAPMOD =2          XPART =0 4          CGDO   =3 50E-10
+CGSO   =3 50E-10    CGBO  =0          CJ     =6 252903E-4
+PB     =0 8904596    MJ    =0 4772585    CJSW   =4 144426E-10
+PBSW   =0 99        MJSW  =0.426664    PVTH0  =0 0597171
+PRDSW  =-980 3241219  PK2   =4 057951E-4   WKETA  =4 488089E-3
+LKETA  =-1.678619E-3 )

```

*

* AMI 0.8 um N97L SPICE BSIM3 VERSION 3.1 PARAMETERS

*Used for simulations to compare to amplifier measurements

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE Aug 18/99

* LOT n97l WAF 03

* Temperature_parameters=Default

```

MODEL CMOSN NMOS (          LEVEL = 49
+VERSION=3 1      TNOM =27      TOX =1 55E-8
+XJ  =2 5E-7      NCH  =8E16      VTH0 =0 641718
+K1   =0 8346873   K2   =-0 042465   K3   =12 7624417
+K3B  =-4 280204   W0   =1 224565E-6   NLX  =1E-8
+DVT0W =0          DVT1W =0          DVT2W =0
+DVT0  =2 3259952   DVT1  =0 5694154   DVT2  =-0 1213192
+U0   =518 874611   UA   =4 751316E-10   UB   =1 421977E-18
+UC   =2 777785E-11  VSAT =1 089724E5   A0   =0 7159742
+AGS  =0 1226906    B0   =1 260351E-6   B1   =5E-6
+KETA  =-9 215897E-3  A1   =0          A2   =1

```

```

+RDSW = 1 959338E3  PRWG = -0 0156176  PRWB = -3 095218E-7
+WR = 1  WINT = 1 794755E-7  LINT = 1 270467E-7
+XL = -2E-7  XW = 0  DWG = -2 481101E-8
+DWB = 1 141719E-8  VOFF = -0 0461706  NFACTOR = 1 2249987
+CIT = 0  CDSC = 8 997141E-5  CDSCD = 0
+CDSCB = 1.601628E-6  ETA0 = 7 778461E-3  ETAB = -0 0159169
+DSUB = 0 5668366  PCLM = 0 6901938  PDIBLC1 = 0 0327512
+PDIBLC2 = 4 519874E-3  PDIBLCB = -6 055372E-5  DROUT = 0 3916408
+PSCBE1 = 6 165635E9  PSCBE2 = 3.895022E-8  PVAG = 8 271536E-3
+DELTA = 0 01  MOBMOD = 1  PRT = 0
+UTE = -1 5  KT1 = -0 11  KT1L = 0
+KT2 = 0 022  UA1 = 4.31E-9  UB1 = -7 61E-18
+UC1 = -5 6E-11  AT = 3 3E4  WL = 0
+WLN = 1  WW = 0  WWN = 1
+WWL = 0  LL = 0  LLN = 1
+LW = 0  LWN = 1  LWL = 0
+CAPMOD = 2  XPART = 0 4  CGDO = 1 82E-10
+CGSO = 1 82E-10  CGBO = 0  CJ = 4 383428E-4
+PB = 0 95242  MJ = 0 440893  CJSW = 3.672664E-10
+PBSW = 0 1203645  MJSW = 0 13661  PVTH0 = -0 0158267
+PRDSW = -565 2171303  PK2 = -1 149287E-3  WKETA = 1 719375E-4
+LKETA = 2.545281E-4  acm=3  hdiff=1 0u )

```

*

```

.MODEL CMOS PMOS (  LEVEL = 49
+VERSION = 3 1  TNOM = 27  TOX = 1 55E-8
+XJ = 2 5E-7  NCH = 5E16  VTH0 = -0 8875042
+K1 = 0 3369914  K2 = 0 0371665  K3 = 19 1068598
+K3B = -4 9002263  W0 = 2 995004E-6  NLX = 2 015444E-7
+DVT0W = 0  DVT1W = 0  DVT2W = 0
+DVT0 = 2 7785049  DVT1 = 0.5598794  DVT2 = -0 0832108
+U0 = 206 4070087  UA = 2 442882E-9  UB = 5 717441E-20
+UC = -5 59977E-11  VSAT = 1 942916E5  A0 = 0 6065878
+AGS = 0 0158204  B0 = 3 358896E-6  B1 = 5E-6
+KETA = 2 311465E-3  A1 = 0  A2 = 1
+RDSW = 2 129402E3  PRWG = 1 262219E-3  PRWB = -0 0228669
+WR = 1  WINT = 1 793093E-7  LINT = 6 008561E-8
+XL = -2E-7  XW = 0  DWG = -1 882411E-8
+DWB = 2 402293E-8  VOFF = -0 047527  NFACTOR = 1 1406197
+CIT = 0  CDSC = 2 771735E-6  CDSCD = 1 041857E-5
+CDSCB = 3 087982E-4  ETA0 = 0 0703497  ETAB = -6 11347E-4
+DSUB = 0 3547864  PCLM = 5 063164  PDIBLC1 = 1 071833E-4
+PDIBLC2 = 0 0215228  PDIBLCB = 0 1  DROUT = 0 0525797
+PSCBE1 = 1 944839E9  PSCBE2 = 2 320666E-9  PVAG = 0 0925467
+DELTA = 0 01  MOBMOD = 1  PRT = 0
+UTE = -1 5  KT1 = -0 11  KT1L = 0
+KT2 = 0 022  UA1 = 4 31E-9  UB1 = -7 61E-18
+UC1 = -5 6E-11  AT = 3 3E4  WL = 0
+WLN = 1  WW = 0  WWN = 1
+WWL = 0  LL = 0  LLN = 1
+LW = 0  LWN = 1  LWL = 0
+CAPMOD = 2  XPART = 0 4  CGDO = 2 91E-10
+CGSO = 2 91E-10  CGBO = 0  CJ = 6 184038E-4
+PB = 0 8945284  MJ = 0 479411  CJSW = 4 379993E-10
+PBSW = 0 99  MJSW = 0 4208291  PVTH0 = 0 0492405

```

```

+PRDSW = -1 3E3    PK2 = 1 348997E-3  WKETA = -7 720116E-3
+LKETA = -8 9419E-3  acm=3 hdif=1 0u )
*
*AMI 1.2 um N88Z SPICE BSIM3 VERSION 3 1 (HSPICE Level 49) PARAMETERS
*Used for initial designs

```

```

* DATE Oct 19/98
* LOT n88z      WAF: 03
* Temperature_parameters=Default
MODEL CMOSN NMOS (          LEVEL = 49
+VERSION = 3 1    TNOM = 27    TOX = 3 04E-8
+XJ = 3E-7    NCH = 7 5E16    VTH0 = 0 5815607
+K1 = 0 9340278  K2 = -0 0670013  K3 = 4 2645743
+K3B = -2 149369  W0 = 2 544414E-7  NLX = 1 146796E-7
+DVT0W = 0    DVT1W = 5 3E6    DVT2W = -0 032
+DVT0 = 1 8024609  DVT1 = 0 4371369  DVT2 = -0 1548912
+U0 = 640 0382895  UA = 1 134603E-9  UB = 4 305021E-18
+UC = 6 425777E-11  VSAT = 1 025002E5  A0 = 0 6075572
+AGS = 0 1089496  B0 = 9 758203E-7  B1 = 9 451406E-7
+KETA = -0 0121885  A1 = 0    A2 = 1
+RDSW = 2 163377E3  PRWG = -1E-3    PRWB = 6 127803E-3
+WR = 1    WINT = 6 756618E-7  LINT = 1 125536E-7
+DWG = -1 937825E-8  DWB = 2 628633E-8  VOFF = -0.0836217
+NFACTOR = 0 4949859  CIT = 0    CDSC = 2 4E-4
+CDSCD = 0    CDSCB = 0    ETA0 = 0 1365138
+ETAB = -0 042698  DSUB = 0 5907438  PCLM = 1 1870837
+PDIBLC1 = 5 419543E-3  PDIBLC2 = 1 208657E-3  PDIBLCB = 0
+DROUT = 0 0281681  PSCBE1 = 1 072772E9  PSCBE2 = 5 002526E-9
+PVAG = 0 0523589  DELTA = 0 01    MOBMOD = 1
+PRT = 0    UTE = -1 5    KT1 = -0 11
+KT1L = 0    KT2 = 0 022  UA1 = 4 31E-9
+UB1 = -7 61E-18  UC1 = -5 6E-11  AT = 3 3E4
+WL = 0    WLN = 1    WW = 0
+WWN = 1    WWL = 0    LL = 0
+LLN = 1    LW = 0    LWN = 1
+LWL = 0    CAPMOD = 2    CGDO = 2 7E-10
+CGSO = 2 7E-10  CGBO = 0    CJ = 2 806451E-4
+PB = 0 9785784  MJ = 0.5305733  CJSW = 1 464911E-10
+PBSW = 0 99    MJSW = 0 1    PVTH0 = -0 0614433
+PRDSW = -989 097  PK2 = -5 38285E-3  WKETA = 4 117011E-3
+LKETA = -9 8354E-4  PAGS = 0 482296 acm=3 hdif=1 0u )
*

```

```

MODEL CMOSP PMOS (          LEVEL = 49
+VERSION = 3 1    TNOM = 27    TOX = 3 04E-8
+XJ = 3E-7    NCH = 2 4E16    VTH0 = -0 8058627
+K1 = 0 4627141  K2 = -3 916965E-3  K3 = 13 4883082
+K3B = -2 5656586  W0 = 2 209688E-7  NLX = 6 936779E-7
+DVT0W = 0    DVT1W = 5 3E6    DVT2W = -0 032
+DVT0 = 2 431363  DVT1 = 0 5455412  DVT2 = -0 0725453
+U0 = 268 4532224  UA = 4 801783E-9  UB = 4 238494E-18
+UC = -1E-10  VSAT = 1 09645E5  A0 = 0 2531802
+AGS = 0 155562  B0 = 4 547478E-6  B1 = 1 951094E-6
+KETA = -0 0135114  A1 = 0    A2 = 1
+RDSW = 1 45858E3  PRWG = -1E-3    PRWB = -1E-3

```

```

+WR =1      WINT =6 473685E-7 LINT =9 093131E-9
+DWG =-1 555331E-8 DWB =3 228232E-8 VOFF =-0 0672947
+NFACTOR =0 9890363 CIT =0      CDSC =4 036955E-4
+CDSCD =0      CDSCB =0      ETA0 =0 0188953
+ETAB =0      DSUB =0 0223077 PCLM =15
+PDIBLC1 =0      PDIBLC2 =1E-5 PDIBLCB =0
+DROUT =3 896422E-3 PSCBE1 =1.83251E10 PSCBE2 =5 004583E-9
+PVAG =0      DELTA =0 01      MOBMOD =1
+PRT =0      UTE =-1.5      KT1 =-0 11
+KT1L =0      KT2 =0 022      UA1 =4 31E-9
+UB1 =-7 61E-18 UC1 =-5 6E-11 AT =3 3E4
+WL =0      WLN =1      WW =0
+WWN =1      WWL =0      LL =0
+LLN =1      LW =0      LWN =1
+LWL =0      CAPMOD =2      CGDO =2 7E-10
+CGSO =2 7E-10 CGBO =0      CJ =2 959698E-4
+PB =0 7491338 MJ =0 4414592 CJSW =1 464496E-10
+PBSW =0 9434007 MJSW =0 1      PVTH0 =0 188273
+PRDSW =-990 PK2 =-0 0146098 WKETA =0 0149993
+LKETA =0 0152763 PAGS =2 85026 acm=3 hdi=1 0u )

```

*

*AMI 1 2 um N95Y SPICE BSIM3 VERSION 3 1 PARAMETERS

*Used for simulations to compare to amplifier measurements and for test transistors

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE Jun 24/99

* LOT n95y WAF 02

* Temperature parameters=Default

MODEL CMOSN NMOS (LEVEL =49

```

+VERSION =3 1      TNOM =27      TOX =3 11E-8
+XJ =3E-7      NCH =7 5E16      VTH0 =0 5834233
+K1 =0 9177281 K2 =-0 0645085 K3 =0 7218676
+K3B =-2 1436597 W0 =1 38605E-6 NLX =2 949215E-8
+DVT0W =0      DVT1W =5 3E6      DVT2W =-0 032
+DVT0 =1 1953557 DVT1 =0 2894027 DVT2 =-0 1073775
+U0 =690 3062808 UA =2 27506E-9 UB =2 747214E-20
+UC =4 103336E-11 VSAT =1 255459E5 A0 =0 7056633
+AGS =0 113066 B0 =1 071322E-6 B1 =4 846043E-6
+KETA =-5 726829E-3 A1 =0      A2 =1
+RDSW =2 797196E3 PRWG =-0 0359635 PRWB =-9 895222E-5
+WR =1      WINT =6 863558E-7 LINT =2 296937E-7
+XL =0      XW =0      DWG =-2 950268E-8
+DWB =2 716552E-8 VOFF =-0 0403502 NFACTOR =0 0481384
+CIT =0      CDSC =2 957397E-4 CDSCD =0
+CDSCB =2 092898E-4 ETA0 =-0 0899643 ETAB =-0 103832
+DSUB =0 7310526 PCLM =0 8928755 PDIBLC1 =0 0657939
+PDIBLC2 =9 574009E-3 PDIBLCB =-1E-3 DROUT =0 3337441
+PSCBE1 =2 457301E9 PSCBE2 =1 09611E-8 PVAG =0 0243388
+DELTA =0 01      MOBMOD =1      PRT =0
+UTE =-1 5      KT1 =-0 11      KT1L =0
+KT2 =0 022      UA1 =4 31E-9      UB1 =-7 61E-18
+UC1 =-5 6E-11 AT =3 3E4      WL =0
+WLN =1      WW =0      WWN =1

```

```

+WWL =0      LL =0      LLN =1
+LW =0      LWL =1      LWL =0
+CAPMOD =2      XPART =0.4      CGDO =1.6E-10
+CGSO =1.6E-10      CGBO =0      CJ =2.831035E-4
+PB =0.9742751      MJ =0.5233163      CJSW =1.499584E-10
+PBSW =0.9899938      MJSW =0.1      PVTH0 =0.0522966
+PRDSW =-816.757313      PK2 =-3.06274E-3      WKETA =-1.604076E-3
+LKETA =-0.0154349      acm=3      hdif=1.0u )

```

*

```

.MODEL CMOS PMOS (      LEVEL =49
+VERSION=3.1      TNOM =27      TOX =3.11E-8
+XJ =3E-7      NCH =2.4E16      VTH0 =-0.8707461
+K1 =0.4533691      K2 =-4.26725E-6      K3 =8.1004871
+K3B =-2.8196525      W0 =1.523558E-6      NLX =5.883224E-7
+DVT0W =0      DVT1W =5.3E6      DVT2W =-0.032
+DVT0 =1.1416024      DVT1 =0.267023      DVT2 =-0.0515191
+U0 =267.9805436      UA =4.851956E-9      UB =1.020281E-20
+UC =-8.83788E-11      VSAT =1.844714E5      A0 =0.3956586
+AGS =0.106958      B0 =4.821438E-6      B1 =5E-6
+KETA =0.0104968      A1 =0      A2 =1
+RDSW =1.658522E3      PRWG =0.0494189      PRWB =-0.4784961
+WR =1      WINT =7.619443E-7      LINT =5.866791E-8
+XL =0      XW =0      DWG =-4.047892E-8
+DWB =2.525684E-8      VOFF =-0.0432922      NFACTOR=0
+CIT =0      CDSC =6.146378E-5      CDSCD =0
+CDSCB =1.741688E-6      ETA0 =0.0128587      ETAB =9.007555E-5
+DSUB =0.014281      PCLM =10.2292554      PDIBLC1=0.094122
+PDIBLC2=1E-6      PDIBLCB=4.381676E-4      DROUT =0.5020934
+PSCBE1=1.905232E10      PSCBE2=5.203185E-9      PVAG =1.7473999
+DELTA =0.01      MOBMOD=1      PRT =0
+UTE =-1.5      KT1 =-0.11      KTIL =0
+KT2 =0.022      UA1 =4.31E-9      UB1 =-7.61E-18
+UC1 =-5.6E-11      AT =3.3E4      WL =0
+WLN =1      WW =0      WWN =1
+WWL =0      LL =0      LLN =1
+LW =0      LWL =1      LWL =0
+CAPMOD =2      XPART =0.4      CGDO =2.11E-10
+CGSO =2.11E-10      CGBO =0      CJ =3.088002E-4
+PB =0.7572848      MJ =0.4470466      CJSW =2.191562E-10
+PBSW =0.9892851      MJSW =0.1420903      PVTH0 =-5.90657E-3
+PRDSW =-681.5148875      PK2 =0.0119686      WKETA =3.49834E-3
+LKETA =-0.0305345      acm=3      hdif=1.0u)

```

*

APPENDIX 4

*AMI 1.2um - Two Stage Amplifier with Enhancement Mode Load
*gain and phase measurement simulation file

```
.param vdd_rail=5
.param cm_v=1.5
.param load_cap=10pf
.param rbias=2203
.param bias_r=('rbias*1')

ac dec 50 100k 1000e6
.op

.tf V(outn,output) Vin

vgnd gnd 0 dc 0
Vpower vdd 0 dc vdd_rail
Einn inn vcm vin 0 0 5
Einp inp vcm vin 0 -0.5
Vicm vcm 0 dc cm_v
Vin vin 0 dc 0 ac 1
Rin vin 0 1k

Cln outn gnd load_cap

Clp outp gnd load_cap

include 'e:\8qm\thesis\amilr2\iclayout\simple_res spice'
include 'n88z_enh.models'

.probe ac
+ tc=par('im1(x2.m1n)/vm(inp)')
+ re=par('1/(im1(x2.m2n)/vm(2))')
+ onesidegain=par('20*log10(vm(outn)/vm(inp)/2)')
+ phase_a=par('VP(outn)-VP(inp)')
+ phase_b=par('VP(outp)-VP(inn)')
+ buffer=par('vm(outn)/vm(2)')

options POST CONVERGE=1 METHOD=GEAR
.alter
.param bias_r=('rbias*0.8')
.alter
.param bias_r=('rbias*1 2')

END
```

APPENDIX 5

*AMI 1.2um - Two Stage Amplifier with Enhancement Mode Load
*noise simulation file

```
param vdd_rail=5  
.param cm_v=2 5  
.param load_cap=5pf  
.param r_bias=2203  
.param bias_r=par('1.7*r_bias')
```

```
.noise v(outp) Vnoise 5
```

```
.ac dec 50 10 500e6  
.op
```

```
vgnd gnd 0 dc 0  
Vpower vdd 0 dc vdd_rail
```

```
Vnoise inp 0 dc 2.5 ac 1  
Vcm inn 0 dc 2.5 ac 0
```

```
Cln outn gnd load_cap
```

```
Clp outp gnd load_cap
```

```
.include 'e:\8qm\thesis\ami1r2\iclayout\simple_res spice'  
.include 'n95y_enh.models'
```

```
.options POST CONVERGE=1
```

```
.END
```

VITA

VITA

Jeffrey Lynn Falin was born in Kingsport, Tennessee on September 7, 1969. He attended Scott County Public schools and graduated as valedictorian from Gate City High School in May 1987. After graduation, Jeff attended Clinch Valley College of the University of Virginia in Wise, Virginia for two years and then graduated Magna Cum Laude with a Bachelor of Science degree in Accounting from Virginia Tech in Blacksburg, Virginia in May 1992. After graduation, Jeff worked as a financial auditor for Ernst & Young, LLP in Charlotte, North Carolina until October 1993 and then as an internal controls and information systems auditor for Deloitte & Touche, LLP in Tampa, Florida and Nashville, Tennessee until January 1996. In January 1996, Jeff entered the University of Tennessee and then graduated Magna Cum Laude with a second Bachelor of Science degree in Electrical Engineering in May of 1998. From May to August of 1998, Jeff worked as a Summer Intern at Lucent Technologies in Allentown, Pennsylvania. Beginning in August of 1998, he entered the University of Tennessee as a graduate student and worked at the Oak Ridge National Laboratory as a research assistant in the UT-ORNL Joint Program in Mixed Signal-VLSI Design. He graduated with a Master of Science degree in Electrical Engineering in May 2000.