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Design, Implementation, and Analysis of a Time of Arrival Measurement System for Rotating Machinery

Bryan Will Hayes
bhayes2@utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Bryan Will Hayes entitled "Design, Implementation, and Analysis of a Time of Arrival Measurement System for Rotating Machinery." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Bruce W. Bomar, Major Professor

We have read this thesis and recommend its acceptance:

L. Montgomery Smith, Bruce A. Whitehead

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Design, Implementation, and Analysis of a Time of Arrival Measurement System for Rotating Machinery

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Abstract

The Non-contact Stress Measurement System (NSMS) acquires critical time of arrival data from multiple optical probes viewing a rotating piece of machinery, such as blades on a turbine engine rotor. The signal from each probe must be converted from light energy to an electrical signal, conditioned, and timed by a high speed counter to measure the time of arrival of the rotating machinery. This thesis describes, in detail, the design and analysis of the photo-detector electronics, analog signal conditioning electronics, and the timing electronics utilized in measuring the time of arrival. To measure the time of arrival with precision, the design of the signal path should minimize noise, jitter, phase delay, and phase mismatch along with maximizing the analog signal rise time. Upon completion of the design, the time of arrival measurement system measured a time of arrival within +/- 3.33 nanoseconds (ns) with an analog bandwidth of 12 Megahertz (MHz).

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Chapter 1

Introduction

Arnold Engineering Development Center (AEDC) is home to the largest collection of advanced flight simulation test facilities in the world [1]. AEDC is under command of the Air Force Material Command, and is a test and evaluation center for the United States Air Force, Department of Defense, National Aeronautics and Space Administration (NASA), and various commercial companies. Engineers at AEDC have been involved in the development, testing, and validation of nearly all U.S. military high performance aircraft, weapon systems, and space systems [2].

Testing at AEDC is divided into three major mission areas: Propulsion Wind Tunnel test complex, Turbine Engine test complex, and Space and Missiles test complex. The Propulsion Wind Tunnel test complex performs the measurement of performance, stability, control systems, and aerodynamic load of an aircraft or other aerodynamic models. The Turbine Engine test complex focuses on the aircraft propulsion system, and on the performance characteristics and structural integrity of these engines under varied flight-test conditions. The Space and Missiles test complex evaluates the performance of rocket systems, from the engine to the flight controls, and includes evaluating system performance of various test articles in a simulated space environment.

A subset of aero-propulsion testing involves measurements of steady and dynamic stresses caused by steady loads and vibrations of rotating hardware, such as blades of a turbine engine rotor. Strain gages have traditionally been utilized for this measurement,

but the Non-contact Stress Measurement System (NSMS) has become more commonly utilized. For NSMS, multiple probes are installed on a turbine engine rotor and are interfaced into a data system for the time of arrival measurement from which component displacements and therefore stresses can be inferred. A once per revolution (1/rev) signal is also interfaced to the data system to be utilized as a time reference signal. The time of arrival measurement for each probe is measured in reference to the 1/rev signal. A computer loaded with custom software acquires the time of arrival of data and converts the timing data to deflection data for each probe. The time of arrival measurements are synchronously acquired, processed, displayed, and stored in near real-time. The time of arrival measurement requires high precision since any induced time distortion of the analog signal from the probe to the measurement electronics and the 1/rev signal is an error in the final deflection data measured.

Approximately 30 years ago, NSMS was first implemented at AEDC. The first generation of NSMS consisted of a single probe channel connected to an oscilloscope and a spectrum analyzer to monitor blade vibration. AEDC, in parallel with turbine engine manufacturers, continued to develop NSMS as electronic and computer technology matured, and produced second and third generation NSMS systems. In the late 1990's, AEDC led a consortium of government agencies and turbine engine manufacturers that was part of an Air Force Research Laboratory (AFRL) contract to produce the fourth generation NSMS with current state-of-the-art technology. At the completion of the

AFRL contract, AEDC continued to develop and mature the fourth generation NSMS utilizing the most current electronic and computer technology [8].

NSMS was first implemented to collect data on all blades and be more cost effective than the conventional strain gage technique. Normally a few blades would have strain gages installed directly on the blade and wired to a slip ring or telemetry system. NSMS inherently collects data on all blades of the rotor in which installed. Although NSMS is cheaper to implement than strain gages, NSMS is not a total replacement of strain gages but rather a complement to strain gages. NSMS and strain gage data can be acquired early in a test to establish a correlation between the two measurements. The correlation of NSMS data to strain gage data is discussed in [9]. After the correlation is complete NSMS can be used as the primary data source for blade vibration for the duration of the test long after all the strain gages have failed. Strain gage failure modes are discussed in [3].

The current NSMS technology utilized at AEDC is considered the fourth generation [8]. The NSMS is composed of an electro-optical system that includes lasers, detectors, and associated signal conditioning electronics, a computer for data acquisition, and online and offline data processing software packages. The computer receives time of arrival data from the NSMS system via Universal Serial Bus (USB) 2.0 interface. A typical NSMS system acquires 24 channels of probe data with a maximum of 48 channels if required. The NSMS system measures up to three 1/rev signals. Each 1/rev signal is associated to a rotor on which each probe is installed. Inter-Range Instrumentation

Group (IRIG) time code format B time stamps are acquired for each revolution of the rotor for correlation purposes to other data sources that are also synchronized to the IRIG time code format B source [5]. The bandwidth of data transmission of time of arrival data is dependent on the number of probes installed, the number of blades, and the rotational speed of the rotor. Maximum data transfer rates are in the range of four Megabytes per second (MB/s) with typical data transfer rates of one MB/s. Multiple NSMS systems can be linked together via Ethernet to synchronize recording the time of arrival data. The computer software converts the acquired time of arrival data to deflection and processed for vibration amplitude, frequency, and phase to display in near real-time.

The basic concept of NSMS is that a rotating component, usually a blade, passes a sensor containing collection optics and reflects light back to a detector that converts the light into an electrical signal. The sensor is typically an optical spot sensor that is composed of a center fiber optic that transmits light from a laser or light-emitting diode to the test object and several surrounding fiber optic cables that collect the reflected light and transmit it to the photo-detector. A 1/rev sensor is utilized to pick up a signal from a target on the rotating shaft. The 1/rev is utilized as the time reference mark and also for the rotor speed. The probe signal has voltage thresholds set to produce a digital trigger pulse that represents the time of arrival of the blade. The 1/rev signal has voltage thresholds set to produce a digital trigger pulse that represents the period of the revolution and the time reference. An example of one probe signal and one 1/rev signal with

voltage thresholds set and producing digital trigger pulses is shown in Figure 1. The example is for a rotor with four blades.

An example of the time of arrival basics of NSMS is shown in Figure 2. The rising edge of the 1/rev digital trigger pulse provides the time reference marker. The rising edge of the blade digital trigger pulse provides the time of arrival of the blade that passed by the probe. The nominal blade time of arrival is shown as the solid black signal and represents a blade passing with no vibration present. The dashed red signal represents a blade time of arrival that is earlier than the nominal blade time of arrival using the 1/rev as the reference. Due to a vibration or deflection of the passing blade, the blade time is earlier. The dashed blue signal represents a blade time of arrival that is later than the nominal blade time of arrival using the 1/rev as the reference. The blade time is later due to a vibration or deflection of the passing blade.

To convert each passing blade's time of arrival to a deflection, the circumference is needed of the rotor being measured. The blade passing velocity is then calculated by taking the circumference of the rotor and dividing by the revolution period. The deflection of each passing blade is calculated by multiplying the blade passing velocity by the blade's measured time of arrival. This simple calculation assumes a constant velocity for each revolution of the rotor but in real world scenarios the velocity is changing by small amounts during the revolution and adds to the measurement uncertainty. A further refinement of the conversion of the blade time of arrival uses acceleration equations to provide a more accurate blade deflection. Once the blade

deflection is calculated, further analysis can be performed on the data to calculate amplitude, frequency, and phase of the vibration present in the data. Figure 3 shows an online display screenshot of blade deflection amplitude, frequency, and phase from simulated data.

This thesis deals with the design, implementation, and analysis of the core hardware and electronics that perform the time of arrival measurement of the NSMS system that the author was directly involved with. The ultimate specifications for the time of arrival measurement are for a 12 MHz analog bandwidth and a timing resolution of 2 ns. Each hardware component had to be researched and studied to define its function in the system and meet the specifications of the design goal. A low noise, high speed photo-detector system was designed to convert the light signal from the probe to an electrical signal. An analog/digital signal conditioning system was designed to modify the electrical signal from the photo-detector system with gain and filtering. The signal flows to a high speed comparator with user-defined thresholds that provides a digital pulse output to the high speed counter system. Finally, the high speed counter system was designed to accept the digital pulse and determine the time between digital pulses referenced to the timing of the 1/rev signal and transmit the time of arrival data to the computer via the USB 2.0 interface.

Chapter 2 provides background information for each system and describes the function of each system in detail. Chapter 3 details the design of the detector system, analog/digital signal conditioning system, and the high speed counter system. Chapter 4

describes the verification hardware utilized to test the hardware individually and as a complete system to see if the system met the specifications of the design. Results of the verification test on the hardware are presented in Chapter 5. A summary of all work performed and recommendations for design improvements are detailed in Chapter 6.

Chapter 2

Design Specifications

The design specifications for the NSMS system were formed by a committee of government and industry engineers. Earlier designs of the NSMS system were performed independently by each government or industry organization, but the current NSMS design was defined to standardize the acquisition of time of arrival data industry-wide. AEDC engineers were the lead for the complete NSMS electro-optical system design that consists of lasers, photo-detectors, analog/digital signal conditioning, and the high speed counter system. This section discusses the design specifications of each sub-system of the electro-optical system excluding the lasers. The overall system block diagram is shown in Figure 4.

2.1 Photo-detector system design specifications

A laser illuminated NSMS probe projects an optical spot onto a passing blade. Light is reflected back into the probe as the blade passes through the optical spot. The photo-detector system is responsible for converting the reflected light from the passing blades into an electrical signal for a time of arrival measurement. Reflected light from the passing blade can vary in optical strength due to the variation of blade tip surface treatments, finishes, or geometries. The photo-detector and associated electronics must have sufficient gain-bandwidth to pass the reflected signal with minimal distortion.

The calculation for the fastest reflected signal rise time was based on the expected highest blade tip velocities of 2250 ft/sec and the blade passing a 5 milli-inch (mil) width

spot resulting in approximately 185 ns rise time. The result of the expected bandwidth of the reflected signal is approximately 2 MHz utilizing Equation 1 from [4].

$$Bandwidth = 0.35 / Rise\ Time$$

Equation 1.

To time the reflected signal accurately, a bandwidth of approximately 2.5 times the calculated expected bandwidth of 2 MHz was chosen resulting in a minimum bandwidth design specification of 5 MHz. A design goal for a bandwidth of 12 MHz (approximately 30 ns rise time using Equation 1) was stated for future expansion as the blade tip velocities increase over time. The lowest reflected optical power to be detected is in the range of nano-watts (nW). A combination of a high internal optical gain, high speed photo-diode and a high analog gain, high speed trans-impedance amplifier is needed to detect the reflected signal with good to signal to noise ratio and sufficient bandwidth.

2.2 Analog/Digital signal conditioning system design specifications

The analog/digital signal conditioning system receives the electrical signal from the photo-detector system and applies gain and a low pass filter to the electrical signal. The analog/digital signal conditioning system must maintain the bandwidth of the photo-detector system of 12 MHz and attenuate unwanted frequencies above 12 MHz. The analog/digital signal conditioning system receives commands from the computer to set gain, trigger voltage level, qualifier voltage level, trigger type, trigger delay, and trigger pulse width. A conditioned electrical signal, along with the user set trigger and qualifier

voltage thresholds, is applied to separate high speed analog comparators to produce a digital pulse output for both the trigger and qualifier. A high speed analog comparator must be able to operate in the linear region and not be restricted by input signal rise times. Output of the analog comparators should be transistor-to-transistor logic (TTL) compatible outputs to interface with the Field Programmable Gate Array (FPGA) that performs the actual trigger generation. User set trigger types of leading edge (LE), trailing edge (TE), or zero crossing (ZC), along with the user set trigger delay and trigger pulse width, determines how the FPGA processes the incoming trigger and qualifier comparator output pulses into a TTL compatible output to interface into the high speed counter system.

2.3 High speed counter system design specifications

The high speed counter system receives the TTL output from the analog/digital signal conditioning system and acquires the time of arrival using the 1/rev as a time reference. The high speed counter system must be able to time asynchronous input signals utilizing 32 bit counters at a clock speed of at least 250 MHz with a design goal of 500 MHz. The probe timing data must be tagged with the channel number and the 1/rev timing data needs to be tagged with an IRIG time. The timing data must then be sent to the computer by a USB 2.0 connection.

Chapter 3

Electronic Designs

3.1 Photo-detector system design

As shown in Figure 5, the photo-detector system design consists of the photo-diode, trans-impedance amplifier, mid-stage amplification, and final stage clamping and amplification. A silicon avalanche photo diode (APD) was chosen as the optical detector. An APD is highly sensitive to light and has an internal gain, typically denoted as M, due to avalanche multiplication of the electrical current when biased near the breakdown voltage of the APD. The breakdown voltage is specified for each APD and on average the APD is biased near 250 volts. The selected APD is rated at a M of 30 that results in a total current output of 0.5 amps (A) per watt (W) of optical power detected, typically in the range of ~5 micro-watts (uW) resulting in ~2.5 micro-amps (uA) nominal output. A maximum bandwidth of 80 MHz is specified for the selected APD. A PIN diode, which does not have the internal avalanche gain, can be used in place of the APD if the reflected optical power is known to be in the range of several micro-watts. A PIN diode contains a p-type semiconductor region and n-type semiconductor region with an intrinsic semiconductor region in the middle which gives the name PIN. The APD was chosen due to the flexibility of being utilized for a broader range of optical reflective powers.

A wide bandwidth junction field-effect transistor (JFET) input stage op-amp was selected for the trans-impedance amplifier stage. The bandwidth of the trans-impedance amplifier is over 1 Gigahertz (GHz) at unity gain. This high bandwidth allows a high

trans-impedance gain to be set and maintains the design specifications of 12 MHz bandwidth. The trans-impedance gain was set to 75,000 using a 75 kilo-ohm resistor. A feedback capacitor was placed in parallel with the gain resistor to maintain a stable operation of the trans-impedance amplifier. The output of the trans-impedance amplifier is AC-coupled to the mid-stage amplifier, a wideband voltage feedback op-amp set to a gain of 2. The output of the mid-stage amplifier feeds a final wideband voltage feedback op-amp with clamped outputs. The final amplifier stage is set to a gain of 5 with the outputs clamped to +/- 3.3 volts (V) and drives an output impedance of 75 ohms. The total electronic gain of the photo-detector system includes a current gain of 75,000 Volts/amp and a voltage gain of 10 Volts/volt. For a nominal return optical power of 5 uW, a detector signal of ~1.875 V is seen at the output of the photo-detector system.

3.2 Analog/digital signal conditioning system design

The analog/digital signal conditioning system consists of variable gain amplifiers, low pass filter stage, analog comparators, and FPGA modules. The analog signal conditioning system accepts the output signal from the photo-detector via a 75 ohm coaxial cable. The input is terminated with 75 ohms to match the output impedance of the photo-detector. The photo-detector signal is then AC-coupled and voltage clamped using a pair of diodes to +/- 3.3V. A buffer amplifier set to a gain of 2 is used to buffer the photo-detector signal from the variable gain amplifier which is setup as an inverting amplifier stage. The variable gain amplifier is discretely controlled to eight levels of gain: 0.08, 0.16, 0.32, 0.64, 1.24, 2.52, 5.01, and 10.00. The variable gain amplifier has

a relatively constant gain bandwidth of 70 MHz independent of the gain setting and feeds a second order Bessel active low-pass filter. The circuit schematic for the variable gain amplifier and low pass filter is shown in Figure 6. The low-pass filter can be set to various cut-off frequencies depending on the frequency content needed. The cutoff frequency is set to 3.5 MHz for most NSMS applications. A cutoff frequency of 12 MHz can be set if needed for high-speed NSMS applications. The output of the low-pass filter is then routed to the high-speed analog comparators and a monitor output to interface to a high speed waveform recording system. The circuit schematic for the high-speed analog comparators is shown in Figure 7. The high-speed analog comparator accepts the output from the low-pass filter on the non-inverting input and the user set voltage threshold on the inverting input. There are two comparators, one for the trigger voltage threshold and one for the qualifier voltage threshold. The user set voltage threshold for both the trigger and qualifier are set using a digital potentiometer with 256 voltage steps from +/- 3.3V. The outputs of the analog comparators are differential TTL compatible. For this design only the non-inverting TTL output was used and serially terminated with 34 ohms resistor which is chosen to match the impedance of the transmission line. The trigger and qualifier TTL signals are routed over to the FPGA on the digital signal conditioning system. The block diagram of the digital signal conditioning system is shown in Figure 8. The FPGA accepts user set values on trigger type, trigger delay, and trigger pulse width from the computer. Utilizing the trigger and qualifier signals, the user set trigger type, trigger delay, and trigger pulse width, state machines produce a digital TTL output

that represents a blade passing event. The state machines were coded utilizing VHDL (VHSIC hardware description language) [6], [7]. The trigger type is decoded and enables the correct state machine to operate. The state machine processes the trigger and qualifier signals, depending on trigger type, and utilizes the trigger delay and pulse width counters to produce a TTL output signal that represents a blade passing event. The trigger delay and pulse width counters utilize a very stable 20 MHz oscillator with 1 part per million (ppm) drift over the operating temperature range of the system which gives the desired system repeatability. The 20 MHz, 1ppm oscillator is fed to the FPGA internal phased locked loop (PLL) and multiplied to achieve a 300 MHz clock speed. Using a 300 MHz counter gives 3.33 ns resolution on marking the blade passing event. The trigger delay is very important in that this is the actual time used to mark the blade passing event. The trigger delay is needed to allow time for the analog signal to pass through the qualifier threshold. The qualifier is used to identify that the signal is actually a blade passing and not noise and helps to prevent other triggers produced due to noise in the signal. The qualifier is typically set at 25% above the set trigger threshold. The trigger pulse width is utilized as a hold-off to keep the system from re-triggering on false blade passing events. An illustration of the trigger and qualifier as well as the trigger delay and trigger pulse width is shown in Figure 9. The TTL output signal from the digital signal conditioning system is serially terminated with 34 ohms and routed to the high speed counter system.

3.3 High speed counter system design

As shown in Figure 10, the high speed counter system consists of an FPGA and Universal Serial Bus (USB) 2.0 interface. The FPGA includes logic for the high speed counters, latches, memory controller, and USB 2.0 communication. The TTL signal from the digital conditioning system is routed to the FPGA. The TTL signal is asynchronous to the FPGA clock and multiple D flip-flops are utilized to synchronize the TTL signal to the FPGA clock and to reduce meta-stability. A state machine detects the edges of the incoming TTL signal and latches the counter data. The counter is clocked at 300 MHz which gives 3.33 ns resolution and does not meet the ultimate design specification of 2 ns. The 3.33 ns resolution was deemed sufficient by the design team, given the cost, complexity, and long lead time of achieving the 2 ns resolution during the design timeframe. The timing portion of the 32 bit up-counter is 29 bits wide with the remaining 3 bits used for marker bits for the 1/rev time and IRIG time stamp data. A custom IRIG time decoder was implemented to decode the IRIG time "B" format. The IRIG time "B" format contains the days, hours, minutes, and seconds which is decoded. A counter running at 1 MHz decodes the microseconds. The counters are reset on the rising the edge of the 1/rev TTL signal. The steps of the counting mechanism are as follows:

1) Counters are reset to zero upon power-up
2) Counters are active after reset and await control from the computer
3) The computer activates the counters

4) Each TTL signal (representing a blade passing) from the sensor latches a 29 bit count representing the blade time of arrival
5) Each TTL 1/rev signal (representing one revolution) from the 1/rev sensor latches a 29 bit count representing the revolution period
6) The 1/rev TTL signal also latches the current IRIG time
7) The data is sent over to a First-In First-Out (FIFO) buffer
8) The FIFO data is then buffered in SDRAM memory
9) As the computer requests the data via USB 2.0 interface, the data is read from SDRAM and transmitted over the USB 2.0 interface to the computer
10) Steps 4 thru 9 loop until the computer stops the data flow

Chapter 4

Verification Hardware

4.1 High speed fiber optic transmitter

A high speed fiber optic transmitter, Agilent HFBR-1412T, was utilized to test the overall bandwidth of the photo-detector system. The implementation of the HFBR-1412T is shown in Figure 11. The rise time of the optical signal generated from the circuit is approximately 12 ns.

4.2 Function generator

A function generator was utilized to test the frequency response of the analog signal conditioning system. A one volt peak to peak sine wave swept from 1 Hz to 10 MHz was applied to the input of the analog signal conditioning system. The output of the analog signal conditioning system was recorded for numerous input frequencies to obtain a frequency response curve as shown in Figure 16.

4.3 Time Interval Analyzer

A time interval analyzer was utilized to test the repeatability and stability of the stable input signal source and the digital signal conditioner system outputs. The stable input signal source was used as the input to the digital signal conditioner. The time interval analyzer recorded statistics for the digital TTL output signals for period, jitter, pulse width, and rise time are discussed in Section 5.4.

4.4 Stable input signal source

A stable input signal source was fabricated using the 20.0 MHz, 1ppm oscillator as a reference source. The oscillator feeds into a FPGA that divides the oscillator to obtain a simulated 1/rev signal and blade signals. The number of blades was set at 16. The resulting simulated 1/rev signal based on the 20.0 MHz oscillator and 16 blades simulated a rotor speed of 9155 revolutions per minute (RPM). The rotor speed for this simulator is the result of dividing down the 20.0 MHz oscillator and is sufficient for use because the rise time of the simulated blade and 1/rev signals are the same regardless of rotor speed. The pulses for the blades are generated such that the first pulse is delayed by one half the times between blades. The time between blades is 409.6 us with a total revolution period of 6553.6 us. The probe and 1/rev signal timing is shown in Figure 12. The stable signal source has 24 sensor outputs and one 1/rev output with all outputs going to a Bayonet Neill-Concelman (BNC) breakout box. A complete end-to-end checkout of the system can be performed by applying the stable input source to the high speed fiber optic transmitter and inputting the signal to the photo-detector system. Channel-to-channel variation due to propagation delay throughout the system can be measured along with the overall repeatability and stability of the overall timing system. The signal from the stable signal source could be applied directly to the analog/digital signal conditioning system and high speed counter system to obtain statistics independent from the photo-detector system.

Chapter 5

Design Results

5.1 Photo-detector design results

The photo-detector design went through several iterations before arriving at the needed bandwidth, noise, and sensitivity specifications. The trans-impedance feedback resistor sets the overall gain and bandwidth of the photo-detector response. The final design implements a 75 kilo-ohm resistor in the feedback of the trans-impedance amplifier. A 0.5 pico-farad capacitor was placed across the feedback resistor for stability. Without the capacitor, the trans-impedance amplifier would go unstable and oscillate with an amplitude of approximately 100 milli-volts. A comparison of the Avalanche Photo-Diode (APD) and a PIN diode was performed for bandwidth, noise, and sensitivity. The PIN diode lacks the APD's internal optical gain of 30 but the PIN diode with the same circuit configuration of the APD reduces the noise with the same increase in bandwidth. The PIN diode could be used where the intensity of reflected optical power from the target is not an issue. The comparison was performed by connecting the high speed fiber optic transmitter to the photo-detector and using the stable input signal source as the test signal. The table of comparison results of the APD and PIN configurations is shown in Table 1. The highlighted row (configuration number 2) is the typical configuration for the photo-detector system. Table 1 also shows an older generation photo-detector design which is configuration number 9. The new design is approximately six times faster with only a slight increase of 20 mV of noise with the

increase in bandwidth. The photo-detector design, configuration number 7, shows that the detector could have a bandwidth as high as ~23 MHz if desired but with a much lower overall gain. The trade-offs in bandwidth, gain, and noise need to be balanced according to the application. The typical configuration for the photo-detector system gives the best overall balance for most NSMS applications. The photo-detector design can be easily modified to accommodate the other configurations as needed.

5.2 Analog/digital signal conditioning design results

The analog signal conditioning system design needed to minimize group delay from channel-to-channel. The group delay is the derivative of the phase response and represents the time distortion present on the system at different frequencies. The group delay needs to be minimized in a time based measurement system. Timing measurement will be distorted from channel-to-channel based on tolerances of resistors and capacitors utilized in building the second order low-pass filter. The analog signal conditioning was originally designed with an active second order Butterworth low-pass filter to maintain a flat magnitude response in the pass-band. The major issue with the Butterworth filter is the non-linear phase response in the pass-band. The final design incorporated a second order low-pass Bessel filter. A P-SPICE software simulation was performed for the Butterworth and the Bessel low-pass filters. The P-SPICE simulation schematic is shown in Figure 13. The best comparison of the Bessel and the Butterworth filters is shown by viewing the plots of the group delay in Figure 14. The Bessel has excellent group delay characteristics (maximally flat and linear in the pass-band) compared to the Butterworth.

Figure 15 shows the comparison of the magnitude response for the second order Butterworth and Bessel low-pass filter. Only a small difference in the magnitude response is noted between the Butterworth and the Bessel filter. The measured magnitude response of the second order Bessel filter as implemented is shown in Figure 16. The minus 3dB point was designed for 3.5 MHz but the actual minus 3dB point is located closer to 4.1 MHz. One percent resistors and five percent capacitors were utilized to implement the filter and could cause the implemented minus 3dB point to move closer to 4.0 MHz than the theoretical value of 3.5 MHz. The 4.0 MHz bandwidth of the analog signal conditioning allows the photo-detector signal pass undisturbed and attenuate unwanted frequencies pass 4.0 MHz. The output of the Bessel low pass filter is applied to an analog comparator that produces a digital pulse to the digital conditioning system. The digital conditioning system was implemented in a FPGA chip that saved board space and external components. The total design fit inside one FPGA chip using 1,444 logic elements and one PLL generating a 300 MHz internal global clock using the stable 20.0 MHz, 1ppm oscillator as the source. The FPGA design included logic for trigger type, trigger delay, and trigger pulse width. A digital trigger pulse was able to be produced and qualified with a timing resolution of 3.33 ns.

5.3 High speed counter system design results

The high speed counter system was fit inside a single FPGA chip using 7,506 logic elements and 164,320 memory bits. The FPGA internal logic was able to be clocked at 300 MHz using a PLL with the stable 20.0 MHz, 1ppm oscillator as the

source. The final logic design was able to count up to 32 probe signal channels at a timing resolution of 3.33 ns with each channel having independent enables. Up to three 1/rev signal channels were implemented with each being user assigned to a probe signal channel in software. The IRIG B time was marked in the timing data stream on each rising edge of the 1/rev signal with 1 us resolution. The FPGA logic controlled the internal FIFO and external SDRAM to buffer the timing data to the USB port. The USB transfer was implemented by a DMA transfer to the computer. The computer was able to acquire, save, and analyze the data in near real time.

5.4 Overall system design results

The overall system design results met the design goals set forth. The overall system analog bandwidth can change based on the application. For most NSMS applications, a bandwidth of 3.5 MHz is suitable. For high speed engines or turbochargers, the overall system bandwidth of 12 MHz or higher is needed, and the system can be easily modified to change the bandwidth needed in the photo-detector and analog signal conditioning systems. The digital signal conditioning system allows user input to set parameters such as trigger type, trigger delay, and trigger pulse width and generates a trigger pulse for each blade based on a 300 MHz clock. The high speed counter system allows the counting of up to 32 channels but typically only 24 channels are needed. The high speed counter system interfaces to the computer using a common USB 2.0 connection that transfers data up to the maximum data rate of 4MB/sec. The system design is flexible enough that the clock rate can be changed from 300 MHz. At

AEDC applications that rotate at a very slow speed are measured with NSMS and the clock rate has been reduced to 20 MHz or even as low as 5 MHz.

The time interval analyzer results of the stable input signal source for the time interval for the probe from the 1/rev signal are a mean of 204.80008 us with a standard deviation of 100 pico-seconds (pS). A block of 1,000 measurements were used to compile the statistics. The time interval analyzer results of the probe blade-to-blade interval times are a mean of 409.60001 us with a standard deviation of 80 pS. The rise time for the probe signal was measured at 25 ns and the 1/rev signal rise time was measured at 15 ns. The measured rise times of the stable signal source are faster than the system's designed rise time and will produce results of the overall system rise time independent of the system input.

The end-to-end checkout results of the system measuring the time of arrival are shown in Figures 17 to 20. Approximately 14,000 time of arrival measurements were utilized for the statistical analysis. The standard deviation of the time of arrival measurement was found to be 0.6 counts (2 ns). The maximum to minimum time of arrival measurement for each blade time was found to be 4 counts (13.33 ns). The histogram of the time of arrival measurement in counts for: blade 1 is shown in Figure 17, blade 8 is shown in Figure 18, blade 16 is shown in Figure 19, and the 1/rev is shown in Figure 20. The spread of the time arrival is shown to be concentrated in the two center bins with very few measurements in the outer bins. Each bin is one count wide which represents 3.33 ns.

The average relative measurement from blade-to-blade was found to be 409.599 us compared to the stable input source blade-to-blade measurement of 409.6 us. This shows an average measurement error of approximately 1 ns. The absolute time of arrival measurement shows a delay of approximately 196 ns. A portion of this delay can be attributed to the approximately 60 ns group delay of the second order Bessel low pass filter. Another portion of this delay can be attributed to the analog comparator maximum propagation delay specification of approximately 20 ns. The remaining approximately 116 ns of the delay cannot be accounted for and will need to be investigated further. The absolute time of arrival measurement is not used for typical NSMS applications since first a baseline is established and then deviations from the baseline are used in the actual measurement and processing algorithms.

The maximum propagation delay difference measured from channel-to-channel for eight separate channels was 8 counts (26.67 ns). This is close to the analog comparator maximum propagation delay specification of 20 ns, but this delay can be a minimum of 12 ns. Another factor in the propagation delay from channel-to-channel is the small variations in the passive components (resistors and capacitors) of the second order Bessel low pass filter that will slightly affect the group delay response of the filter. Other factors contributing to the propagation delay could be the individual differences in the phase delay of all active components in the signal path.

Chapter 6

Summary and Recommendations

The time of arrival measurement system design met or exceeded the design goals for channels implemented, analog bandwidth, and timing resolution. The time of arrival measurement system (NSMS) is currently utilized on a routine basis at AEDC and off-site test locations. NSMS is easier and cheaper to implement than the conventional technique of applying strain gages to the blades directly and wiring to a slip ring or telemetry system. NSMS can be utilized on any rotating component and is not limited to blades from a turbine engine rotor. Other applications may be the painting of reflective stripes on shafts to measure the vibration seen on the shaft or to monitor gear teeth, if needed. NSMS has been applied to large plant compressors as a near real time health monitor and this area will continue to grow in the future years. The future of the time of arrival measurement will be the implementation of the time measurement on a sampled probe waveform. With the current advances in computer bus technology, such as Peripheral Control Interface (PCI) Express, advances in the data transfer of hard drives, and RAID hard drive configurations, the data transfer from a analog-to-digital card will allow near-real time measurements to be performed on the probe signals without the need for the analog/digital signal conditioning and the high speed counter system. The detector will still be needed to convert the returned optical power into the electrical signal but all time measurement will be performed by the computer. This implementation will

allow a cheaper and more compact design for the time of arrival measurement system, and allow the archival of probe waveforms for possible further analysis of data if needed.

List of References

[1] Arnold Engineering and Development Center's Test Facility Guide retrieved from http://www.arnold.af.mil/shared/media/document/AFD-080625-010.pdf

[2] Arnold Engineering and Development Center's Beyond the Speed of Sound retrieved from http://www.arnold.af.mil/shared/media/document/AFD-100323-069.pdf

[3] Ellis, Brent L. & Smith, L. Montgomery, *Modeling and Experimental Testing of Strain Gauges in Operational and Failure Modes*, IEEE Transactions on Instrumentation and Measurement, Vol. 58, No. 7, pp. 2222-2227, July, 2009.

[4] Johnson, Howard & Graham, Martin. (1993). *High-Speed Digital Design: A Handbook of Black Magic*. New Jersey: Prentice Hall.

[5] Range Commander's Council. (2004). IRIG Standard 200-04. New Mexico: White Sands Missile Range.

[6] Salcic, Zoran (1998). *VHDL and FPLDs in Digital Systems Design, Prototyping, and Customization*. Boston: Kluwer Academic Publishers.

[7] Salcic, Zoran & Smailagic, Asim (1997). *Digital Systems Design and Prototyping Using Field Programmable Logic*. Boston: Kluwer Academic Publishers.

[8] Vining, Charles R., Hayes, Bryan W., Arnold, Steve A., Holt, Lanny L., Jones, Brandon, & Bomar, Bruce W., *PC-Based Generation 4 Non-Contact Stress Measurement System*, High Cycle Fatigue Conference, New Orleans, LA, March 8-11, 2005.

[9] Vining, Charles R., Hayes, Bryan W., Arnold, Steve A., & Howard, Robert P., *Comparison of Non-contact Stress Measurement Data to Strain Gage Data*, High Cycle Fatigue Conference, New Orleans, LA, March 8-11, 2005.

Bibliography

Horowitz, Paul & Hill, Winfield. (1989). *The Art of Electronics*. New York: Cambridge University Press.

Jackson, Leland B. (1991). *Signals, Systems, and Transforms*. Reading: Addison-Wesley Publishing Company.

Proakis, John G. & Manolakis, Dimitris G. (1996). *Digital Signal Processing: Principles, Algorithms, and Applications*. New Jersey: Prentice Hall.

Robinson, Woodrow. (1996). *Evolution of NSMS for Rotor Blading Stress Measurements in Aircraft Gas Turbine Engine Testing*. ISA Conference.

Appendix

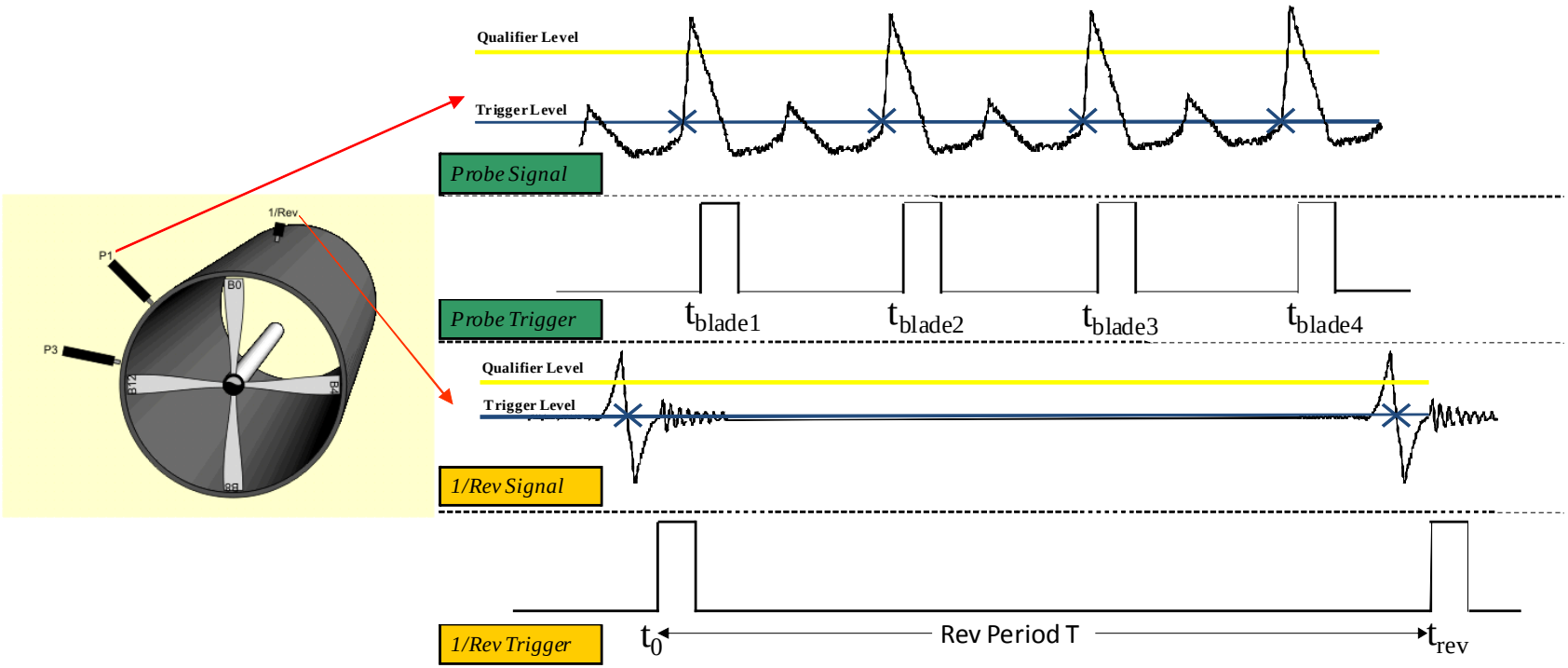

Figure 1. Example of NSMS measurement signals

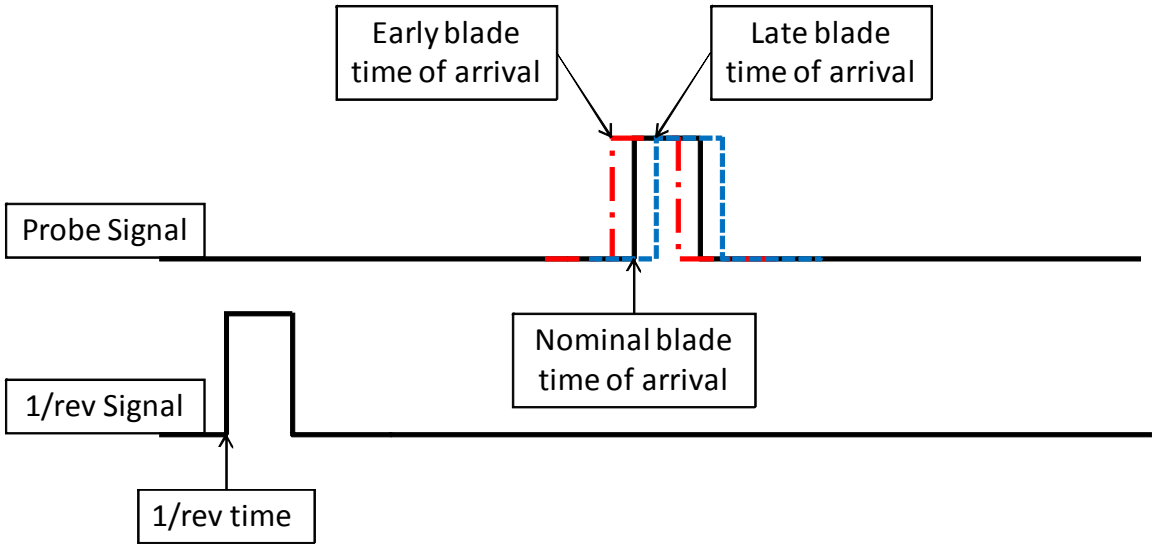

Figure 2. Example of NSMS time of arrival basics

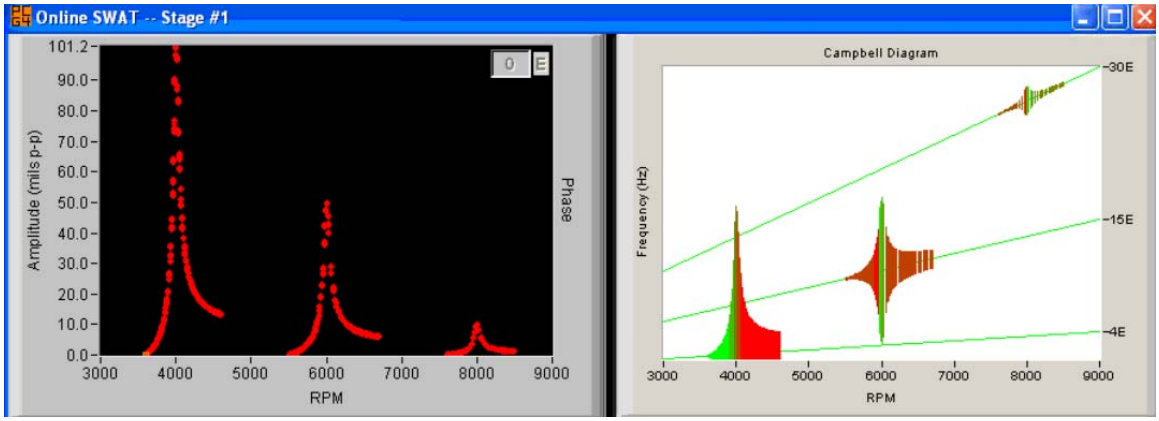

Figure 3. Online screenshot displaying blade deflection amplitude, frequency, and phase from simulated data

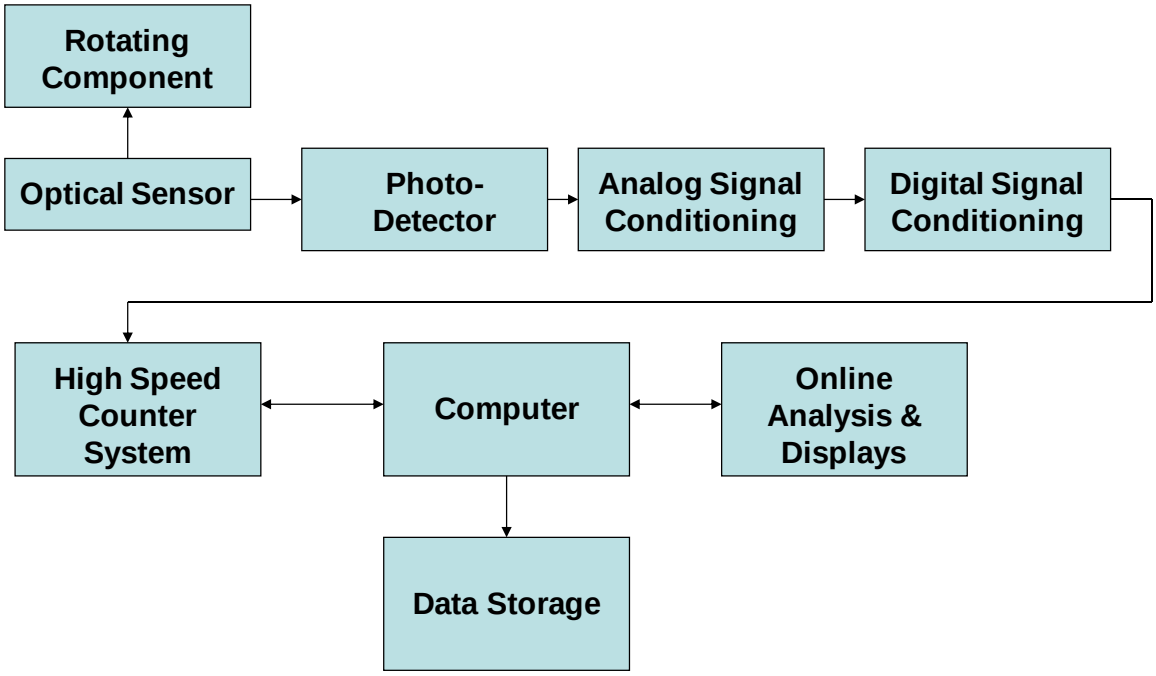

Figure 4. Overall system block diagram

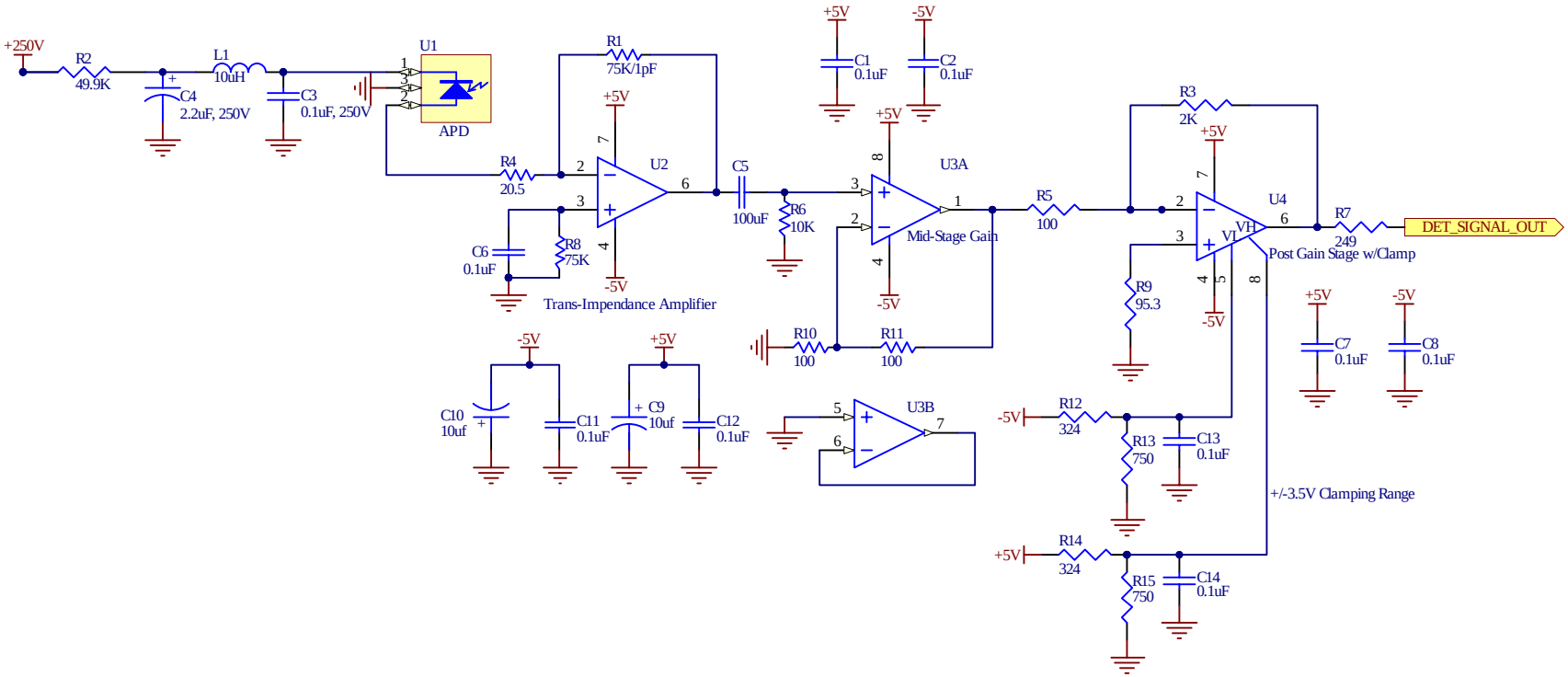

Figure 5. Photo-detector system schematic

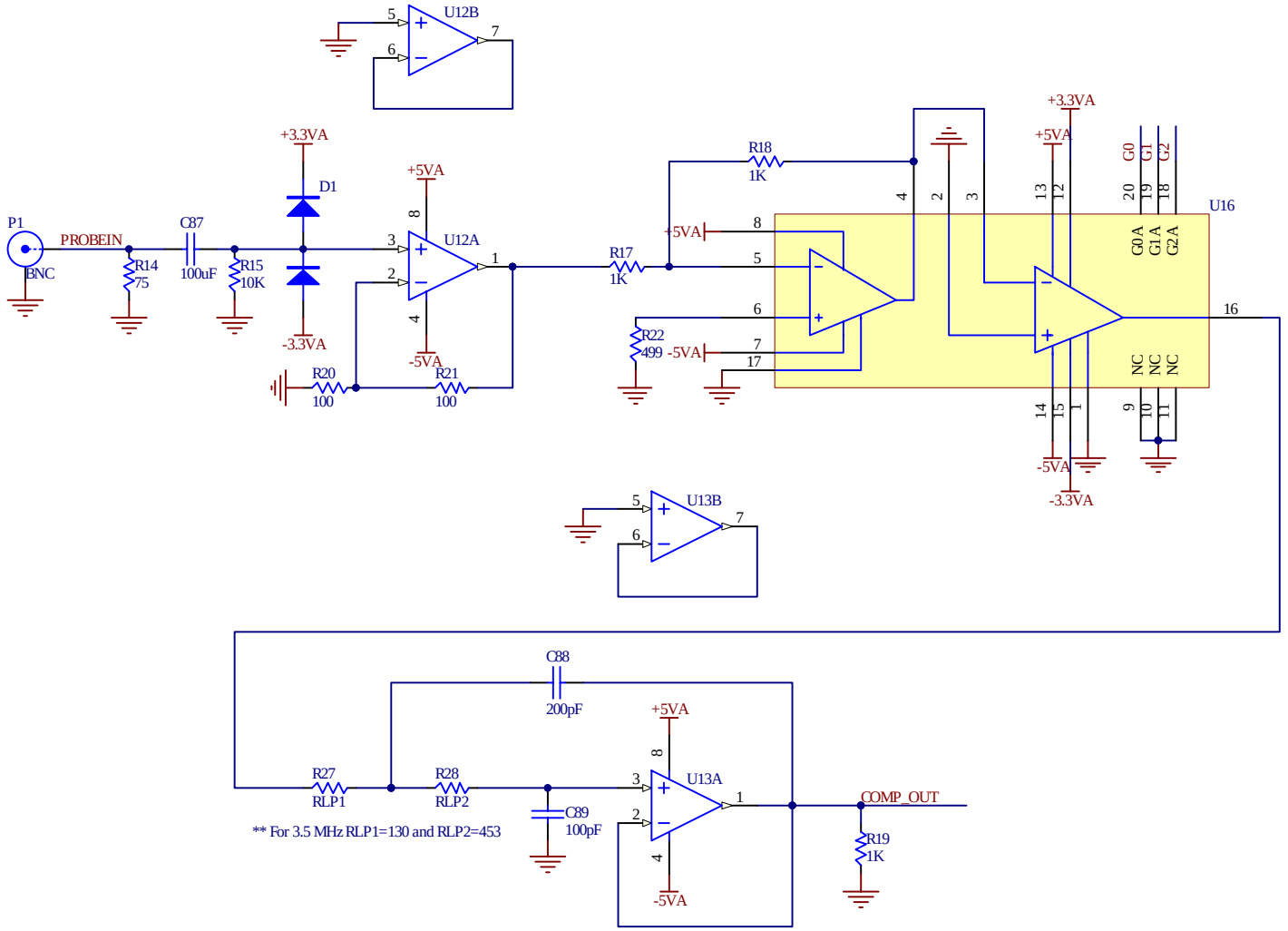

Figure 6. Analog signal conditioning schematic including variable gain amplifier and low-pass filter

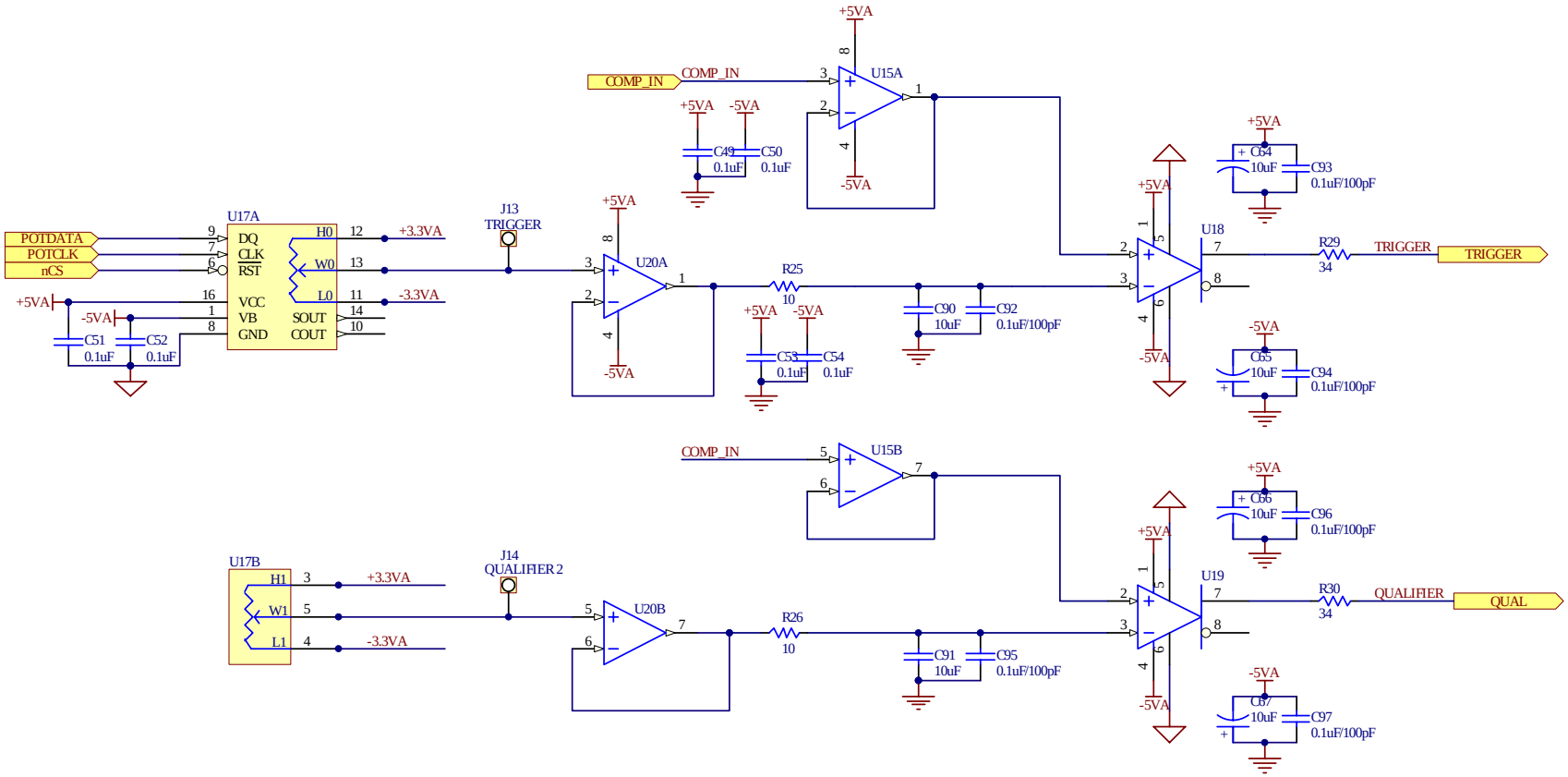

Figure 7. Analog signal conditioning schematic including trigger and qualifier comparators

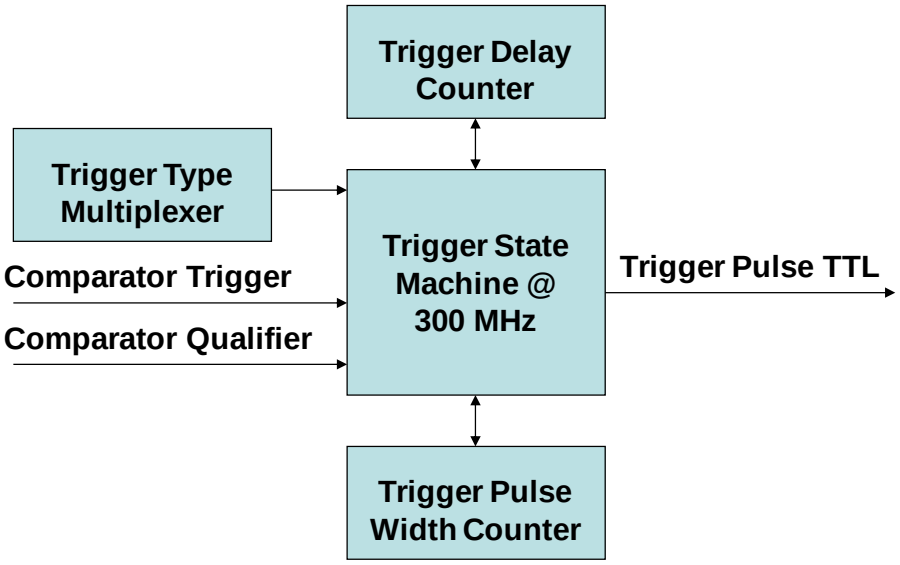

Figure 8. Digital signal conditioning block diagram

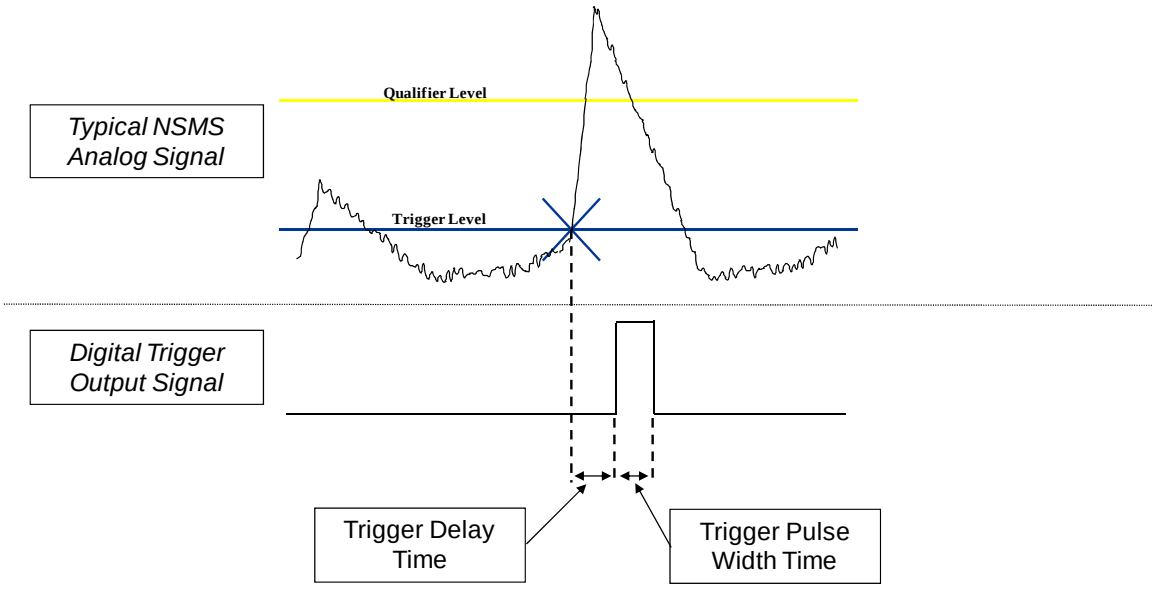

Figure 9. Illustration of trigger and qualifier levels including trigger delay and trigger pulse width

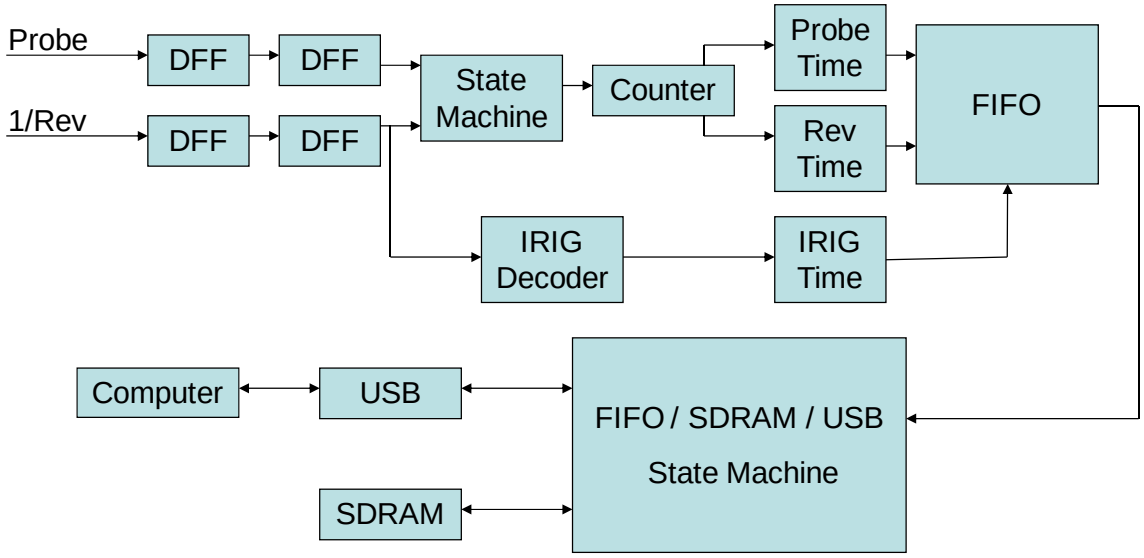

Figure 10. High speed counter design block diagram

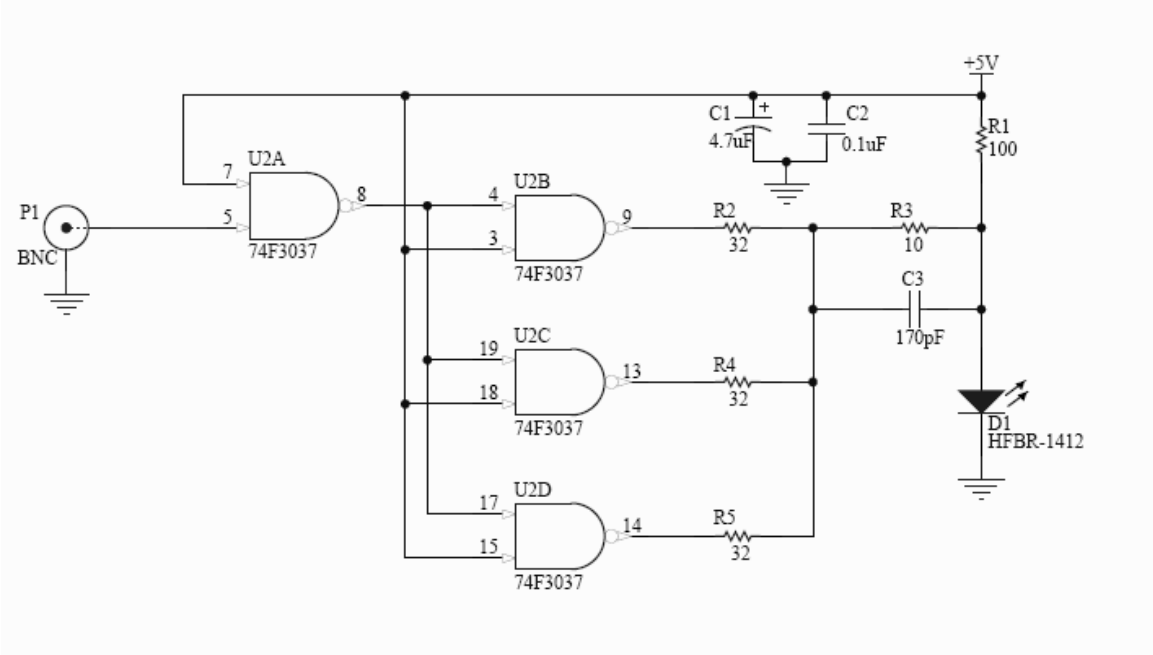

Figure 11. High speed fiber optic transmitter

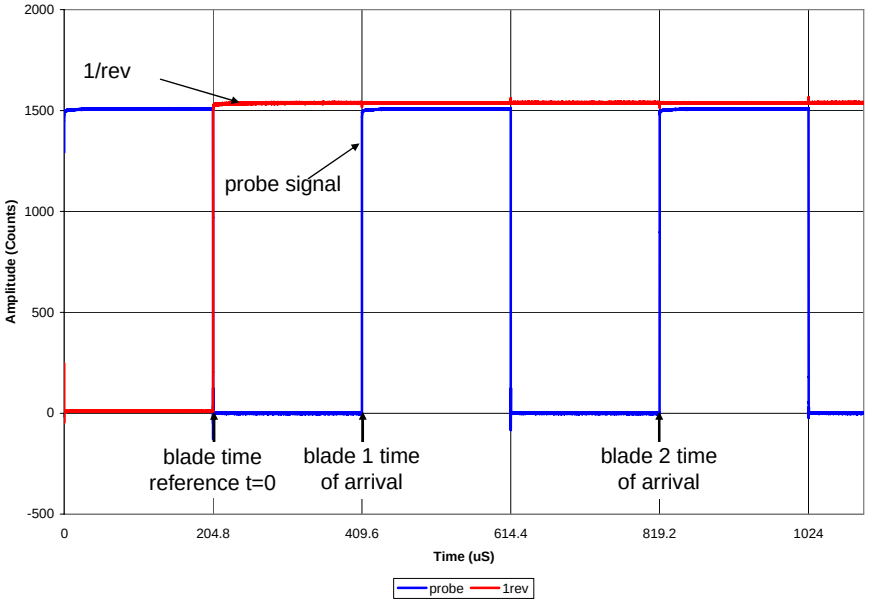

Figure 12. Stable input source probe and 1/rev signals

Configuration Number	TIA Feedback Resistor (kilo-Ohms)	TIA Feedback Cap (pico-Farads)	Rise Time (nS)	Bandwidth (MHz)	Noise (mV pk-pk)	Mid-Stage Amplifier Gain	Post Amplifier Gain	APD or PIN
1	75	0.50	100	3.50	200	2	20	APD
2	75	0.50	100	3.50	50	2	5	APD
3	75	0.00	20	17.50	100	2	5	PIN
4	75	0.50	100	3.50	20	2	5	PIN
5	75	0.50	110	3.18	40	2	20	PIN
6	10	0.50	15	23.33	20	2	5	PIN
7	10	0.50	15	23.33	40	2	5	APD
8	10	0.50	40	8.75	20	2	20	PIN
9	NA	NA	600	0.58	30	NA	NA	APD

Highlighted in Yellow is typical configuration

**Configuration Number 9 represents an earlier generation design

Detector Bandwidth Tester Rise Time = 12nS

Table 1. Photo-detector design comparison table

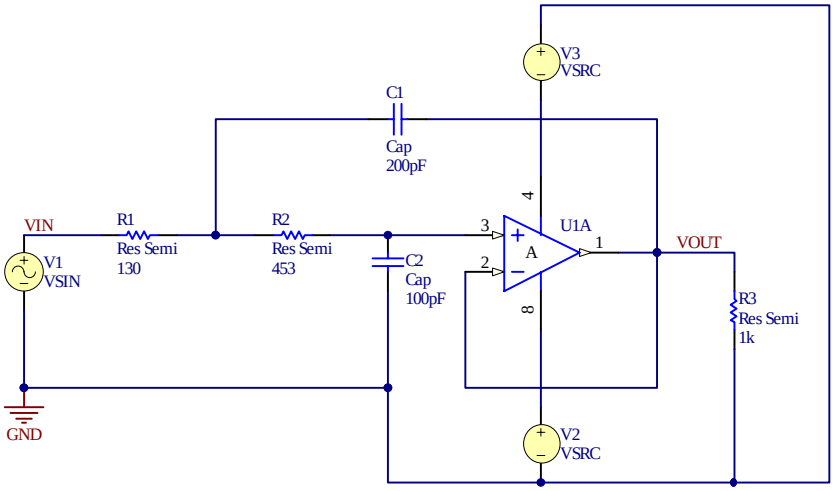

Figure 13. Low-pass filter P-SPICE simulation schematic

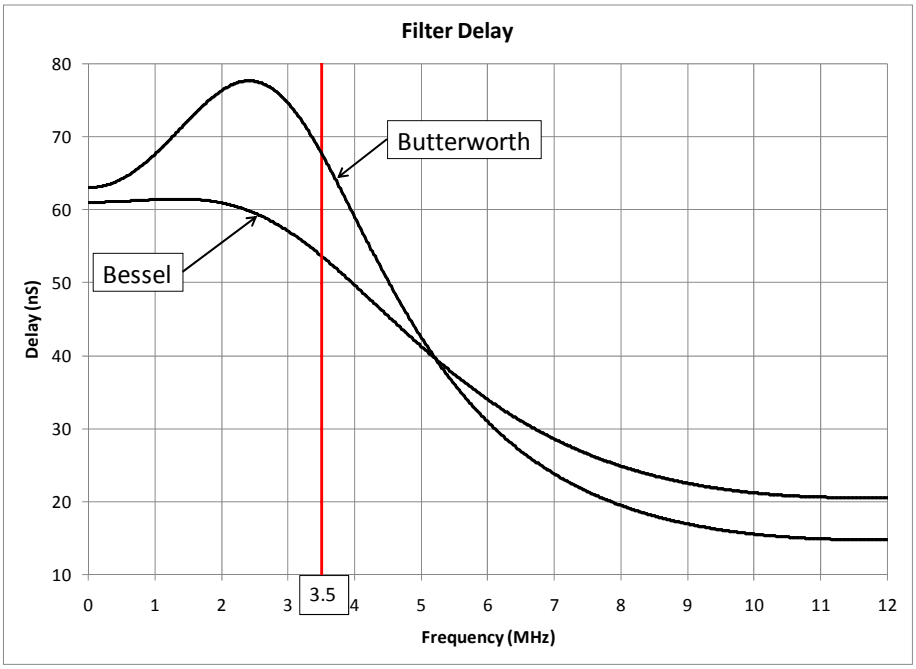

Figure 14. Comparison of group delay for the second order Butterworth and Bessel low-pass filters

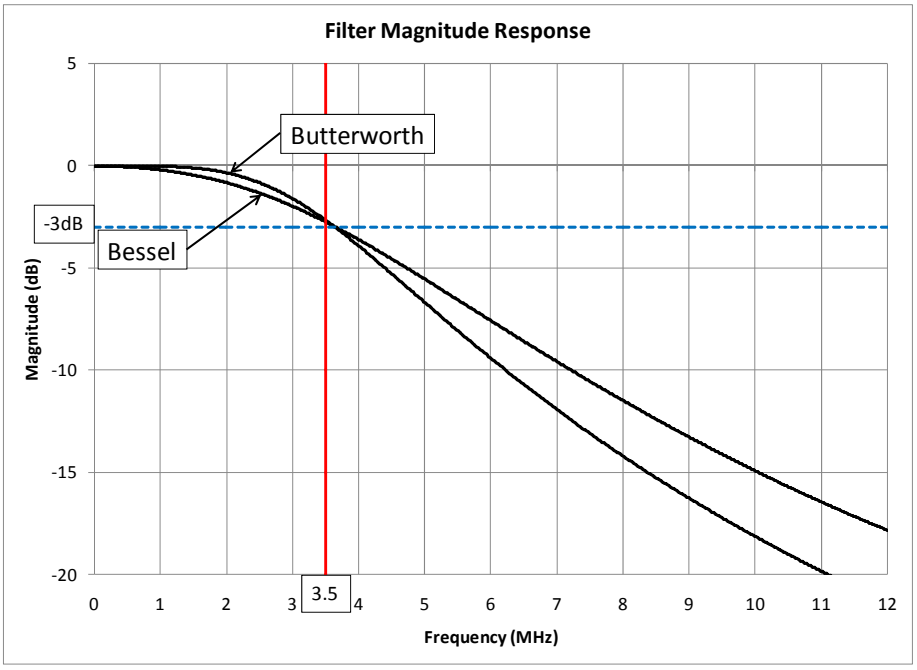

Figure 15. Comparison of magnitude response for the second order Butterworth and Bessel low-pass filters

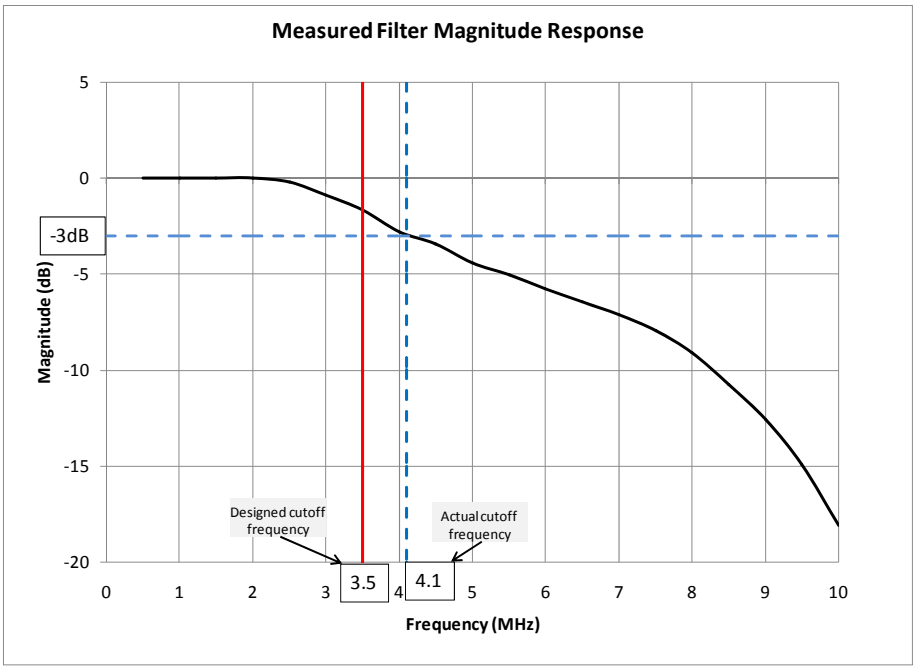

Figure 16. Measured magnitude response for the second order Bessel low-pass filter as implemented

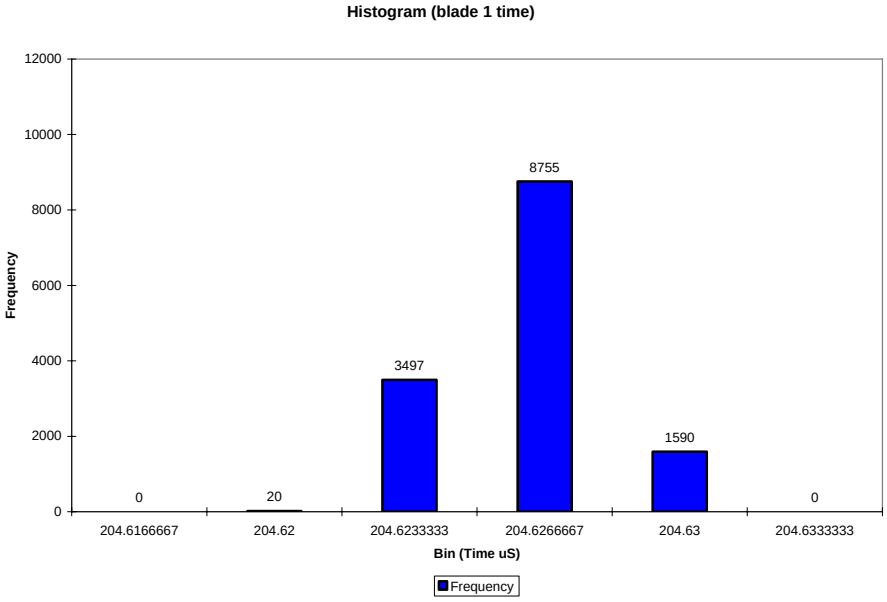

Figure 17. Histogram of Blade 1 time of arrival measurement

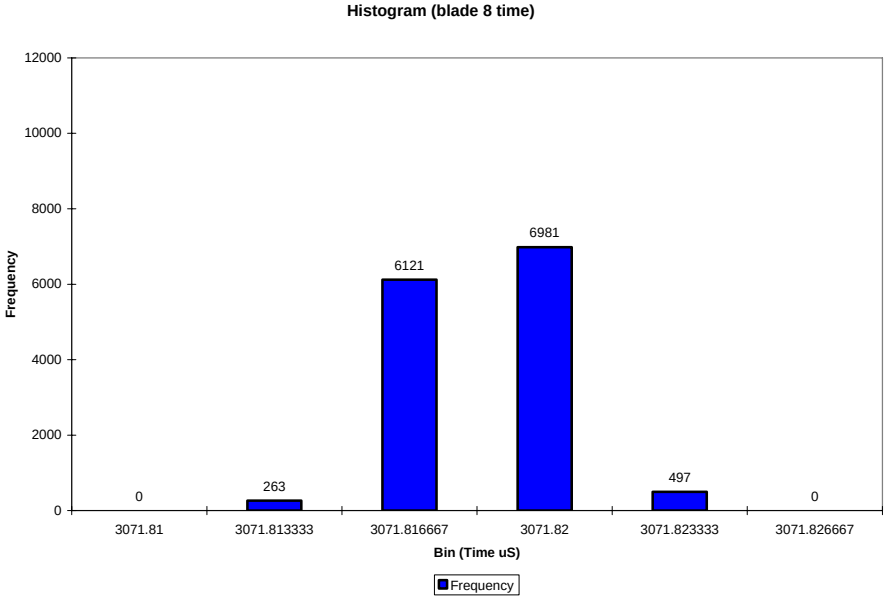

Figure 18. Histogram of Blade 8 time of arrival measurement

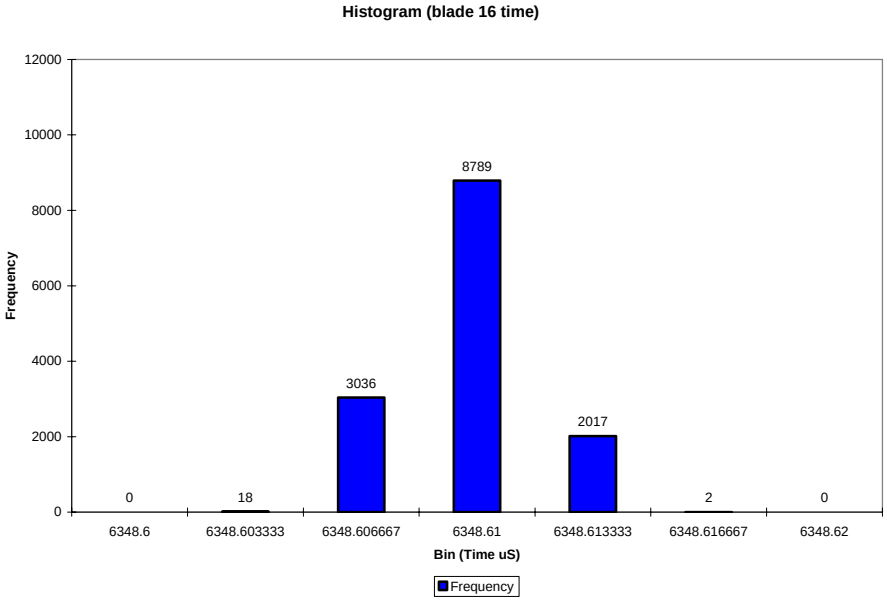

Figure 19. Histogram of Blade 16 time of arrival measurement

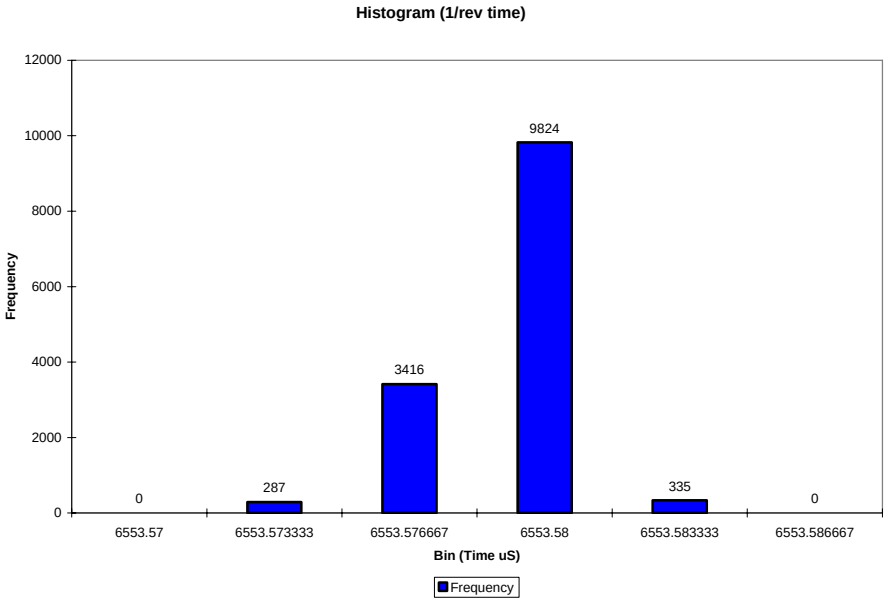

Figure 20. Histogram of 1/rev time of arrival measurement

Vita

Bryan W. Hayes was born in Tullahoma, Tennessee. He received his Bachelor's of Science degree in Electrical and Computer Engineering from Tennessee Technological University in July 1999. He is currently employed by Aerospace Testing Alliance (ATA) at Arnold Air Force Base, Tennessee as a Senior Electrical Engineer II and NSMS Technical Lead. He has worked at ATA for 12 years, and currently resides in Tullahoma, Tennessee and is married to Christy Hayes.